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MCP3913

3V Six-Channel Analog Front End

Features:

- Six Synchronous Sampling 24-bit Resolution Delta-Sigma A/D Converters
- 94.5 dB SINAD, -107 dBc Total Harmonic Distortion (THD) (up to 35th Harmonic), 112 dBFS SFDR for Each Channel
- Enables 0.1% Typical Active Power Measurement Error over a 10,000:1 Dynamic Range
- Advanced Security Features:
  - 16-bit Cyclic Redundancy Check (CRC) Checksum on All Communications for Secure Data Transfers
  - 16-bit CRC Checksum and Interrupt Alert for Register Map Configuration
  - Register Map lock with 8-bit Secure Key
- 2.7V-3.6V AV_{DD}, DV_{DD}
- Programmable Data Rate up to 125 ksps:
  - 4 MHz Maximum Sampling Frequency
  - 16 MHz Maximum Master Clock
- Oversampling Ratio up to 4096
- Ultra-Low Power Shutdown Mode with < 10 µA
- -122 dB Crosstalk between Channels
- Low Drift 1.2V Internal Voltage Reference: 9 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain PGA on Each Channel (up to 32 V/V)
- Phase Delay Compensation with 1 µs Time Resolution
- Separate Data Ready Pin for Easy Synchronization
- Individual 24-bit Digital Offset and Gain Error Correction for Each Channel
- High-Speed 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Continuous Read/Write Modes for Minimum Communication Time with Dedicated 16/32-bit Modes
- Available in a 40-lead UQFN and 28-lead SSOP Packages
- Extended Temperature Range: -40°C to +125°C

Description:

The MCP3913 is a 3V six-channel Analog Front End (AFE), containing six synchronous sampling delta-sigma, Analog-to-Digital Converters (ADC), six PGAs, phase delay compensation block, low-drift internal voltage reference, digital offset and gain error calibration registers, and high-speed 20 MHz SPI-compatible serial interface.

The MCP3913 ADCs are fully configurable, with features such as: 16/24-bit resolution, Oversampling Ratio (OSR) from 32 to 4096, gain from 1x to 32x, independent Shutdown and Reset, dithering and auto-zeroing. The communication is largely simplified with 8-bit commands, including various continuous read/write modes and 16/24/32-bit data formats that can be accessed by the Direct Memory Access (DMA) of an 8/16- or 32-bit MCU, and with the separate data ready pin that can directly be connected to an Interrupt Request (IRQ) input of an MCU.

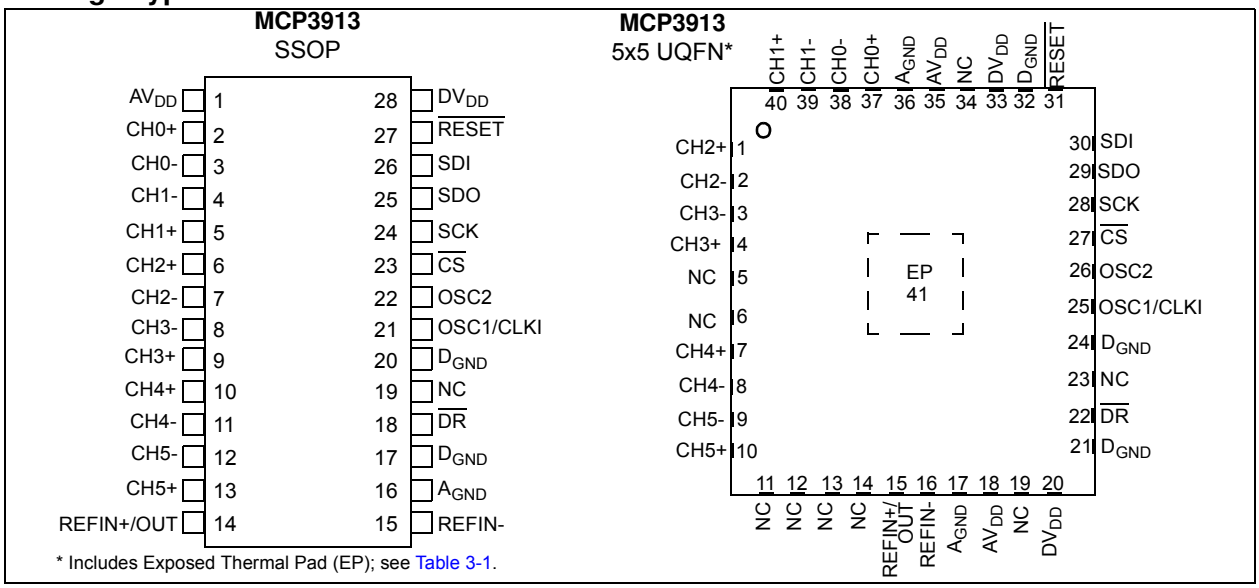
The MCP3913 includes advanced security features to secure the communications and the configuration settings, such as a CRC-16 checksum on both serial data outputs and static register map configuration. It also includes a register-map lock through an 8-bit secure key to stop unwanted write commands from processing.

The MCP3913 is capable of interfacing with a variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall-effect sensors.

Applications:

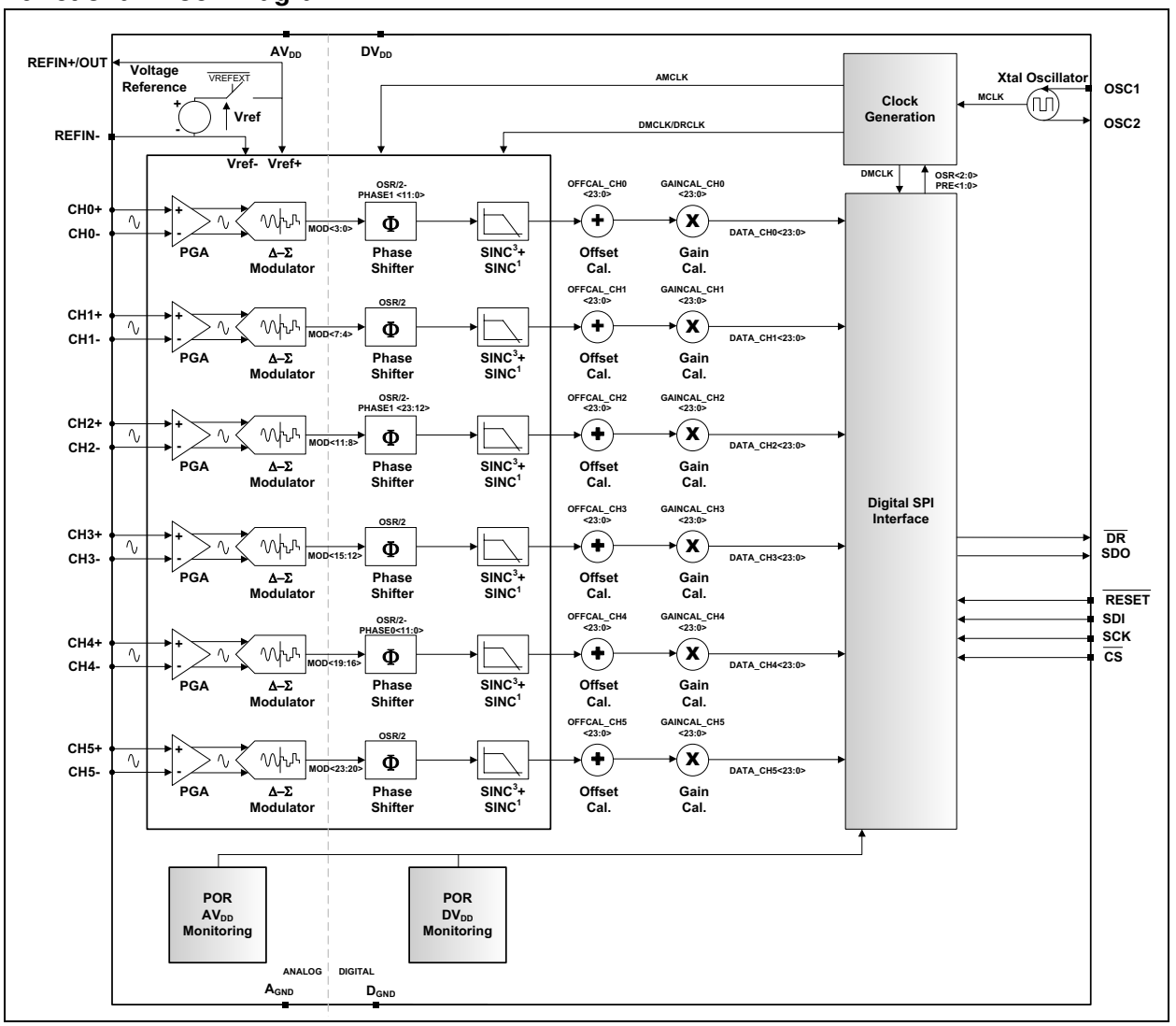
- Polyphase Energy Meters
- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring
- Audio/Voice Recognition

Package Type



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} ..... -0.3V to 4.0V
Digital inputs and outputs w.r.t. A_{GND} ..... --0.3V to 4.0V
Analog input w.r.t. A_{GND} ....-2V to +2V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to V_{DD} +0.6V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) ..... 1.5 kV, 300V
ESD on all other pins (HBM,MM) ..... 2 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Electrical Specifications

TABLE 1-1: ANALOG SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
ADC Performance						
Resolution (No missing codes)		24	—	—	bits	OSR = 256 or greater
Sampling Frequency	f_S(DMCLK)	—	1	4	MHz	For maximum condition, BOOST<1:0> = 11
Output Data Rate	f_D(DRCLK)	—	4	125	ksps	For maximum condition, BOOST<1:0> = 11, OSR = 32
Analog Input Absolute Voltage on CHn+/- pins, n between 0 and 5	CHn+/-	-1	—	+1	V	All analog input channels, measured to A_{GND}
Analog Input Leakage Current	I_{IN}	—	+/-1	—	nA	RESET<5:0> = 111111, MCLK running continuously
Differential Input Voltage Range	(CH_{n+}-CH_{n-})	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	0.2	1	mV	**Note 5**
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	**Note 5**
Gain Error Drift		—	1	—	ppm/°C	

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 000000, RESET<5:0> = 000000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 111111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Integral Non-Linearity	INL	—	5	—	ppm	
Measurement Error	ME	—	0.1	—	%	Measured with a 10,000:1 dynamic range (from 600 mV_{Peak} to 60 μV_{Peak}), AV_{DD} = DV_{DD} = 3V, measurement points averaging time: 20 seconds, measured on each channel pair (CH0/1, CH2/3, CH4/5)
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1, proportional to 1/AMCLK
		142	—	—	kΩ	G = 2, proportional to 1/AMCLK
		72	—	—	kΩ	G = 4, proportional to 1/AMCLK
		38	—	—	kΩ	G = 8, proportional to 1/AMCLK
		36	—	—	kΩ	G = 16, proportional to 1/AMCLK
		33	—	—	kΩ	G = 32, proportional to 1/AMCLK
Signal-to-Noise and Distortion Ratio (**Note 1**)	SINAD	92	94.5	—	dB	
Total Harmonic Distortion (**Note 1**)	THD	—	-107	-103	dBc	Includes the first 35 harmonics
Signal-to-Noise Ratio (**Note 1**)	SNR	92	95	—	dB	
Spurious Free Dynamic Range (**Note 1**)	SFDR	—	112	—	dBFS	
Crosstalk (50, 60 Hz)	CTALK	—	-122	—	dB	**Note 4**
AC Power Supply Rejection	AC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 3V + 0.6V_{PP} 50/60 Hz, 100/120 Hz
DC Power Supply Rejection	DC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 2.7V to 3.6V
DC Common Mode Rejection	DC CMRR	—	-100	—	dB	V_{CM} from -1V to +1V

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 000000, RESET<5:0> = 000000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 111111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference						
Tolerance	V_{REF}	1.176	1.2	1.224	V	VREFEXT = 0, T_A = +25°C only
Temperature Coefficient	TCV_{REF}	—	9	—	ppm/°C	T_A = -40°C to +125°C, VREFEXT = 0, VREFCAL<7:0> = 0x50
Output Impedance	$ZOUTV_{REF}$	—	0.6	—	kΩ	VREFEXT = 0
Internal Voltage Reference Operating Current	$AI_{DD}V_{REF}$	—	54	—	µA	VREFEXT = 0, SHUTDOWN<5:0> = 111111
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Differential Input Voltage Range (V_{REF+} – V_{REF-})	V_{REF}	1.1	—	1.3	V	VREFEXT = 1
Absolute Voltage on REFIN+ pin	V_{REF+}	V_{REF-} + 1.1	—	V_{REF-} + 1.3	V	VREFEXT = 1
Absolute Voltage REFIN- pin	V_{REF-}	-0.1	—	+0.1	V	REFIN- should be connected to A_{GND} when VREFEXT = 0
Master Clock Input						
Master Clock Input Frequency Range	f_{MCLK}	—	—	20	MHz	CLKEXT = 1, **(Note 7)**
Crystal Oscillator Operating Frequency Range	f_{XTAL}	1	—	20	MHz	CLKEXT = 0, **(Note 7)**
Analog Master Clock	AMCLK	—	—	16	MHz	**(Note 7)**
Crystal Oscillator Operating Current	DIDDXTAL	—	80	—	µA	CLKEXT = 0
Power Supply						
Operating Voltage, Analog	AV_{DD}	2.7	—	3.6	V	
Operating Voltage, Digital	DV_{DD}	2.7	—	3.6	V	
Operating Current, Analog **(Note 2)**	$I_{DD,A}$	—	4.5	6	mA	BOOST<1:0> = 00
		—	5.4	8	mA	BOOST<1:0> = 01
		—	7.4	10	mA	BOOST<1:0> = 10
		—	12.9	17.5	mA	BOOST<1:0> = 11

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 000000, RESET<5:0> = 000000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 111111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Current, Digital	$I_{DD,D}$	—	0.5	1	mA	MCLK = 4 MHz, proportional to MCLK (**Note 2**)
		—	1.5	—	mA	MCLK = 16 MHz, proportional to MCLK (**Note 2**)
Shutdown Current, Analog	$I_{DDS,A}$	—	0.01	2	µA	AV_{DD} pin only (**Note 3**)
Shutdown Current, Digital	$I_{DDS,D}$	—	0.01	7	µA	DV_{DD} pin only (**Note 3**)
Pull-down Current on OSC2 Pin (External Clock mode only)	I_{OSC2}	—	35	—	µA	CLKEXT = 1

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 000000, RESET<5:0> = 000000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<5:0> = 111111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

1.2 Serial Interface Characteristics

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, C_{LOAD} = 30 pF, applies to all digital I/O.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
High-Level Input Voltage	V_{IH}	0.7 DV_{DD}	—	—	V	Schmitt-Triggered
Low-Level Input Voltage	V_{IL}	—	—	0.3 DV_{DD}	V	Schmitt-Triggered
Input Leakage Current	I_{LI}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{IN} = D_{GND} to DV_{DD}
Output Leakage Current	I_{LO}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{OUT} = D_{GND} or DV_{DD}
Hysteresis Of Schmitt-Trigger Inputs	V_{HYS}	—	500	—	mV	DV_{DD} = 3.3V only, **Note 2**
Low-Level Output Voltage	V_{OL}	—	—	0.2 DV_{DD}	V	I_{OL} = +1.7 mA
High-Level Output Voltage	V_{OH}	0.8 DV_{DD}	—	—	V	I_{OH} = -1.7 mA
Internal Capacitance (All Inputs And Outputs)	C_{INT}	—	—	7	pF	T_A = +25°C, SCK = 1.0 MHz, DV_{DD} =3.3V (**Note 1**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-3: SERIAL AC CHARACTERISTICS TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, GAIN = 1, C_{LOAD} = 30 pF						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Serial Clock Frequency	f_{SCK}	—	—	20	MHz	
$\overline{CS}$ Setup Time	t_{CSS}	25	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	50	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	50	—	—	ns	
Data Setup Time	t_{SU}	5	—	—	ns	
Data Hold Time	t_{HD}	10	—	—	ns	
Serial Clock High Time	t_{HI}	20	—	—	ns	
Serial Clock Low Time	t_{LO}	20	—	—	ns	
Serial Clock Delay Time	t_{CLD}	50	—	—	ns	
Serial Clock Enable Time	t_{CLE}	50	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	25	ns	
Output Hold Time	t_{HO}	0	—	—	ns	**Note 1**
Output Disable Time	t_{DIS}	—	—	25	ns	**Note 1**
Reset Pulse Width ($\overline{RESET}$)	t_{MCLR}	100	—	—	ns	
Data Transfer Time to $\overline{DR}$ (Data Ready)	t_{DODR}	—	—	25	ns	**Note 2**
Modulator Mode Entry to Modulator Data Present	t_{MODSU}	—	—	100	ns	
Data Ready Pulse Low Time	t_{DRP}	—	1/(2 x DMCLK)	—	µs	

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7 to 3.6V, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units.**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28L SSOP	θ_{JA}	—	80	—	°C/W	
Thermal Resistance, 40L 5x5 UQFN	θ_{JA}	—	41	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

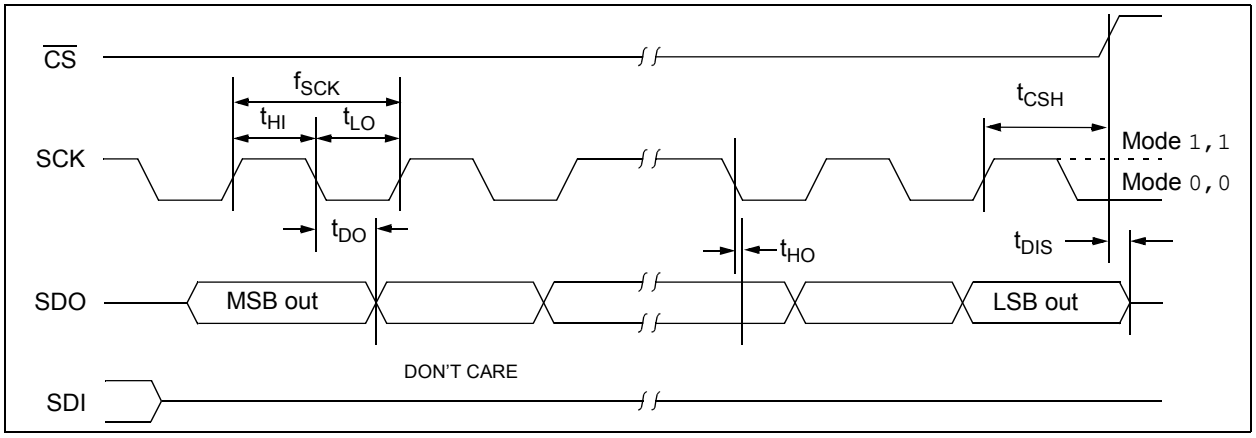


FIGURE 1-1: *Serial Output Timing Diagram.*

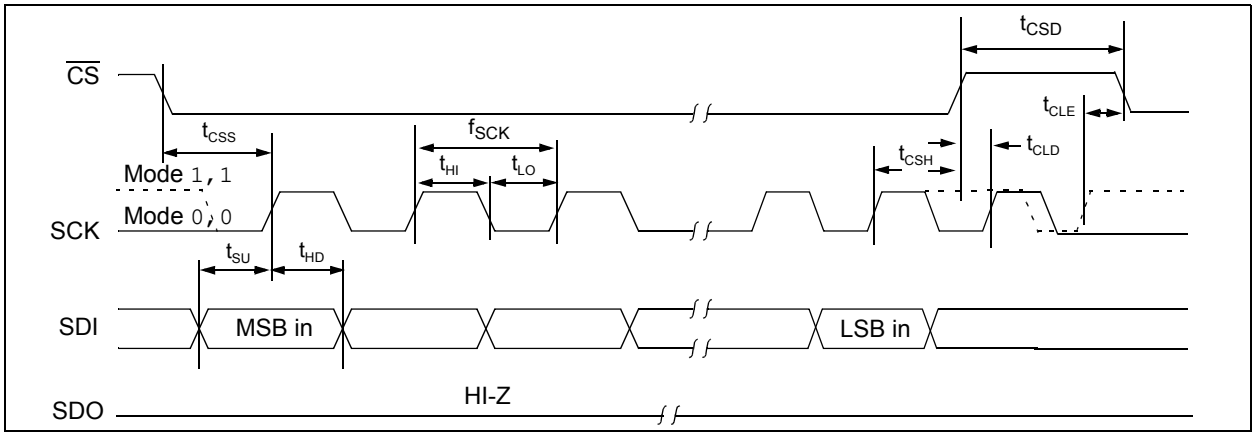


FIGURE 1-2: *Serial Input Timing Diagram.*

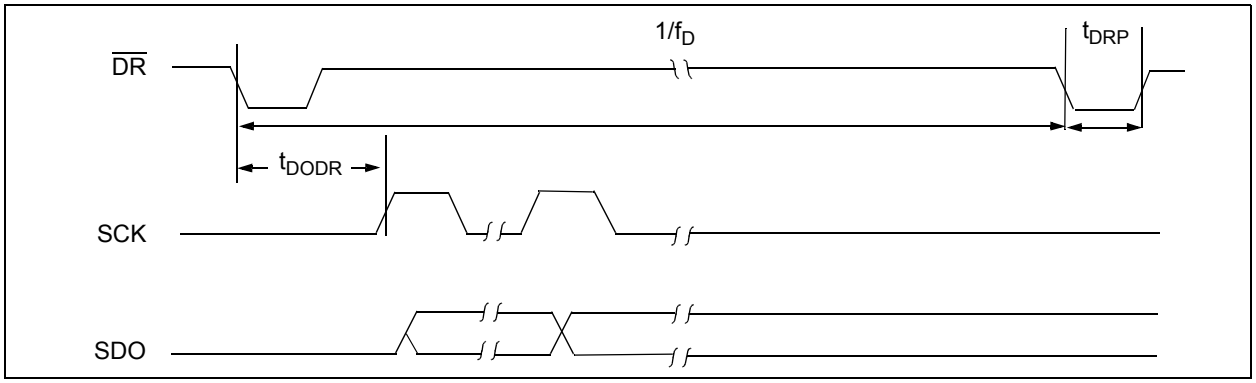


FIGURE 1-3: *Data Ready Pulse / Sampling Timing Diagram.*

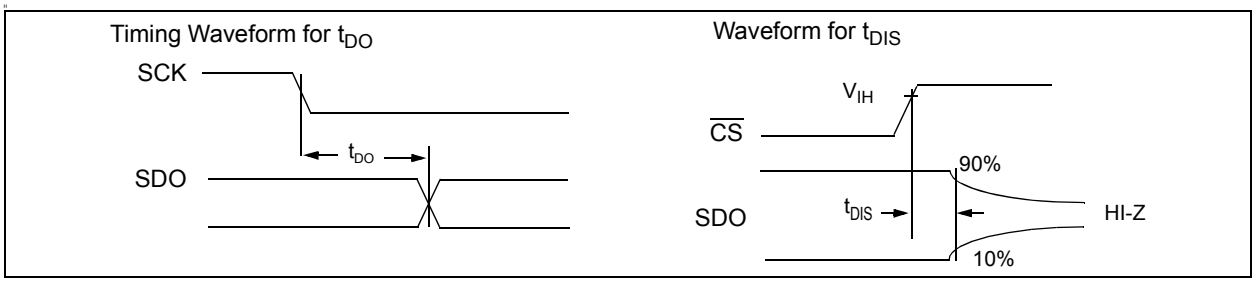


FIGURE 1-4: *Timing Diagrams, continued.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

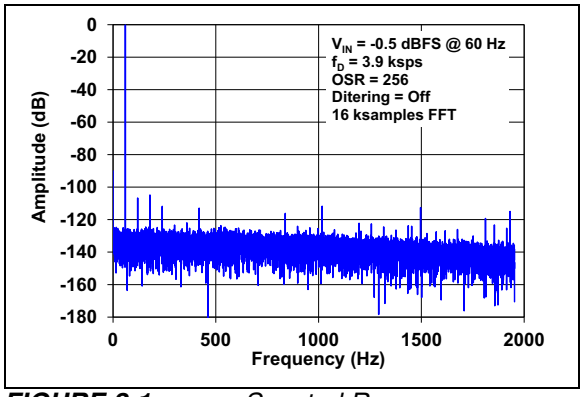


FIGURE 2-1: *Spectral Response.*

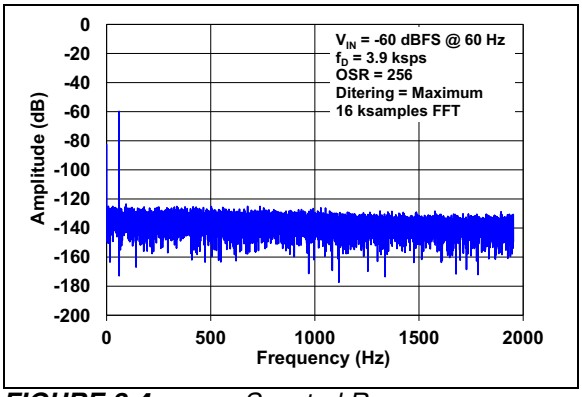


FIGURE 2-4: *Spectral Response.*

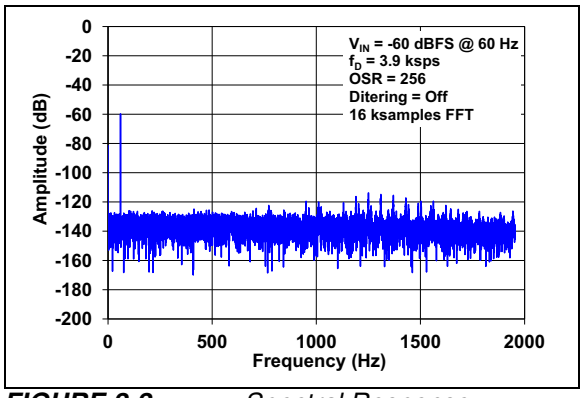


FIGURE 2-2: *Spectral Response.*

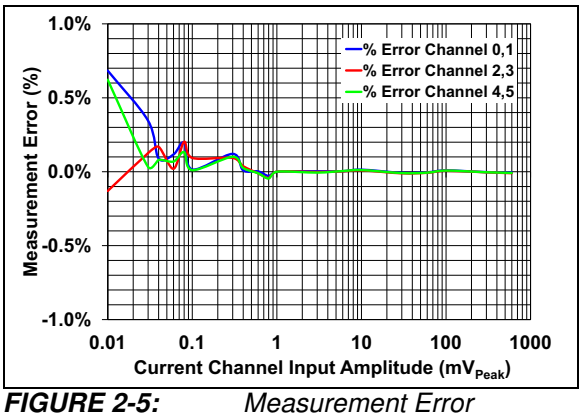


FIGURE 2-5: *Measurement Error with 1-Point Calibration.*

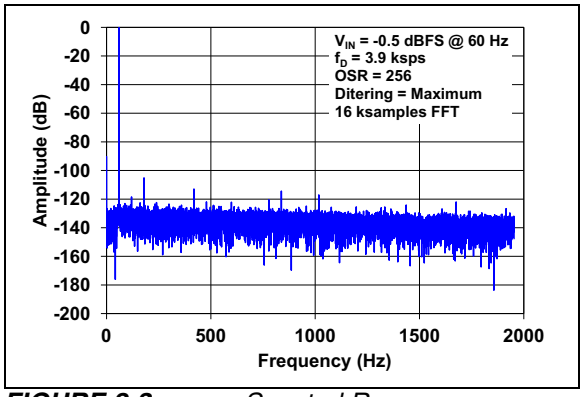


FIGURE 2-3: *Spectral Response.*

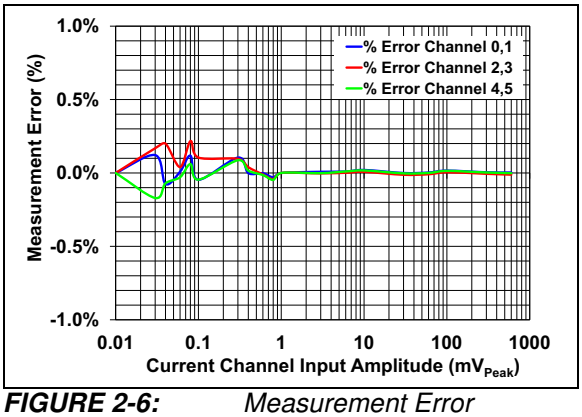


FIGURE 2-6: *Measurement Error with 2-Point Calibration.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

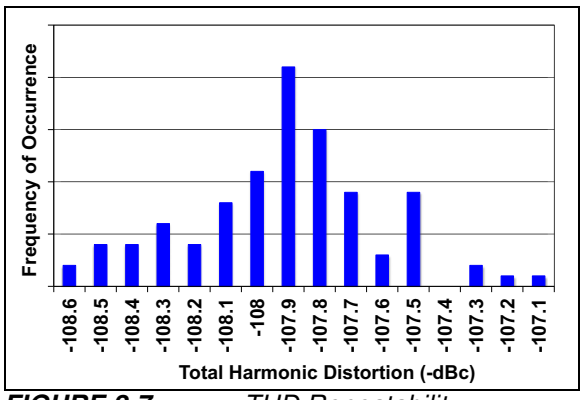


FIGURE 2-7: *THD Repeatability Histogram.*

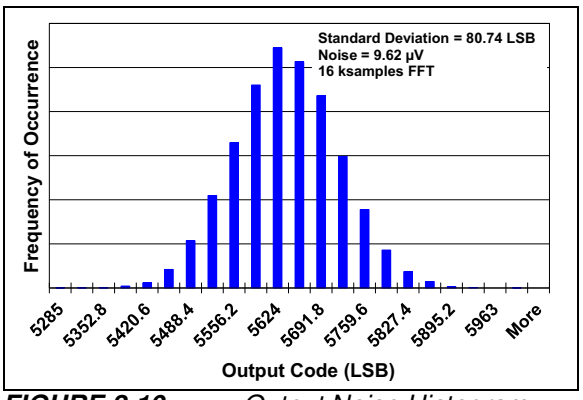


FIGURE 2-10: *Output Noise Histogram.*

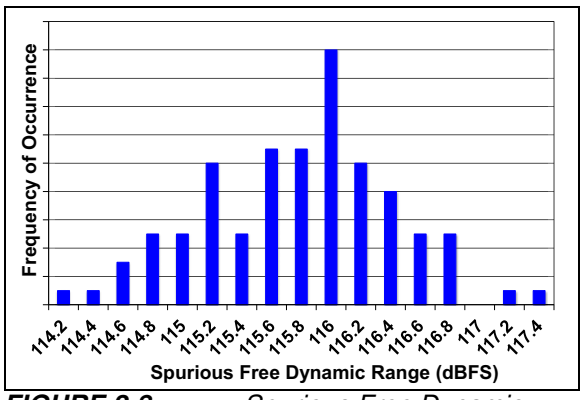


FIGURE 2-8: *Spurious Free Dynamic Range Repeatability Histogram.*

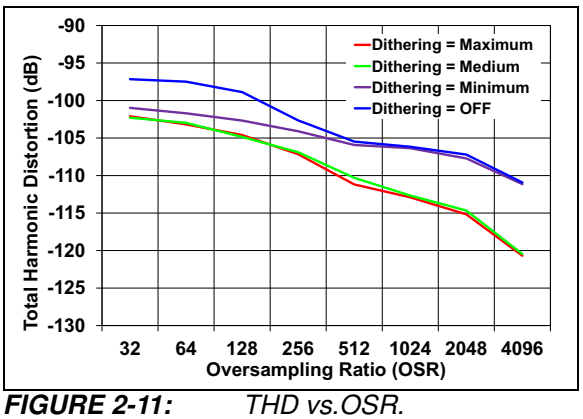


FIGURE 2-11: *THD vs.OSR.*

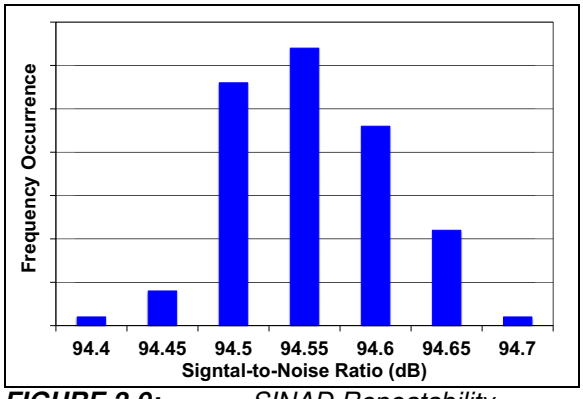


FIGURE 2-9: *SINAD Repeatability Histogram.*

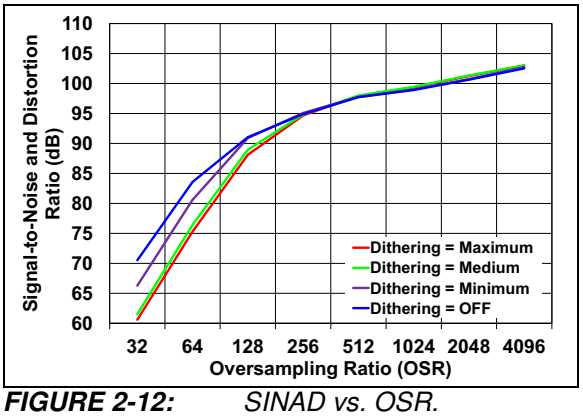


FIGURE 2-12: *SINAD vs. OSR.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

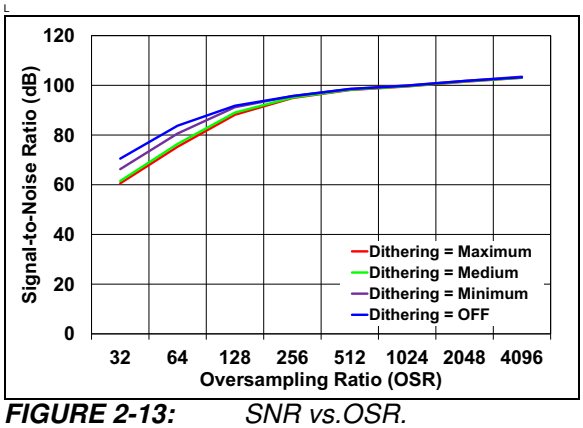


FIGURE 2-13: *SNR vs.OSR.*

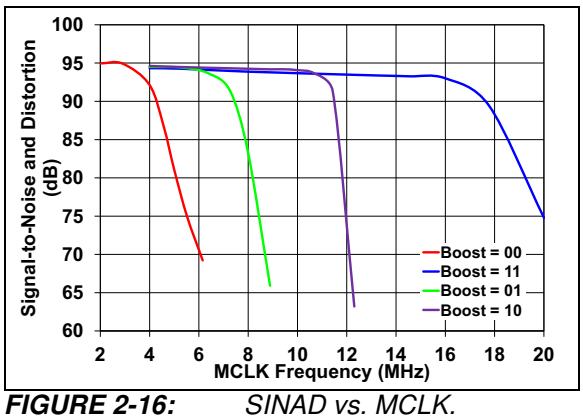


FIGURE 2-16: *SINAD vs. MCLK.*

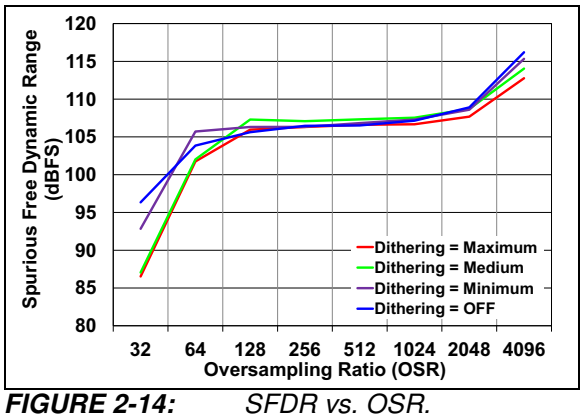


FIGURE 2-14: *SFDR vs. OSR.*

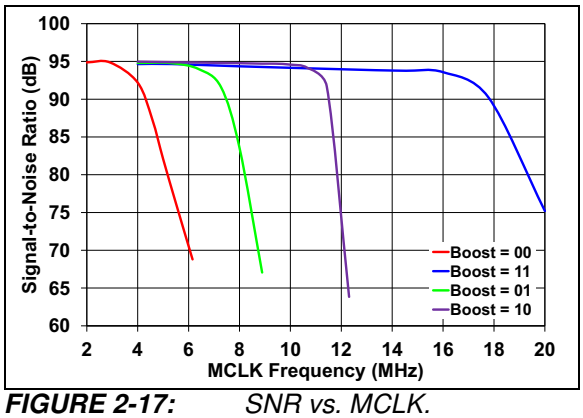


FIGURE 2-17: *SNR vs. MCLK.*

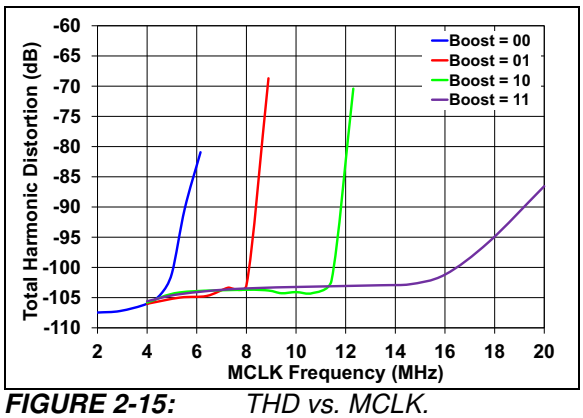


FIGURE 2-15: *THD vs. MCLK.*

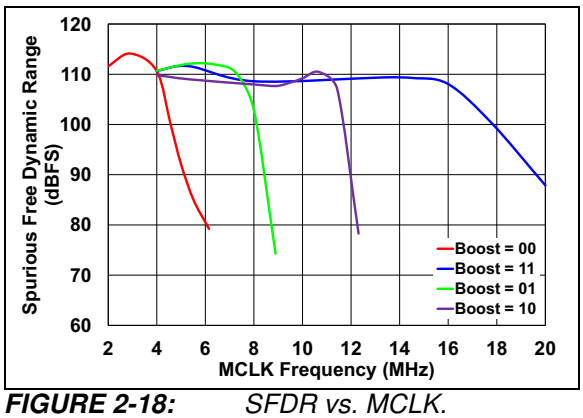


FIGURE 2-18: *SFDR vs. MCLK.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

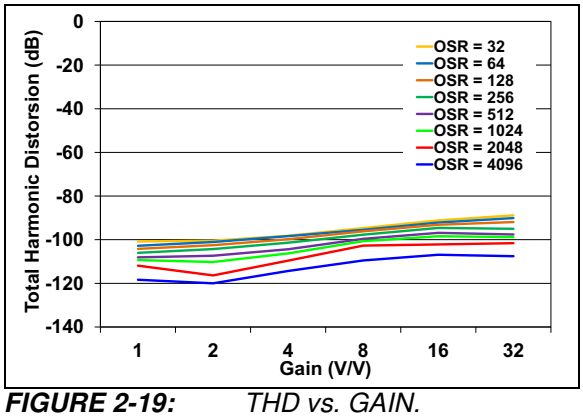


FIGURE 2-19: *THD vs. GAIN.*

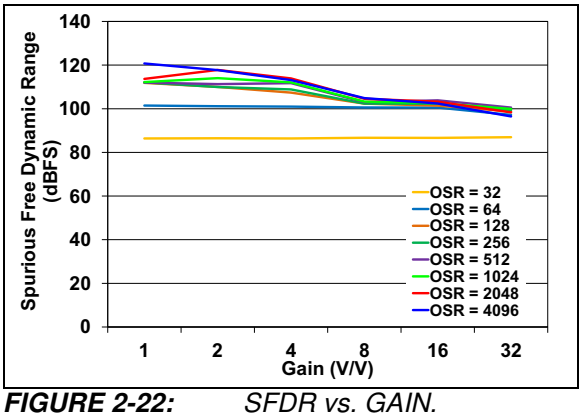


FIGURE 2-22: *SFDR vs. GAIN.*

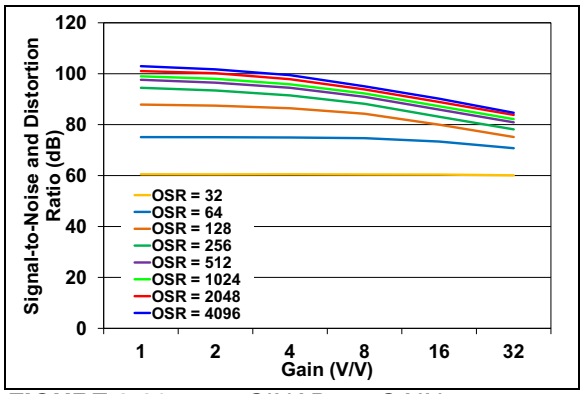


FIGURE 2-20: *SINAD vs. GAIN.*

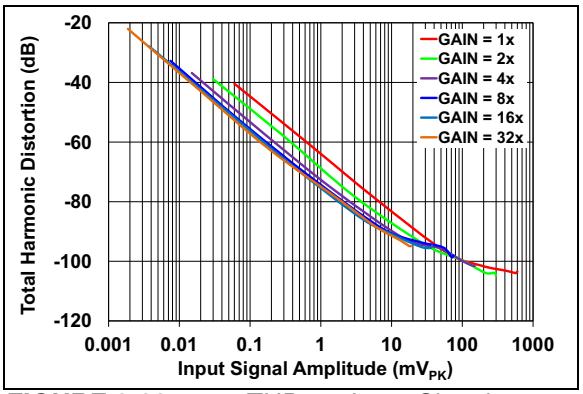


FIGURE 2-23: *THD vs. Input Signal Amplitude.*

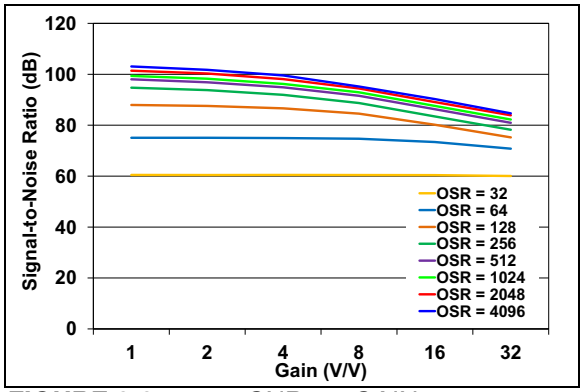


FIGURE 2-21: *SNR vs. GAIN.*

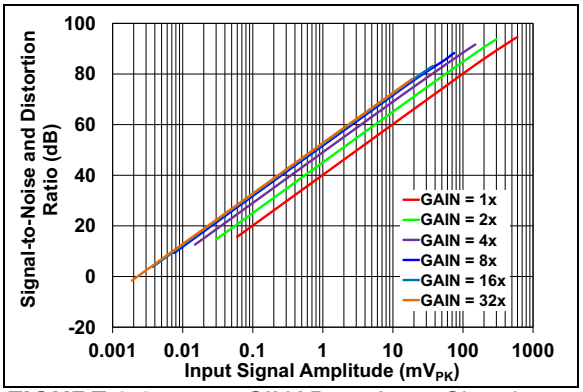


FIGURE 2-24: *SINAD vs. Input Signal Amplitude.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

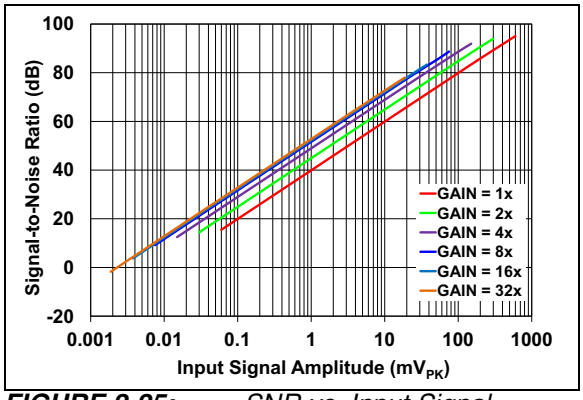


FIGURE 2-25: *SNR vs. Input Signal Amplitude.*

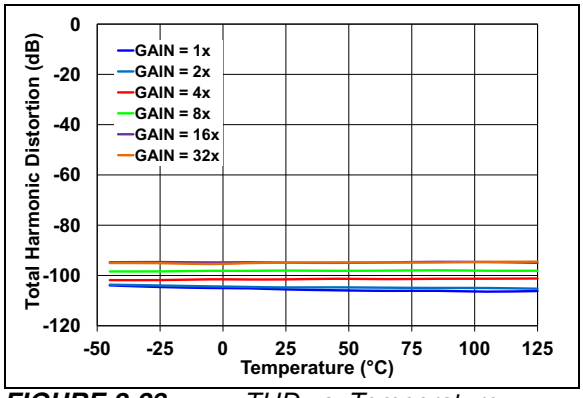


FIGURE 2-28: *THD vs. Temperature.*

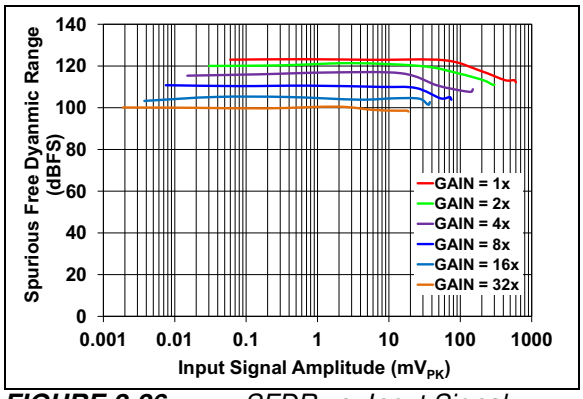


FIGURE 2-26: *SFDR vs. Input Signal Amplitude.*

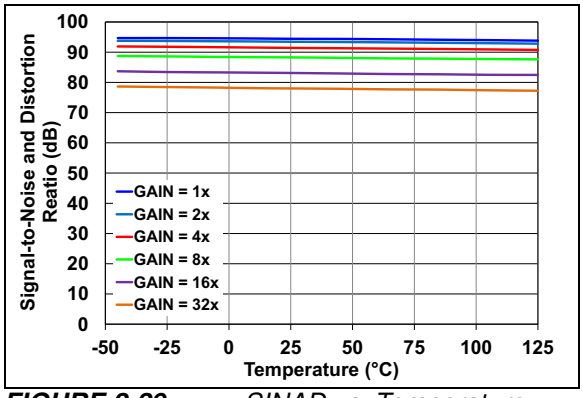


FIGURE 2-29: *SINAD vs. Temperature.*

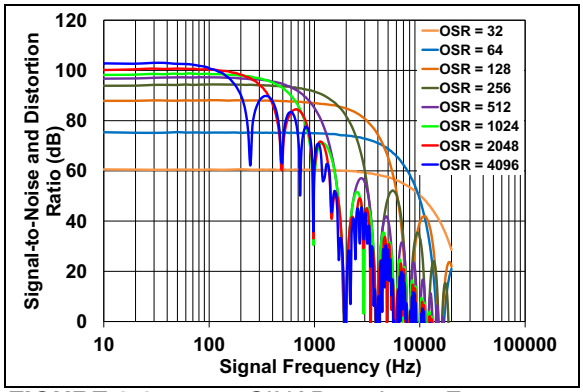


FIGURE 2-27: *SINAD vs. Input Frequency.*

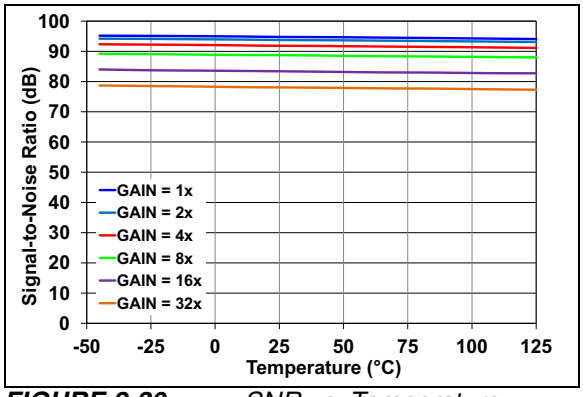


FIGURE 2-30: *SNR vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

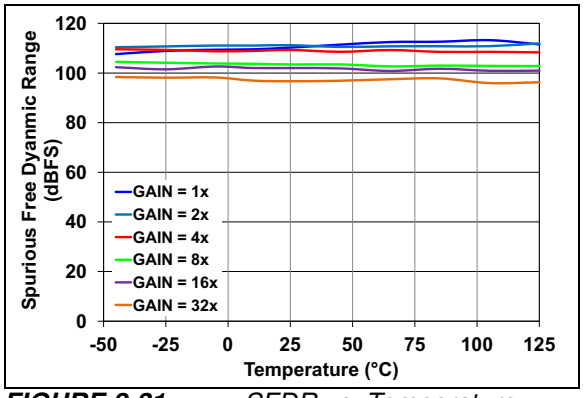


FIGURE 2-31: *SFDR vs. Temperature.*

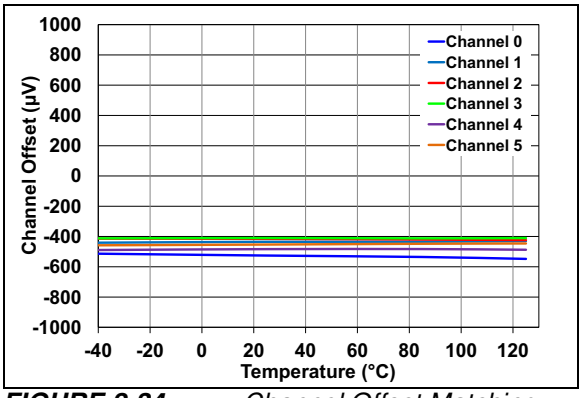


FIGURE 2-34: *Channel Offset Matching vs. Temperature.*

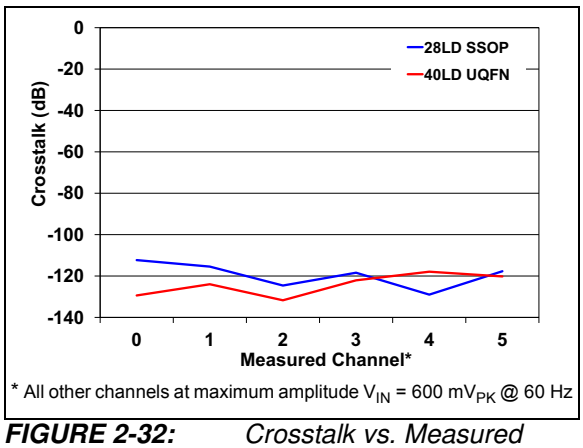


FIGURE 2-32: *Crosstalk vs. Measured Channel.*

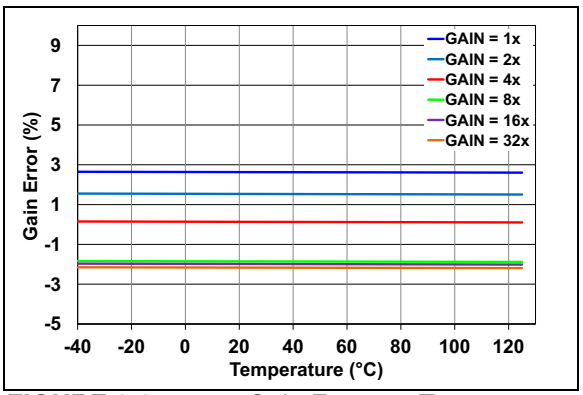


FIGURE 2-35: *Gain Error vs. Temperature vs. Gain.*

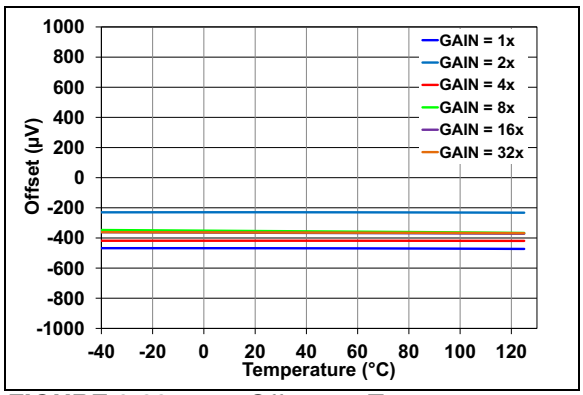


FIGURE 2-33: *Offset vs. Temperature vs. Gain.*

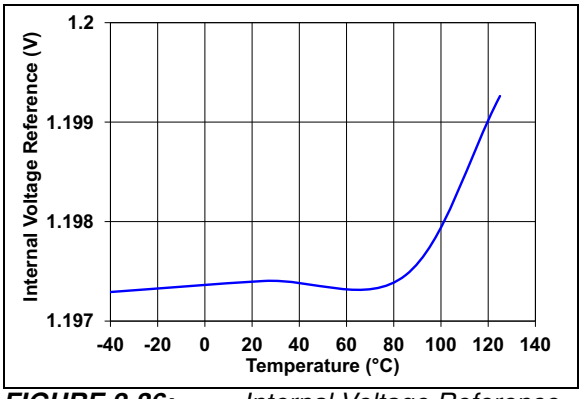


FIGURE 2-36: *Internal Voltage Reference vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

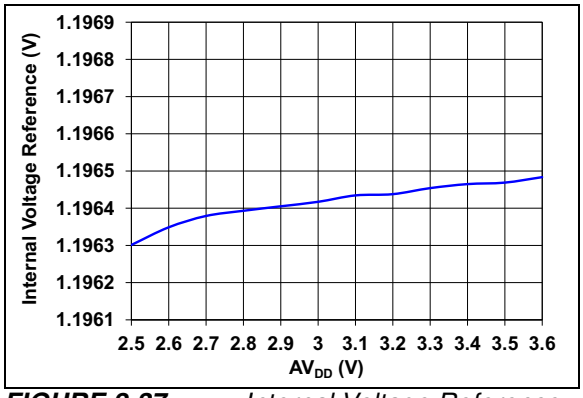


FIGURE 2-37: *Internal Voltage Reference vs. Supply Voltage.*

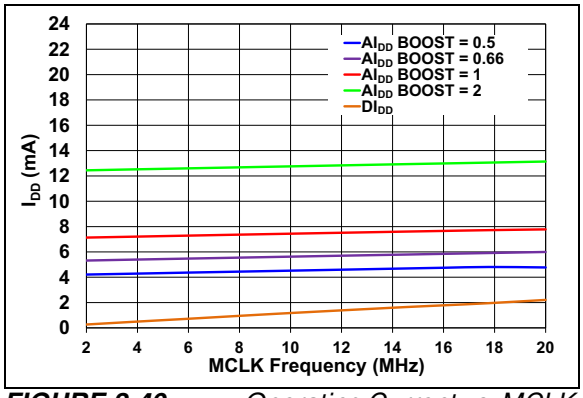


FIGURE 2-40: *Operating Current vs. MCLK Frequency vs. Boost, V_{DD} = 3.3V.*

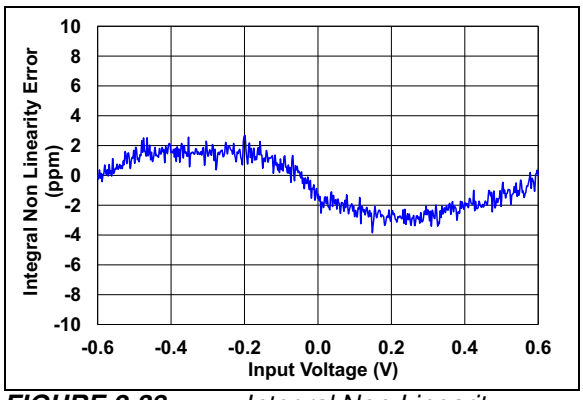


FIGURE 2-38: *Integral Non-Linearity (Dithering Maximum).*

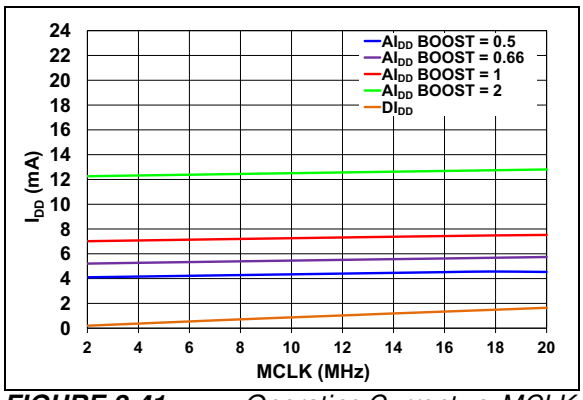


FIGURE 2-41: *Operating Current vs. MCLK Frequency vs. Boost, V_{DD} = 2.7V.*

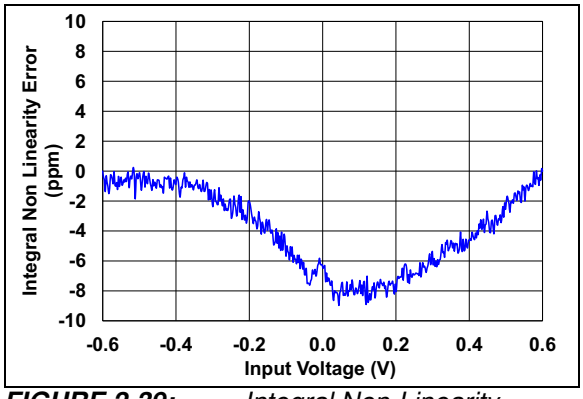


FIGURE 2-39: *Integral Non-Linearity (Dithering Off).*

NOTES:

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: SIX CHANNEL MCP3913 PIN FUNCTION TABLE

MCP3913 SSOP	MCP3913 UQFN	Symbol	Function
1	18, 35	AV_{DD}	Analog Power Supply Pin
2	37	CH0+	Non-Inverting Analog Input Pin for Channel 0
3	38	CH0-	Inverting Analog Input Pin for Channel 0
4	39	CH1-	Inverting Analog Input Pin for Channel 1
5	40	CH1+	Non-Inverting Analog Input Pin for Channel 1
6	1	CH2+	Non-Inverting Analog Input Pin for Channel 2
7	2	CH2-	Inverting Analog Input Pin for Channel 2
8	3	CH3-	Inverting Analog Input Pin for Channel 3
9	4	CH3+	Non-Inverting Analog Input Pin for Channel 3
10	7	CH4+	Non-Inverting Analog Input Pin for Channel 4
11	8	CH4-	Inverting Analog Input Pin for Channel 4
12	9	CH5-	Inverting Analog Input Pin for Channel 5
13	10	CH5+	Non-Inverting Analog Input Pin for Channel 5
14	15	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output Pin
15	16	REFIN-	Inverting Voltage Reference Input Pin
16	17, 36	A_{GND}	Analog Ground Pin, Return Path for Internal Analog Circuitry
17, 20	21, 24, 32	D_{GND}	Digital Ground Pin, Return Path for Internal Digital Circuitry
18	22	$\overline{DR}$	Data Ready Signal Output Pin
19	5, 6, 11, 12, 13, 14, 19, 23, 34	NC	No Connect (for better EMI results connect to A_{GND})
21	25	OSC1/CLKI	Oscillator Crystal Connection Pin or External Clock Input Pin
22	26	OSC2	Oscillator Crystal Connection Pin
23	27	$\overline{CS}$	Serial Interface Chip Select Input Pin
24	28	SCK	Serial Interface Clock Input Pin for SPI
25	29	SDO	Serial Interface Data Output Pin
26	30	SDI	Serial Interface Data Input Pin
27	31	$\overline{RESET}$	Master Reset Logic Input Pin
28	20, 33	DV_{DD}	Digital Power Supply Pin
—	41	EP	Exposed Thermal Pad. Must be connected to A_{GND} or floating.

3.1 Analog Power Supply (AV_{DD})

AV_{DD} is the power supply voltage for the analog circuitry within the MCP3913. It is distributed on several pins (pins 18 and 35 in the UQFN package, one pin only in the SSOP-28 package). For optimal performance, connect these pins together using a star connection, and connect the appropriate bypass capacitors (typically a 10 µF in parallel with a 0.1 µF ceramic). AV_{DD} should be maintained between 2.7V and 3.6V for specified operation.

To ensure proper functionality of the device, at least one of these pins must be properly connected. To ensure optimal performance of the device, all the pins must be properly connected. If any of these pins are left floating, the accuracy and noise specifications are not ensured.

3.2 ADC Differential Analog Inputs (CHn+/CHn-)

The CHn+/- pins (n comprised between 0 and 5) are the six fully-differential analog voltage inputs for the delta-sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each CHn+/- input pin is ±1V with no distortion, and ±2V with no breaking after continuous voltage. This maximum absolute voltage is not proportional to the V_{REF} voltage.

3.3 Non-Inverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for all ADCs or the internal voltage reference output.

When VREFEXT = 1, an external voltage reference source can be used, and the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its V_{REF+} pin. When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = 0, the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability and thus needs proper buffering and bypass capacitances (a 0.1 µF ceramic capacitor is sufficient in most cases), if used as a voltage source.

If the voltage reference is only used as an internal V_{REF}, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy, but a minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin if left floating.

3.4 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for all ADCs. When using an external differential voltage reference, it should be connected to its V_{REF-} pin. When using an external single-ended voltage reference, or when VREFEXT = 0 (default) and using the internal voltage reference, the pin should be directly connected to A_{GND}.

3.5 Analog Ground (A_{GND})

A_{GND} is the ground reference voltage for the analog circuitry within the MCP3913. It is distributed on several pins (pins 17 and 36 in the UQFN package, one pin only in the SSOP-28 package). For optimal performance, it is recommended to connect these pins together using a star connection, and to connect it to the same ground node voltage as D_{GND}, again preferably with a star connection.

At least one of these pins need to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured. If an analog ground plane is available, it is recommended that these pins be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

3.6 Digital Ground (D_{GND})

D_{GND} is the ground reference voltage for the digital circuitry within the MCP3913. It is distributed on several pins: 21, 24 and 32 in the UQFN package (two pins only in the SSOP-28 package). For optimal performance, connect these pins together using a star connection and connect it to the same ground node voltage as A_{GND}, again preferably with a star connection.

At least one of these pins need to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured. If a digital ground plane is available, it is recommended that these pins be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

3.7 Data Ready Output ($\overline{DR}$)

The data ready pin indicates if a new conversion result is ready to be read. The default state of this pin is logic high when $\overline{DR\_HIZ}$ = 1, and is high-impedance when $\overline{DR\_HIZ}$ = 0 (default). After each conversion is finished, a logic low pulse will take place on the data ready pin to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The data ready pin is independent of the SPI interface and acts like an interrupt output. The data ready pin state is not latched, and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate, and internal clock prescale settings. The data ready pulse width is equal to half a DMCLK period and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

Note:	This pin should not be left floating when the $\overline{DR\_HIZ}$ bit is low; a 100 kΩ pull-up resistor connected to DV_{DD} is recommended.

3.8 Oscillator and Master Clock Input Pin (OSC1/CLKI)

OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = 0, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation.

The typical clock frequency specified is 4 MHz. For proper operation, and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 for the function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2. Appropriate load capacitance should be connected to these pins for proper operation.

Note:	When CLKEXT = 1, the crystal oscillator is disabled. OSC1 becomes the master clock input CLKI, a direct path for an external clock source. One example would be a clock source generated by an MCU.

3.9 Crystal Oscillator (OSC2)

When CLKEXT = 0 (default), a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation. Appropriate load capacitance should be connected to these pins for proper operation.

When CLKEXT = 1, this pin should be connected to D_{GND} at all times (an internal pull down operates this function, if the pin is left floating).

3.10 Chip Select ($\overline{CS}$)

This pin is the Serial Peripheral Interface (SPI) chip select that enables serial communication. When this pin is logic high, no communication can take place. A chip select falling edge initiates serial communication, and a chip select rising edge terminates the communication. No communication can take place even when $\overline{CS}$ is logic low, if $\overline{RESET}$ is also logic low.

This input is Schmitt-triggered.

3.11 Serial Data Clock (SCK)

This is the serial clock pin for SPI communication. Data is clocked into the device on the rising edge of SCK. Data is clocked out of the device on the falling edge of SCK.

The MCP3913 SPI interface is compatible with SPI 0,0 and 1,1 modes. SPI modes can be changed during a $\overline{CS}$ high time.

The maximum clock speed specified is 20 MHz. SCK and MCLK are two different and asynchronous clocks; SCK is only required when a communication happens, while MCLK is continuously required when the part is converting analog inputs.

This input is Schmitt-triggered.

3.12 Serial Data Output (SDO)

This is the SPI data output pin. Data is clocked out of the device on the falling edge of SCK.

This pin remains in a high-impedance state during the command byte. It also stays high-impedance during the entire communication for write commands and when the $\overline{CS}$ pin is logic high, or when the $\overline{RESET}$ pin is logic low. This pin is active only when a read command is processed. The interface is half-duplex (inputs and outputs do not happen at the same time).

3.13 Serial Data Input (SDI)

This is the SPI data input pin. Data is clocked into the device on the rising edge of SCK. When $\overline{CS}$ is logic low, this pin is used to communicate with a series of 8-bit commands. The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge followed by an 8-bit command word, entered through the SDI pin. Each command is either a Read or a Write command. Toggling SDI after a Read command or when $\overline{CS}$ is logic high has no effect.

This input is Schmitt-triggered.

3.14 Master Reset ($\overline{\text{RESET}}$)

This pin is active low and places the entire chip in a Reset state when active.

When $\overline{\text{RESET}}$ is logic low, all registers are reset to their default value, no communication can take place, and no clock is distributed inside the part, except in the input structure if MCLK is applied (if MCLK is idle, then no clock is distributed). This state is equivalent to a Power-On Reset (POR) state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{\text{RESET}}$ is logic low is equivalent to when $\overline{\text{RESET}}$ is logic high. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic, and is reduced drastically when there is no clock running.

All the analog biases are enabled during a Reset, so that the part is fully operational just after a $\overline{\text{RESET}}$ rising edge, if MCLK is applied when $\overline{\text{RESET}}$ is logic low. If MCLK is not applied, there is a time after a hard reset when the conversion may not accurately correspond to the startup of the input structure.

This input is Schmitt-triggered.

3.15 Digital Power Supply (DV_{DD})

DV_{DD} is the power supply voltage for the digital circuitry within the MCP3913. It is distributed on several pins (pins 20 and 33 in the UQFN package, one pin only in the SSOP-28 package). For optimal performance, it is recommended to connect these pins together using a star connection and to connect appropriate bypass capacitors (typically a 10 µF in parallel with a 0.1 µF ceramic). DV_{DD} should be maintained between 2.7V and 3.6V for specified operation.

At least one of these pins need to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured.

3.16 Exposed Thermal Pad

This pin must be connected to A_{GND} or left floating for proper operation. Connecting it to A_{GND} is preferable for lowest noise performance and best thermal behavior.

4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

- **MCLK – Master Clock**
- **AMCLK – Analog Master Clock**
- **DMCLK – Digital Master Clock**
- **DRCLK – Data Rate Clock**
- **OSR – Oversampling Ratio**
- **Offset Error**
- **Gain Error**
- **Integral Non-Linearity Error**
- **Signal-to-Noise Ratio (SNR)**
- **Signal-To-Noise Ratio And Distortion (SINAD)**
- **Total Harmonic Distortion (THD)**
- **Spurious-Free Dynamic Range (SFDR)**
- **MCP3913 Delta-Sigma Architecture**
- **Idle Tones**
- **Dithering**
- **Crosstalk**
- **PSRR**
- **CMRR**
- **ADC Reset Mode**
- **Hard Reset Mode (RESET = 0)**
- **ADC Shutdown Mode**
- **Full Shutdown Mode**
- **Measurement Error**

4.1 MCLK – Master Clock

This is the fastest clock present on the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0, or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1. See Figure 4-1.

4.2 AMCLK – Analog Master Clock

AMCLK is the clock frequency that is present on the analog portion of the device, after prescaling has occurred via the CONFIG0 PRE<1:0> register bits (see Equation 4-1). The analog portion includes the PGAs and the delta-sigma modulators.

EQUATION 4-1:

$$AMCLK = \frac{MCLK}{PRESCALE}$$

TABLE 4-1: MCP3913 OVERSAMPLING RATIO SETTINGS

Config. PRE<1:0>		Analog Master Clock Prescale
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8

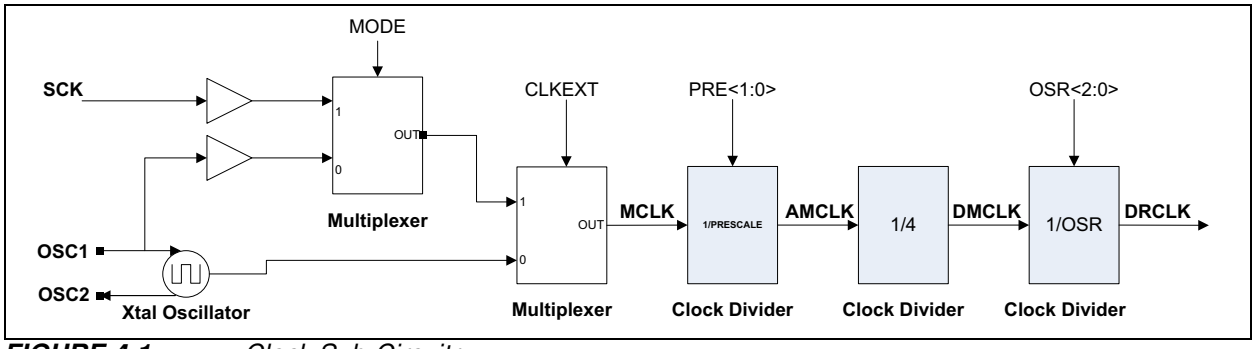


FIGURE 4-1: *Clock Sub-Circuitry.*

4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device, after prescaling and division by four (Equation 4-2). This is also the sampling frequency, which is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output. See Figure 4-1.

EQUATION 4-2:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

4.4 DRCLK – Data Rate Clock

This is the output data rate, i.e., the rate at which the ADCs output new data. Each new data is signaled by a data ready pulse on the $\overline{DR}$ pin.

This data rate is depending on the OSR and the prescaler with the formula in Equation 4-3.

EQUATION 4-3:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate, and because the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

Table 4-2 describes the various combinations of OSR and PRESCALE, and their associated AMCLK, DMCLK and DRCLK rates.

TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE, MCLK = 4 MHZ

PRE<1:0>		OSR<2:0>			OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)	SINAD (dB) Note 1	ENOB from SINAD (bits) Note 1
1	1	1	1	1	4096	MCLK/8	MCLK/32	MCLK/131072	.035	102.5	16.7
1	1	1	1	0	2048	MCLK/8	MCLK/32	MCLK/65536	.061	100	16.3
1	1	1	0	1	1024	MCLK/8	MCLK/32	MCLK/32768	.122	97	15.8
1	1	1	0	0	512	MCLK/8	MCLK/32	MCLK/16384	.244	96	15.6
1	1	0	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.488	95	15.5
1	1	0	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976	91	14.8
1	1	0	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95	84	13.6
1	1	0	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9	70	11.3
1	0	1	1	1	4096	MCLK/4	MCLK/16	MCLK/65536	.061	102.5	16.7
1	0	1	1	0	2048	MCLK/4	MCLK/16	MCLK/32768	.122	100	16.3
1	0	1	0	1	1024	MCLK/4	MCLK/16	MCLK/16384	.244	97	15.8
1	0	1	0	0	512	MCLK/4	MCLK/16	MCLK/8192	.488	96	15.6
1	0	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976	95	15.5
1	0	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95	91	14.8
1	0	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9	84	13.6
1	0	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125	70	11.3
0	1	1	1	1	4096	MCLK/2	MCLK/8	MCLK/32768	.122	102.5	16.7
0	1	1	1	0	2048	MCLK/2	MCLK/8	MCLK/16384	.244	100	16.3
0	1	1	0	1	1024	MCLK/2	MCLK/8	MCLK/8192	.488	97	15.8
0	1	1	0	0	512	MCLK/2	MCLK/8	MCLK/4096	.976	96	15.6
0	1	0	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95	95	15.5
0	1	0	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9	91	14.8
0	1	0	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125	84	13.6
0	1	0	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625	70	11.3
0	0	1	1	1	4096	MCLK	MCLK/4	MCLK/16384	.244	102.5	16.7
0	0	1	1	0	2048	MCLK	MCLK/4	MCLK/8192	.488	100	16.3
0	0	1	0	1	1024	MCLK	MCLK/4	MCLK/4096	.976	97	15.8
0	0	1	0	0	512	MCLK	MCLK/4	MCLK/2048	1.95	96	15.6
0	0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9	95	15.5
0	0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125	91	14.8
0	0	0	0	1	64	MCLK	MCLK/4	MCLK/256	15.625	84	13.6
0	0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25	70	11.3

Note 1: For OSR = 32 and 64, DITHER = None. For OSR = 128 and higher, DITHER = Maximum. The SINAD values are given from GAIN = 1.

4.5 OSR – Oversampling Ratio

This is the ratio of the sampling frequency to the output data rate; OSR = DMCLK/DRCLK. The default OSR<2:0> is 256, or with MCLK = 4 MHz, PRESCALE = 1, AMCLK = 4 MHz, f_S = 1 MHz, and f_D = 3.90625 ksps. The OSR<2:0> bits in Table 4-3 in the CONFIG0 register are used to change the oversampling ratio (OSR).

TABLE 4-3: MCP3913 OVERSAMPLING RATIO SETTINGS

OSR<2:0>			Oversampling Ratio OSR
0	0	0	32
0	0	1	64
0	1	0	128
0	1	1	256 (Default)
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip-to-chip. The offset is specified in µV. The offset error can be digitally compensated independently on each channel through the OFFCAL_CHn registers with a 24-bit calibration word.

The offset on the MCP3913 has a low-temperature coefficient.

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in %, compared to the ideal transfer function defined in Equation 5-3. The specification incorporates both PGA and ADC gain error contributions, but not the V_{REF} contribution (it is measured with an external V_{REF}).

This error varies with PGA and OSR settings. The gain error can be digitally compensated independently on each channel through the GAINCAL_CHn registers with a 24-bit calibration word.

The gain error on the MCP3913 has a low temperature coefficient.

4.8 Integral Non-Linearity Error

Integral non-linearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

4.9 Signal-to-Noise Ratio (SNR)

For the MCP3913 ADCs, the signal-to-noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal), when the input is a sine wave at a predetermined frequency (see Equation 4-4). It is measured in dB. Usually, only the maximum signal-to-noise ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

EQUATION 4-4: SIGNAL-TO-NOISE RATIO

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

4.10 Signal-To-Noise Ratio And Distortion (SINAD)

The most important Figure of Merit for analog performance of the ADCs present on the MCP3913 is the Signal-to-Noise And Distortion (SINAD) specification.

The Signal-to-Noise And Distortion ratio is similar to signal-to-noise ratio, with the exception that you must include the harmonic's power in the noise power calculation (see Equation 4-5). The SINAD specification depends mainly on the OSR and DITHER settings.

EQUATION 4-5: SINAD EQUATION

$$SINAD(dB) = 10log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD, see Equation 4-6.

EQUATION 4-6: SINAD, THD AND SNR RELATIONSHIP

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

4.11 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the output harmonic's power to the fundamental signal power for a sine wave input, and is defined in Equation 4-7.

EQUATION 4-7:

$$THD(dB) = 10log\left(\frac{HarmonicsPower}{FundamentalPower}\right)$$

The THD calculation includes the first 35 harmonics for the MCP3913 specifications. The THD is usually measured only with respect to the ten first harmonics, which leads artificially to better figures. THD is sometimes expressed in %. Equation 4-8 converts the THD in %.

EQUATION 4-8:

$$THD(\%) = 100 \times 10^{\frac{THD(dB)}{20}}$$

This specification depends mainly on the DITHER setting.

4.12 Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio between the output power of the fundamental and the highest spur in the frequency spectrum (see Equation 4-9). The spur frequency is not necessarily a harmonic of the fundamental, even though it is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the DITHER setting.

EQUATION 4-9:

$$SFDR(dB) = 10log\left(\frac{FundamentalPower}{HighestSpurPower}\right)$$

4.13 MCP3913 Delta-Sigma Architecture

The MCP3913 incorporates six delta-sigma ADCs with a multi-bit architecture. A delta-sigma ADC is an oversampling converter that incorporates a built-in modulator, which digitizes the quantity of charges integrated by the modulator loop (see Figure 5-1). The quantizer is the block that is performing the analog-to-digital conversion. The quantizer is typically 1-bit, or a simple comparator, which helps maintain the linearity performance of the ADC (the DAC structure is, in this case, inherently linear).

Multi-bit quantizers help to lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. However, typically, the linearity of such architectures is more difficult to achieve since the DAC linearity is as difficult to attain, and its linearity limits the THD of such ADCs.

The quantizer present in each ADC channel in the MCP3913 is a Flash ADC composed of four comparators arranged with equally spaced thresholds and a thermometer coding. The MCP3913 also includes proprietary five-level DAC architecture that is inherently linear for improved THD figures.

4.14 Idle Tones

A delta-sigma converter is an integrating converter. It also has a finite quantization step (LSB) that can be detected by its quantizer. A DC input voltage that is below the quantization step should only provide an all zeros result, since the input is not large enough to be detected. As an integrating device, any delta-sigma ADC will show idle tones. This means that the output will have spurs in the frequency content that depend on the ratio between quantization step voltage and the input voltage. These spurs are the result of the integrated sub-quantization step inputs that will eventually cross the quantization steps after a long enough integration. This will induce an AC frequency at the output of the ADC, and can be shown in the ADC output spectrum.

These idle tones are residues that are inherent to the quantization process and the fact that the converter is integrating at all times without being reset. They are residues of the finite resolution of the conversion process. They are very difficult to attenuate and they are heavily signal dependent. They can degrade the SFDR and THD of the converter, even for DC inputs. They can be localized in the baseband of the converter and are thus difficult to filter from the actual input signal.

For power metering applications, idle tones can be very disturbing, because energy can be detected even at the 50 or 60 Hz frequency, depending on the DC offset of the ADCs, while no power is really present at the inputs. The only practical way to suppress or attenuate the idle tones phenomenon is to apply dithering to the ADC. The amplitudes of the idle tones are a function of the order of the modulator, the OSR and the number of levels in the quantizer of the modulator. A higher order, a higher OSR or a higher number of levels for the quantizer will attenuate the amplitudes of the idle tones.

4.15 Dithering

In order to suppress or attenuate the idle tones present in any delta-sigma ADCs, dithering can be applied to the ADC. Dithering is the process of adding an error to the ADC feedback loop in order to "decorrelate" the outputs and "break" the idle tone's behavior. Usually a random or pseudo-random generator adds an analog or digital error to the feedback loop of the delta-sigma ADC in order to ensure that no tonal behavior can happen at its outputs. This error is filtered by the feedback loop and typically has a zero average value, so that the converter static transfer function is not disturbed by the dithering process. However, the dithering process slightly increases the noise floor (it adds noise to the part) while reducing its tonal behavior and thus improving SFDR and THD. The dithering process scrambles the idle tones into baseband white noise and ensures that dynamic specs (SNR, SINAD, THD, SFDR) are less signal dependent. The MCP3913 incorporates a proprietary dithering algorithm on all ADCs in order to remove idle tones and improve THD, which is crucial for power metering applications.

4.16 Crosstalk

Crosstalk is defined as the perturbation caused on one ADC channel by all the other ADC channels present in the chip. It is a measurement of the isolation between each channel present in the chip.

This measurement is a two-step procedure:

1. Measure one ADC input with no perturbation on the other ADC (ADC inputs shorted).
2. Measure the same ADC input with a perturbation sine wave signal on all the other ADCs at a certain predefined frequency.

Crosstalk is the ratio between the output power of the ADC when the perturbation is and is not present, divided by the power of the perturbation signal. A lower crosstalk value implies more independence and isolation between the channels.

The measurement of this signal is performed under the default conditions of MCLK = 4 MHz:

- GAIN = 1
- PRESCALE = 1
- OSR = 256
- MCLK = 4 MHz

Step 1 for CH0 Crosstalk Measurement:

- CH0+ = CH0- = AGND
- CHn+ = CHn- = AGND
  n comprised between 1 and 5

Step 2 for CH0 Crosstalk Measurement:

- CH0+ = CH0-=AGND
- CHn+ - CHn- = 1.2V_{P-P} @ 50/60 Hz (full-scale sine wave), n comprised between 1 and 5

The crosstalk for Channel 0 is then calculated with the formula in Equation 4-10.

EQUATION 4-10:

$$CTalk(dB) = 10log\left(\frac{\Delta CH0Power}{\Delta CHnPower}\right)$$

The crosstalk depends slightly on the position of the channels in the MCP3913 device. This dependency is shown in the Figure 2-32, where the inner channels show more crosstalk than the outer channels, since they are located closer to the perturbation sources. The outer channels have the preferred locations to minimize crosstalk.

4.17 PSRR

This is the ratio between a change in the power supply voltage and the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs.

The PSRR specification can be DC (the power supply is taking multiple DC values), or AC (the power supply is a sine wave at a certain frequency with a certain common mode). In AC, the amplitude of the sine wave represents the change in the power supply. It is defined in Equation 4-11.

EQUATION 4-11:

$$PSRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where: V_{OUT} is the equivalent input voltage that the output code translates to, with the ADC transfer function.

In the MCP3913 specification for DC PSRR, AV_{DD} varies from 2.7V to 3.6V, and for AC PSRR, a 50/60 Hz sine wave is chosen centered around 3.0V, with a maximum 300 mV amplitude. The PSRR specification is measured with AV_{DD} = DV_{DD}.

4.18 CMRR

CMRR is the ratio between a change in the common-mode input voltage and the ADC output codes. It measures the influence of the common-mode input voltage on the ADC outputs.

The CMRR specification can be DC (the common-mode input voltage is taking multiple DC values) or AC (the common-mode input voltage is a sine wave at a certain frequency with a certain common mode). In AC, the amplitude of the sine wave represents the change in the power supply. It is defined in Equation 4-12.