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## 3V Single-Channel Analog Front End

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### Features:

- One 24-bit Resolution Delta-Sigma A/D Converter
- 93.5 dB SINAD, -107 dBc Total Harmonic Distortion (THD) (up to 35<sup>th</sup> harmonic), 112 dB Spurious-Free Dynamic Range (SFDR)
- Flexible Serial Interface that Includes Both SPI and a Simple 2-Wire Interface Ideal for Polyphase Shunt Energy Meters
- Advanced Security Features:
  - 16-bit Cyclic Redundancy Check (CRC) Checksum on All Communications for Secure Data Transfers
  - 16-bit CRC Checksum and Interrupt Alert for Register-Map Configuration
  - Register-Map Lock with 8-bit Secure Key
- 2.7V – 3.6V AV<sub>DD</sub>, DV<sub>DD</sub>
- Programmable Data Rate, up to 125 kbps:
  - 4 MHz Maximum Sampling Frequency
  - 16 MHz Maximum Master Clock
- Oversampling Ratio, up to 4096
- Ultra Low-Power Shutdown Mode with < 10  $\mu$ A
- Low-Drift 1.2V Internal Voltage Reference: 9 ppm/ $^{\circ}$ C
- Differential Voltage Reference Input Pins
- High-Gain Programmable Gain Amplifier (PGA) (up to 32 V/V)
- Phase Delay Compensation with 1  $\mu$ s Time Resolution
- Separate Data Ready Pin for Easy Synchronization
- Individual 24-bit Digital Offset and Gain Error Correction
- High-Speed 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Continuous Read/Write Modes for Minimum Communication with Dedicated 16-/32-bit Modes
- Available in 20-lead QFN and SSOP Packages
- Extended Temperature Range: -40 $^{\circ}$ C to +125 $^{\circ}$ C (all specifications are valid down to -45 $^{\circ}$ C)

### Description:

The MCP3918 is a 3V single-channel Analog Front End (AFE), containing one delta-sigma, Analog-to-Digital Converter (ADC), one programmable gain amplifier (PGA), phase delay compensation block, low-drift internal voltage reference, digital offset and gain errors calibration registers, and high-speed 20 MHz SPI-compatible serial interface.

The MCP3918 ADC is fully configurable with features such as: 16-/24-bit resolution, Oversampling Ratio (OSR) from 32 to 4096, gain from 1x to 32x, independent Shutdown and Reset, dithering and auto-zeroing. Communication is largely simplified with 8-bit commands, including various continuous read/write modes and 16-/24-/32-bit data formats that can be accessed by the Direct Memory Access (DMA) of an 8-/16-/32-bit MCU, and with the separate Data Ready pin that can be directly connected to an Interrupt Request (IRQ) input of an MCU.

The MCP3918 includes advanced security features to secure the communications and the configuration settings, such as a CRC-16 checksum on both serial data outputs and on the register-map static configuration. It also includes a register-map lock through an 8-bit password to avoid the processing of any unwanted write commands.

For polyphase shunt-based energy meters, the MCP3918 2-Wire serial interface greatly reduces system cost, requiring only a single bidirectional isolator per phase.

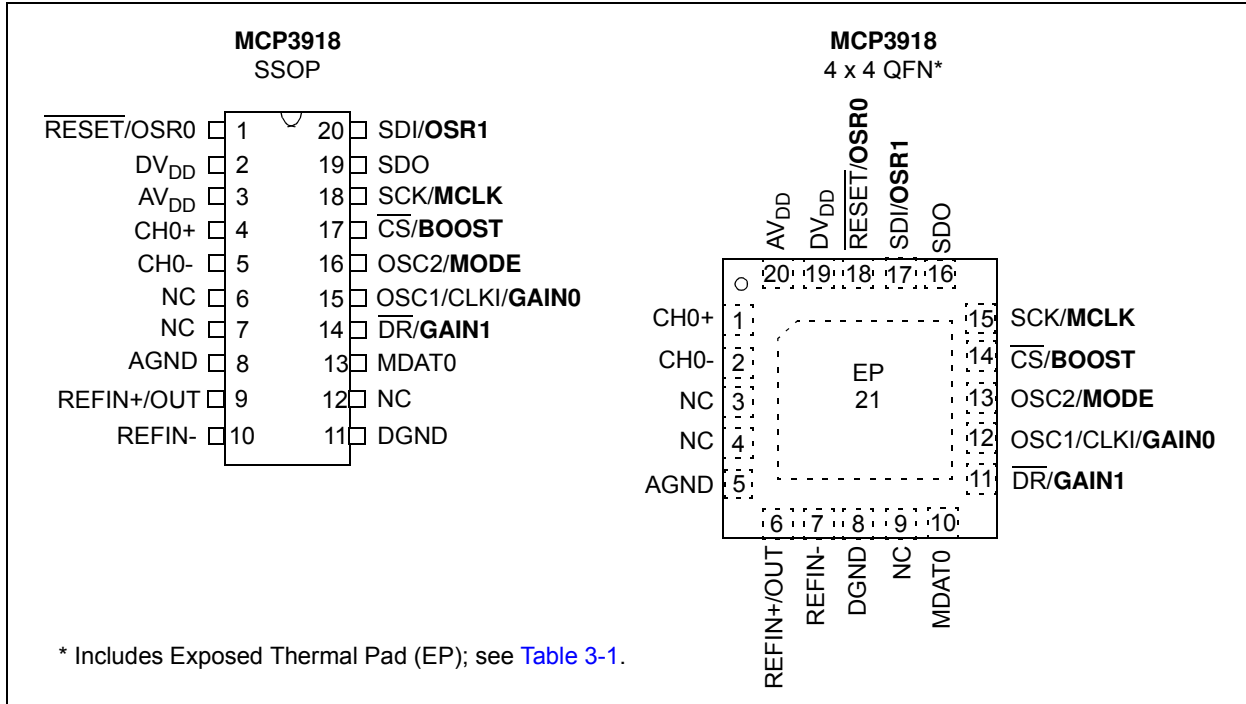
The MCP3918 is capable of interfacing a variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall effect sensors.

### Applications:

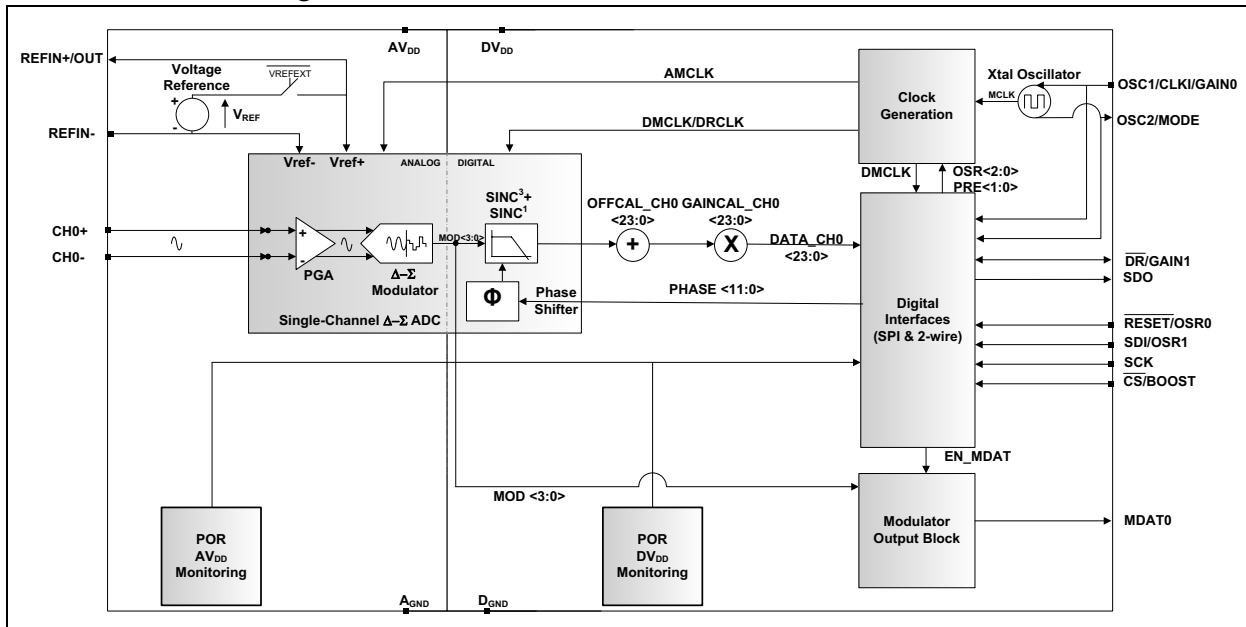
- Single-Phase and Polyphase Energy Meters
- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring
- Audio/Voice Recognition
- Isolator Sensor Application

# MCP3918

## Package Type



## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD}$ .....	-0.3V to 4.0V
Digital inputs and outputs w.r.t. $A_{GND}$ .....	-0.3V to 4.0V
Analog input w.r.t. $A_{GND}$ .....	-2V to +2V
$V_{REF}$ input w.r.t. $A_{GND}$ .....	-0.6V to $V_{DD} + 0.6V$
Storage temperature .....	-65°C to +150°C
Ambient temp. with power applied .....	-65°C to +125°C
Soldering temperature of leads (10 seconds) .....	+300°C
ESD on the analog inputs (HBM, MM) .....	4.0 kV, 200V
ESD on all other pins (HBM, MM) .....	4.0 kV, 200V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 1.1 Electrical Specifications

**TABLE 1-1: ANALOG SPECIFICATIONS**

<b>Electrical Specifications:</b> Unless otherwise indicated, all parameters apply at $AV_{DD} = DV_{DD} = 3V$ , $MCLK = 4 MHz$ ; $PRE<1:0> = 00$ ; $OSR = 256$ ; $GAIN = 1$ ; $VREFEXT = 0$ , $CLKEXT = 1$ , $DITHER<1:0> = 11$ ; $BOOST<1:0> = 10$ , $V_{CM} = 0V$ ; $T_A = -40^{\circ}C$ to $+125^{\circ}C$ ( <b>Note 1</b> ); $V_{IN} = 1.2 V_{PP} = -0.5 dBFS @ 50/60 Hz$ on all channels.						
Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>ADC Performance</b>						
Resolution (No Missing Codes)		24	—	—	bits	$OSR = 256$ or greater
Sampling Frequency	$f_S(DMCLK)$	—	1	4	MHz	For maximum condition, $BOOST<1:0> = 11$
Output Data Rate	$f_D(DRCLK)$	—	4	125	ksps	For maximum condition, $BOOST<1:0> = 11$ , $OSR = 32$
Analog Input Absolute Voltage on $CH0+/-$ pins	$CH0+/-$	-1	—	+1	V	All analog input channels, measured to $A_{GND}$
Analog Input Leakage Current	$I_{IN}$	—	+/-1	—	nA	$RESET<0> = 1$ , $MCLK$ running continuously
Differential Input Voltage Range	$(CH_{0+} - CH_{0-})$	-600/GAIN	—	+600/GAIN	mV	$V_{REF} = 1.2V$ , proportional to $V_{REF}$
Offset Error	$V_{OS}$	-1	0.2	1	mV	<b>Note 5</b>
Offset Error Drift		—	0.5	—	$\mu V/^{\circ}C$	
Gain Error	GE	-4	—	+4	%	<b>Note 5</b>
Gain Error Drift		—	1	—	ppm/ $^{\circ}C$	
Integral Non-Linearity	INL	—	5	—	ppm	

**Note 1:** All specifications are valid down to  $-45^{\circ}C$ .

- This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at  $-0.5 dB$  below the maximum signal range,  $V_{IN} = 1.2 V_{PP} = 424 mV_{RMS}$ ,  $V_{REF} = 1.2V @ 50/60 Hz$ . See **Section 4.0 “Terminology and Formulas”** for definition. This parameter is established by characterization and not 100% tested.
- For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 0$ ,  $RESET<0> = 0$ ,  $VREFEXT = 0$ ,  $CLKEXT = 0$ .
- For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 1$ ,  $VREFEXT = 1$ ,  $CLKEXT = 1$ .
- Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 “Typical Performance Curves”** for typical performance.
- Outside this range, the ADC accuracy is not specified. An extended input range of  $\pm 2V$  can be applied continuously to the part, with no damage.
- For proper operation and for optimizing the ADC accuracy,  $AMCLK$  should be limited to the maximum frequency defined in **Table 5-2**, as a function of the  $BOOST$  and  $PGA$  setting chosen.  $MCLK$  can take larger values as long as the prescaler settings ( $PRE<1:0>$ ) limit  $AMCLK = MCLK/PRESCALE$  within the defined range in **Table 5-2**.

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**TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)**

<b>Electrical Specifications:</b> Unless otherwise indicated, all parameters apply at $AV_{DD} = DV_{DD} = 3V$ , $MCLK = 4\text{ MHz}$ ; $PRE<1:0> = 00$ ; $OSR = 256$ ; $GAIN = 1$ ; $VREFEXT = 0$ , $CLKEXT = 1$ , $DITHER<1:0> = 11$ ; $BOOST<1:0> = 10$ , $V_{CM} = 0V$ ; $T_A = -40^{\circ}C$ to $+125^{\circ}C$ ( <b>Note 1</b> ); $V_{IN} = 1.2 V_{PP} = -0.5\text{ dBFS @ } 50/60\text{ Hz}$ on all channels.						
Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Measurement Error	ME	—	0.1	—	%	Measured with a 10,000:1 dynamic range (from 600 mV <sub>Peak</sub> to 6 $\mu$ V <sub>Peak</sub> ), $AV_{DD} = DV_{DD} = 3V$ , measurement points averaging time: 20 seconds.
Differential Input Impedance	$Z_{IN}$	232	—	—	k $\Omega$	G = 1, proportional to 1/AMCLK
		142	—	—	k $\Omega$	G = 2, proportional to 1/AMCLK
		72	—	—	k $\Omega$	G = 4, proportional to 1/AMCLK
		38	—	—	k $\Omega$	G = 8, proportional to 1/AMCLK
		36	—	—	k $\Omega$	G = 16, proportional to 1/AMCLK
		33	—	—	k $\Omega$	G = 32, proportional to 1/AMCLK
Signal-to-Noise and Distortion Ratio ( <b>Note 2</b> )	SINAD	92	93.5	—	dB	
Total Harmonic Distortion ( <b>Note 2</b> )	THD	—	-107	-103	dBc	Includes the first 35 harmonics
Signal-to-Noise Ratio ( <b>Note 2</b> )	SNR	92	94	—	dB	
Spurious-Free Dynamic Range ( <b>Note 2</b> )	SFDR	—	112	—	dBFS	
AC Power Supply Rejection	AC PSRR	—	-73	—	dB	$AV_{DD} = DV_{DD} = 3V + 0.6V_{PP}$ 50/60 Hz, 100/120 Hz
DC Power Supply Rejection	DC PSRR	—	-73	—	dB	$AV_{DD} = DV_{DD} = 2.7V$ to $3.6V$
DC Common Mode Rejection	DC CMRR	—	-105	—	dB	$V_{CM}$ from -1V to +1V

**Note 1:** All specifications are valid down to  $-45^{\circ}C$ .

- 2: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at -0.5 dB below the maximum signal range,  $V_{IN} = 1.2 V_{PP} = 424\text{ mV}_{RMS}$ ,  $V_{REF} = 1.2V @ 50/60\text{ Hz}$ . See **Section 4.0 "Terminology and Formulas"** for definition. This parameter is established by characterization and not 100% tested.
- 3: For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 0$ ,  $RESET<0> = 0$ ,  $VREFEXT = 0$ ,  $CLKEXT = 0$ .
- 4: For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 1$ ,  $VREFEXT = 1$ ,  $CLKEXT = 1$ .
- 5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.
- 6: Outside this range, the ADC accuracy is not specified. An extended input range of  $\pm 2V$  can be applied continuously to the part, with no damage.
- 7: For proper operation and for optimizing the ADC accuracy, AMCLK should be limited to the maximum frequency defined in **Table 5-2**, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings ( $PRE<1:0>$ ) limit  $AMCLK = MCLK/PRESCALE$  within the defined range in **Table 5-2**.

**TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)**

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at  $V_{DD} = DV_{DD} = 3V$ ,  $MCLK = 4\text{ MHz}$ ;  $PRE<1:0> = 00$ ;  $OSR = 256$ ;  $GAIN = 1$ ;  $VREFEXT = 0$ ,  $CLKEXT = 1$ ,  $DITHER<1:0> = 11$ ;  $BOOST<1:0> = 10$ ,  $V_{CM} = 0V$ ;  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (**Note 1**);  $V_{IN} = 1.2\text{ V}_{PP} = -0.5\text{ dBFS}$  @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Internal Voltage Reference</b>						
Tolerance	$V_{REF}$	1.176	1.2	1.224	V	$VREFEXT = 0$ , $T_A = +25^\circ\text{C}$ only
Temperature Coefficient	$TCV_{REF}$	—	9	—	ppm/ $^\circ\text{C}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $VREFEXT = 0$
Output Impedance	$ZOUTV_{REF}$	—	0.6	—	$k\Omega$	$VREFEXT = 0$
Internal Voltage Reference Operating Current	$AI_{DD}V_{REF}$	—	54	—	$\mu\text{A}$	$VREFEXT = 0$ , $SHUTDOWN<0> = 1$
<b>Voltage Reference Input</b>						
Input Capacitance		—	—	10	pF	
Differential Input Voltage Range ( $V_{REF+} - V_{REF-}$ )	$V_{REF}$	1.1	—	1.3	V	$VREFEXT = 1$
Absolute Voltage on $REFIN+$ pin	$V_{REF+}$	$V_{REF-} + 1.1$	—	$V_{REF-} + 1.3$	V	$VREFEXT = 1$
Absolute Voltage on $REFIN-$ pin	$V_{REF-}$	-0.1	—	+0.1	V	$REFIN-$ should be connected to $A_{GND}$ when $VREFEXT = 0$
<b>Master Clock Input</b>						
Master Clock Input Frequency Range	$f_{MCLK}$		—	20	MHz	$CLKEXT = 1$ ( <b>Note 7</b> )
Crystal Oscillator Operating Frequency Range	$f_{XTAL}$	1	—	20	MHz	$CLKEXT = 0$ ( <b>Note 7</b> )
Analog Master Clock	AMCLK	—	—	16	MHz	<b>Note 7</b>
Crystal Oscillator Operating Current	DIDDXTAL	—	80	—	$\mu\text{A}$	$CLKEXT = 0$
<b>Power Supply</b>						
Operating Voltage, Analog	$AV_{DD}$	2.7	—	3.6	V	
Operating Voltage, Digital	$DV_{DD}$	2.7	—	3.6	V	
Operating Current, Analog ( <b>Note 3</b> )	$I_{DD,A}$	—	0.8	1	mA	$BOOST<1:0> = 00$
		—	1	1.2	mA	$BOOST<1:0> = 01$
		—	1.3	1.7	mA	$BOOST<1:0> = 10$
		—	2.2	2.9	mA	$BOOST<1:0> = 11$

**Note 1:** All specifications are valid down to  $-45^\circ\text{C}$ .

- This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at -0.5 dB below the maximum signal range,  $V_{IN} = 1.2\text{ V}_{PP} = 424\text{ mV}_{RMS}$ ,  $V_{REF} = 1.2V$  @ 50/60 Hz. See **Section 4.0 “Terminology and Formulas”** for definition. This parameter is established by characterization and not 100% tested.
- For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 0$ ,  $RESET<0> = 0$ ,  $VREFEXT = 0$ ,  $CLKEXT = 0$ .
- For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 1$ ,  $VREFEXT = 1$ ,  $CLKEXT = 1$ .
- Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 “Typical Performance Curves”** for typical performance.
- Outside this range, the ADC accuracy is not specified. An extended input range of  $\pm 2V$  can be applied continuously to the part, with no damage.
- For proper operation and for optimizing the ADC accuracy, AMCLK should be limited to the maximum frequency defined in **Table 5-2**, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings ( $PRE<1:0>$ ) limit  $AMCLK = MCLK/PRESCALE$  within the defined range in **Table 5-2**.

# MCP3918

**TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)**

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at  $AV_{DD} = DV_{DD} = 3V$ ,  $MCLK = 4\text{ MHz}$ ;  $PRE<1:0> = 00$ ;  $OSR = 256$ ;  $GAIN = 1$ ;  $VREFEXT = 0$ ,  $CLKEXT = 1$ ,  $DITHER<1:0> = 11$ ;  $BOOST<1:0> = 10$ ,  $V_{CM} = 0V$ ;  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (**Note 1**);  $V_{IN} = 1.2\text{ V}_{PP} = -0.5\text{ dBFS}$  @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Current, Digital	$I_{DD,D}$	—	0.2	0.3	mA	$MCLK = 4\text{ MHz}$ , proportional to $MCLK$
		—	0.7	—	mA	$MCLK = 16\text{ MHz}$ , proportional to $MCLK$
Shutdown Current, Analog	$I_{DDS,A}$	—	—	1	$\mu\text{A}$	$AV_{DD}$ pin only ( <b>Note 4</b> )
Shutdown Current, Digital	$I_{DDS,D}$	—	—	2	$\mu\text{A}$	$DV_{DD}$ pin only ( <b>Note 4</b> )
Pull-Down Current on OSC2 Pin (External Clock Mode)	$I_{OSC2}$	—	35	—	$\mu\text{A}$	$CLKEXT = 1$

**Note 1:** All specifications are valid down to  $-45^\circ\text{C}$ .

- 2: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at  $-0.5\text{ dB}$  below the maximum signal range,  $V_{IN} = 1.2\text{ V}_{PP} = 424\text{ mV}_{RMS}$ ;  $V_{REF} = 1.2V$  @ 50/60 Hz. See **Section 4.0 “Terminology and Formulas”** for definition. This parameter is established by characterization and not 100% tested.
- 3: For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 0$ ,  $RESET<0> = 0$ ,  $VREFEXT = 0$ ,  $CLKEXT = 0$ .
- 4: For these operating currents, the following configuration bit settings apply:  $SHUTDOWN<0> = 1$ ,  $VREFEXT = 1$ ,  $CLKEXT = 1$ .
- 5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 “Typical Performance Curves”** for typical performance.
- 6: Outside this range, the ADC accuracy is not specified. An extended input range of  $\pm 2V$  can be applied continuously to the part, with no damage.
- 7: For proper operation and for optimizing the ADC accuracy,  $AMCLK$  should be limited to the maximum frequency defined in **Table 5-2**, as a function of the  $BOOST$  and  $PGA$  setting chosen.  $MCLK$  can take larger values as long as the prescaler settings ( $PRE<1:0>$ ) limit  $AMCLK = MCLK/PRESCALE$  within the defined range in **Table 5-2**.

## 1.2 Serial Interface Characteristics

**TABLE 1-2: SERIAL DC CHARACTERISTICS**

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at  $DV_{DD} = 2.7$  to  $3.6\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (**Note 1**),  $C_{LOAD} = 30\text{ pF}$ , applies to all digital I/O.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
High-Level Input Voltage	$V_{IH}$	$0.7\text{ DV}_{DD}$	—	—	V	Schmitt-Triggered
Low-Level Input Voltage	$V_{IL}$	—	—	$0.3\text{ DV}_{DD}$	V	Schmitt-Triggered
Input Leakage Current	$I_{LI}$	—	—	$\pm 1$	$\mu\text{A}$	$\overline{CS} = DV_{DD}$ , $V_{IN} = D_{GND}$ to $DV_{DD}$
Output Leakage Current	$I_{LO}$	—	—	$\pm 1$	$\mu\text{A}$	$\overline{CS} = DV_{DD}$ , $V_{OUT} = D_{GND}$ or $DV_{DD}$
Hysteresis of Schmitt-Triggered Inputs	$V_{HYS}$	—	300	—	mV	$DV_{DD} = 3.3V$ only ( <b>Note 3</b> )
Low-Level Output Voltage	$V_{OL}$	—	—	$0.4V$	V	$I_{OL} = +1.7\text{ mA}$ , $DV_{DD} = 3.3V$
High-Level Output Voltage	$V_{OH}$	$DV_{DD} - 0.5$	—	—	V	$I_{OH} = -1.7\text{ mA}$ , $DV_{DD} = 3.3V$
Internal Capacitance (All Inputs and Outputs)	$C_{INT}$	—	—	7	pF	$T_A = +25^\circ\text{C}$ , $SCK = 1.0\text{ MHz}$ , $DV_{DD} = 3.3V$ ( <b>Note 2</b> )

**Note 1:** All specifications are valid down to  $-45^\circ\text{C}$ .

- 2: This parameter is periodically sampled and not 100% tested.
- 3: This parameter is established by characterization and not production tested.

**TABLE 1-3: SERIAL AC CHARACTERISTICS**

<b>Electrical Specifications:</b> Unless otherwise indicated, all parameters apply at $DV_{DD} = 2.7$ to $3.6$ V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ( <b>Note 1</b> ), $GAIN = 1$ , $C_{LOAD} = 30$ pF.						
Characteristic	Sym	Min	Typ	Max	Units	Conditions
Serial Clock Frequency	$f_{SCK}$	—	—	20	MHz	
$\overline{CS}$ Setup Time	$t_{CSS}$	25	—	—	ns	
$\overline{CS}$ Hold Time	$t_{CSH}$	50	—	—	ns	
$\overline{CS}$ Disable Time	$t_{CSD}$	50	—	—	ns	
Data Setup Time	$t_{SU}$	5	—	—	ns	
Data Hold Time	$t_{HD}$	10	—	—	ns	
Serial Clock High Time	$t_{HI}$	20	—	—	ns	
Serial Clock Low Time	$t_{LO}$	20	—	—	ns	
Serial Clock Delay Time	$t_{CLD}$	50	—	—	ns	
Serial Clock Enable Time	$t_{CLE}$	50	—	—	ns	
Output Valid from SCK Low	$t_{DO}$	—	—	25	ns	
Output Hold Time	$t_{HO}$	0	—	—	ns	
Output Disable Time	$t_{DIS}$	—	—	25	ns	
Reset Pulse Width ( $\overline{RESET}$ )	$t_{MCLR}$	100	—	—	ns	
Data Transfer Time to $\overline{DR}$ (Data Ready)	$t_{DODR}$	—	—	25	ns	<b>Note 2</b>
Modulator Mode Entry to Modulator Data Present	$t_{MODSU}$	—	—	100	ns	
Data Ready Pulse Low Time	$t_{DRP}$	—	$1/(2 \times DMCLK)$	—	$\mu\text{s}$	
2-Wire Mode Enable Time	$t_{MODE}$	—	—	50	ns	
2-Wire Mode Watchdog Timer	$t_{WATCH}$	3.5	—	35	$\mu\text{s}$	

**Note 1:** All specifications are valid down to  $-45^\circ\text{C}$ .

**2:** This parameter is established by characterization and not production tested.

**TABLE 1-4: TEMPERATURE SPECIFICATIONS**

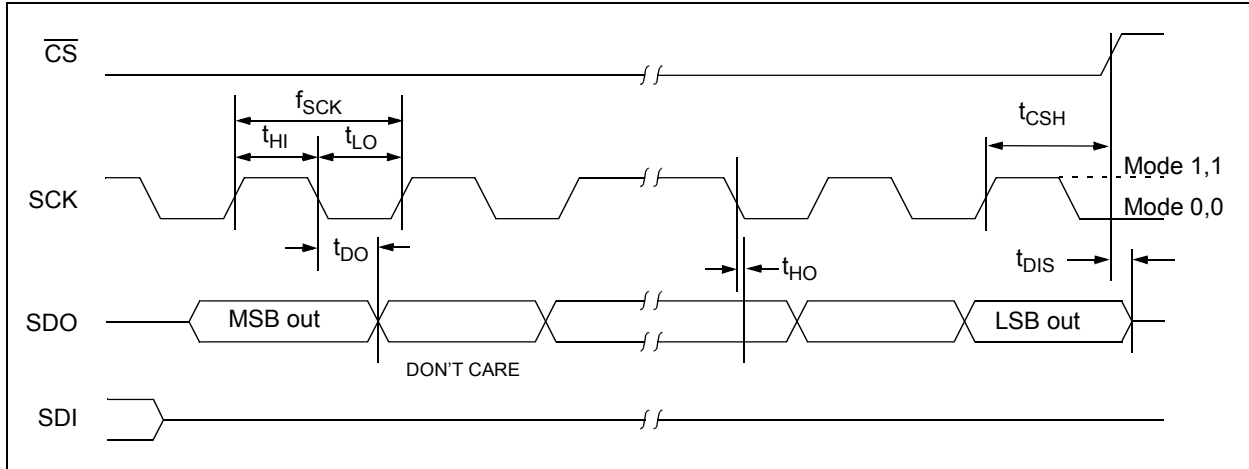
<b>Electrical Specifications:</b> Unless otherwise indicated, all parameters apply at $AV_{DD} = 2.7$ to $3.6$ V, $DV_{DD} = 2.7$ to $3.6$ V.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	<b>Note 1, Note 2</b>
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ\text{C}$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 20L 4x4 QFN	$\theta_{JA}$	—	46.2	—	$^\circ\text{C/W}$	
Thermal Resistance, 20L SSOP	$\theta_{JA}$	—	87.3	—	$^\circ\text{C/W}$	

**Note 1:** The internal junction temperature ( $T_J$ ) must not exceed the absolute maximum specification of  $+150^\circ\text{C}$ .

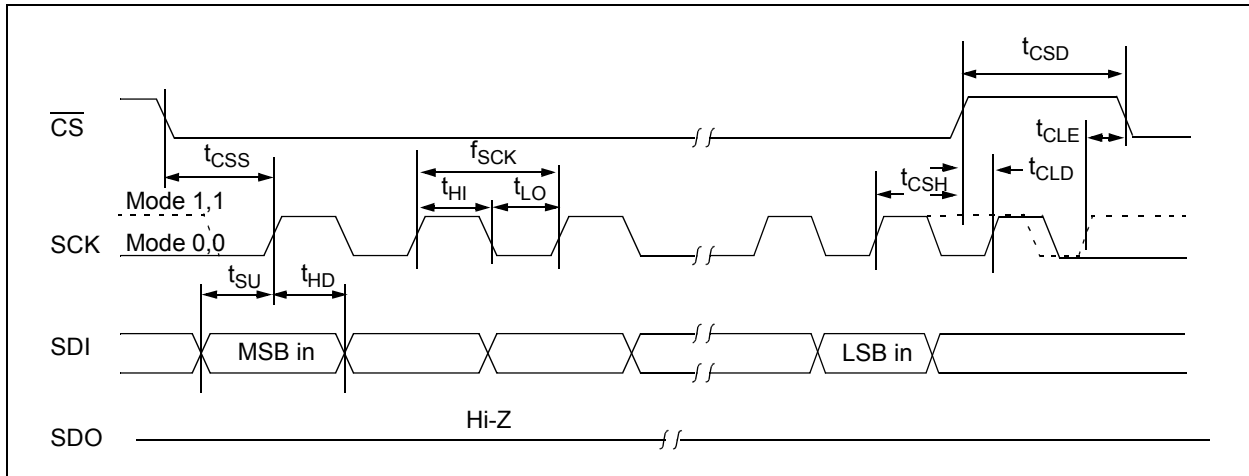
**2:** All specifications are valid down to  $-45^\circ\text{C}$ .



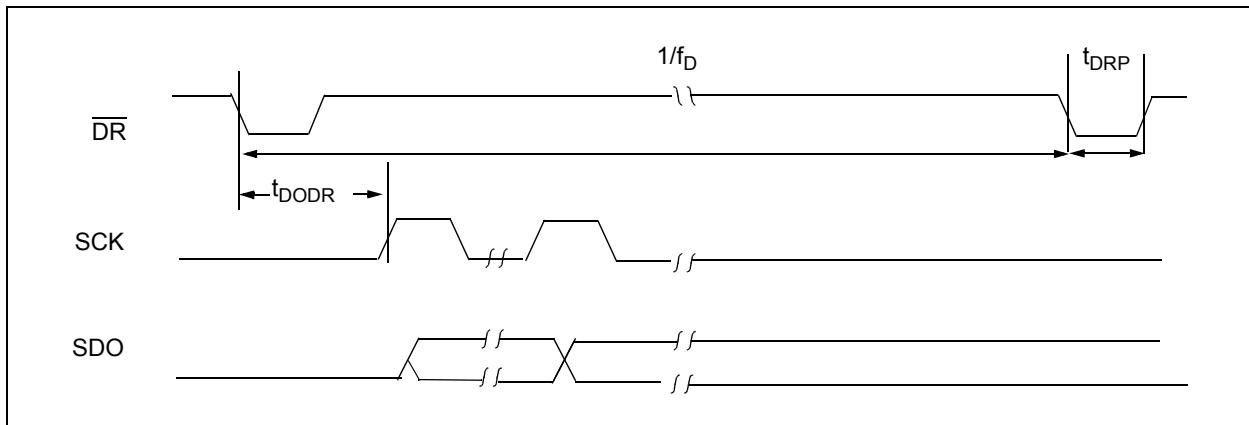
# MCP3918



**FIGURE 1-1:** Serial Output Timing Diagram.



**FIGURE 1-2:** Serial Input Timing Diagram.



**FIGURE 1-3:** Data Ready Pulse/Sampling Timing Diagram.

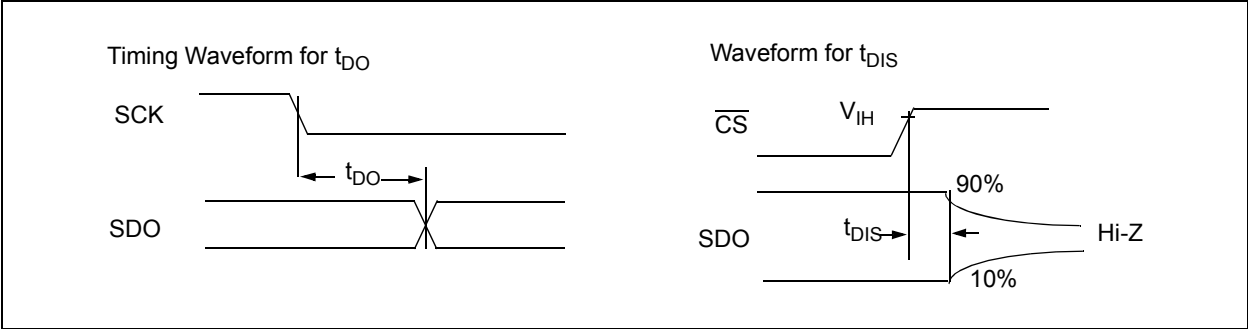


FIGURE 1-4: Timing Diagrams, continued.

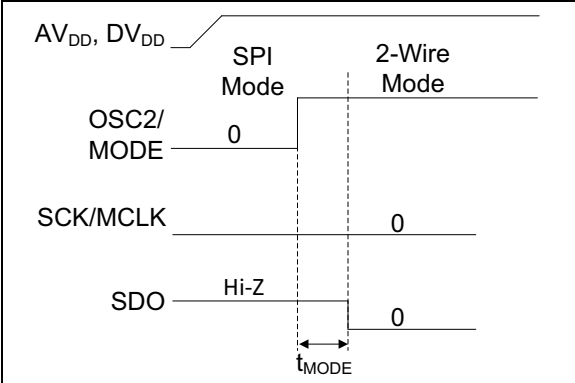


FIGURE 1-5: Entering 2-Wire Interface Mode Timing Diagram.

# MCP3918

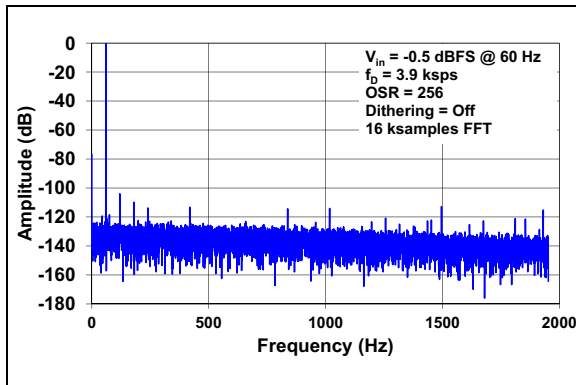
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NOTES:

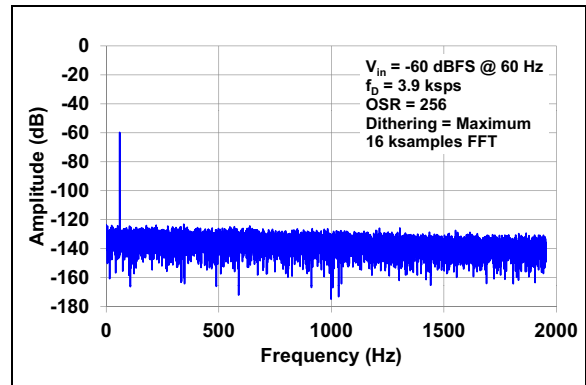
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

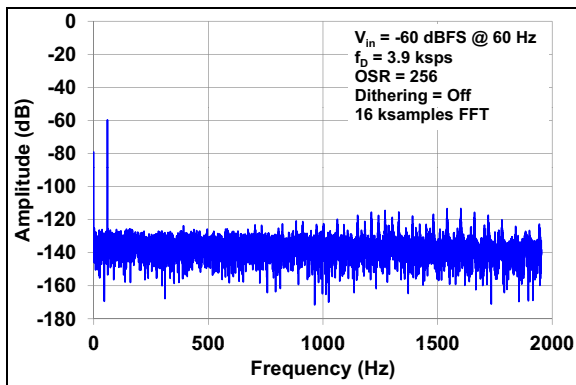
**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ;  $Dithering = Maximum$ ;  $V_{IN} = -0.5\text{ dBFS @ }60\text{ Hz}$  on all channels,  $VREFEXT = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



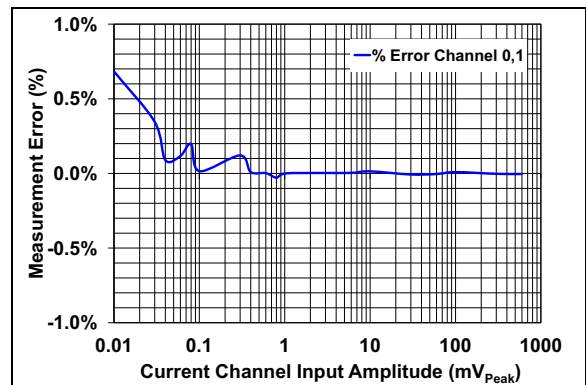
**FIGURE 2-1:** Spectral Response.



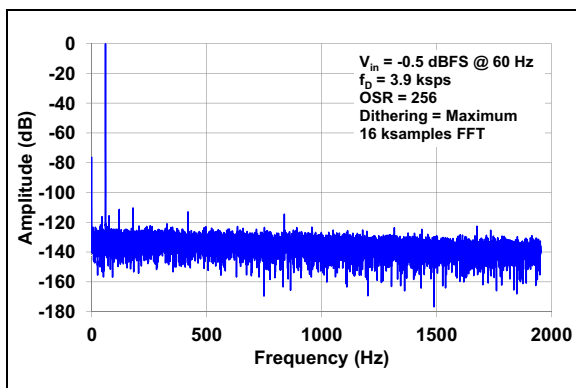
**FIGURE 2-4:** Spectral Response.



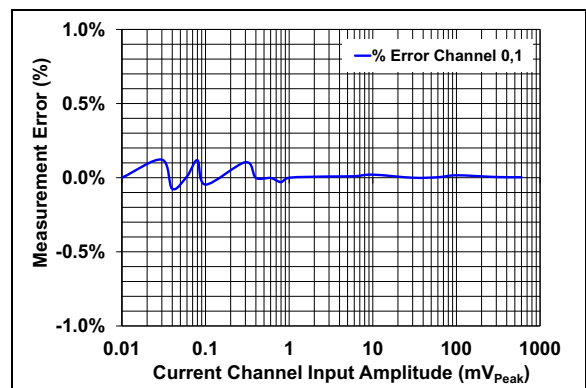
**FIGURE 2-2:** Spectral Response.



**FIGURE 2-5:** Measurement Error with 1-Point Calibration.



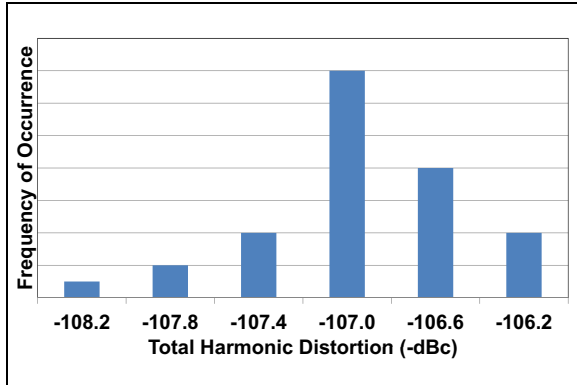
**FIGURE 2-3:** Spectral Response.



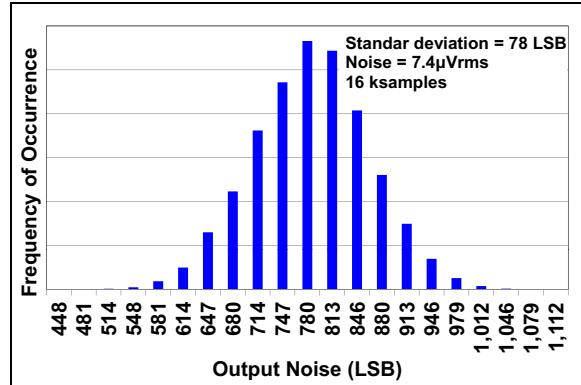
**FIGURE 2-6:** Measurement Error with 2-Point Calibration.

# MCP3918

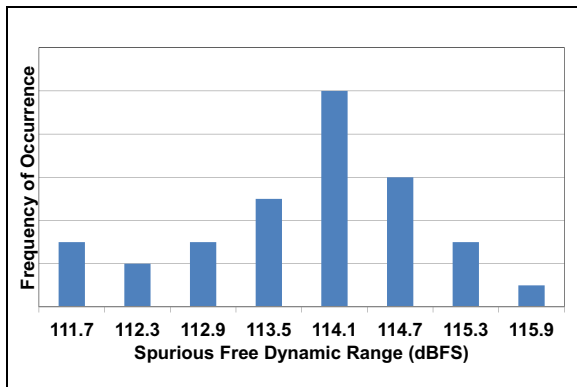
**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ; Dithering = Maximum;  $V_{IN} = -0.5\text{ dBFS}$  @ 60 Hz on all channels,  $VREFEXT = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



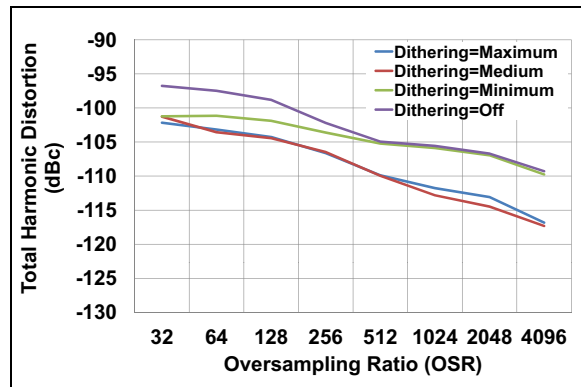
**FIGURE 2-7:** THD Repeatability Histogram.



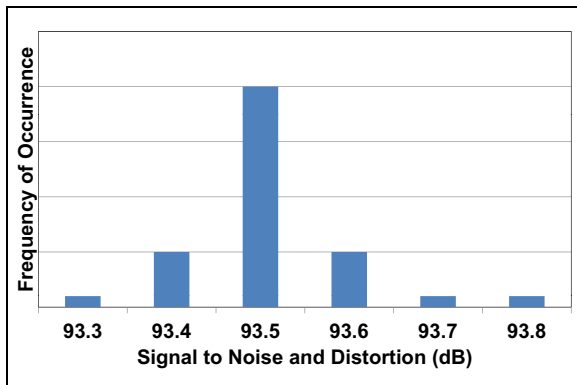
**FIGURE 2-10:** Output Noise Histogram.



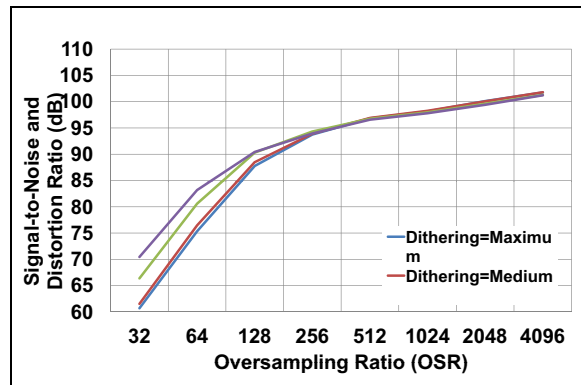
**FIGURE 2-8:** Spurious-Free Dynamic Range Repeatability Histogram.



**FIGURE 2-11:** THD vs. OSR.

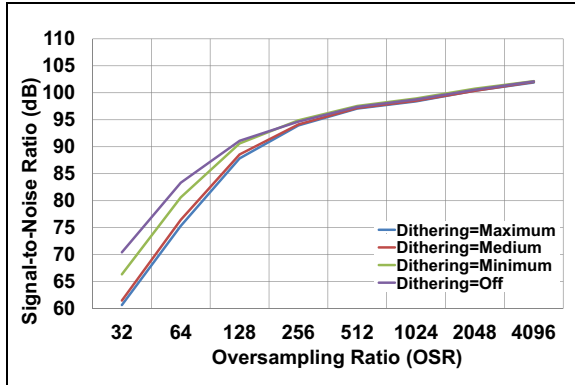


**FIGURE 2-9:** SINAD Repeatability Histogram.

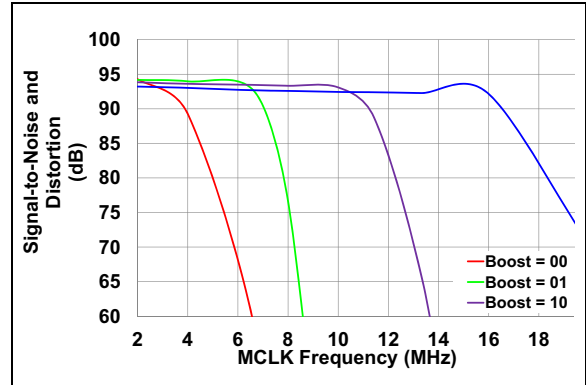


**FIGURE 2-12:** SINAD vs. OSR.

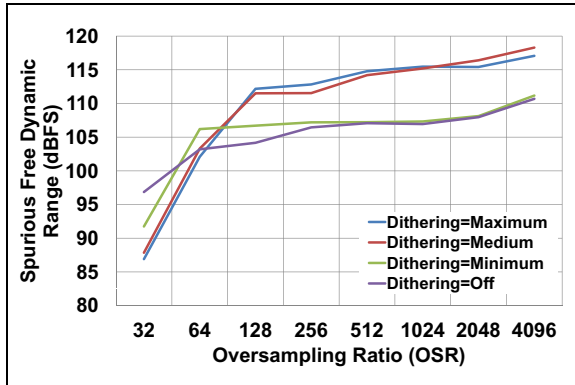
**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ;  $Dithering = \text{Maximum}$ ;  $V_{IN} = -0.5\text{ dBFS}$  @ 60 Hz on all channels,  $VREFEXT = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



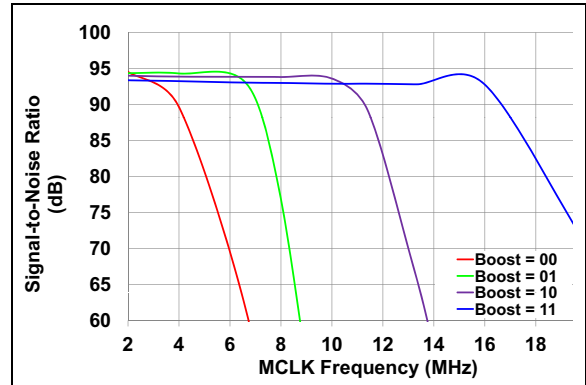
**FIGURE 2-13:** SNR vs. OSR.



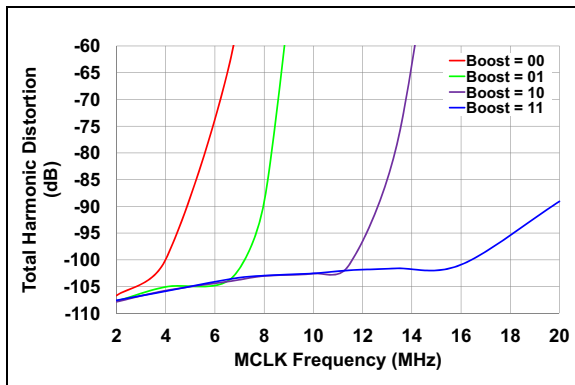
**FIGURE 2-16:** SINAD vs. MCLK.



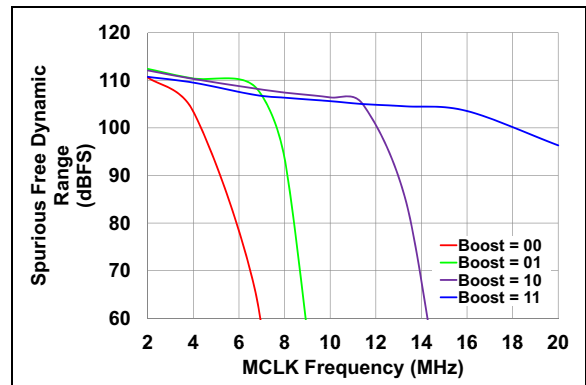
**FIGURE 2-14:** SFDR vs. OSR.



**FIGURE 2-17:** SNR vs. MCLK.



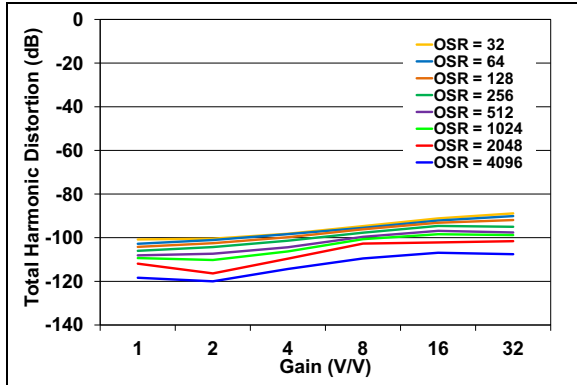
**FIGURE 2-15:** THD vs. MCLK.



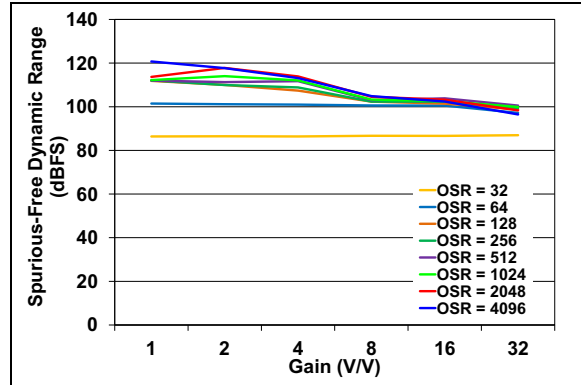
**FIGURE 2-18:** SFDR vs. MCLK.

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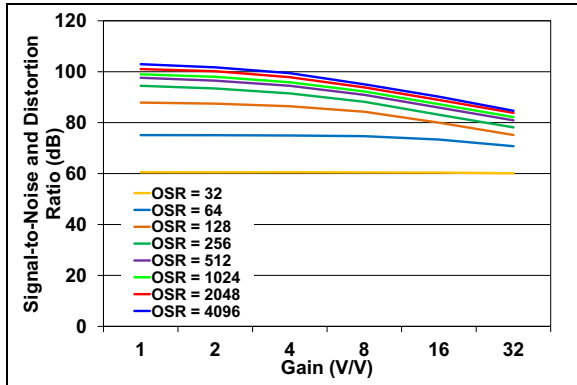
**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ; Dithering = Maximum;  $V_{IN} = -0.5\text{ dBFS @ }60\text{ Hz}$  on all channels,  $VREFEXT = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



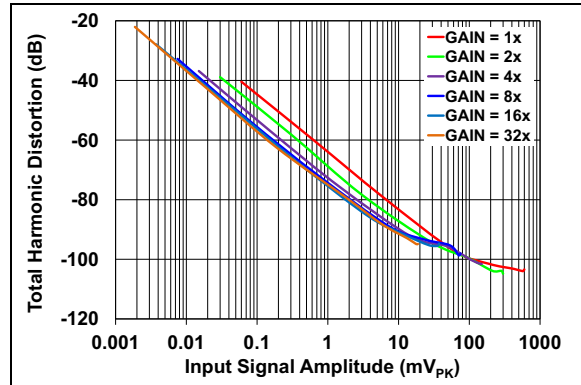
**FIGURE 2-19:** THD vs. GAIN.



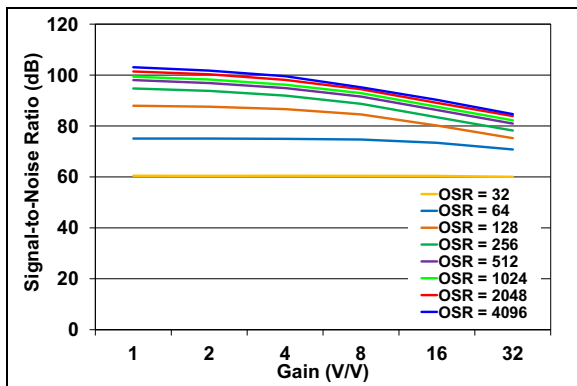
**FIGURE 2-22:** SFDR vs. GAIN.



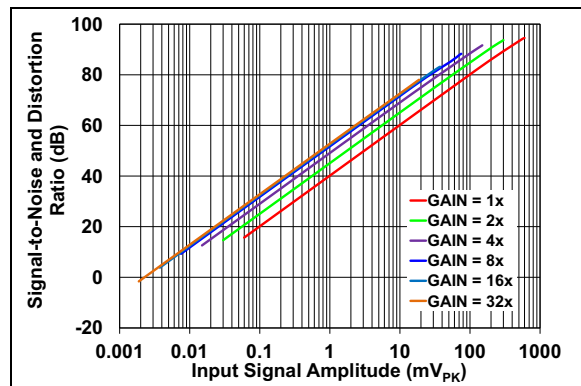
**FIGURE 2-20:** SINAD vs. GAIN.



**FIGURE 2-23:** THD vs. Input Signal Amplitude.

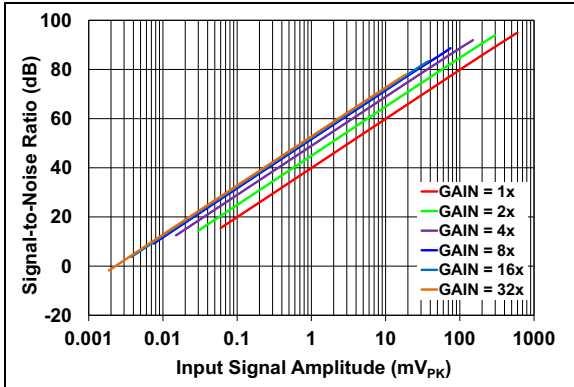


**FIGURE 2-21:** SNR vs. GAIN.

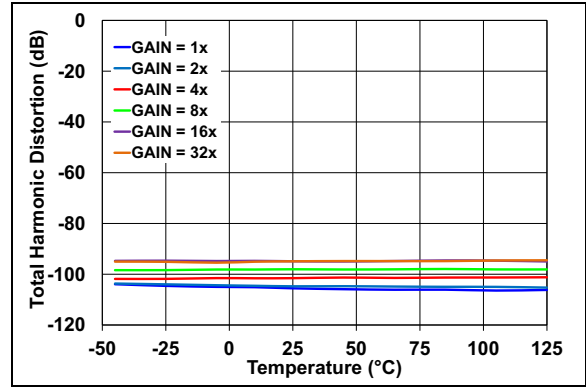


**FIGURE 2-24:** SINAD vs. Input Signal Amplitude.

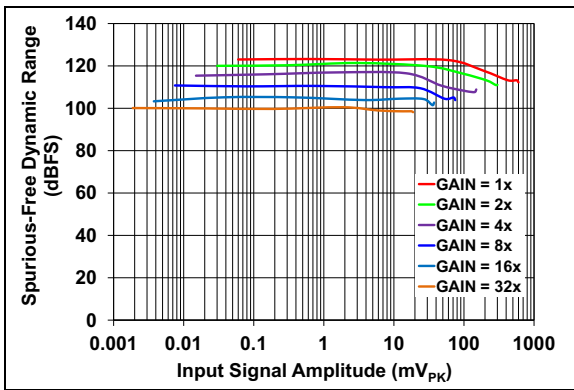
**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ; Dithering = Maximum;  $V_{IN} = -0.5\text{ dBFS}$  @ 60 Hz on all channels,  $VREFEXT = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



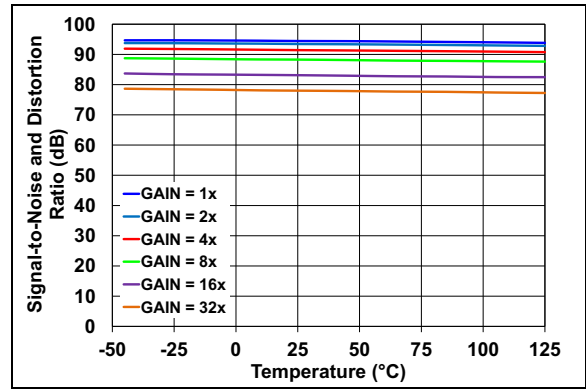
**FIGURE 2-25:** SNR vs. Input Signal Amplitude.



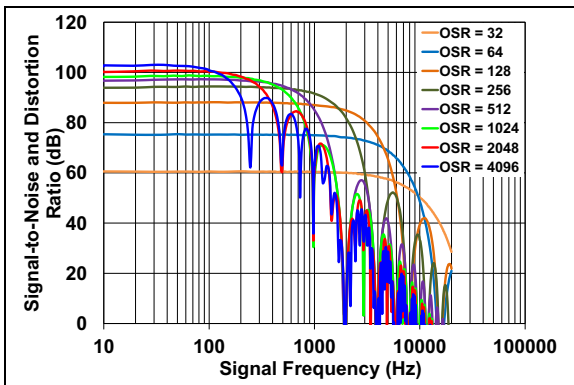
**FIGURE 2-28:** THD vs. Temperature.



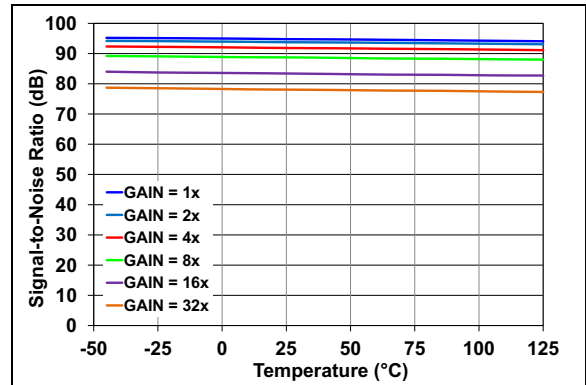
**FIGURE 2-26:** SFDR vs. Input Signal Amplitude.



**FIGURE 2-29:** SINAD vs. Temperature.



**FIGURE 2-27:** SINAD vs. Input Frequency.

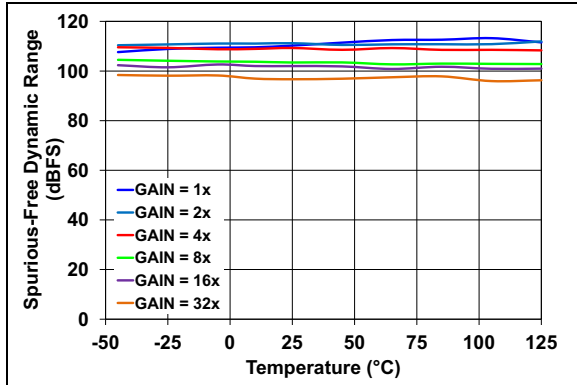


**FIGURE 2-30:** SNR vs. Temperature.

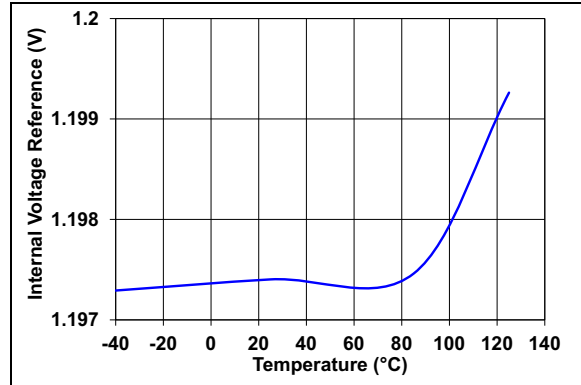


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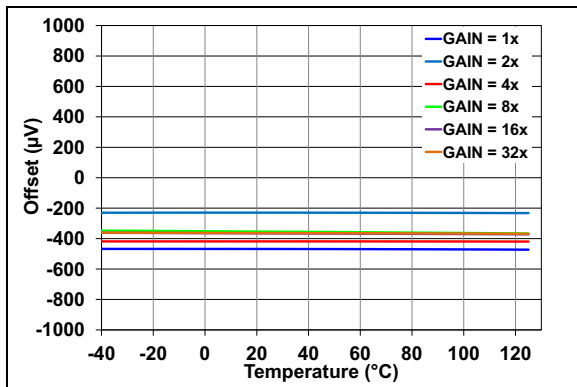
**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ;  $Dithering = \text{Maximum}$ ;  $V_{IN} = -0.5\text{ dBFS}$  @  $60\text{ Hz}$  on all channels,  $VREFEXT = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



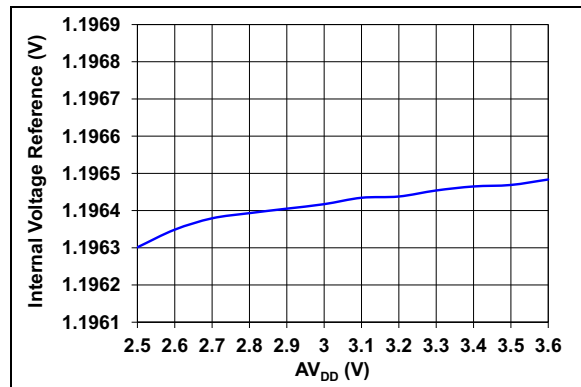
**FIGURE 2-31:** SFDR vs. Temperature.



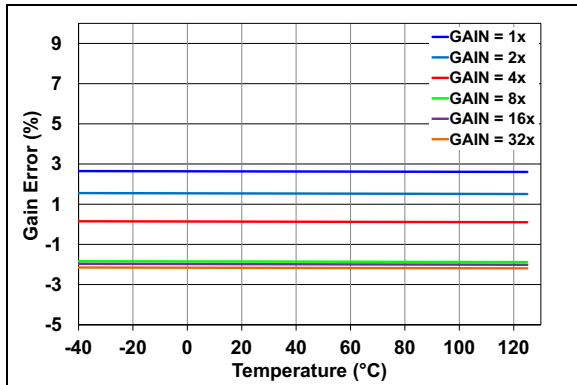
**FIGURE 2-34:** Internal Voltage Reference vs. Temperature.



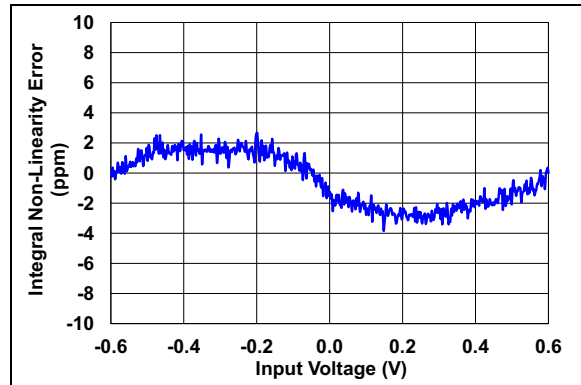
**FIGURE 2-32:** Offset vs. Temperature vs. Gain.



**FIGURE 2-35:** Internal Voltage Reference vs. Supply Voltage.

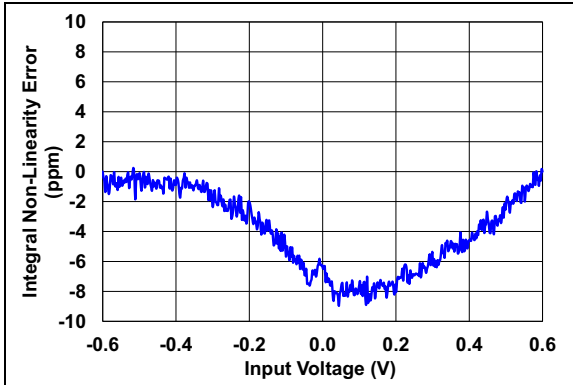


**FIGURE 2-33:** Gain Error vs. Temperature vs. Gain.

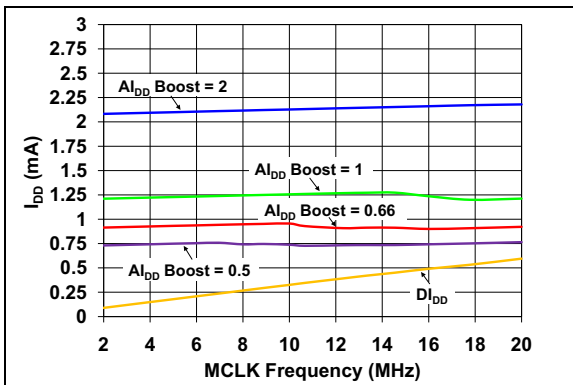


**FIGURE 2-36:** Integral Non-Linearity (Dithering Maximum).

**Note:** Unless otherwise indicated,  $AV_{DD} = 3V$ ,  $DV_{DD} = 3V$ ;  $T_A = +25^\circ C$ ,  $MCLK = 4\text{ MHz}$ ;  $PRESCALE = 1$ ;  $OSR = 256$ ;  $GAIN = 1$ ;  $Dithering = \text{Maximum}$ ;  $V_{IN} = -0.5\text{ dBFS @ }60\text{ Hz}$  on all channels,  $V_{REFEXT} = 0$ ;  $CLKEXT = 1$ ;  $BOOST<1:0> = 10$ .



**FIGURE 2-37:** Integral Non-Linearity (Dithering Off).



**FIGURE 2-38:** Operating Current vs. MCLK Frequency vs. Boost,  $V_{DD} = 3.0V$ .

# MCP3918

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NOTES:

### 3.0 PIN DESCRIPTION

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: SIX-CHANNEL MCP3918 PIN FUNCTION TABLE**

MCP3918 SSOP	MCP3918 QFN	Symbol	Function
1	18	$\overline{\text{RESET}}/\text{OSR0}$	Master Reset Logic Input Pin or OSR0 Logic Input Pin
2	19	$\text{DV}_{\text{DD}}$	Digital Power Supply Pin
3	20	$\text{AV}_{\text{DD}}$	Analog Power Supply Pin
4	1	CH0+	Non-Inverting Analog Input Pin for Channel 0
5	2	CH0-	Inverting Analog Input Pin for Channel 0
6	3	NC	Not connected
7	4	NC	Not connected
8	5	$\text{A}_{\text{GND}}$	Analog Ground Pin, Return Path for internal analog circuitry
9	6	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output Pin
10	7	REFIN-	Inverting Voltage Reference Input Pin
11	8	$\text{D}_{\text{GND}}$	Digital Ground Pin, Return Path for internal digital circuitry
12	9	NC	Not connected
13	10	MDAT0	Modulator Data Output Pin for Channel 0
14	11	$\overline{\text{DR}}/\text{GAIN1}$	Data Ready Signal Output Pin or GAIN1 Logic Input Pin
15	12	OSC1/CLKI/GAIN0	Oscillator Crystal Connection Pin or External Clock Input Pin or GAIN0 Logic Input Pin
16	13	OSC2/MODE	Oscillator Crystal Connection Input Pin or Serial Interface Mode Logic Input Pin
17	14	$\overline{\text{CS}}/\text{BOOST}$	Serial Interface Chip Select Input Pin or BOOST Logic Input Pin
18	15	SCK/MCLK	Serial Interface Clock Pin or Master Clock Input Pin
19	16	SDO	Serial Interface Data Input Pin
20	17	SDI/OSR1	Serial Interface Data Input Pin or OSR1 Logic Input Pin
—	21	EP	Exposed Thermal Pad

#### 3.1 Master Reset/OSR0 Logic Input (RESET/OSR0)

In SPI mode, this pin is active low and places the entire chip in a Reset state when active.

When  $\overline{\text{RESET}}$  is logic low, all registers are reset to their default value, no communication can take place, and no clock is distributed inside the part, except in the input structure if MCLK is applied (if MCLK is idle, then no clock is distributed). This state is equivalent to a Power-On Reset (POR) state.

Since the default state of the ADC is on, the analog power consumption when  $\overline{\text{RESET}}$  is logic low is equivalent to when  $\overline{\text{RESET}}$  is logic high. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no clock running.

If MCLK is applied when  $\overline{\text{RESET}}$  is logic low, all the analog biases are enabled during a reset, so that the part is fully operational just after a  $\overline{\text{RESET}}$  rising edge. If MCLK is not applied, there is a time after a hard reset when the conversion may not accurately correspond to the start-up of the input structure.

This input is Schmitt-triggered.

In 2-Wire Interface mode, this is the OSR0 logic select pin (see [Section 7.0 “2-Wire Serial Interface Description”](#) for the logic input table for OSR0 and OSR1). The pin state is latched when the MODE changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

# MCP3918

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## 3.2 Digital $V_{DD}$ ( $DV_{DD}$ )

$DV_{DD}$  is the power supply voltage for the digital circuitry within the MCP3918. For optimal performance, it is recommended to connect appropriate bypass capacitors (typically a 10  $\mu\text{F}$  in parallel with a 0.1  $\mu\text{F}$  ceramic).  $DV_{DD}$  should be maintained between 2.7V and 3.6V for specified operation.

## 3.3 Analog Power Supply ( $AV_{DD}$ )

$AV_{DD}$  is the power supply voltage for the analog circuitry within the MCP3918. It is recommended to connect appropriate bypass capacitors (typically a 10  $\mu\text{F}$  in parallel with a 0.1  $\mu\text{F}$  ceramic).  $AV_{DD}$  should be maintained between 2.7V and 3.6V for specified operation.

## 3.4 ADC Differential Analog Inputs ( $CH0+/CH0-$ )

The  $CH0+/-$  pins are the fully differential analog voltage inputs for the delta-sigma ADC.

The linear and specified region of the channels is dependent on the PGA gain. This region corresponds to a differential voltage range of  $\pm 600 \text{ mV}/\text{GAIN}$  with  $V_{REF} = 1.2\text{V}$ .

The maximum absolute voltage, with respect to  $A_{GND}$ , for each  $CH0+/-$  input pin is  $\pm 1\text{V}$  with no distortion and  $\pm 2\text{V}$  with no breaking after continuous voltage. This maximum absolute voltage is not proportional to the  $V_{REF}$  voltage.

## 3.5 Analog Ground ( $A_{GND}$ )

$A_{GND}$  is the ground reference voltage for the analog circuitry within the MCP3918. For optimal performance, it is recommended to connect it to the same ground node voltage as  $D_{GND}$ , preferably with a star connection.

If an analog ground plane is available, it is recommended that these pins be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other analog circuitry in the system.

## 3.6 Non-Inverting Reference Input, Internal Reference Output ( $REFIN+/OUT$ )

This pin is the non-inverting side of the differential voltage reference input for the ADC or the internal voltage reference output.

When  $VREFEXT = 1$ , an external voltage reference source can be used, and the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its  $V_{REF+}$  pin. When using an external single-ended reference, it should be connected to this pin.

When  $VREFEXT = 0$ , the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability and thus needs proper buffering and bypass capacitances (a 0.1  $\mu\text{F}$  ceramic capacitor is sufficient in most cases), if used as a voltage source.

If the voltage reference is only used as an internal  $V_{REF}$ , adding bypass capacitance on  $REFIN+/OUT$  is not necessary for keeping ADC accuracy, but a minimal 0.1  $\mu\text{F}$  ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the  $REFIN+/OUT$  pin if left floating.

## 3.7 Inverting Reference Input ( $REFIN-$ )

This pin is the inverting side of the differential voltage reference input for the ADC. When using an external differential voltage reference, it should be connected to its  $V_{REF-}$  pin. When using an external single-ended voltage reference, or when  $VREFEXT = 0$  (default) and using the internal voltage reference, the pin should be directly connected to  $A_{GND}$ .

## 3.8 Digital Ground Connection ( $D_{GND}$ )

$D_{GND}$  is the ground reference voltage for the digital circuitry within the MCP3918. For optimal performance, it is recommended to connect it to the same ground node voltage as  $A_{GND}$ , preferably with a star connection.

If a digital ground plane is available, it is recommended that this pin be tied to this plane of the PCB. This plane should also reference all other digital circuitry in the system.

### 3.9 Modulator Output (MDAT0)

MDAT0 is the output pin for the modulator serial bit streams of the ADC. This pin is high-impedance when the EN\_MDAT bit is logic low. When the EN\_MDAT bit is enabled, the modulator bit stream of the ADC is present on the pin and updated at the AMCLK frequency (see [Section 5.3.5 “Modulator Output Block”](#) for a complete description of the modulator output). This pin can be directly connected to an MCU or a DSP when a specific digital filtering is needed. When the MDAT0 output pin is enabled, the DR output is disabled. In 2-Wire Interface mode, this pin is automatically inactive. Its state is high-impedance during the 2-Wire mode (therefore this pin can be left grounded in applications using exclusively the 2-Wire Interface mode; this configuration improves the EMI/EMC susceptibility of the device).

### 3.10 Data Ready Output/GAIN1 Logic Input (DR/GAIN1)

In SPI mode, the Data Ready pin indicates if a new conversion result is ready to be read. The default state of this pin is logic high when  $\overline{\text{DR\_HIZ}} = 1$  and is high-impedance when  $\overline{\text{DR\_HIZ}} = 0$  (default). After each conversion is finished, a logic low pulse will take place on the Data Ready pin to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The Data Ready pin is independent from the SPI interface and acts like an interrupt output. The Data Ready pin state is not latched, and the pulse width (and period) are both determined by the MCLK frequency, oversampling rate, and internal clock prescale settings. The Data Ready pulse width is equal to half a DMCLK period and the frequency of the pulses is equal to DRCLK (see [Figure 1-3](#)).

In 2-Wire Interface mode, this is the GAIN1 logic select pin. See [Section 7.0 “2-Wire Serial Interface Description”](#) for the logic input table for GAIN0 and GAIN1. The pin state is latched when the MODE changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

**Note:** This pin should not be left floating when the DR\_HIZ bit is low; a 100 k $\Omega$  pull-up resistor connected to DV<sub>DD</sub> is recommended.

### 3.11 Crystal Oscillator/Master Clock Input/GAIN0 Logic Input (OSC1/CLKI/GAIN0)

In SPI mode, OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = 0, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation.

The typical clock frequency specified is 4 MHz. For proper operation and in order to optimize ADC accuracy, AMCLK should be limited to the maximum frequency defined in [Table 5-2](#) for the function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit  $\text{AMCLK} = \text{MCLK}/\text{PRESCALE}$  in the defined range in [Table 5-2](#). Appropriate load capacitance should be connected to these pins for proper operation.

In 2-Wire Interface mode, this is the GAIN0 logic select pin. See [Section 7.0 “2-Wire Serial Interface Description”](#) for the logic input table for GAIN0 and GAIN1. The pin state is latched when the MODE changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

**Note:** When CLKEXT = 1, the crystal oscillator is disabled. OSC1 becomes the master clock input CLKI, a direct path for an external clock source. One example would be a clock source generated by an MCU.

### 3.12 Crystal Oscillator Output/Interface MODE Logic Input (OSC2/MODE)

When CLKEXT = 0 (default), a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation. Appropriate load capacitance should be connected to these pins for proper operation.

When CLKEXT = 1 (default condition at POR), this pin is the MODE selection pin for the digital interface. When MODE is logic low, the SPI interface is selected (see [Section 6.0 “SPI Serial Interface Description”](#)). When MODE is logic high, the 2-Wire interface is selected (see [Section 7.0 “2-Wire Serial Interface Description”](#)). The MODE input is latched after a POR, a Master Reset and/or a Watchdog Timer Reset.

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## 3.13 Chip Select/ Boost Logic Input (CS/BOOST)

In SPI mode, this pin is the SPI chip select that enables serial communication. When this pin is logic high, no communication can take place. A chip select falling edge initiates serial communication, and a chip select rising edge terminates the communication. No communication can take place even when  $\overline{CS}$  is logic low, if RESET is also logic low.

This input is Schmitt-triggered.

In the 2-Wire Interface mode, this is the Boost logic select pin. See [Section 7.0 “2-Wire Serial Interface Description”](#) for the logic input table for Boost. The pin state is latched when the mode changes to 2-Wire Interface mode, and is re-latched at each watchdog timer reset.

## 3.14 Serial Data Clock/ Master Clock Input (SCK/MCLK)

In SPI mode, this is the serial clock pin for SPI communication. Data is clocked into the device on the rising edge of SCK. Data is clocked out of the device on the falling edge of SCK.

The MCP3918 SPI interface is compatible with SPI 0,0 and 1,1 modes. SPI modes can be changed during a CS high time.

The maximum clock speed specified is 20 MHz. SCK and MCLK are two different and asynchronous clocks; SCK is only required when a communication happens, while MCLK is continuously required when the part is converting analog inputs.

This input is Schmitt-triggered.

In the 2-Wire Interface mode, this pin is defining the master clock of the device (MCLK) and the serial clock (SCK) for the interface simultaneously. In this mode, the clock has to be provided continuously to ensure proper operation. See [Section 7.0 “2-Wire Serial Interface Description”](#) for more information and timing diagrams of the 2-Wire interface protocol.

## 3.15 Serial Data Output (SDO)

This is the SPI data output pin. Data is clocked out of the device on the falling edge of SCK.

This pin remains in a high-impedance state during the command byte. It also stays high-impedance during the entire communication for Write commands and when the CS pin is logic high or when the RESET pin is logic low. This pin is active only when a Read command is processed. The interface is half-duplex (inputs and outputs do not happen at the same time).

In the 2-Wire Interface Mode, this pin is the only digital output pin, and sends synchronous frames at each data ready with data bits clocked out on the falling edge of SCK.

## 3.16 Serial Data/OSR1 Logic Input (SDI/OSR1)

In SPI mode, this is the SPI data input pin. Data is clocked into the device on the rising edge of SCK. When  $\overline{CS}$  is logic low, this pin is used to communicate with 8-bit commands followed by data bytes that can be 16-/24- or 32-bit wide. The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge followed by an 8-bit command word, entered through the SDI pin. Each command is either a Read or a Write command. Toggling SDI during a Read command has no effect.

This input is Schmitt-triggered.

In 2-Wire Interface mode, this is the OSR1 logic select pin. See [Section 7.0 “2-Wire Serial Interface Description”](#) for the logic input table for OSR0 and OSR1. The pin state is latched when the mode changes to 2-Wire Interface Mode, and is re-latched at each watchdog timer reset.

## 3.17 Exposed Pad (EP)

Exposed Thermal Pad. This pin must be connected to A<sub>GND</sub> for optimal accuracy and thermal performance. This pad can also be left floating if necessary. Connecting it to A<sub>GND</sub> is preferable for the lowest noise performance and best thermal behavior.

## 4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

- **MCLK – Master Clock**
- **AMCLK – Analog Master Clock**
- **DMCLK – Digital Master Clock**
- **DRCLK – Data Rate Clock**
- **OSR – Oversampling Ratio**
- **Offset Error**
- **Gain Error**
- **Integral Non-Linearity Error**
- **Signal-to-Noise Ratio (SNR)**
- **Signal-to-Noise and Distortion Ratio (SINAD)**
- **Total Harmonic Distortion (THD)**
- **Spurious-Free Dynamic Range (SFDR)**
- **MCP3918 Delta-Sigma Architecture**
- **Idle Tones**
- **Dithering**
- **PSRR**
- **CMRR**
- **ADC Reset Mode**
- **Hard Reset Mode (RESET = 0)**
- **ADC Shutdown Mode**
- **Full Shutdown Mode**

## 4.1 MCLK – Master Clock

This is the fastest clock present on the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1. In the 2-Wire mode, this is the frequency present at the SCK input pin. See [Figure 4-1](#).

## 4.2 AMCLK – Analog Master Clock

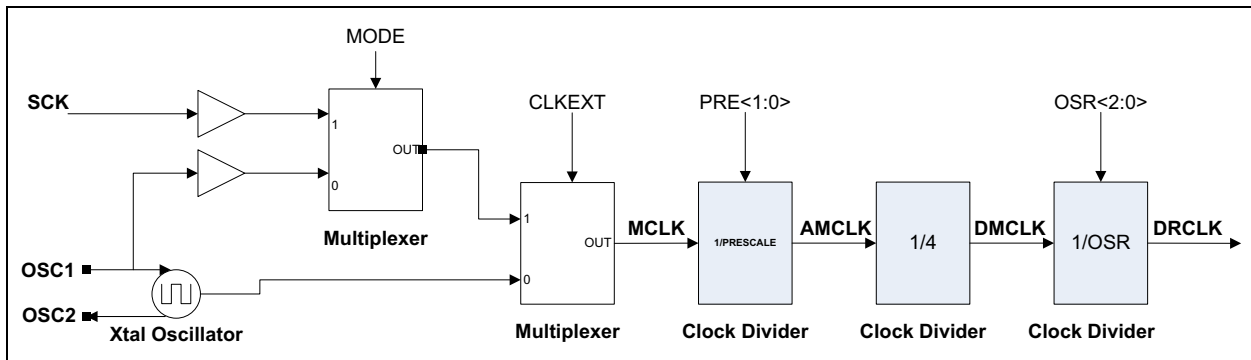
AMCLK is the clock frequency that is present on the analog portion of the device, after prescaling has occurred via the PRE<1:0> bits in the CONFIG0 register (see [Equation 4-1](#)). The analog portion includes the PGA and one delta-sigma modulator.

**EQUATION 4-1:**

$$AMCLK = \frac{MCLK}{PRESCALE}$$

**TABLE 4-1: MCP3918 OVERSAMPLING RATIO SETTINGS**

CONFIG0		Analog Master Clock Prescale
PRE<1:0>		
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8



**FIGURE 4-1:** Clock Sub-Circuitry.

## 4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device, after prescaling and division by four ([Equation 4-2](#)). This is also the sampling frequency, which is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output. See [Figure 4-1](#).

**EQUATION 4-2:**

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

## 4.4 DRCLK – Data Rate Clock

This is the output data rate, i.e. the rate at which the ADC outputs new data. Each new data is signaled by a Data Ready pulse on the Data Ready pin.

This data rate is dependent on the OSR and the prescaler with the formula in [Equation 4-3](#).

**EQUATION 4-3:**

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$



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Since this is the output data rate, and because the decimation filter is a sinc (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

Table 4-2 describes the various combinations of OSR and PRESCALE, and their associated AMCLK, DMCLK and DRCLK rates.

**TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE, MCLK = 4 MHZ**

PRE<1:0>		OSR<2:0>			OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)	SINAD (dB) Note 1	ENOB from SINAD (bits) Note 1
1	1	1	1	1	4096	MCLK/8	MCLK/32	MCLK/131072	0.035	102.5	16.7
1	1	1	1	0	2048	MCLK/8	MCLK/32	MCLK/65536	0.061	100	16.3
1	1	1	0	1	1024	MCLK/8	MCLK/32	MCLK/32768	0.122	97	15.8
1	1	1	0	0	512	MCLK/8	MCLK/32	MCLK/16384	0.244	96	15.6
1	1	0	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.488	95	15.5
1	1	0	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976	90	14.7
1	1	0	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95	83	13.5
1	1	0	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9	70	11.3
1	0	1	1	1	4096	MCLK/4	MCLK/16	MCLK/65536	0.061	102.5	16.7
1	0	1	1	0	2048	MCLK/4	MCLK/16	MCLK/32768	0.122	100	16.3
1	0	1	0	1	1024	MCLK/4	MCLK/16	MCLK/16384	0.244	97	15.8
1	0	1	0	0	512	MCLK/4	MCLK/16	MCLK/8192	0.488	96	15.6
1	0	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976	95	15.5
1	0	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95	90	14.7
1	0	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9	83	13.5
1	0	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125	70	11.3
0	1	1	1	1	4096	MCLK/2	MCLK/8	MCLK/32768	0.122	102.5	16.7
0	1	1	1	0	2048	MCLK/2	MCLK/8	MCLK/16384	0.244	100	16.3
0	1	1	0	1	1024	MCLK/2	MCLK/8	MCLK/8192	0.488	97	15.8
0	1	1	0	0	512	MCLK/2	MCLK/8	MCLK/4096	0.976	96	15.6
0	1	0	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95	95	15.5
0	1	0	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9	90	14.7
0	1	0	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125	83	13.5
0	1	0	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625	70	11.3
0	0	1	1	1	4096	MCLK	MCLK/4	MCLK/16384	0.244	102.5	16.7
0	0	1	1	0	2048	MCLK	MCLK/4	MCLK/8192	0.488	100	16.3
0	0	1	0	1	1024	MCLK	MCLK/4	MCLK/4096	0.976	97	15.8
0	0	1	0	0	512	MCLK	MCLK/4	MCLK/2048	1.95	96	15.6
0	0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9	95	15.5
0	0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125	90	14.7
0	0	0	0	1	64	MCLK	MCLK/4	MCLK/256	15.625	83	13.5
0	0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25	70	11.3

**Note 1:** For OSR = 32 and 64, DITHER = None. For OSR = 128 and higher, DITHER = Maximum. The SINAD values are given for GAIN = 1.

## 4.5 OSR – Oversampling Ratio

This is the ratio of the sampling frequency to the output data rate:  $OSR = DMCLK/DRCLK$ . The default OSR is 256, with  $MCLK = 4\text{ MHz}$ ,  $PRESCALE = 1$ ,  $AMCLK = 4\text{ MHz}$ ,  $f_S = 1\text{ MHz}$ , and  $f_D = 3.90625\text{ kbps}$ . The bits in [Table 4-3](#), available in the CONFIG0 register, are used to change the oversampling ratio (OSR).

**TABLE 4-3: MCP3918 OVERSAMPLING RATIO SETTINGS**

CONFIG0			Oversampling Ratio (OSR)
OSR<2:0>			
0	0	0	32
0	0	1	64
0	1	0	128
0	1	1	256 (Default)
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

## 4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together ( $V_{IN} = 0V$ ). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip to chip. The offset is specified in  $\mu V$ . The offset error can be digitally compensated independently on each channel through the OFFCAL\_CH0 register with a 24-bit calibration word.

The offset on the MCP3918 has a low temperature coefficient.

## 4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in %, compared to the ideal transfer function defined in [Equation 5-3](#). The specification incorporates both PGA and ADC gain error contributions, but not the  $V_{REF}$  contribution (it is measured with an external  $V_{REF}$ ).

This error varies with PGA and OSR settings. The gain error can be digitally compensated independently on each channel through the GAINCAL\_CH0 register with a 24-bit calibration word.

The gain error on the MCP3918 has a low temperature coefficient.

## 4.8 Integral Non-Linearity Error

Integral non-linearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

## 4.9 Signal-to-Noise Ratio (SNR)

For the MCP3918 ADC, the signal-to-noise ratio is a ratio of the output fundamental signal power to noise power (not including the harmonics of the signal), when the input is a sine wave at a predetermined frequency (see [Equation 4-4](#)). It is measured in dB. Usually, only the maximum signal-to-noise ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

**EQUATION 4-4: SIGNAL-TO-NOISE RATIO**

$$SNR(dB) = 10\log\left(\frac{SignalPower}{NoisePower}\right)$$

## 4.10 Signal-to-Noise and Distortion Ratio (SINAD)

The most important figure of merit for the analog performance of the ADC present on the MCP3918 is the Signal-to-Noise and Distortion (SINAD) specification.

The Signal-to-Noise and Distortion ratio is similar to signal-to-noise ratio, with the exception that you must include the harmonics power in the noise power calculation (see [Equation 4-5](#)). The SINAD specification depends mainly on the OSR and DITHER settings.

**EQUATION 4-5: SINAD EQUATION**

$$SINAD(dB) = 10\log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD (see [Equation 4-6](#)).

**EQUATION 4-6: SINAD, THD AND SNR RELATIONSHIP**

$$SINAD(dB) = 10\log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$