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MCP3919

3V Three-Channel Analog Front End

Features:

- Three Synchronous Sampling 24-bit Resolution Delta-Sigma A/D Converters
- 93.5 dB SINAD, -107 dBc Total Harmonic Distortion (THD) (up to 35th Harmonic), 112 dBFS SFDR for Each Channel
- Enables 0.1% Typical Active Power Measurement Error over a 10,000:1 Dynamic Range
- Advanced Security Features:
  - 16-bit Cyclic Redundancy Check (CRC) Checksum on All Communications for Secure Data Transfers
  - 16-bit CRC Checksum and Interrupt Alert for Register Map Configuration
  - Register Map Lock with 8-bit Secure Key
- 2.7V-3.6V AV_{DD}, DV_{DD}
- Programmable Data Rate up to 125 ksps:
  - 4 MHz Maximum Sampling Frequency
  - 16 MHz Maximum Master Clock
- Oversampling Ratio up to 4096
- Ultra-Low Power Shutdown Mode with < 10 µA
- -122 dB Crosstalk between Channels
- Low Drift 1.2V Internal Voltage Reference: 9 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain PGA on Each Channel (up to 32 V/V)
- Phase Delay Compensation with 1 µs Time Resolution
- Separate Data Ready Pin for Easy Synchronization
- Individual 24-bit Digital Offset and Gain Error Correction for Each Channel
- High-Speed 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Continuous Read/Write Modes for Minimum Communication Time with Dedicated 16/32-bit Modes
- Available in a 28-lead 5 x 5 mm QFN and 28-lead SSOP Packages
- Extended Temperature Range: -40°C to +125°C

Description:

The MCP3919 is a 3V three-channel Analog Front End (AFE) containing three synchronous sampling delta-sigma Analog-to-Digital Converters (ADC), three PGAs, phase delay compensation block, low-drift internal voltage reference, digital offset and gain error calibration registers and high-speed 20 MHz SPI-compatible serial interface.

The MCP3919 ADCs are fully configurable with features such as: 16/24-bit resolution, Oversampling Ratio (OSR) from 32 to 4096, gain from 1x to 32x, independent Shutdown and Reset, dithering and auto-zeroing. The communication is largely simplified with 8-bit commands including various continuous read/write modes and 16/24/32-bit data formats that can be accessed by the Direct Memory Access (DMA) of an 8/16- or 32-bit MCU and with the separate data ready pin that can directly be connected to an Interrupt Request (IRQ) input of an MCU.

The MCP3919 includes advanced security features to secure the communications and the configuration settings such as a CRC-16 checksum on both serial data outputs and static register map configuration. It also includes a register-map lock through an 8-bit secure key to stop unwanted write commands from processing.

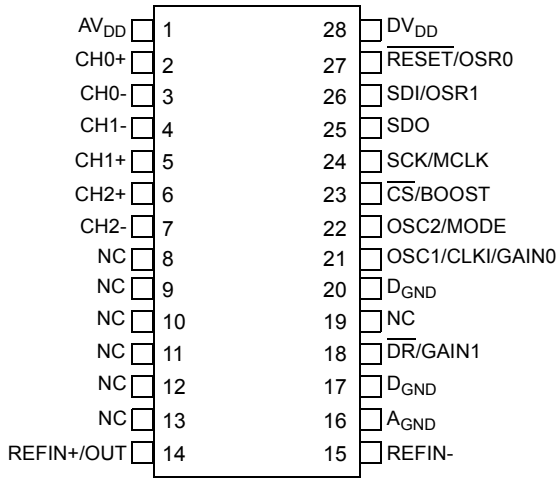
The MCP3919 is capable of interfacing with a variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall-effect sensors.

Applications:

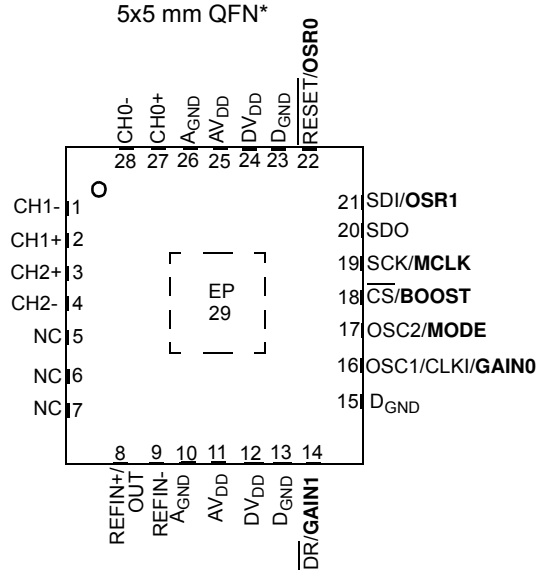
- Polyphase Energy Meters
- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring
- Audio/Voice Recognition

Package Type

MCP3919
SSOP

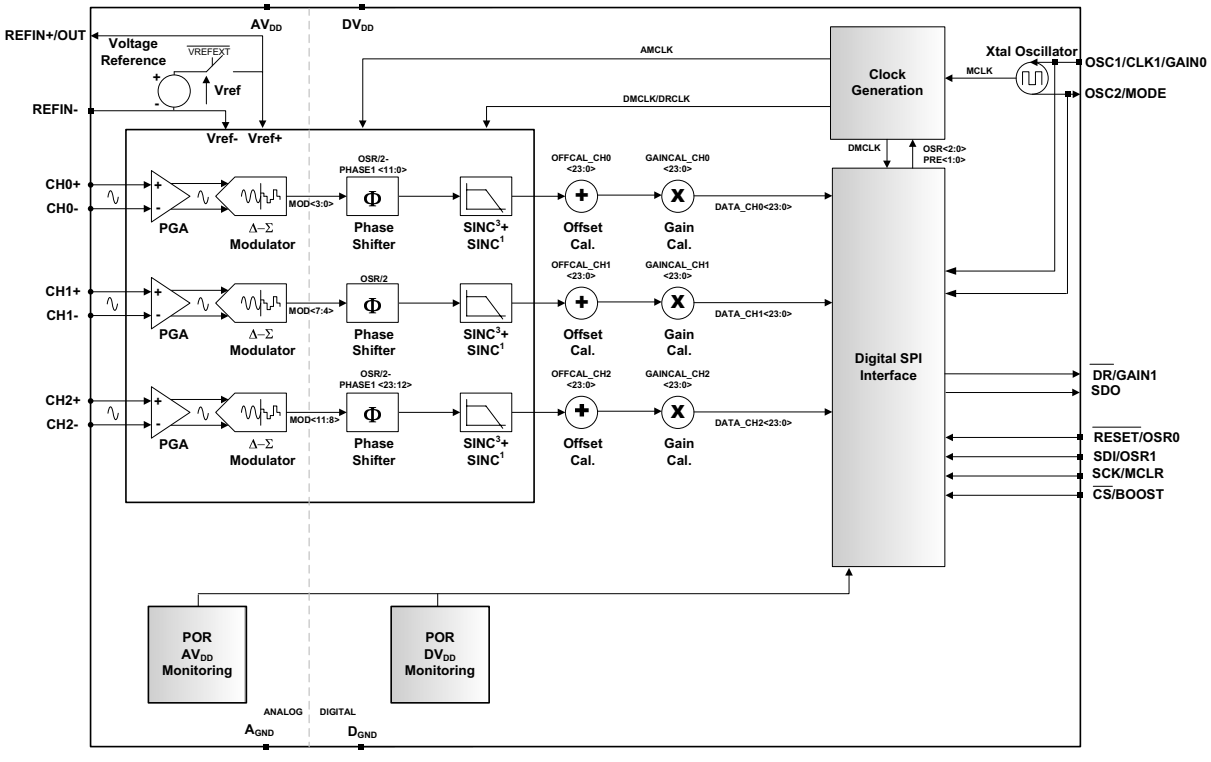


MCP3919
5x5 mm QFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} ..... -0.3V to 4.0V
Digital inputs and outputs w.r.t. A_{GND} ..... --0.3V to 4.0V
Analog input w.r.t. A_{GND} ....-2V to +2V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to V_{DD} +0.6V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on all pins (HBM,MM) ..... 4 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Electrical Specifications

TABLE 1-1: ANALOG SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Performance						
Resolution (No missing codes)		24	—	—	bits	OSR = 256 or greater
Sampling Frequency	f_S(DMCLK)	—	1	4	MHz	For maximum condition, BOOST<1:0> = 11
Output Data Rate	f_D(DRCLK)	—	4	125	ksps	For maximum condition, BOOST<1:0> = 11, OSR = 32
Analog Input Absolute Voltage on CHn+/- pins, n between 0 and 2	CHn+/-	-1	—	+1	V	All analog input channels, measured to A_{GND}
Analog Input Leakage Current	I_{IN}	—	+/-1	—	nA	RESET<2:0> = 111, MCLK running continuously
Differential Input Voltage Range	(CH_{n+}-CH_{n-})	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	0.2	1	mV	**Note 5**
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-5	—	+5	%	**Note 5**

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 000, RESET<2:0> = 000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The specification is the average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Gain Error Drift		—	1	—	ppm/°C	
Integral Nonlinearity	INL	—	5	—	ppm	
Measurement Error	ME	—	0.1	—	%	Measured with a 10,000:1 dynamic range (from 600 mV_{Peak} to 60 μV_{Peak}), AV_{DD} = DV_{DD} = 3V, measurement points averaging time: 20 seconds, measured on each channel pair (CH0/1, CH1/2)
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1, proportional to 1/AMCLK
		142	—	—	kΩ	G = 2, proportional to 1/AMCLK
		72	—	—	kΩ	G = 4, proportional to 1/AMCLK
		38	—	—	kΩ	G = 8, proportional to 1/AMCLK
		36	—	—	kΩ	G = 16, proportional to 1/AMCLK
		33	—	—	kΩ	G = 32, proportional to 1/AMCLK
Signal-to-Noise and Distortion Ratio (**Note 1**)	SINAD	92	93.5	—	dB	
Total Harmonic Distortion (**Note 1**)	THD	—	-107	-103	dBc	Includes the first 35 harmonics
Signal-to-Noise Ratio (**Note 1**)	SNR	92	94	—	dB	
Spurious Free Dynamic Range (**Note 1**)	SFDR	—	112	—	dBFS	
Crosstalk (50, 60 Hz)	CTALK	—	-122	—	dB	**Note 4**
AC Power Supply Rejection	AC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 3V + 0.6V_{PP} 50/60 Hz, 100/120 Hz
DC Power Supply Rejection	DC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 2.7V to 3.6V
DC Common Mode Rejection	DC CMRR	—	-100	—	dB	V_{CM} from -1V to +1V

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 000, RESET<2:0> = 000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The specification is the average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference						
Tolerance	V_{REF}	1.176	1.2	1.224	V	VREFEXT = 0, T_A = +25°C only
Temperature Coefficient	TCV_{REF}	—	9	—	ppm/°C	T_A = -40°C to +125°C, VREFEXT = 0, VREFCAL<7:0> = 0x50
Output Impedance	$ZOUTV_{REF}$	—	0.6	—	kΩ	VREFEXT = 0
Internal Voltage Reference Operating Current	$AI_{DD}V_{REF}$	—	54	—	µA	VREFEXT = 0, SHUTDOWN<2:0> = 111
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Differential Input Voltage Range (V_{REF+} – V_{REF-})	V_{REF}	1.1	—	1.3	V	VREFEXT = 1
Absolute Voltage on REFIN+ pin	V_{REF+}	V_{REF-} + 1.1	—	V_{REF-} + 1.3	V	VREFEXT = 1
Absolute Voltage REFIN- pin	V_{REF-}	-0.1	—	+0.1	V	REFIN- should be connected to A_{GND} when VREFEXT = 0
Master Clock Input						
Master Clock Input Frequency Range	f_{MCLK}	—	—	20	MHz	CLKEXT = 1, **(Note 7)**
Crystal Oscillator Operating Frequency Range	f_{XTAL}	1	—	20	MHz	CLKEXT = 0, **(Note 7)**
Analog Master Clock	AMCLK	—	—	16	MHz	**(Note 7)**
Crystal Oscillator Operating Current	DIDDXTAL	—	80	—	µA	CLKEXT = 0
Power Supply						
Operating Voltage, Analog	AV_{DD}	2.7	—	3.6	V	
Operating Voltage, Digital	DV_{DD}	2.7	—	3.6	V	

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 000, RESET<2:0> = 000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The specification is the average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C;V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Current, Analog (**Note 2**)	$I_{DD,A}$	—	2.1	3.1	mA	BOOST<1:0> = 00
		—	2.6	3.9	mA	BOOST<1:0> = 01
		—	3.5	4.9	mA	BOOST<1:0> = 10
		—	6.1	8.8	mA	BOOST<1:0> = 11
Operating Current, Digital	$I_{DD,D}$	—	0.26	0.45	mA	MCLK = 4 MHz, proportional to MCLK (**Note 2**)
		—	1	—	mA	MCLK = 16 MHz, proportional to MCLK (**Note 2**)
Shutdown Current, Analog	$I_{DDS,A}$	—	0.01	2	µA	AV_{DD} pin only (**Note 3**), (**Note 8**)
Shutdown Current, Digital	$I_{DDS,D}$	—	0.01	4	µA	DV_{DD} pin only (**Note 3**), (**Note 8**)
Pull-Down Current on OSC2 Pin (External Clock mode only)	I_{OSC2}	—	35	—	µA	CLKEXT = 1

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 000, RESET<2:0> = 000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<2:0> = 111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The specification is the average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

1.2 Serial Interface Characteristics

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, C_{LOAD} = 30 pF, applies to all digital I/O.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
High-Level Input Voltage	V_{IH}	0.7 DV_{DD}	—	—	V	Schmitt-Triggered
Low-Level Input Voltage	V_{IL}	—	—	0.3 DV_{DD}	V	Schmitt-Triggered
Input Leakage Current	I_{LI}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{IN} = D_{GND} to DV_{DD}
Output Leakage Current	I_{LO}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{OUT} = D_{GND} or DV_{DD}
Hysteresis Of Schmitt-Trigger Inputs	V_{HYS}	—	500	—	mV	DV_{DD} = 3.3V only, **Note 2**
Low-Level Output Voltage	V_{OL}	—	—	0.2 DV_{DD}	V	I_{OL} = +1.7 mA
High-Level Output Voltage	V_{OH}	0.75 DV_{DD}	—	—	V	I_{OH} = -1.7 mA
Internal Capacitance (All Inputs And Outputs)	C_{INT}	—	—	7	pF	T_A = +25°C, SCK = 1.0 MHz, DV_{DD} =3.3V **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-3: SERIAL AC CHARACTERISTICS TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, GAIN = 1, C_{LOAD} = 30 pF						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Serial Clock Frequency	f_{SCK}	—	—	20	MHz	
$\overline{CS}$ Setup Time	t_{CSS}	25	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	50	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	50	—	—	ns	
Data Setup Time	t_{SU}	5	—	—	ns	
Data Hold Time	t_{HD}	10	—	—	ns	
Serial Clock High Time	t_{HI}	20	—	—	ns	
Serial Clock Low Time	t_{LO}	20	—	—	ns	
Serial Clock Delay Time	t_{CLD}	50	—	—	ns	
Serial Clock Enable Time	t_{CLE}	50	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	25	ns	
Output Hold Time	t_{HO}	0	—	—	ns	**Note 1**
Output Disable Time	t_{DIS}	—	—	25	ns	**Note 1**
Reset Pulse Width ($\overline{RESET}$)	t_{MCLR}	100	—	—	ns	
Data Transfer Time to $\overline{DR}$ (Data Ready)	t_{DODR}	—	—	25	ns	**Note 2**
Data Ready Pulse Low Time	t_{DRP}	—	1/(2 x DMCLK)	—	µs	
2-Wire Mode Enable Time	t_{MODE}	—	—	50	ns	
2-Wire Mode Watchdog Timer	t_{WATCH}	3.6	—	35	µs	

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7 to 3.6V, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units.**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28L SSOP	θ_{JA}	—	80	—	°C/W	
Thermal Resistance, 28L 5x5 QFN	θ_{JA}	—	41	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

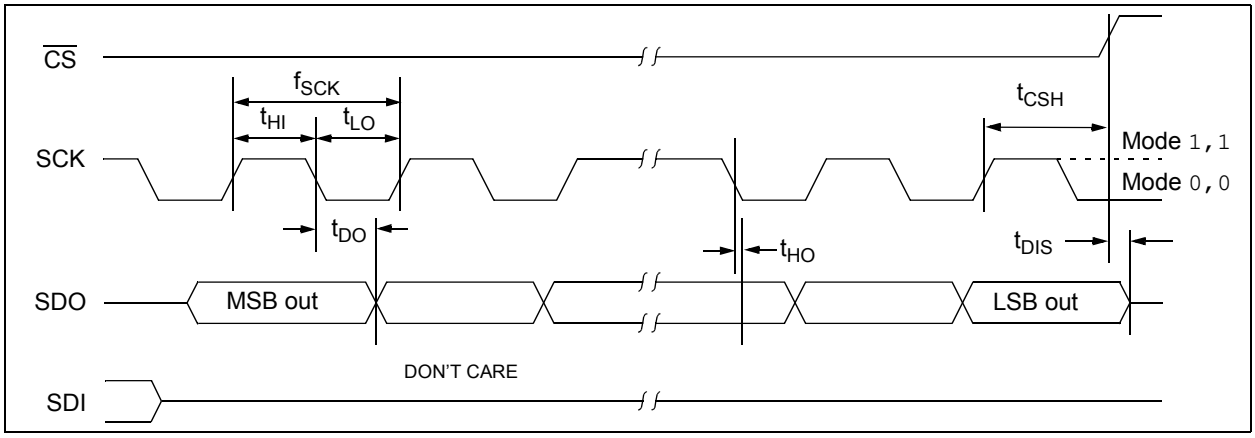


FIGURE 1-1: *Serial Output Timing Diagram.*

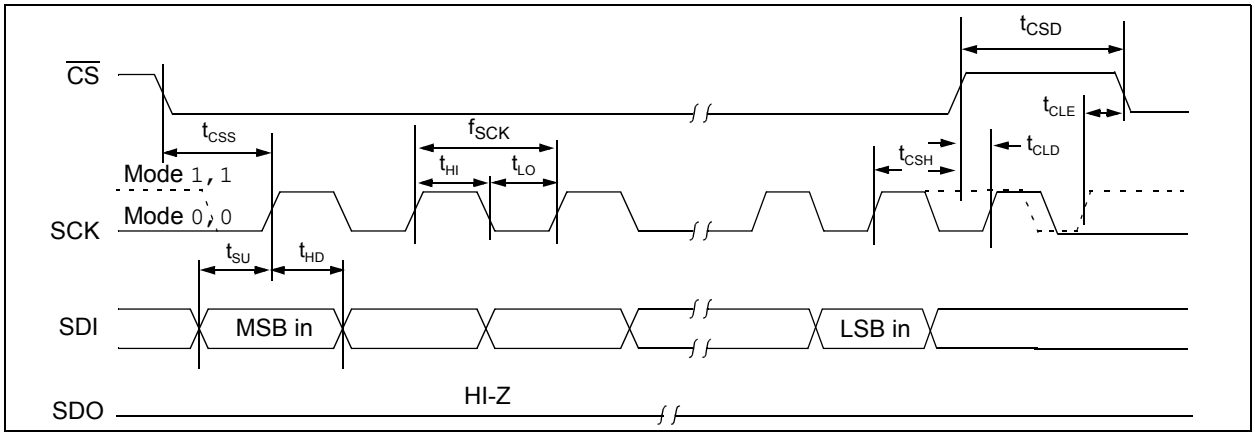


FIGURE 1-2: *Serial Input Timing Diagram.*

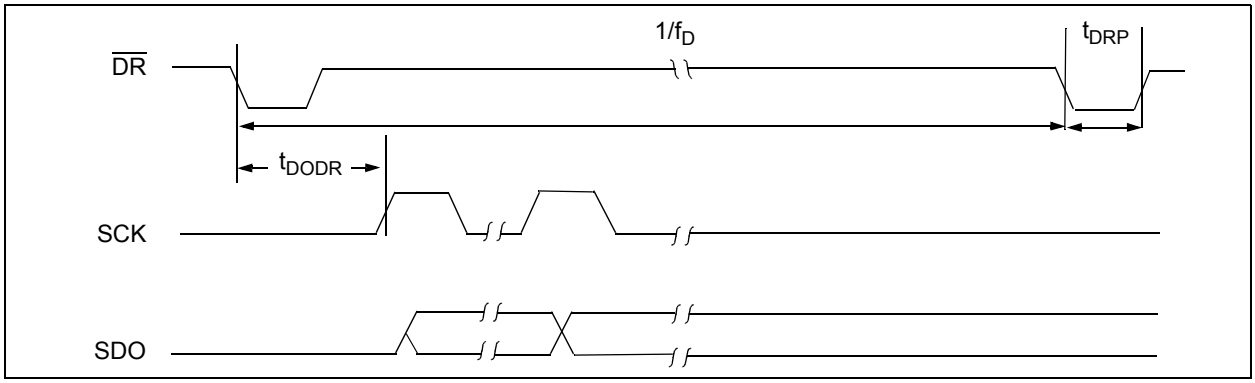


FIGURE 1-3: *Data Ready Pulse / Sampling Timing Diagram.*

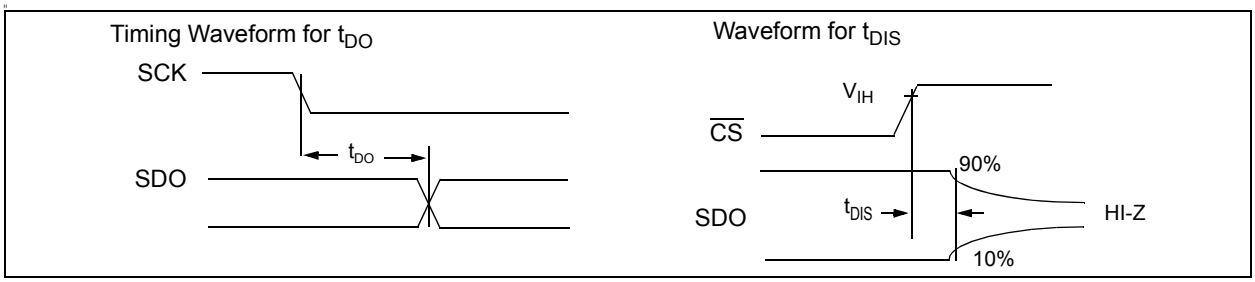


FIGURE 1-4: *Timing Diagrams, continued.*

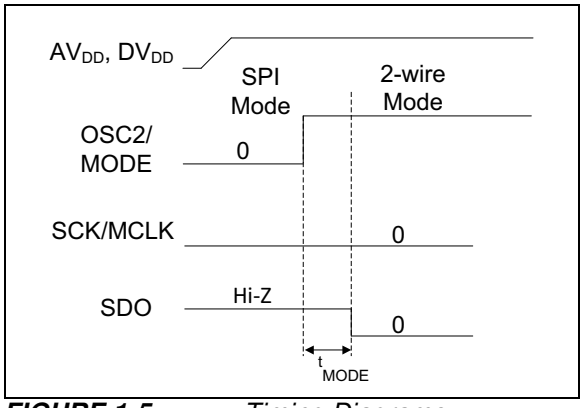


FIGURE 1-5: *Timing Diagrams, continued.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

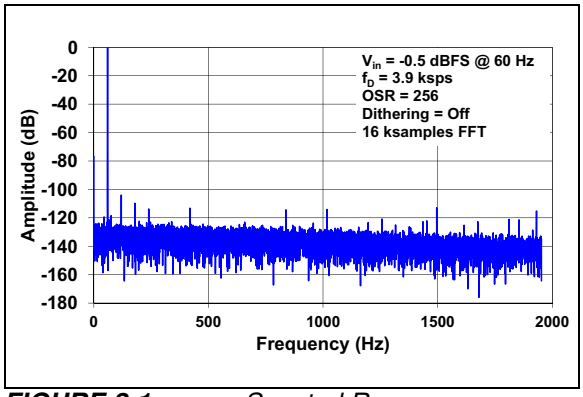


FIGURE 2-1: *Spectral Response.*

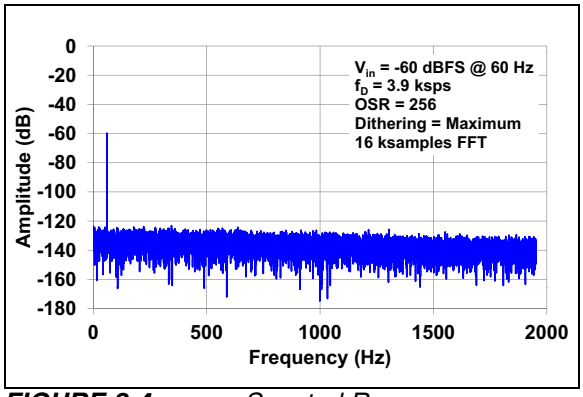


FIGURE 2-4: *Spectral Response.*

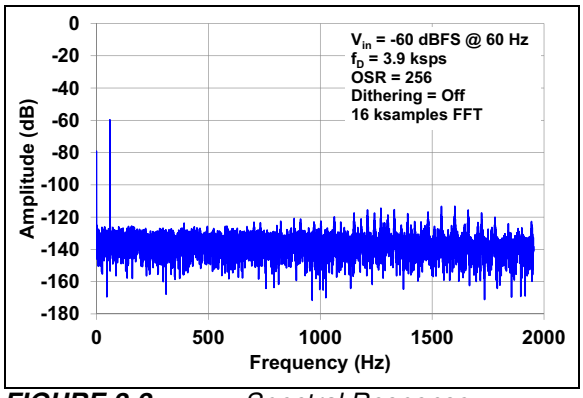


FIGURE 2-2: *Spectral Response.*

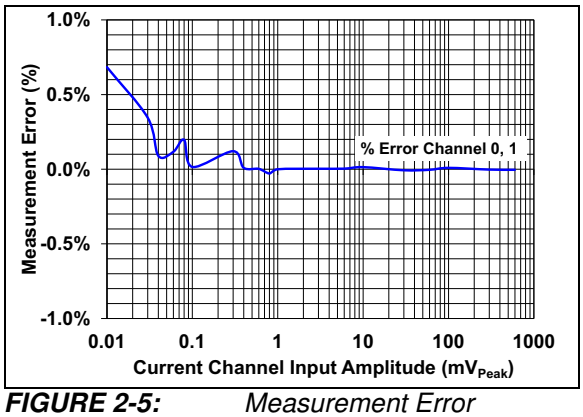


FIGURE 2-5: *Measurement Error with 1-Point Calibration.*

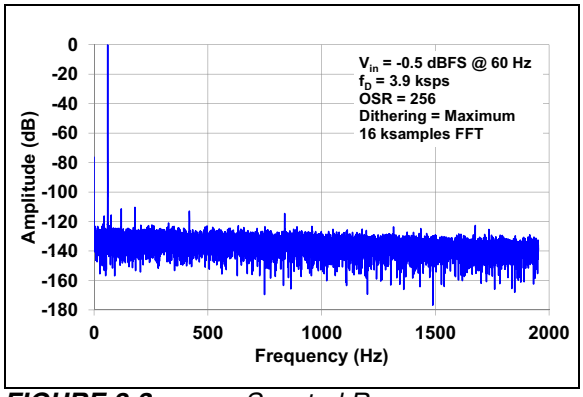


FIGURE 2-3: *Spectral Response.*

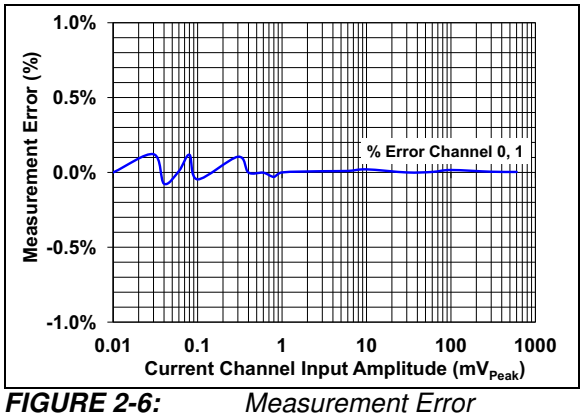


FIGURE 2-6: *Measurement Error with 2-Point Calibration.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

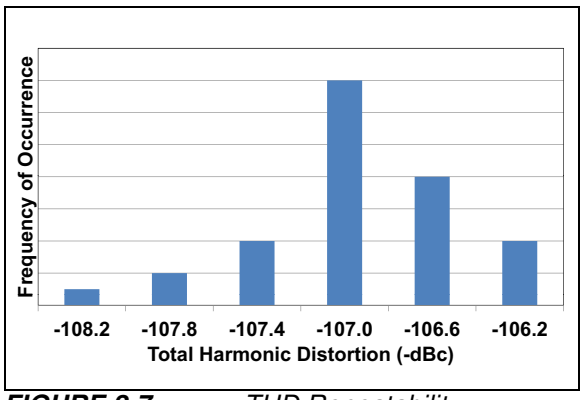


FIGURE 2-7: *THD Repatability Histogram.*

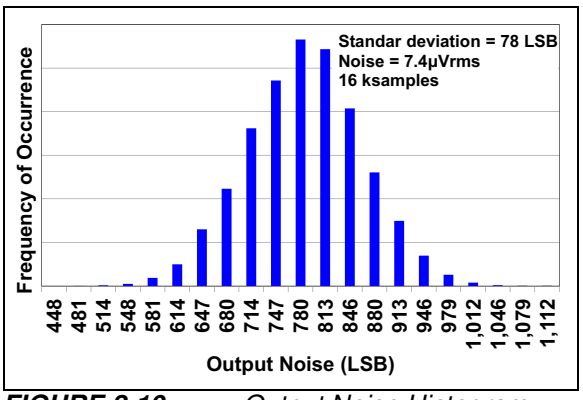


FIGURE 2-10: *Output Noise Histogram.*

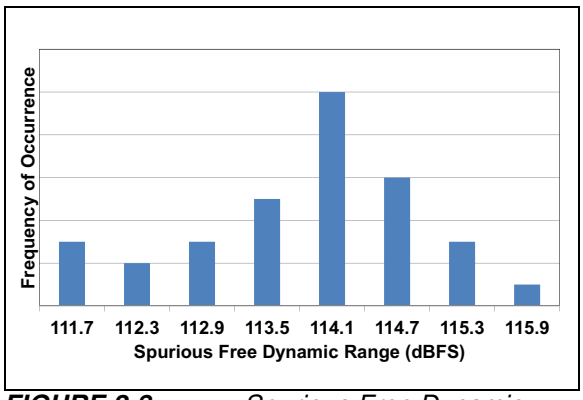


FIGURE 2-8: *Spurious Free Dynamic Range Repeatability Histogram.*

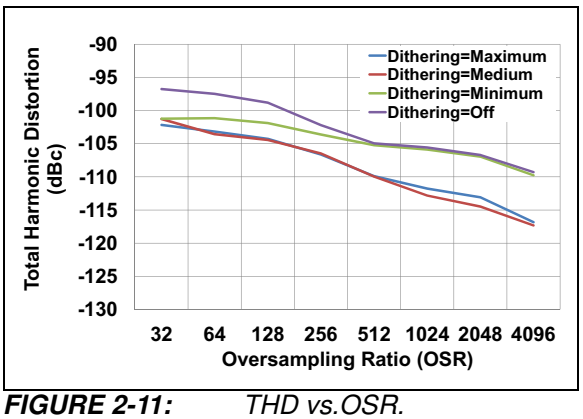


FIGURE 2-11: *THD vs.OSR.*

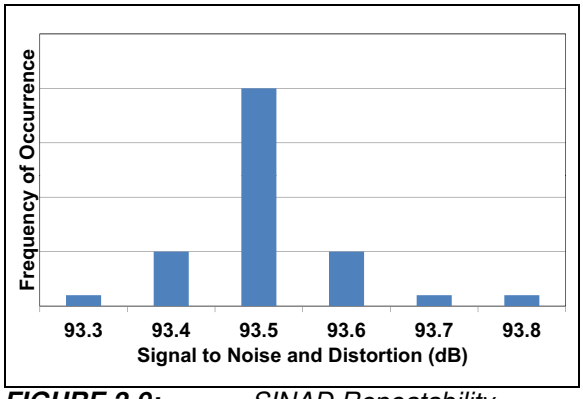


FIGURE 2-9: *SINAD Repeatability Histogram.*

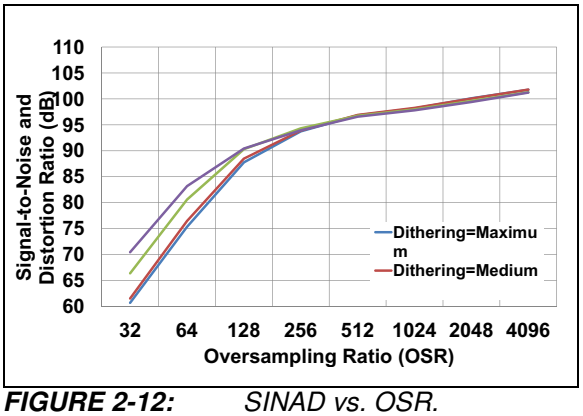


FIGURE 2-12: *SINAD vs. OSR.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

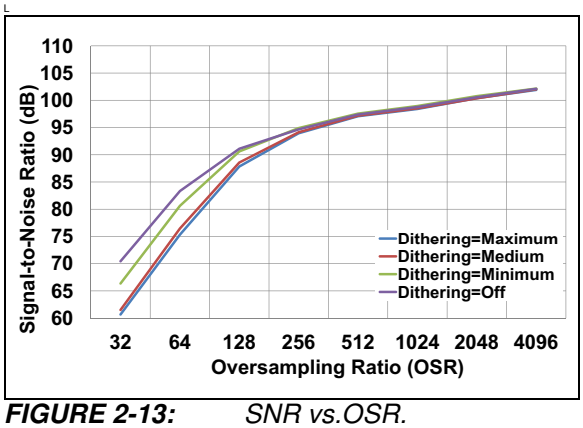


FIGURE 2-13: *SNR vs.OSR.*

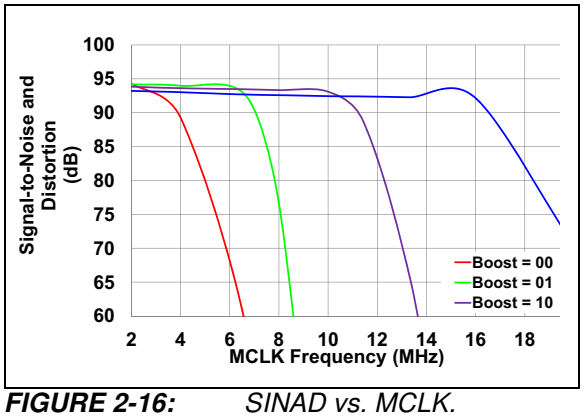


FIGURE 2-16: *SINAD vs. MCLK.*

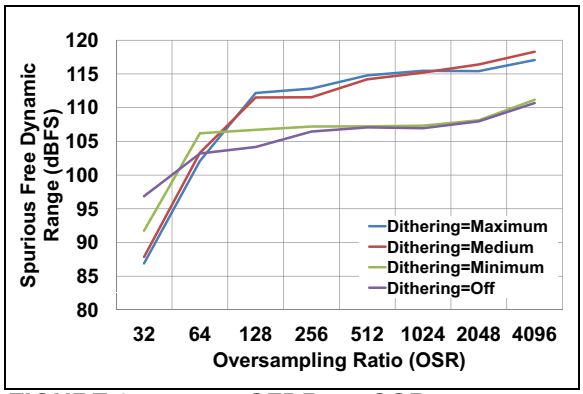


FIGURE 2-14: *SFDR vs. OSR.*

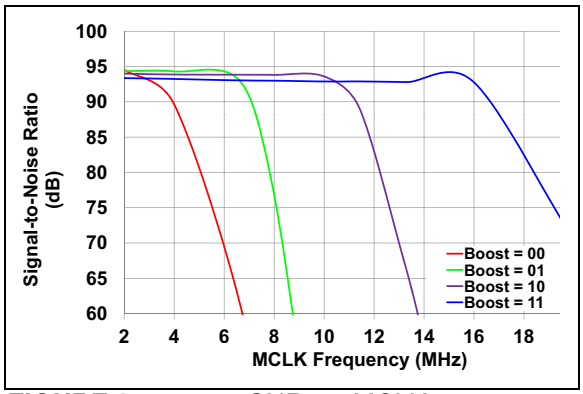


FIGURE 2-17: *SNR vs. MCLK.*

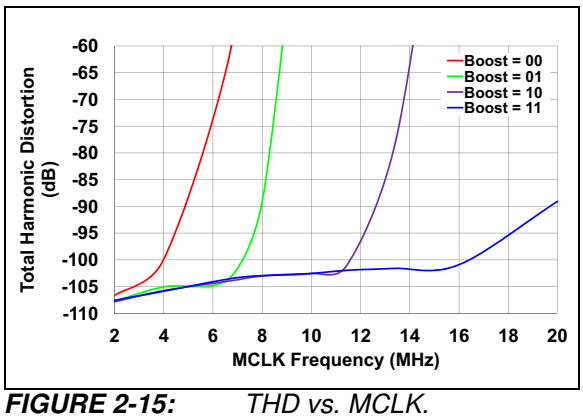


FIGURE 2-15: *THD vs. MCLK.*

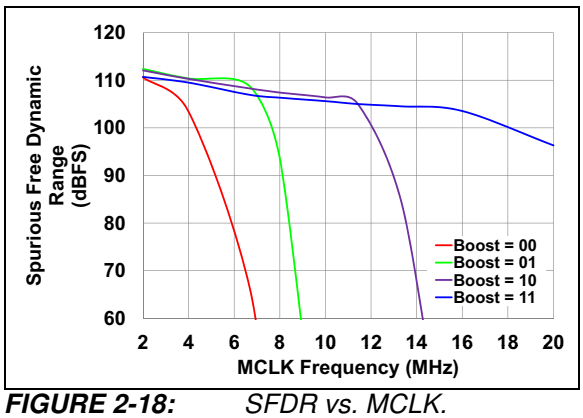


FIGURE 2-18: *SFDR vs. MCLK.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

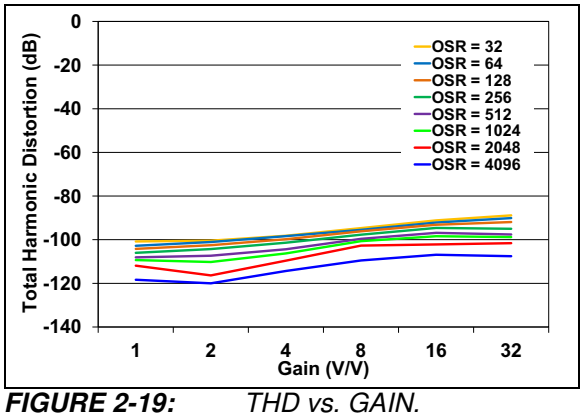


FIGURE 2-19: *THD vs. GAIN.*

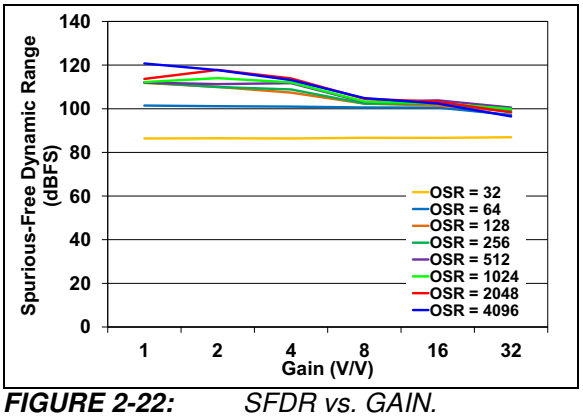


FIGURE 2-22: *SFDR vs. GAIN.*

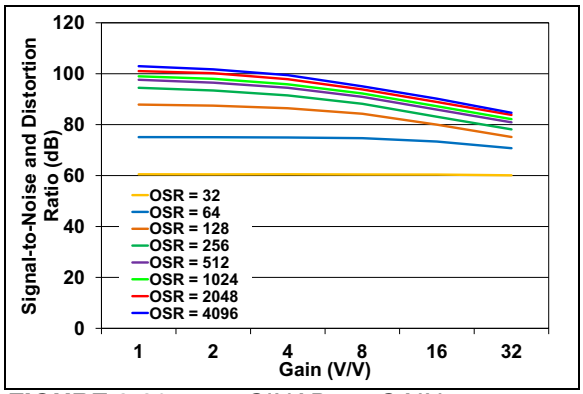


FIGURE 2-20: *SINAD vs. GAIN.*

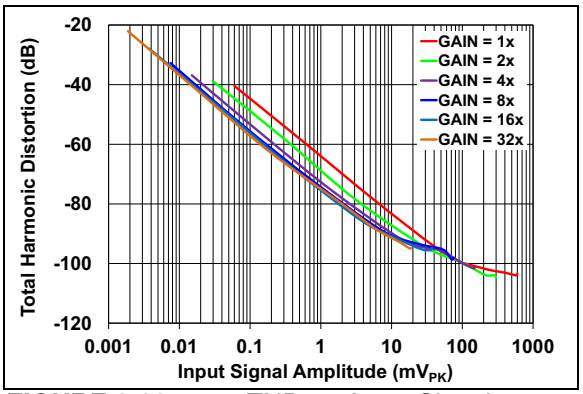


FIGURE 2-23: *THD vs. Input Signal Amplitude.*

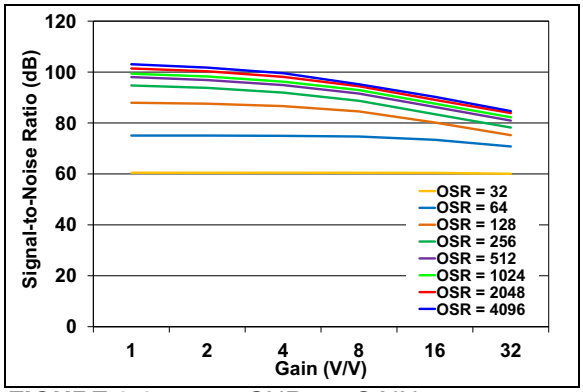


FIGURE 2-21: *SNR vs. GAIN.*

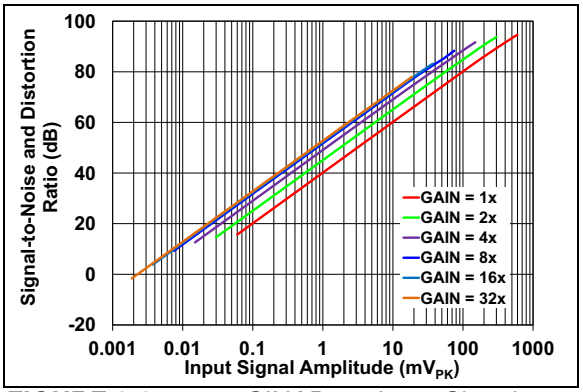


FIGURE 2-24: *SINAD vs. Input Signal Amplitude.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

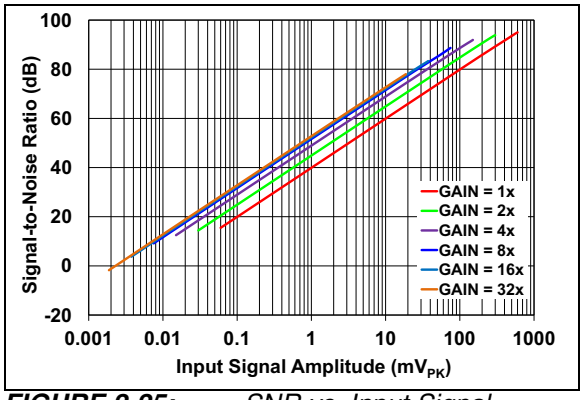


FIGURE 2-25: *SNR vs. Input Signal Amplitude.*

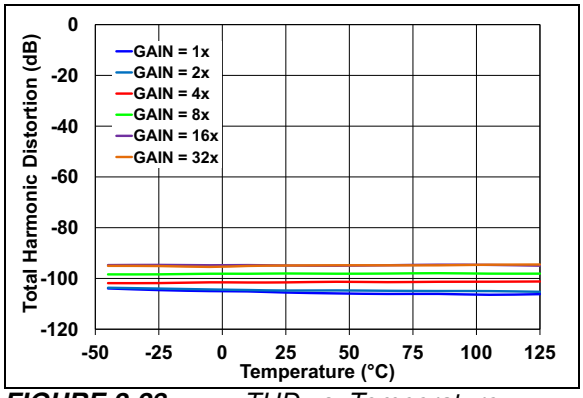


FIGURE 2-28: *THD vs. Temperature.*

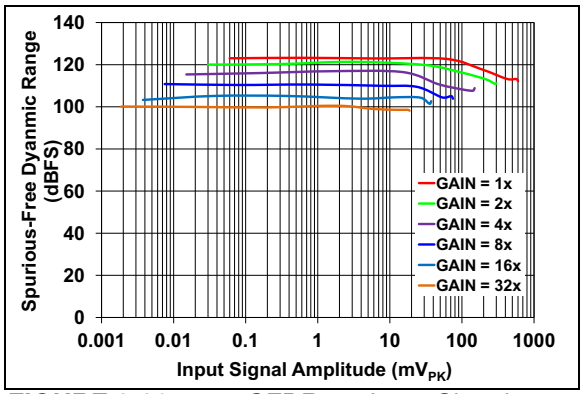


FIGURE 2-26: *SFDR vs. Input Signal Amplitude.*

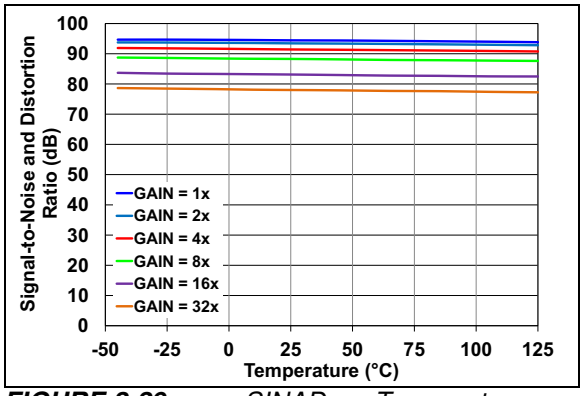


FIGURE 2-29: *SINAD vs. Temperature.*

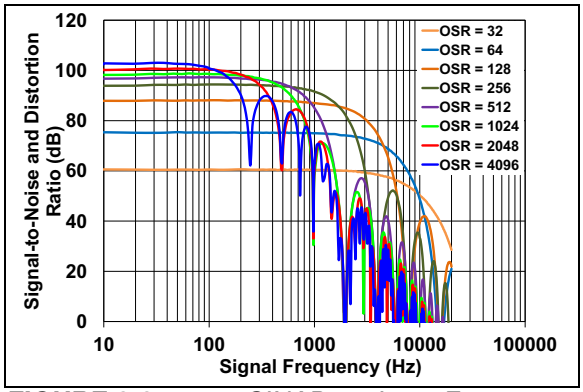


FIGURE 2-27: *SINAD vs. Input Frequency.*

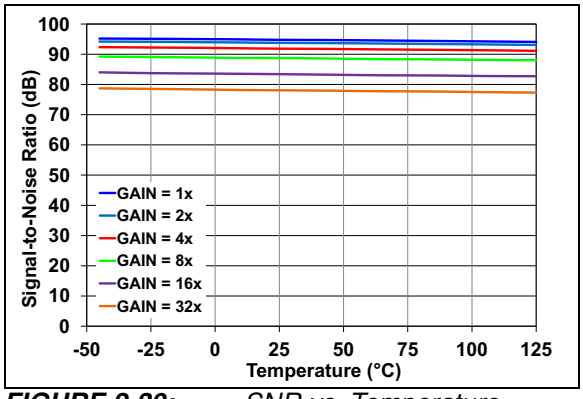


FIGURE 2-30: *SNR vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

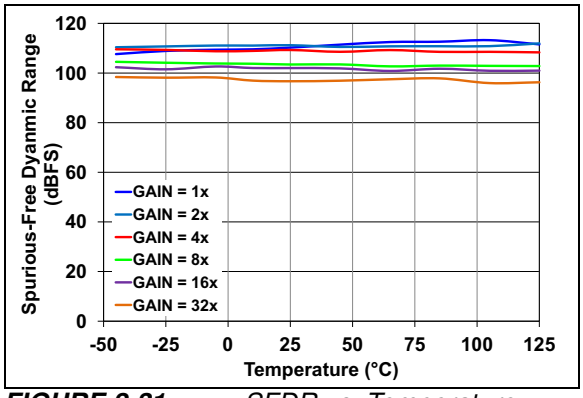


FIGURE 2-31: *SFDR vs. Temperature.*

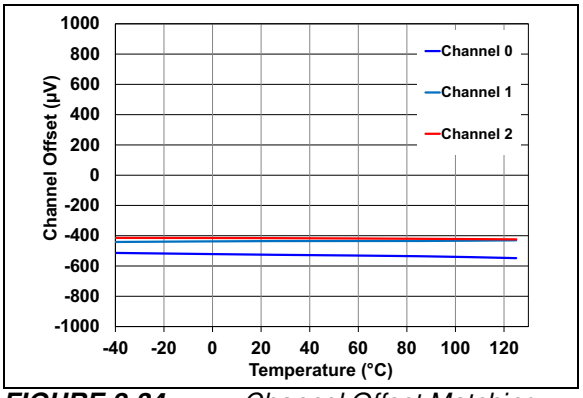


FIGURE 2-34: *Channel Offset Matching vs. Temperature.*

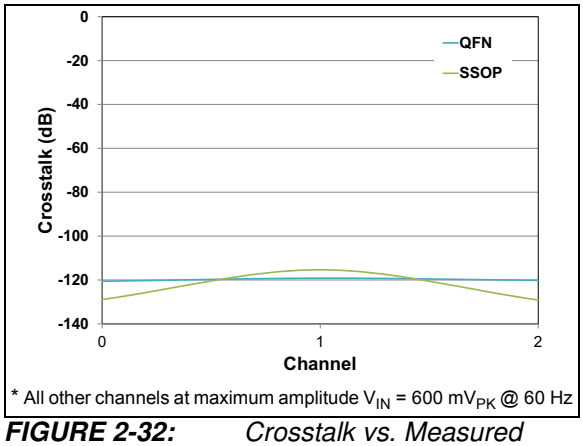


FIGURE 2-32: *Crosstalk vs. Measured Channel.*

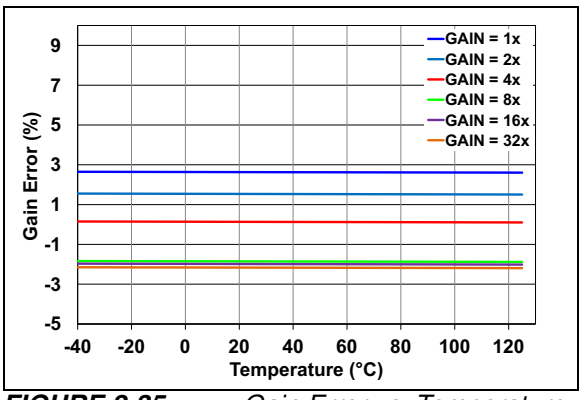


FIGURE 2-35: *Gain Error vs. Temperature vs. Gain.*

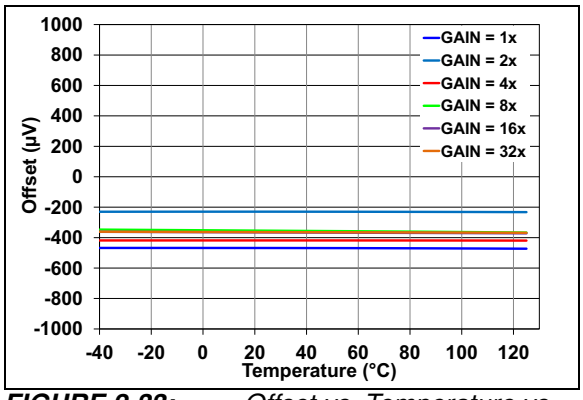


FIGURE 2-33: *Offset vs. Temperature vs. Gain.*

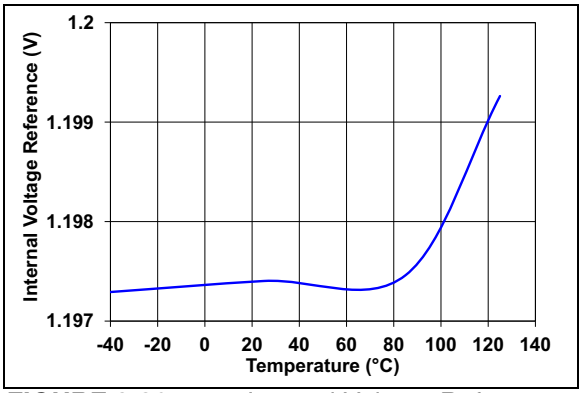


FIGURE 2-36: *Internal Voltage Reference vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

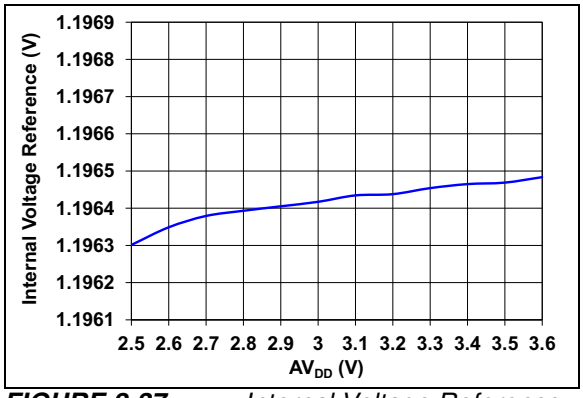


FIGURE 2-37: *Internal Voltage Reference vs. Supply Voltage.*

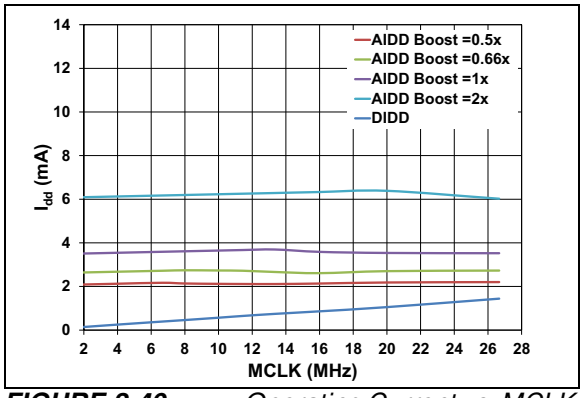


FIGURE 2-40: *Operating Current vs. MCLK Frequency vs. Boost, V_{DD} = 3V.*

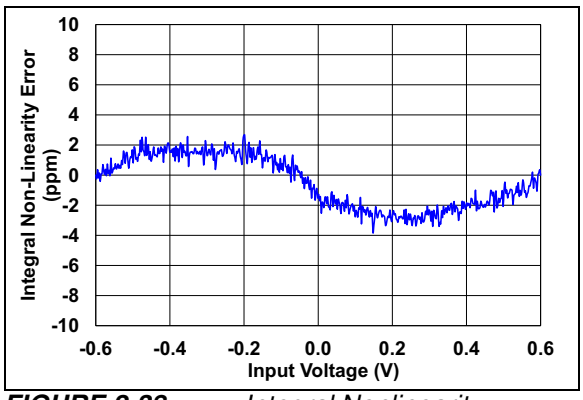


FIGURE 2-38: *Integral Nonlinearity (Dithering Maximum).*

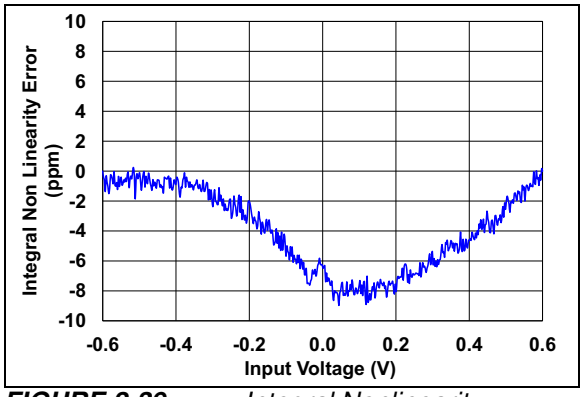


FIGURE 2-39: *Integral Nonlinearity (Dithering Off).*

NOTES:

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: THREE CHANNEL MCP3919 PIN FUNCTION TABLE

MCP3919 SSOP	MCP3919 QFN	Symbol	Function
1	25, 11	AV_{DD}	Analog Power Supply Pin
2	27	CH0+	Noninverting Analog Input Pin for Channel 0
3	28	CH0-	Inverting Analog Input Pin for Channel 0
4	1	CH1-	Inverting Analog Input Pin for Channel 1
5	2	CH1+	Noninverting Analog Input Pin for Channel 1
6	3	CH2+	Noninverting Analog Input Pin for Channel 2
7	4	CH2-	Inverting Analog Input Pin for Channel 2
8, 9, 10, 11, 12, 13, 19	5, 6, 7	NC	No Connect (for better EMI results connect to A_{GND})
14	8	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output Pin
15	9	REFIN-	Inverting Voltage Reference Input Pin
16	10, 26	A_{GND}	Analog Ground Pin, Return Path for Internal Analog Circuitry
17, 20	13, 15, 23	D_{GND}	Digital Ground Pin, Return Path for Internal Digital Circuitry
18	14	$\overline{DR}$/GAIN1	Data Ready Signal Output Pin or GAIN1 Logic Input Pin
21	16	OSC1/CLKI/GAIN0	Oscillator Crystal Connection Pin or External Clock Input Pin or GAIN0 Logic Input Pin
22	17	OSC2/MODE	Oscillator Crystal Connection Pin or Serial Interface Mode Logic Input Pin
23	18	$\overline{CS}$/BOOST	Serial Interface Chip Select Input Pin or BOOST Logic Input Pin
24	19	SCK/MCLK	Serial Interface Clock Input Pin or Master Clock Input Pin
25	20	SDO	Serial Interface Data Output Pin
26	21	SDI/OSR1	Serial Interface Data Input Pin or OSR1 Logic Input Pin
27	22	$\overline{RESET}$/OSR0	Master Reset Logic Input Pin or OSR0 Logic Input Pin
28	12, 24	DV_{DD}	Digital Power Supply Pin
—	29	EP	Exposed Thermal Pad. Must be connected to A_{GND} or floating.

3.1 Analog Power Supply (AV_{DD})

AV_{DD} is the power supply voltage for the analog circuitry within the MCP3919. It is distributed on several pins (pins 11 and 25 in the QFN-28 package, one pin only in the SSOP-28 package). For optimal performance, connect these pins together using a star connection and connect the appropriate bypass capacitors (typically a 10 µF in parallel with a 0.1 µF ceramic). AV_{DD} should be maintained between 2.7V and 3.6V for specified operation.

To ensure proper functionality of the device, at least one of these pins must be properly connected. To ensure optimal performance of the device all the pins must be properly connected. If any of these pins are left floating, the accuracy and noise specifications are not ensured.

3.2 ADC Differential Analog Inputs (CHn+/CHn-)

The CHn+/- pins (n comprised between 0 and 2) are the three fully-differential analog voltage inputs for the delta-sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each CHn+/- input pin is ±1V with no distortion and ±2V with no breaking after continuous voltage. This maximum absolute voltage is not proportional to the V_{REF} voltage.

3.3 Noninverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for all ADCs or the internal voltage reference output.

When VREFEXT = 1, an external voltage reference source can be used and the internal voltage reference is disabled. When using an external differential voltage reference it should be connected to its V_{REF+} pin. When using an external single-ended reference it should be connected to this pin.

When VREFEXT = 0 the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability and thus needs proper buffering and bypass capacitances (a 0.1 µF ceramic capacitor is sufficient in most cases) if used as a voltage source.

If the voltage reference is only used as an internal V_{REF}, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy, but a minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin if left floating.

3.4 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for all ADCs. When using an external differential voltage reference it should be connected to its V_{REF-} pin. When using an external single-ended voltage reference, or when VREFEXT = 0 (default) and using the internal voltage reference, the pin should be directly connected to A_{GND}.

3.5 Analog Ground (A_{GND})

A_{GND} is the ground reference voltage for the analog circuitry within the MCP3919. It is distributed on several pins (pins 10 and 26 in the QFN-28 package, one pin only in the SSOP-28 package). For optimal performance, it is recommended to connect these pins together using a star connection and to connect it to the same ground node voltage as D_{GND}, again preferably with a star connection.

At least one of these pins need to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured. If an analog ground plane is available it is recommended that these pins be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

3.6 Digital Ground (D_{GND})

D_{GND} is the ground reference voltage for the digital circuitry within the MCP3919. It is distributed on several pins (pins 13, 15 and 23 in the QFN package, two pins only in the SSOP-28 package). For optimal performance, connect these pins together using a star connection and connect it to the same ground node voltage as A_{GND}, again preferably with a star connection.

At least one of these pins need to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured. If a digital ground plane is available it is recommended that these pins be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

3.7 Data Ready Output/GAIN1 Logic Input (DR/GAIN1)

The data ready pin indicates if a new conversion result is ready to be read. The default state of this pin is logic high when DR_HIZ = 1 and is high-impedance when DR_HIZ = 0 (default). After each conversion is finished, a logic low pulse will take place on the data ready pin to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The data ready pin is independent of the SPI interface and acts like an interrupt output. The data ready pin state is not latched, and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate, and internal clock prescale settings. The data ready pulse width is equal to half a DMCLK period and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

In the 2-Wire Interface mode, this is the GAIN1 logic select input pin (See **Section 7.0 "2-Wire Serial Interface Description"** for the logic input table for GAIN0 and GAIN1). The pin state is latched when the MODE changes to 2-Wire Interface mode and is relatched at each watchdog timer reset.

Note:	This pin should not be left floating when the DR_HIZ bit is low; a 100 kΩ pull-up resistor connected to DV_{DD} is recommended.

3.8 Crystal Oscillator/Master Clock Input/GAIN0 Logic Input Pin (OSC1/CLKI/GAIN0)

OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = 0, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation.

The typical clock frequency specified is 4 MHz. For proper operation, and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 for the function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2. Appropriate load capacitance should be connected to these pins for proper operation.

In 2-Wire Interface mode, this is the GAIN1 logic select input pin (See **Section 7.0 "2-Wire Serial Interface Description"** for the logic input table for GAIN0 and GAIN1). The pin state is latched when the MODE changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

Note:	When CLKEXT = 1, the crystal oscillator is disabled. OSC1 becomes the master clock input CLKI, a direct path for an external clock source. One example would be a clock source generated by an MCU.

3.9 Crystal Oscillator Output/Interface MODE Logic Input (OSC2/MODE)

When CLKEXT = 0, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation. Appropriate load capacitance should be connected to these pins for proper operation.

When CLKEXT = 1 (default condition at POR), this pin is the MODE selection pin for the digital interface. When MODE is logic low, the SPI interface is selected (see **Section 6.0 "SPI Serial Interface Description"**); when MODE is logic high, the 2-Wire interface (see **Section 7.0 "2-Wire Serial Interface Description"**) is selected. The MODE input is latched after a POR, a Master Reset and/or a watchdog timer reset.

3.10 Chip Select/Boost Logic Input (CS/BOOST)

This pin is the Serial Peripheral Interface (SPI) chip select that enables serial communication. When this pin is logic high, no communication can take place. A chip select falling edge initiates serial communication, and a chip select rising edge terminates the communication. No communication can take place even when CS is logic low, if RESET is also logic low.

This input is Schmitt-triggered.

In 2-Wire Interface mode, this is the BOOST logic select input pin (see **Section 7.0 "2-Wire Serial Interface Description"** for the logic input table for BOOST).

The pin state is latched when the MODE changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

3.11 Serial Data Clock/Master Clock Input (SCK/MCLK)

This is the serial clock pin for SPI communication. Data is clocked into the device on the rising edge of SCK. Data is clocked out of the device on the falling edge of SCK.

The MCP3919 SPI interface is compatible with SPI 0,0 and 1,1 modes. SPI modes can be changed during a $\overline{CS}$ high time.

The maximum clock speed specified is 20 MHz. SCK and MCLK are two different and asynchronous clocks; SCK is only required when a communication happens, while MCLK is continuously required when the part is converting analog inputs.

This input is Schmitt-triggered.

In the 2-Wire Interface mode, this pin defines the master clock of the device (MCLK) and simultaneously the serial clock (SCK) for the interface. In this mode, the clock has to be provided continuously to ensure proper operation. See **Section 7.0 "2-Wire Serial Interface Description"** for more information and timing diagrams of the 2-wire interface protocol.

3.12 Serial Data Output (SDO)

This is the SPI data output pin. Data is clocked out of the device on the falling edge of SCK.

This pin remains in a high-impedance state during the command byte. It also stays high-impedance during the entire communication for write commands and when the $\overline{CS}$ pin is logic high, or when the $\overline{RESET}$ pin is logic low. This pin is active only when a read command is processed. The interface is half-duplex (inputs and outputs do not happen at the same time).

3.13 Serial Data/OSR1 Logic Input (SDI/OSR1)

This is the SPI data input pin. Data is clocked into the device on the rising edge of SCK. When $\overline{CS}$ is logic low, this pin is used to communicate with a series of 8-bit commands. The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge followed by an 8-bit command word, entered through the SDI pin. Each command is either a Read or a Write command. Toggling SDI after a Read or Write command or when $\overline{CS}$ is logic high has no effect.

This input is Schmitt-triggered.

In 2-Wire Interface mode, this is the OSR1 logic select input pin (see **Section 7.0 "2-Wire Serial Interface Description"** for the logic input table for OSR0 and OSR1). The pin state is latched when the MODE changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

3.14 Master Reset/OSR0 Logic Input (RESET/OSR0)

In SPI mode, this pin is active low and places the entire chip in a Reset state when active.

When $\overline{RESET}$ is logic low, all registers are reset to their default value, no communication can take place and no clock is distributed inside the part, except in the input structure if MCLK is applied (if MCLK is idle, then no clock is distributed). This state is equivalent to a Power-On Reset (POR) state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{RESET}$ is logic low is equivalent to when $\overline{RESET}$ is logic high. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no clock running.

All the analog biases are enabled during a Reset, so that the part is fully operational just after a $\overline{RESET}$ rising edge, if MCLK is applied when $\overline{RESET}$ is logic low. If MCLK is not applied, there is a time after a hard reset when the conversion may not accurately correspond to the startup of the input structure.

This input is Schmitt-triggered.

In 2-Wire Interface mode, this is the OSR0 logic select pin (see **Section 7.0 "2-Wire Serial Interface Description"** for the logic input table for OSR0 and OSR1). The pin state is latched when the mode changes to 2-Wire Interface mode, and is relatched at each watchdog timer reset.

3.15 Digital Power Supply (DV_{DD})

DV_{DD} is the power supply voltage for the digital circuitry within the MCP3919. It is distributed on several pins (pins 12 and 24 in the QFN package, one pin only in the SSOP-28 package). For optimal performance, it is recommended to connect these pins together using a star connection and to connect appropriate bypass capacitors (typically a 10 µF in parallel with a 0.1 µF ceramic). DV_{DD} should be maintained between 2.7V and 3.6V for specified operation.

At least one of these pins need to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured.

3.16 Exposed Thermal Pad

This pin must be connected to A_{GND} or left floating for proper operation. Connecting it to A_{GND} is preferable for lowest noise performance and best thermal behavior.

4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

- **MCLK – Master Clock**
- **AMCLK – Analog Master Clock**
- **DMCLK – Digital Master Clock**
- **DRCLK – Data Rate Clock**
- **OSR – Oversampling Ratio**
- **Offset Error**
- **Gain Error**
- **Integral Nonlinearity Error**
- **Signal-to-Noise Ratio (SNR)**
- **Signal-To-Noise Ratio And Distortion (SINAD)**
- **Total Harmonic Distortion (THD)**
- **Spurious-Free Dynamic Range (SFDR)**
- **MCP3919 Delta-Sigma Architecture**
- **Idle Tones**
- **Dithering**
- **Crosstalk**
- **PSRR**
- **CMRR**
- **ADC Reset Mode**
- **Hard Reset Mode (RESET = 0)**
- **ADC Shutdown Mode**
- **Full Shutdown Mode**
- **Measurement Error**

4.1 MCLK – Master Clock

This is the fastest clock present on the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1. See Figure 4-1.

4.2 AMCLK – Analog Master Clock

AMCLK is the clock frequency that is present on the analog portion of the device after prescaling has occurred via the CONFIG0 PRE<1:0> register bits (see Equation 4-1). The analog portion includes the PGAs and the delta-sigma modulators.

EQUATION 4-1:

$$AMCLK = \frac{MCLK}{PRESCALE}$$

TABLE 4-1: MCP3919 OVERSAMPLING RATIO SETTINGS

CONFIG0 PRE<1:0>		Analog Master Clock Prescale
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8

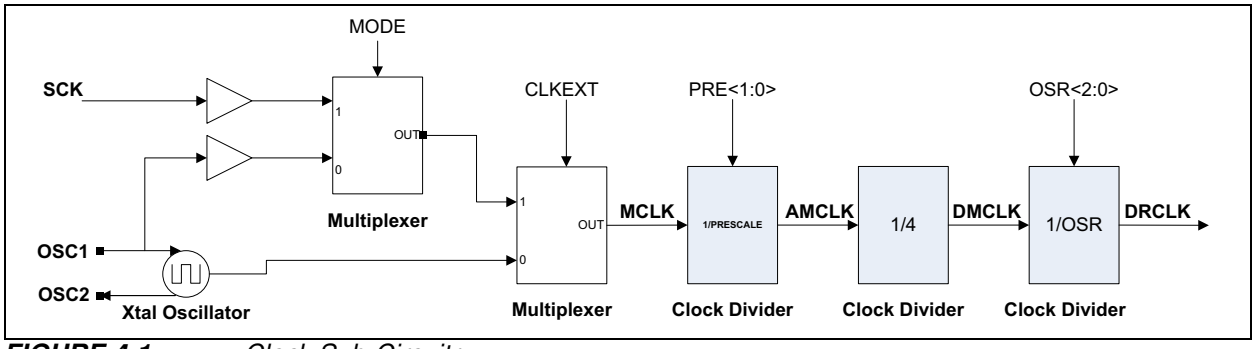


FIGURE 4-1: *Clock Sub-Circuitry.*

4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device after prescaling and division by four (Equation 4-2). This is also the sampling frequency, which is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output. See Figure 4-1.

EQUATION 4-2:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

4.4 DRCLK – Data Rate Clock

This is the output data rate, i.e., the rate at which the ADCs output new data. Each new data is signaled by a data ready pulse on the $\overline{DR}$ pin.

This data rate is depending on the OSR and the prescaler with the formula in Equation 4-3.

EQUATION 4-3:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate, and because the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

Table 4-2 describes the various combinations of OSR and PRESCALE, and their associated AMCLK, DMCLK and DRCLK rates.

TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE, MCLK = 4 MHZ

PRE<1:0>		OSR<2:0>			OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)	SINAD (dB) Note 1	ENOB from SINAD (bits) Note 1
1	1	1	1	1	4096	MCLK/8	MCLK/32	MCLK/131072	.035	102.5	16.7
1	1	1	1	1	2048	MCLK/8	MCLK/32	MCLK/65536	.061	100	16.3
1	1	1	1	1	1024	MCLK/8	MCLK/32	MCLK/32768	.122	97	15.8
1	1	1	1	1	512	MCLK/8	MCLK/32	MCLK/16384	.244	96	15.6
1	1	0	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.488	94	15.3
1	1	0	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976	90	14.7
1	1	0	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95	83	13.5
1	1	0	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9	70	11.3
1	0	1	1	1	4096	MCLK/4	MCLK/16	MCLK/65536	.061	102.5	16.7
1	0	1	1	1	2048	MCLK/4	MCLK/16	MCLK/32768	.122	100	16.3
1	0	1	1	1	1024	MCLK/4	MCLK/16	MCLK/16384	.244	97	15.8
1	0	1	1	1	512	MCLK/4	MCLK/16	MCLK/8192	.488	96	15.6
1	0	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976	94	15.3
1	0	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95	90	14.7
1	0	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9	83	13.5
1	0	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125	70	11.3
0	1	1	1	1	4096	MCLK/2	MCLK/8	MCLK/32768	.122	102.5	16.7
0	1	1	1	1	2048	MCLK/2	MCLK/8	MCLK/16384	.244	100	16.3
0	1	1	1	1	1024	MCLK/2	MCLK/8	MCLK/8192	.488	97	15.8
0	1	1	1	1	512	MCLK/2	MCLK/8	MCLK/4096	.976	96	15.6
0	1	0	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95	94	15.3
0	1	0	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9	90	14.7
0	1	0	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125	83	13.5
0	1	0	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625	70	11.3
0	0	1	1	1	4096	MCLK	MCLK/4	MCLK/16384	.244	102.5	16.7
0	0	1	1	0	2048	MCLK	MCLK/4	MCLK/8192	.488	100	16.3
0	0	1	0	1	1024	MCLK	MCLK/4	MCLK/4096	.976	97	15.8
0	0	1	0	0	512	MCLK	MCLK/4	MCLK/2048	1.95	96	15.6
0	0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9	94	15.3
0	0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125	90	14.7
0	0	0	0	1	64	MCLK	MCLK/4	MCLK/256	15.625	83	13.5
0	0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25	70	11.3

Note 1: For OSR = 32 and 64, DITHER = None. For OSR = 128 and higher, DITHER = Maximum. The SINAD values are given from GAIN = 1.

4.5 OSR – Oversampling Ratio

This is the ratio of the sampling frequency to the output data rate; OSR = DMCLK/DRCLK. The default OSR<2:0> is 256, or with MCLK = 4 MHz, PRESCALE = 1, AMCLK = 4 MHz, f_S = 1 MHz and f_D = 3.90625 ksps. The OSR<2:0> bits in Table 4-3 in the CONFIG0 register are used to change the oversampling ratio (OSR).

TABLE 4-3: MCP3919 OVERSAMPLING RATIO SETTINGS

OSR<2:0>			Oversampling Ratio OSR
0	0	0	32
0	0	1	64
0	1	0	128
0	1	1	256 (Default)
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip-to-chip. The offset is specified in µV. The offset error can be digitally compensated independently on each channel through the OFFCAL_CHn registers with a 24-bit calibration word.

The offset on the MCP3919 has a low-temperature coefficient.

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in % compared to the ideal transfer function defined in Equation 5-3. The specification incorporates both PGA and ADC gain error contributions but not the V_{REF} contribution (it is measured with an external V_{REF}).

This error varies with PGA and OSR settings. The gain error can be digitally compensated independently on each channel through the GAINCAL_CHn registers with a 24-bit calibration word.

The gain error on the MCP3919 has a low temperature coefficient.

4.8 Integral Nonlinearity Error

Integral nonlinearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

4.9 Signal-to-Noise Ratio (SNR)

For the MCP3919 ADCs, the signal-to-noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal) when the input is a sine wave at a predetermined frequency (see Equation 4-4). It is measured in dB. Usually, only the maximum signal-to-noise ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

EQUATION 4-4: SIGNAL-TO-NOISE RATIO

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

4.10 Signal-To-Noise Ratio And Distortion (SINAD)

The most important Figure of Merit for analog performance of the ADCs present on the MCP3919 is the Signal-to-Noise And Distortion (SINAD) specification.

The Signal-to-Noise And Distortion ratio is similar to signal-to-noise ratio, with the exception that you must include the harmonic's power in the noise power calculation (see Equation 4-5). The SINAD specification depends mainly on the OSR and DITHER settings.

EQUATION 4-5: SINAD EQUATION

$$SINAD(dB) = 10log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD, see Equation 4-6.

EQUATION 4-6: SINAD, THD AND SNR RELATIONSHIP

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$