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MCP39F501

Single-Phase, Power-Monitoring IC with Calculation and Event Detection

Features:

- Power Monitoring Accuracy capable of 0.1% error across 4000:1 dynamic range
- Fast Calibration Routines
- Programmable Event Notifications such as over-current and voltage sag, surge protection
- 512 bytes User-accessible EEPROM through page read/write commands
- Non-volatile On-chip Memory, no external memory required
- Built-in calculations on fast 16-bit processing core
  - Active, Reactive and Apparent Power
  - True RMS Current, RMS Voltage
  - Line Frequency, Power Factor
- Two-Wire Serial Protocol using a 2-wire Universal Asynchronous Receiver/Transmitter (UART) interface supporting multiple devices on a single bus
- Low-Drift Internal Voltage Reference, 10 ppm/°C typical
- 28-lead 5x5 QFN package
- Extended Temperature Range -40°C to +125°C

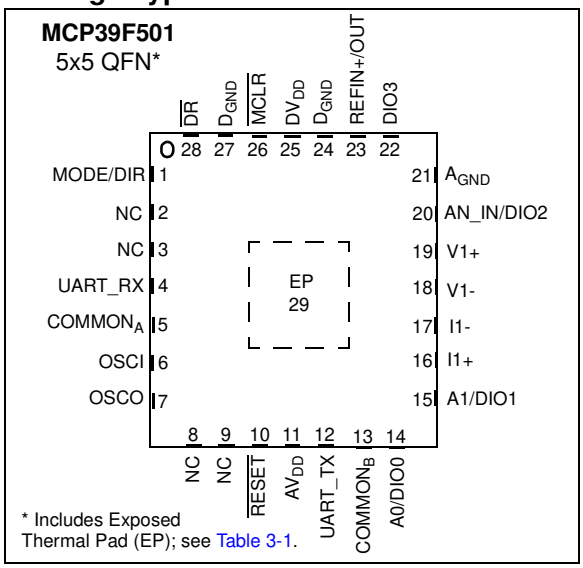
Applications:

- Real-time Measurement of Input Power for AC/DC supplies
- Intelligent Power Distribution Units

Description:

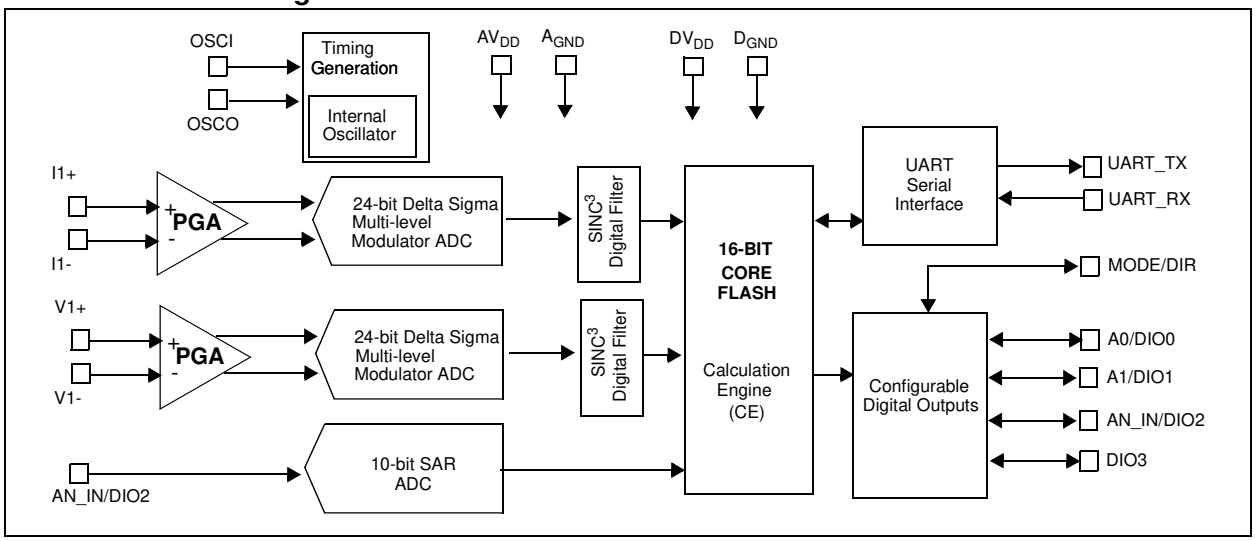
The MCP39F501 is a highly integrated, single-phase power-monitoring IC designed for real-time measurement of input power for AC/DC power supplies, power distribution units and industrial applications. It includes dual-channel delta sigma ADCs, a 16-bit calculation engine, EEPROM and a flexible 2-wire interface. An integrated low-drift voltage reference with 10 ppm/°C in addition to 94.5 dB of SINAD performance on each measurement channel allows for better than 0.1% accurate designs across a 4000:1 dynamic range.

Package Type



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



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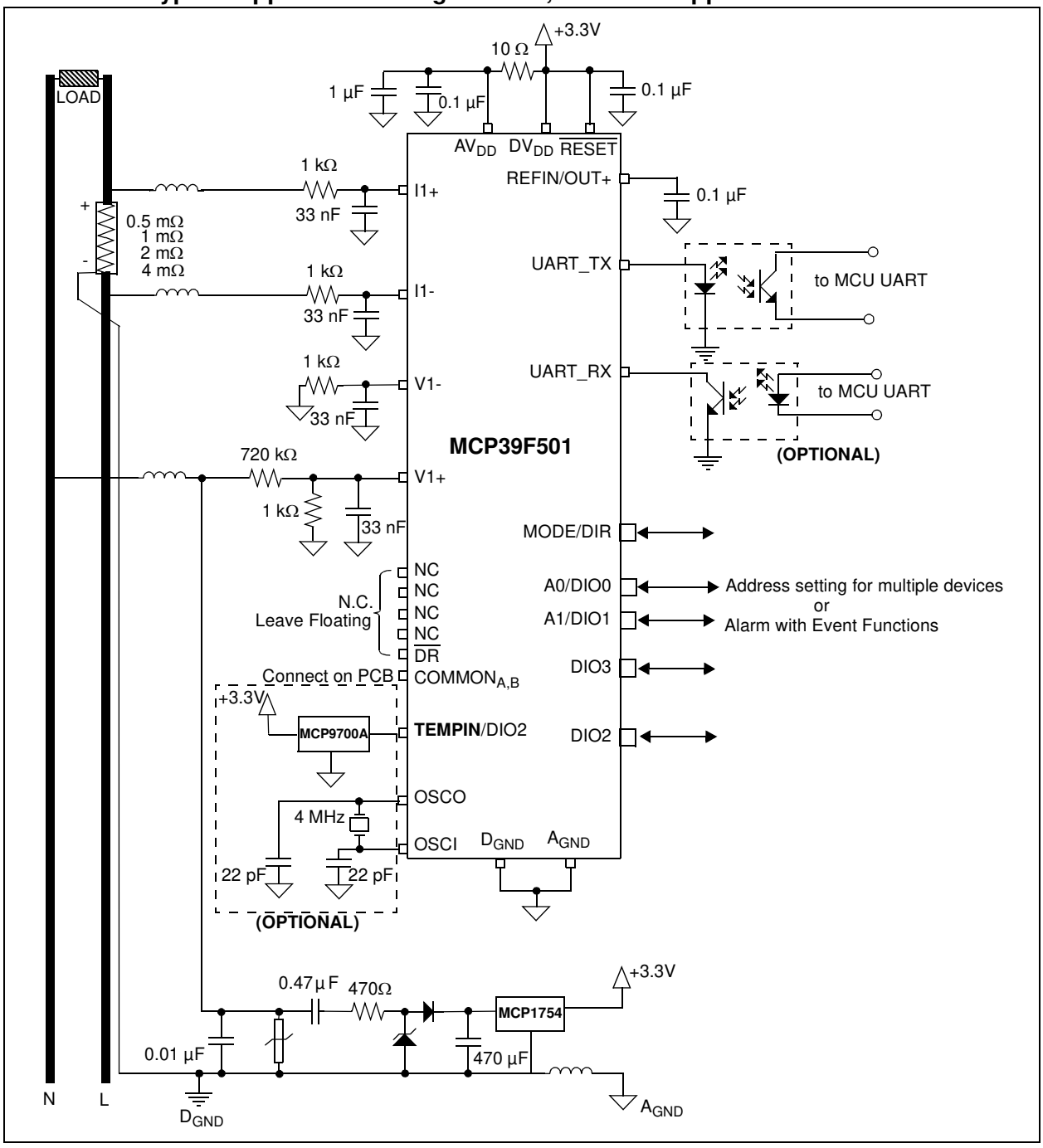
MCP39F501 Typical Application – Single Phase, Two-Wire Application Schematic



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} .....-0.3 to 4.5V
AV_{DD} .....-0.3 to 4.0V
Digital inputs and outputs w.r.t. A_{GND}..... -0.3V to 4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} ....-2V to +2V
V_{REF} input w.r.t. A_{GND} .....-0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin.....300 mA
Maximum Current into DV_{DD} pin.....250 mA
Maximum Output Current Sunk by Digital IO.....25 mA
Maximum Current Sourced by Digital IO.....25 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) .....4.0 kV, 200V
ESD on all other pins (HBM,MM) .....4.0 kV, 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Power Measurement						
Active Power **(Note 2)**	P	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Reactive Power **(Note 2)**	Q	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Apparent Power **(Note 2)**	S	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Current RMS **(Note 2)**	I_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Voltage RMS **(Note 2)**	V_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Voltage Channel **(Note 1)**
Power Factor **(Note 2)**	Φ	—	±0.1	—	%	
Line Frequency **(Note 2)**	V_{RMS}	—	±0.1	—	%	
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x ($1/f_{LINE}$)	—	ms	**Note 7**
Minimum Calculation and Event Detection Time	t_{CALC_EVENT}	2^N x ($1/f_{LINE}$)	—	—	ms	
Minimum Time for Voltage Sag Detection	t_{AC_DROP}	—	see **Section 7.7**	—	ms	**Note 4**

Note 1: Specification by design and characterization; not production tested.
2: Calculated from reading the register values.
3: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.
4: Applies to Voltage Sag and Voltage Surge Events Only.
5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.
6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.
7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
24-Bit Delta Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (V1+ – V1-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	**Note 6**
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	**Note 3**
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	**Note 3**
Signal-to-Noise Ratio	SNR	92	95	—	dB	**Note 3**
Spurious Free Dynamic Range	SFDR	—	111	—	dB	**Note 3**
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + 0.6V_{PP}, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.0 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V
10-Bit SAR ADC Performance for Temperature Measurement						
Resolution	N_R	—	10	—	bits	
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	D_{GND} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Non-Linearity	I_{NL}	—	±1	±2	LSb	

Note 1: Specification by design and characterization; not production tested.

2: Calculated from reading the register values.

3: V_{IN} = 1V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

4: Applies to Voltage Sag and Voltage Surge Events Only.

5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Differential Non-Linearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Temperature Measurement Rate		—	$f_{LINE}/2^N$	—	sps	**Note 7**
Clock and Timings						
UART Baud Rate	UDB	—	4.8	—	kbps	See **Section 3.2** for protocol details
Master Clock and Crystal Frequency	f_{MCLK}	-2%	4	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40 to +85°C only (**Note 5**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	
Temperature Coefficient	TCV_{REF}	—	10	—	ppm/°C	T_A = -40°C to +85°C, VREFEXT = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	
Current, V_{REF}	$AI_{DD}V_{REF}$	—	40	—	µA	
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.1V	V	
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	
DV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0 – 3.3V in 0.1s, 0 – 2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power On Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms

Note 1: Specification by design and characterization; not production tested.

2: Calculated from reading the register values.

3: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

4: Applies to Voltage Sag and Voltage Surge Events Only.

5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Operating Current	I_{DD}	—	13	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	Years	Provided no other specifications are violated
Supply Current during Programming	I_{DDPD}	—	7	—	mA	

Note 1: Specification by design and characterization; not production tested.

2: Calculated from reading the register values.

3: V_{IN} = 1V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

4: Applies to Voltage Sag and Voltage Surge Events Only.

5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	V_{SS}	—	0.2 V_{SSD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
		—	0.050	0.100	µA	DIO pins only

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	35.3	—	°C/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

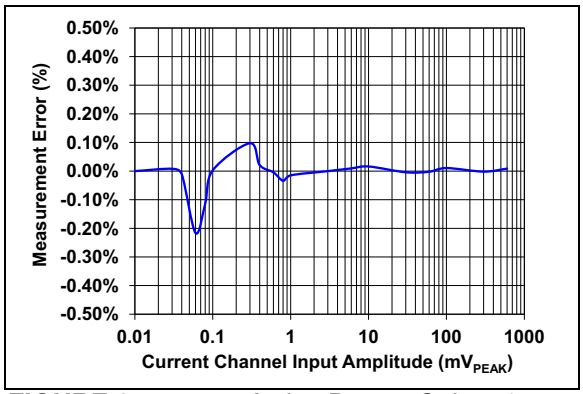

FIGURE 2-1: *Active Power, Gain = 1.*

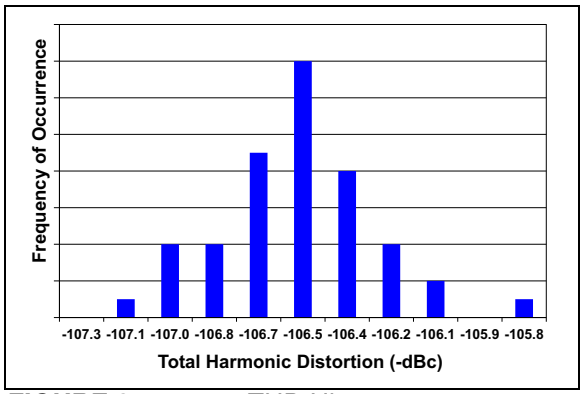

FIGURE 2-4: *THD Histogram.*

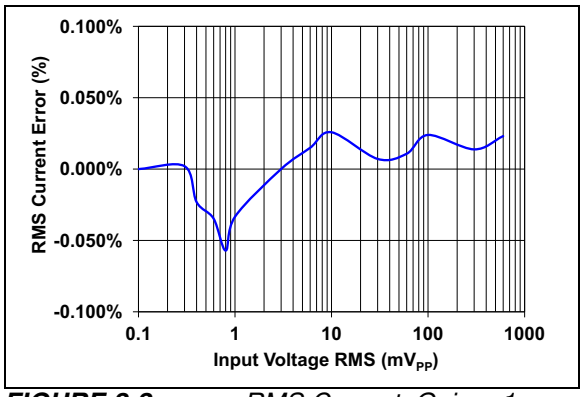

FIGURE 2-2: *RMS Current, Gain = 1.*

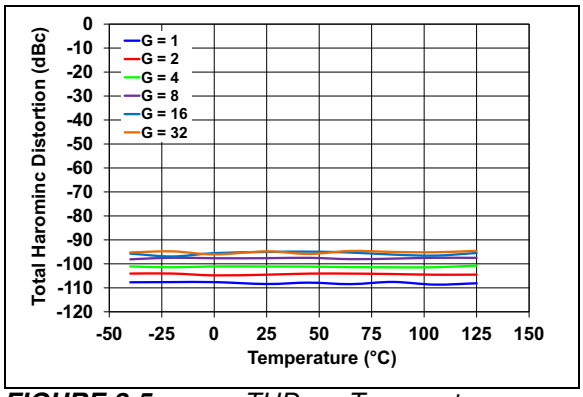

FIGURE 2-5: *THD vs. Temperature.*

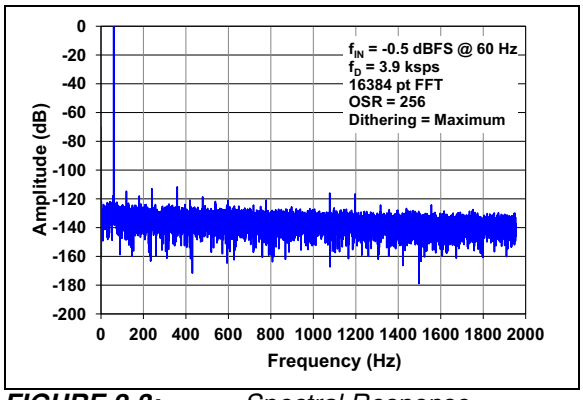

FIGURE 2-3: *Spectral Response.*

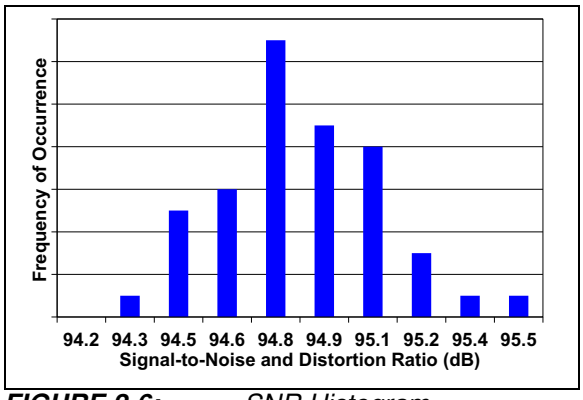

FIGURE 2-6: *SNR Histogram.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

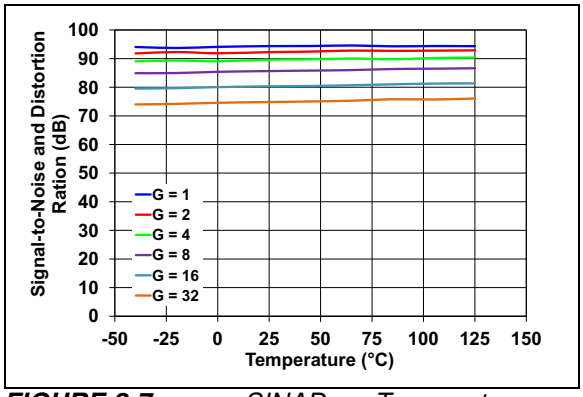

FIGURE 2-7: *SINAD vs. Temperature.*

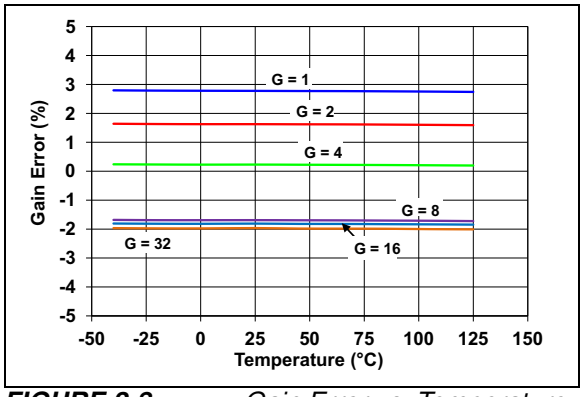

FIGURE 2-8: *Gain Error vs. Temperature.*

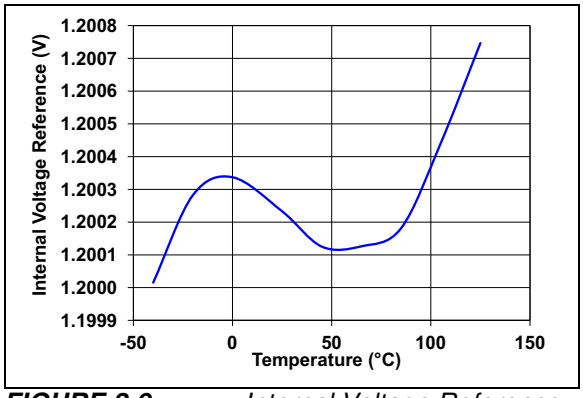

FIGURE 2-9: *Internal Voltage Reference vs. Temperature.*

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3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F501 5x5 QFN	Symbol	Function
1	MODE/DIR	Single or Multiple Device mode with direction control for RS-485 drivers
2	NC	No Connect (must be left floating)
3	NC	No Connect (must be left floating)
4	UART_RX	UART Communication RX Pin
5	$COMMON_A$	Common pin A, to be connected to $COMMON_B$
6	OSCI	Oscillator Crystal Connection Pin or External Clock Input Pin
7	OSCO	Oscillator Crystal Connection Pin
8	NC	No Connect (must be left floating)
9	NC	No Connect (must be left floating)
10	$\overline{RESET}$	Reset Pin for Delta Sigma ADCs
11	AV_{DD}	Analog Power Supply Pin
12	UART_TX	UART Communication TX Pin
13	$COMMON_B$	Common pin B, to be connected to $COMMON_A$
14	A0/DIO0	Address Select Pin 0 / Configurable digital I/O 0
15	A1/DIO1	Address Select Pin 1 / Configurable digital I/O 1
16	I1+	Non-Inverting Current Channel Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel Input for 24-bit ΔΣ ADC
18	V1-	Inverting Voltage Channel Input for 24-bit ΔΣ ADC
19	V1+	Non-Inverting Voltage Channel Input for 24-bit ΔΣ ADC
20	AN_IN/DIO2	Analog Input for SAR ADC / Configurable Digital Input/Output 2 Pin
21	A_{GND}	Analog Ground Pin, Return Path for internal analog circuitry
22	DIO3	Configurable Digital Input/Output 3
23	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output Pin
24	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
25	DV_{DD}	Power Supply Pin
26	$\overline{MCLR}$	Master Clear for Device
27	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to D_{GND})

3.1 Single/Multiple Device Mode and Direction Pin (MODE/DIR)

When using multiple devices on a single bus, this pin should be tied to the DIR pin of the transceiver for direction control. This will cause the A0/DIO0 and A1/DIO1 pins to act as address pins A0,A1. If additional devices are required, the Device Address register can be programmed to allow for more than four devices. For this operation, a 4.7 kΩ pull-down resistor should be connected to this pin.

If only a single device is being used, the MODE pin should be driven high at power-on reset (POR), making the A0/DIO0 and A1/DIO1 pins additional configurable digital I/O (DIO).

3.2 UART Communication Pins (UART_TX, UART_RX)

The MCP39F501 device contains an asynchronous full-duplex UART. The UART communication is 8 bits with Start and Stop bit. See **Section 4.2 "UART Settings"** for more information.

3.3 Common Pins (COMMON A and B)

The $COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F501. These two pins should be connected together in the application.

3.4 Data Ready Pin ($\overline{DR}$)

The data ready pin indicates if a new delta-sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the Data Ready pin to indicate the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with line frequency and has a predefined and constant width.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.5 Oscillator Pins (OSCO/OSCI)

OSCO and OSCI provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 4 MHz crystal can be connected to these pins. If a crystal of external clock source is not detected, the device will clock from the internal 4 MHz oscillator.

3.6 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the delta-sigma ADCs, PGA, internal V_{REF} and other blocks associated with the analog front-end in a reset state when pulled low. This input is Schmitt-triggered.

3.7 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F501.

This pin requires appropriate bypass capacitors and should be maintained to 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.8 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F501. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.9 Configurable Digital Input/Output Pins (DIOn)

These digital I/O pins can be configured to act as input or as output events, such as alarm events or interrupt flags, based on the device configuration. For more information, see **Section 8.0 "Configurable Digital I/O Pins (DIO Configuration – 0x0046)"**.

3.10 24-Bit Delta Sigma ADC Differential Current Channel Input Pins (I1+/I1-)

I1- and I1+ are the two fully-differential current channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.11 24-Bit Delta Sigma ADC Differential Voltage Channel Inputs (V1+/V1-)

V1- and V1+ are the two fully-differential voltage channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each V_N+/- input pin is ±1V with no distortion and ±6V, with no breaking after continuous voltage.

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3.12 Analog Input for Temperature Measurement/Configurable Digital Output 2 Pin (AN_IN/DIO2)

This is the input to the analog-to-digital converter to be used for temperature measurement. If temperature sensing is required in the application, it is advised to connect the low-power active thermistor IC™ MCP9700A to this pin.

3.13 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground pin is available on the PCB, it is recommended that this pin be tied to that plane.

3.14 Non-inverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for the delta sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.15 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.16 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to D_{GND}.

NOTES:

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4.0 COMMUNICATION PROTOCOL

The communication protocol for the MCP39F501 device is based on the Simple Sensor Interface (SSI) protocol. This protocol is used for point-to-point communication from a single-host MCU to a single-slave MCP39F501. The protocol supports the ability for multiple devices to be on a single bus, but it is only designed to communicate to one device at a time.

All communication to the device occurs in frames. Each frame consists of a header byte, the number of bytes in the frame, command packet (or command packets) and a checksum.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

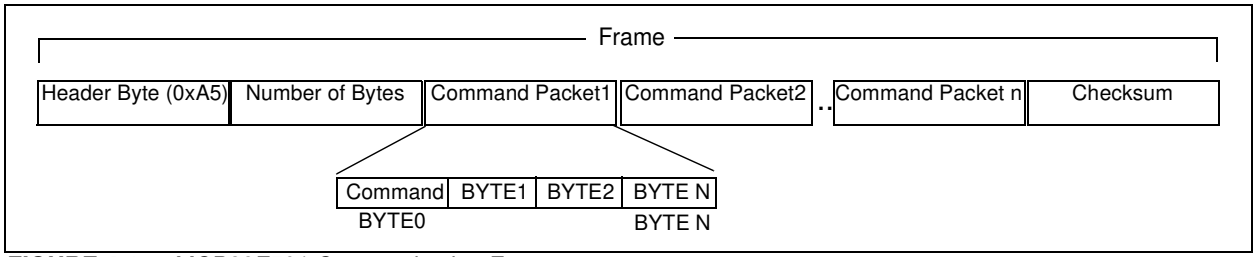

FIGURE 4-1: *MCP39F501 Communication Frame.*

This approach allows for single, secure transmission from the host processor to the MCP39F501 with either a single command, or multiple commands. No command in a frame is processed until the frame is complete and the checksum and number of bytes are validated.

The number of bytes in an individual *command packet* depends on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

This protocol can also be used to set up transmission from the MCP39F501 on specific registers. A predetermined single-wire transmission frame is defined for one wire interfaces. The Auto-transmit mode can be initiated by setting the SINGLE_WIRE bit in the System Configuration register, allowing for single-wire communication within the application. See **Section 4.9 "Single-Wire Transmission Mode"** for more information on this communication.

4.1 Checksum

The checksum is generated using simple byte addition and taking modulus to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F501 will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F501, the frame and checksum are created in the same way, with the header byte becoming an acknowledge (0x06). Communication examples are given in **Section 4.6 "Example Communication Frames and MCP39F501 Responses"**.

4.2 UART Settings

The default baud rate is 4.8 kbps. The UART operates in 8-bit mode, plus one start bit and one stop bit, for a total of 10 bits per byte, as shown in Figure 4-1.

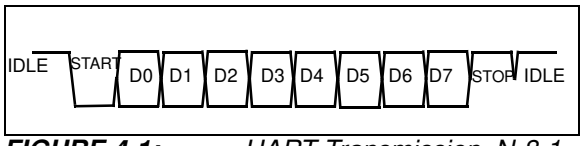

FIGURE 4-1: *UART Transmission, N-8-1.*

The baud rate is fixed at 4.8 kbps.

4.3 Multiple Devices

In order to support multiple devices on a single bus, a device must be selected before any communication occurs between the host MCU and the individual MCP39F501 devices using the `Select Device` command. Once selected, the device will assert the DIR pin until it is deselected.

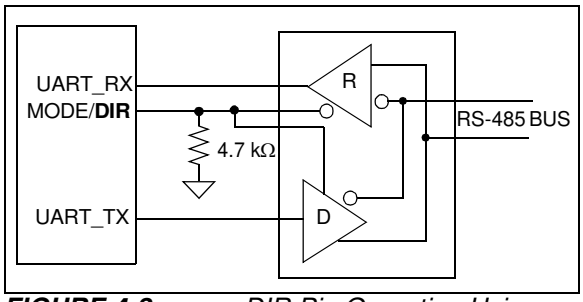

FIGURE 4-2: *DIR Pin Operation Using Example RS-485 Bus Transceiver.*

Based on this operation, the sequence of events when communicating to an MCP39F501 on a bus with multiple devices must be as follows:

1. Select the device.
2. Communicate to selected device through a communication frame.
3. Repeat **Step 2**, if necessary.
4. De-select the device.

4.4 Device Address

A device is selected by issuing the `Select Device` command, followed by the appropriate Device Address. The device address is set through the A0, A1 pins and also through the writing of the Device Address register (Location 0x0026), as shown in Figure 4-3.

A7	A6	A5	A4	A3	A2	A1	A0
Set through Register Write						A1, A0 pins	

FIGURE 4-3: *Device Address Register.*

The default address and default register value is **0x4C.** If the device is in Multiple Device mode (MODE/DIR = `0` at POR), pins A1 and A0 will override bits 0 and 1 and initial possible addresses include 0x4C, 0x4D, 0x4E and 0x4F depending on the state of these pins.

4.5 Command List

The following table is a list of all accepted command bytes for the MCP39F501.

TABLE 4-1: MCP39F501 INSTRUCTION SET

Command	Command ID	Instruction Parameter	Number of Bytes in Command Packet	Successful Response UART_TX
`Register Read, 16 bits`	0x52	---------	1	ACK, Data, CRC
`Register Read, 32 bits`	0x44	---------	1	ACK, Data, CRC
`Register Write, 16 bits`	0x57	Data	3	ACK
`Register Write, 32 bits`	0x45	Data	5	ACK
`Register Read, N bits`	0x4E	Number of Bytes	2	ACK, Data, CRC
`Register Write, N bits`	0x4D	Number of Bytes	1+N	ACK
`Select Device`	0x4C	Device Address	2	ACK
`De-Select Device`	0x4B	Device Address	2	ACK
`Set Address Pointer`	0x41	ADDRESS	3	ACK
`Save Registers To Flash`	0x53	Device Address	2	ACK
`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, CRC
`Page Write EEPROM`	0x50	PAGE	18	ACK
`Bulk Erase EEPROM`	0x4F	Device Address	2	ACK
`Auto-Calibration Gain`	0x5A	Device Address	**Note 1**	
`Auto-Calibration Reactive Gain`	0x7A	Device Address	**Note 1**	
`Auto-Calibration Frequency`	0x76	Device Address	**Note 1**	

Note 1: See **Section 9.0, MCP39F501 Calibration** for more information on calibration.

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4.6 Example Communication Frames and MCP39F501 Responses

TABLE 4-2: FRAME EXAMPLE, SELECT DEVICE COMMAND

Transmit Frame		Response from MCP39F501	
0xA5	Header Byte	0x06	Acknowledge
0x05	Number of Bytes		
0x4C	Command (Select Device)		
0x4D	Device Address		
0x42	Checksum		

TABLE 4-3: FRAME EXAMPLE, READ-16 COMMAND

Transmit Frame		Response from MCP39F501	
0xA5	Header Byte	0x06	Acknowledge
0x07	Number of Bytes	0x05	Number of Bytes
0x41	Command (Set Address Pointer)	0x00	Data Byte
0x00	Address0	0x4D	Data Byte
0x54	Address1	0x58	Checksum
0x52	Command (Read 16)		
0x93	Checksum		

TABLE 4-4: FRAME EXAMPLE, BULK ERASE EEPROM

Transmit Frame		Response from MCP39F501	
0xA5	Header Byte	0x06	Acknowledge
0x05	Number of Bytes		
0x4F	Command (Bulk Erase EE)		
0x4D	Device Address		
0x46	Checksum		

4.7 Command Descriptions

4.7.1 REGISTER READ, 16-BIT (0X52)

The `Register Read, 16-bit` command, returns the two bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. With this command the data is returned MSB first.

4.7.2 REGISTER READ, 32-BIT (0X44)

The `Register Read, 32-bit` command, returns the four bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. With this command data is returned MSB first.

4.7.3 REGISTER WRITE, 16-BIT (0X57)

The `Register Write, 16-bit` command is followed by bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other write commands. An acknowledge is the response for this command.

4.7.4 REGISTER WRITE, 32-BIT (0X45)

The `Register Write, 32-bit` command is followed by four bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other write commands. An acknowledge is the response for this command.

4.7.5 REGISTER READ, N BIT (0X4M)

The `Register Read, N-bit` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. The maximum number of bytes that can be read with this command is 48. If there are other read commands within a frame, the maximum number of bytes that can be read is 48 minus the number of bytes being read in the frame. With this command, the data is returned LSB first.

4.7.6 REGISTER WRITE, N BIT (0X4D)

The `Register Write, N-bit` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other write commands. An acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 64. If there are other write commands within a frame, the maximum number of bytes that can be written is 64 minus the number of bytes being written in the frame

4.7.7 SELECT DEVICE (0X4C)

The `Select Device` command is used to drive the direction of the bus in Multiple Device mode by asserting the MODE/**DIR** pin. When the device is in Single Device mode, this command has no effect on the state of the pin. This command is expecting the device address as the command parameter, or the following byte. The device address is a single byte length. If the device address sent with this command matches the value in the MCP39F501's Device Address register, the pin will be asserted and an acknowledge returned.

4.7.8 DE-SELECT DEVICE (0X4B)

The `Select Device` command is used to drive the direction of the bus by deasserting the MODE/**DIR** pin. When the device is in Single Device mode, this command has no effect on the state of the pin. This command is expecting the Device Address as the command parameter, which is the following byte. The Device Address is a single byte length. If the device address sent with this command matches the value in the MCP39F501's Device Address register, the pin will be deasserted and an acknowledge returned.

4.7.9 SET ADDRESS POINTER (0X41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an acknowledge will be returned.

4.7.10 SAVE REGISTERS TO FLASH (0X53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to flash. This includes all R/W registers in the register set. This command is expecting the device address as the instruction parameter, or the following byte. The device address is a single byte length. If the device address matches, the response to this command is an acknowledge.

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4.7.11 PAGE READ EEPROM (0X42)

The `Read Page EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F501. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an acknowledge, 16-bytes of data and CRC checksum.

4.7.12 PAGE WRITE EEPROM (0X50)

The `Write Page EEPROM` command is expecting 17 additional bytes in the command parameters, which are EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"** The response to this command is an acknowledge.

4.7.13 BULK ERASE EEPROM (0X4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the device address as the command parameter for additional security when bulk erasing the EEPROM of a device.

4.7.14 AUTO-CALIBRATION GAIN (0X5A)

The `Auto-Calibration Gain` command initiates the single point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and active power based on the target values written in the corresponding registers. See **Section 9.0 "MCP39F501 Calibration"** for more information on device calibration.

4.7.15 CALIBRATE FREQUENCY (0X76)

For applications not using an external crystal and running the MCP39F501 off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency (0x00AE) register is set such that the frequency indication matches what is set in the Line Frequency Reference (0x0094) register. See **Section 9.0 "MCP39F501 Calibration"** for more information on device calibration.

4.8 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F501:

TABLE 4-5: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
`u32`	Unsigned, 32-bit register
`s32`	Signed, 32-bit register
`u16`	Unsigned, 16-bit register
`s16`	Signed, 16-bit register
`b32`	32-bit register containing discrete Boolean bit settings

4.9 Single-Wire Transmission Mode

In Single-wire Transmission mode, at the end of each computation cycle, the device automatically transmits a frame of power data. This allows for single-wire communication after the device has been configured.

The single-wire transmission frame consists of 16 bytes: three Header Bytes, one Checksum and 12 bytes of power data (including RMS current, RMS voltage, Active Power and Line Frequency).

TABLE 4-6: SINGLE-WIRE TRANSMISSION FRAME

#	Byte
1	HEADERBYTE (0xAB)
2	HEADERBYTE2 (0xCD)
3	HEADERBYTE3 (0xEF)
4	CURRENT RMS – Byte 0
5	CURRENT RMS – Byte 1
6	CURRENT RMS – Byte 2
7	CURRENT RMS – Byte 3
8	VOLTAGE RMS – Byte 0
9	VOLTAGE RMS – Byte 1
10	ACTIVE POWER – Byte 0
11	ACTIVE POWER – Byte 1
12	ACTIVE POWER – Byte 2
13	ACTIVE POWER – Byte 3
14	LINE FREQUENCY – Byte 0
15	LINE FREQUENCY – Byte 1
16	CHECKSUM

Note 1: For custom single-wire transmission packets, contact a Microchip sales office.

NOTES:

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5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F501 uses a coherent sampling algorithm to lock the sampling rate to the line frequency, and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the output power quantities.

5.2 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F501 is shown in Figure 5-1. All conditions set in this diagram effect all of the output registers (RMS current, RMS voltage, active power, reactive power, apparent power, etc.). The gain of the PGA, the shutdown and reset status of the 24-bit ADCs are all controlled through the System Configuration (0X0042) register.

For DC applications, offset can be removed by using the DC Offset Current (0x003C) register. To compensate for any external phase error between the current and voltage channels, the Phase Compensation register (0x003E) can be used.

See **Section 9.0 "MCP39F501 Calibration"** for more information on device calibration.

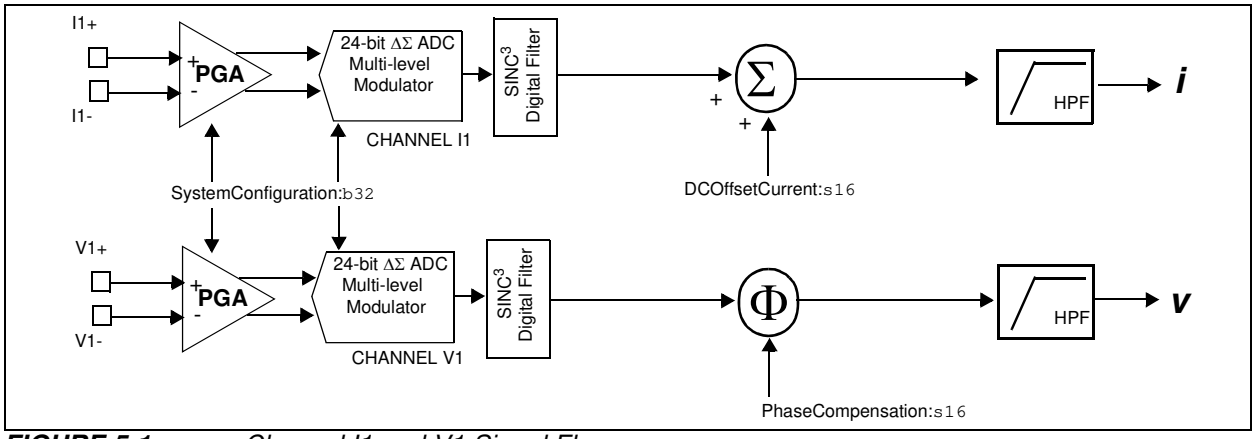


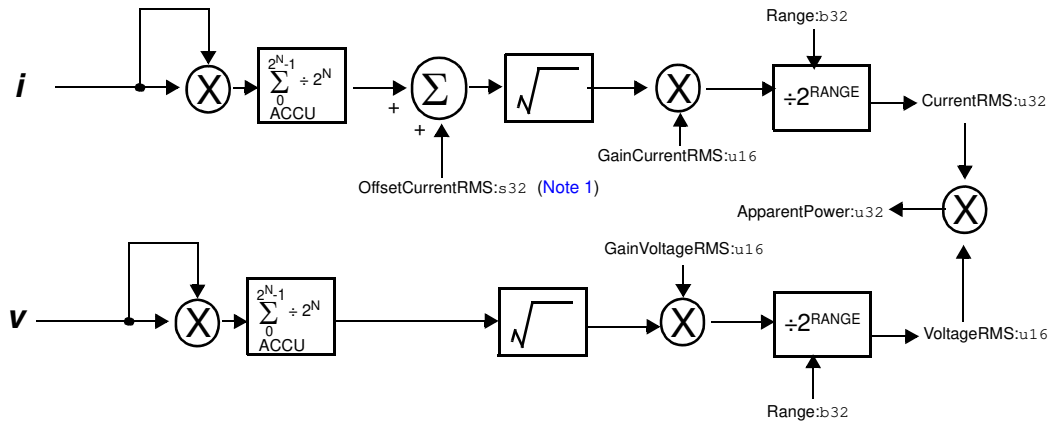
FIGURE 5-1: *Channel I1 and V1 Signal Flow.*

5.3 RMS Current and RMS Voltage (0x0004, 0x0008)

The MCP39F501 device provides true RMS measurements. The MCP39F501 device has two simultaneous sampling 24-bit A/D converters for the current and voltage measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$



Note 1: The value of the Offset Current RMS register is squared internal to the calculation engine, so only the lower 16 bits should be used. The sign of the offset correction is the most significant bit (MSb) of the 32 bit register.

FIGURE 5-2: *RMS Current and Voltage Calculation Signal Flow.*

5.4 Apparent Power (0x0012)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER

$$S = I_{RMS} \times V_{RMS}$$

For scaling of the apparent power indication, the calculation engine uses the register Apparent Power Divisor (0x0040). This is described in the following register operations, per Equation 5-3.

EQUATION 5-3: APPARENT POWER

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{ApparentPowerDivisor}}$$

5.5 Active Power (0x000A)

The MCP39F501 has two simultaneous sampling A/D converters. For the active power calculation, the instantaneous current and instantaneous voltages are multiplied together to create instantaneous power. This instantaneous power is then converted to active power by averaging or taking the DC component.

Equation 5-4 controls the number of samples used in this accumulation prior to updating the Active Power output register.

EQUATION 5-4: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

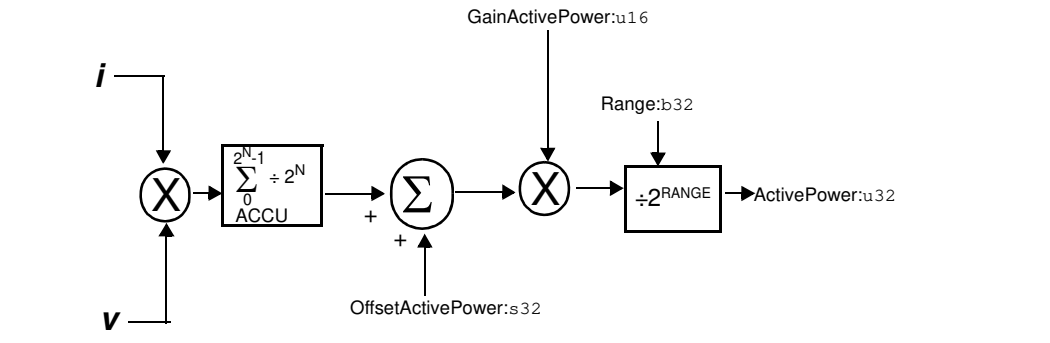


FIGURE 5-3: *Active Power Calculation Signal Flow.*

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5.6 Power Factor (0x0016)

Power factor is calculated by the ratio of P to S or active power divided by apparent power.

EQUATION 5-5: POWER FACTOR

$$PF = \frac{P}{S}$$

The Power Factor Reading is stored in a signed 16-bit register (Power Factor, 0x0016). This register is a signed, 2's complement register with the MSB representing the polarity of the power factor. Positive means inductive load, negative means capacitive load. Each LSB is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.7 Reactive Power (0x000E)

In the MCP39F501, Reactive Power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with active power where ACCU acts as the accumulator. Any light load or residual power can be removed by using the Offset Reactive Power (0x0038) register. Gain is corrected by the Gain Reactive Power (0x002E) register. The final output is an unsigned 32-bit value located in the Reactive Power register (0x000E).

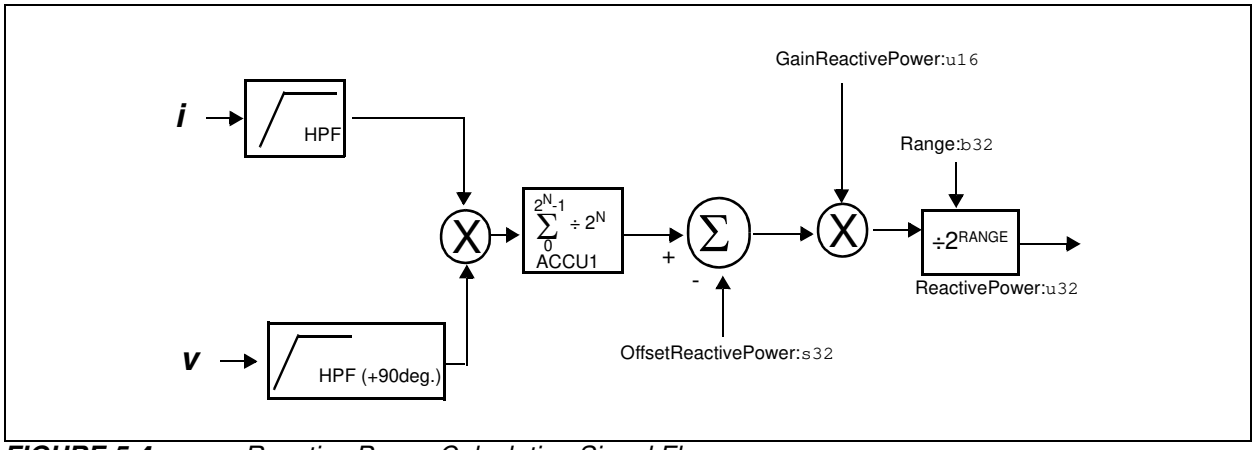

FIGURE 5-4: *Reactive Power Calculation Signal Flow.*

5.8 Accumulation Interval Parameter (0x005A)

The accumulation interval is defined as an 2^N number of line cycles, where N is the value in the Accumulation-IntervalParameter register (0x005A).

5.9 Thermistor Voltage (0x001A)

When a voltage output temperature sensor such as the MCP9700 is connected to the AN_IN/DIO2 pin and the DIO2[n] bits of the DOUT Configuration register are set to 110 for temperature input, the device performs an analog-to-digital conversion on the AN_IN/DIO2 pin.

The least 10 significant bits of the 16-bit Thermistor Voltage register contain the output of the ADC. The conversion rate of the temperature measurement occurs once every computation cycle.

Note that if the AN_IN/DIO2 pin is configured through the DIO Configuration register (0x0046) as an output, then the Thermistor Voltage register value will equal zero.

The Thermistor Voltage is used for temperature compensation of the calculation engine. See **Section 9.8 "Temperature Compensation (Addresses 0x00B0/B2/B4/B6)"** for more information.

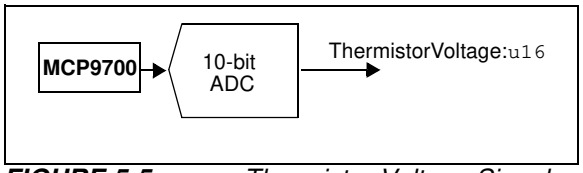

FIGURE 5-5: *Thermistor Voltage Signal Flow.*

NOTES:

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6.0 REGISTERS DESCRIPTION

6.1 Register Map

The following table describes the registers for the MCP39F501 device.

TABLE 6-1: MCP39F501 REGISTER MAP

Address	Register Name	Section Number	Read/ Write	Data type	Description
Output Registers					
0x0000	Address Pointer	6.2	R	u16	Address pointer for read or write commands
0x0002	System Version	6.3	R	u16	System version date code information for MCP39F501, set at the Microchip factory; format YMDD
0x0004	Current RMS	5.3	R	u32	RMS Current output
0x0008	Voltage RMS	5.3	R	u16	RMS Voltage output
0x000A	Active Power	5.5	R	u32	Active Power output
0x000E	Reactive Power	5.7	R	u32	Reactive Power output
0x0012	Apparent Power	5.4	R	u32	Apparent Power output
0x0016	Power Factor	5.6	R	s16	Power Factor output
0x0018	Line Frequency	9.7	R	u16	Line Frequency output
0x001A	Thermistor Voltage	5.9	R	u16	Temperature Monitor output
0x001C	Event Flag	7.2	R	b16	Status of all enabled events
0x001E	System Status	6.4	R	b16	System Status Register
0x0020	Reserved	—	—	u16	Reserved
0x0022	Reserved	—	—	u16	Reserved
Calibration Registers					
0x0024	Reserved	—	—	u16	Reserved
0x0026	Device Address	4.4	R/W	u16	Device Address for the device
0x0028	Gain Current RMS	9.3	R/W	u16	Gain Calibration Factor for RMS Current
0x002A	Gain Voltage RMS	9.3	R/W	u16	Gain Calibration Factor for RMS Voltage
0x002C	Gain Active Power	9.3	R/W	u16	Gain Calibration Factor for Active Power
0x002E	Gain Reactive Power	9.3	R/W	u16	Gain Calibration Factor for Reactive Power
0x0030	Offset Current RMS	9.6.1	R/W	s32	Offset Calibration Factor for RMS Current
0x0034	Offset Active Power	9.6.1	R/W	s32	Offset Calibration Factor for Active Power
0x0038	Offset Reactive Power	9.6.1	R/W	s32	Offset Calibration Factor for Reactive Power
0x003C	DC Offset Current	9.6.2	R/W	s16	Offset Calibration Factor for DC Current
0x003E	Phase Compensation	9.5	R/W	s16	Phase Compensation
0x0040	Apparent Power Divisor	5.4	R/W	u16	Number of Digits for apparent power divisor to match I_{RMS} and V_{RMS} resolution
Design Configuration Registers					
0x0042	System Configuration	6.5	R/W	b32	Control for device configuration, including ADC configuration
0x0046	DIO Configuration	8.0	R/W	b16	Configurable digital output settings for alarm, and event flags
0x0048	Range	6.6	R/W	b32	Scaling factor for Outputs

Note 1: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

TABLE 6-1: MCP39F501 REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data type	Description
0x004C	Calibration Current	9.3.1	R/W	u32	Target Current to be used during single-point calibration
0x0050	Calibration Voltage	9.3.1	R/W	u16	Target Voltage to be used during single-point calibration
0x0052	Calibration Active Power	9.3.1	R/W	u32	Target Active Power to be used during single-point calibration
0x0056	Calibration Reactive Power	9.5.1	R/W	u32	Target Reactive Power to be used during single-point calibration
0x005A	Accumulation Interval Parameter	5.8	R/W	u16	N for 2^N number of line cycles to be used during a single computation cycle
0x005C	Reserved	—	R/W	u16	Reserved
Event Notification Registers					
0x005E	Over Current Limit	7.0	R/W	u32	RMS Current threshold at which an event flag is recorded
0x0062	Reserved	7.0	R/W	u16	Reserved
0x0064	Over Power Limit	7.0	R/W	u32	Active Power threshold at which an event flag is recorded
0x0068	Reserved	7.0	R/W	u16	Reserved
0x006A	Over Frequency Limit	7.0	R/W	u16	Line Frequency threshold at which an event flag is recorded
0x006C	Under Frequency Limit	7.0	R/W	u16	Line Frequency threshold at which an event flag is recorded
0x006E	Over Temperature Limit	7.0	R/W	u16	Temperature threshold at which an event flag is recorded
0x0070	Under Temperature Limit	7.0	R/W	u16	Temperature threshold at which an event flag is recorded
0x0072	Voltage Sag Limit	7.7	R/W	u16	RMS Voltage threshold at which an event flag is recorded
0x0074	Voltage Surge Limit	7.7	R/W	u16	RMS Voltage threshold at which an event flag is recorded
0x0076	Over Current Hold	7.0	R/W	u16	Number of computation cycles for which the Over Current Limit must be breached
0x0078	Reserved	—	R/W	u16	Reserved
0x007A	Over Power Hold	7.0	R/W	u16	Number of computation cycles for which the Over Power Limit must be held
0x007C	Reserved	—	R/W	u16	Reserved
0x007E	Over Frequency Hold	7.0	R/W	u16	Number of computation cycles for which the Over Frequency Limit must be held
0x0080	Under Frequency Hold	7.0	R/W	u16	Number of computation cycles for which the Under Frequency Limit must be held
0x0082	Over Temperature Hold	7.0	R/W	u16	Number of computation cycles for which the Over Temperature Limit must be held
0x0084	Under Temperature Hold	7.0	R/W	u16	Hold time for which the Under Temperature Limit must be held
0x0086	Reserved	—	R/W	u16	Reserved

Note 1: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

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TABLE 6-1: MCP39F501 REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data type	Description
0x0088	Reserved	—	R/W	u16	Reserved
0x008A	Event Enable	7.1	R/W	u16	Enable Event Register
0x008C	Event Mask Critical	7.3	R/W	u16	Mask for event notifications to be put on DIO pin selected as “Event Critical”
0x008E	Event Mask Standard	7.4	R/W	u16	Mask for event notification to be put on DIO pin selected as “Event Standard”
0x0090	Event Test	7.5	R/W	u16	Register used to set events for testing purposes
0x0092	Event Clear	7.6	R/W	u16	Register used to clear events
0x0094	Line Frequency Ref.	9.7.1	R/W	u16	Reference Value for the nominal line frequency
0x0096	Reserved	—	R	u16	Reserved
0x00AE	Gain Line Frequency	9.7	R/W	u16	Correction Factor for Line Frequency Indication
EMI Filter Compensation Registers (Note 1)					
0x0098	Reserved	—	R	u16	Reserved
0x009A	Reserved	—	R	u16	Reserved
0x009C	Reserved	—	R	u16	Reserved
0x009E	Reserved	—	R	u16	Reserved
0x00A0	Reserved	—	R	u16	Reserved
0x00A2	Reserved	—	R	u16	Reserved
0x00A4	Reserved	—	R	u16	Reserved
0x00A6	Reserved	—	R	u16	Reserved
0x00A8	Reserved	—	R	u16	Reserved
0x00AA	Reserved	—	R	u16	Reserved
0x00AC	Reserved	—	R	u16	Reserved
TEMPERATURE COMPENSATION REGISTERS					
0x00B0	Temperature Compensation for Frequency	9.8	R/W		Correction factor for compensating the line frequency indication over temperature
0x00B2	Temperature Compensation for Current	9.8	R/W		Correction factor for compensating the Current RMS indication over temperature
0x00B4	Temperature Compensation for Power	9.8	R/W		Correction factor for compensating the active power indication over temperature
0x0B6	Ambient Temperature Reference Voltage	9.8	R/W		Register for storing the reference temperature during calibration

Note 1: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.