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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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MCP39F511A

AC/DC Dual-Mode Power-Monitoring IC with Calculation and Energy Accumulation

Features

- Real-Time Measurement of Input Power for AC or DC Supplies
- AC/DC Dual-Mode Power Monitoring Accuracy Capable of 0.1% Error Across 4000:1 Dynamic Range
- Automatic Sensing and Switching Between AC and DC Modes
- Built-In Calculations on Fast 16-Bit Processing Core
  - Active and Reactive Energy Accumulation
  - Active, Reactive, Apparent Power
  - True RMS Current, RMS Voltage
  - Line Frequency, Power Factor
- 64-bit Wide Import and Export Active Energy Accumulation Registers
- 64-bit Four Quadrant Reactive Energy Accumulation Registers
- Automatic Saving the Energy Accumulation Registers into EEPROM at Power Off
- Automatic Loading the Energy Accumulation Registers from EEPROM at Power On
- Signed Active and Reactive Power Outputs
- Dedicated Zero Crossing Detection (ZCD) Pin Output with Less than 200 µs Latency
- Dedicated PWM Output Pin with Programmable Frequency and Duty Cycle
- Automatic Event Pin Control through Fast Voltage Sag/Surge Detection
- Two Wire Serial Protocol with Selectable Baud Rate Up to 115.2 kbps using Universal Asynchronous Receiver/Transmitter (UART)
- Four Independent Registers for Minimum and Maximum Output Quantity Tracking
- Fast Calibration Routines and Simplified Command Protocol
- 512 Bytes User-Accessible EEPROM through Page Read/Write Commands
- Low-Drift Internal Voltage Reference, 7 ppm/°C Typical
- 28-lead 5x5 QFN Package
- Extended Temperature Range -40°C to +125°C

Applications

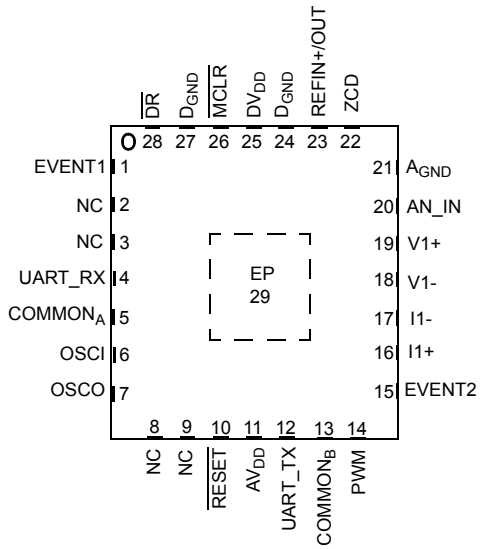
- Power Monitoring and Management for Smart Home/City
- Industrial Lighting Power Monitoring
- Power Measurement for Renewable Energy System
- Intelligent Power Distribution Units
- Server Power Monitor

Description

The MCP39F511A device is a highly-integrated, complete single-phase power-monitoring IC designed for real-time measurement of input power for AC or DC power supplies, making it suitable for a wide range of consumer and industrial applications. It is capable of detecting the input voltage in order to work as DC or AC mode. It includes dual-channel Delta-Sigma ADCs, a 16-bit calculation engine, EEPROM and a flexible 2-wire interface. Separate AC and DC calibration registers are provided, to ensure high-accuracy measurements in both modes. An integrated low-drift voltage reference with 7 ppm/°C in addition to 94.5 dB of SINAD performance on each measurement channel allows for better than 0.1% accurate designs across a 4000:1 dynamic range.

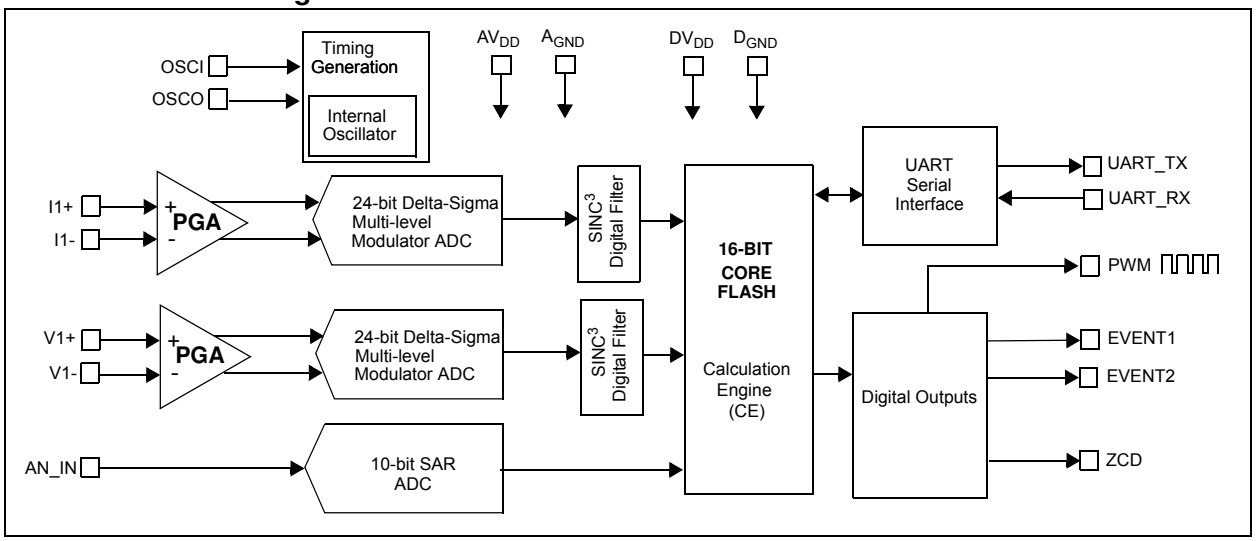
Package Types

MCP39F511A
5x5 QFN*

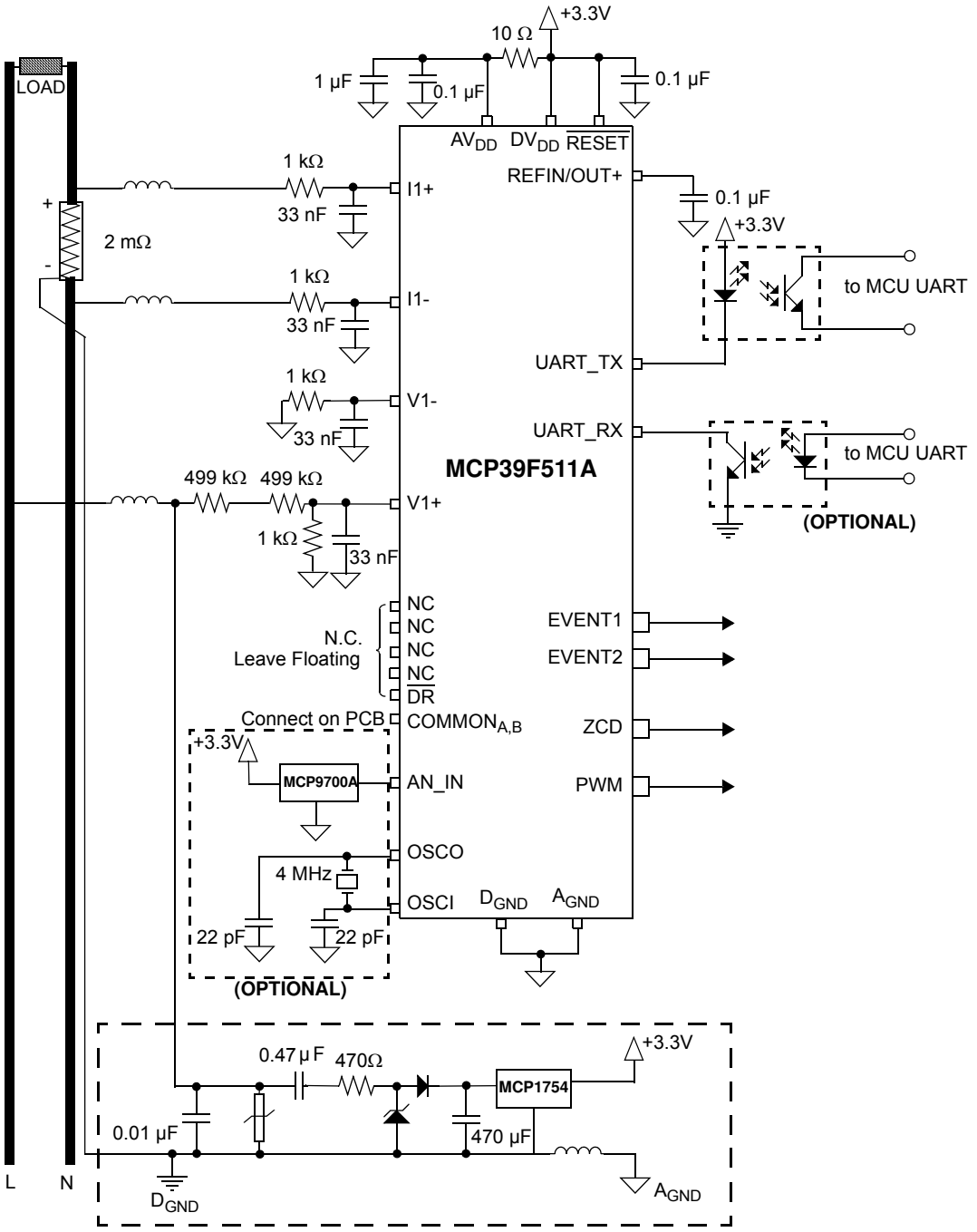


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



MCP39F511A Typical Application – Single Phase, Two-Wire Application Schematic



Note 1: The MCP39F511A demonstration board uses a switching power supply, however a low-cost capacitive-based supply, as shown here, is sufficient for many applications.

2: The external sensing components shown here, a 2 mΩ shunt, two 499 kΩ and 1 kΩ resistors for the 1000:1 voltage divider, are specifically chosen to match the default values for the calibration registers defined in **Section 6.0 "Register Descriptions"**. By choosing low-tolerance components of these values (for instance 1% tolerance), measurement accuracy in the 2-3% range can be achieved with zero calibration (AC only, offset calibration may be needed in DC mode). See **Section 9.0 "MCP39F511A Calibration"** for more information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} ..... -0.3 to +4.5V
AV_{DD} ..... -0.3 to +4.0V
Digital inputs and outputs w.r.t. A_{GND} .....-0.3V to +4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} .....-2V to +2V
V_{REF} input w.r.t. A_{GND} ....-0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin.....300 mA
Maximum Current into DV_{DD} pin.....250 mA
Maximum Output Current Sunk by Digital IO .....25 mA
Maximum Current Sourced by Digital IO.....25 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM).....4.0 kV, 200V
ESD on all other pins (HBM,MM).....4.0 kV, 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Measurement						
Active Power (**Note 1**)	P	—	±0.1	—	%	4000:1 Dynamic range on current channel (**Note 2**)
Reactive Power (**Note 1**)	Q	—	±0.1	—	%	4000:1 Dynamic range on current channel (**Note 2**)
Apparent Power (**Note 1**)	S	—	±0.1	—	%	4000:1 Dynamic range on current channel (**Note 2**)
Current RMS (**Note 1**)	I_{RMS}	—	±0.1	—	%	4000:1 Dynamic range on current channel (**Note 2**)
Voltage RMS (**Note 1**)	V_{RMS}	—	±0.1	—	%	4000:1 (DC mode), 20:1 (AC mode) Dynamic range on voltage channel (**Note 2**, **8**)
Power Factor (**Note 1**)	Φ	—	±0.1	—	%	
Line Frequency (**Note 1**)	LF	—	±0.1	—	%	
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x $(1/f_{LINE})$	—	ms	**Note 3**

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.
2: Specification by design and characterization; not production tested.
3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.
4: Applies to Voltage Sag and Voltage Surge events only.
5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.
6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.
7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.
8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Minimum Time for Voltage Surge/Sag Detection	t_{AC_SASU}	—	5, see Section 7.2	—	ms	Note 4
24-Bit Delta-Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (V1+ – V1-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	Note 5
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	Note 6
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	Note 6
Signal-to-Noise Ratio	SNR	92	95	—	dB	Note 6
Spurious Free Dynamic Range	SFDR	—	111	—	dB	Note 6
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + 0.6V_{PP}, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.0 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V
10-Bit SAR ADC Performance for Temperature Measurement						
Resolution	N_R	—	10	—	bits	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.

7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.

8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	D_{VDD} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Nonlinearity	I_{NL}	—	±1	±2	LSb	
Differential Nonlinearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Temperature Measurement Rate		—	$f_{LINE}/2^N$	—	sps	**Note 7**
Clock and Timings						
UART Baud Rate	UDB	1.2	9.6	115.2	kbps	See **Section 3.2** for protocol details
Master Clock and Crystal Frequency	f_{MCLK}	-2%	4	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40 to +85°C only (**Note 7**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	V_{REFEXT} = 0, T_A = +25°C only
Temperature Coefficient	TCV_{REF}	—	7	—	ppm/°C	T_A = -40°C to +125°C, V_{REFEXT} = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	V_{REFEXT} = 0
Current, V_{REF}	$AI_{DD}V_{REF}$	—	25	—	µA	V_{REFEXT} = 0 SHUTDOWN<1:0> = 11

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.

7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.

8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.3V	V	
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	
DV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0–3.3V in 0.1s, 0–2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms
Operating Current	I_{DD}	—	13	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	years	Provided no other specifications are violated
Supply Current During Programming	I_{DDPD}	—	7	—	mA	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.

7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.

8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to+ 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 DV_{DD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
			0.050	0.100		Digital Output pins only (ZCD, PWM, EVENT1, EVENT2)

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	36.9	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are **not** tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = +3.3V, DV_{DD} = +3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

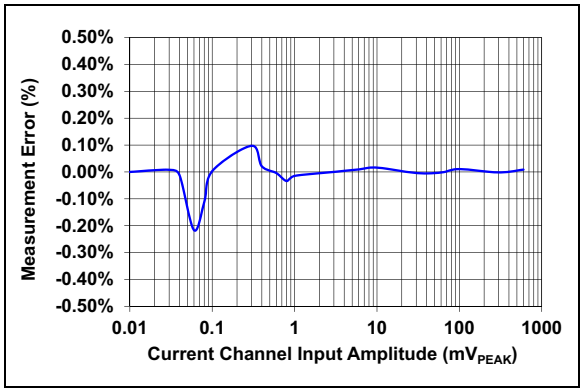


FIGURE 2-1: *Active Power, Gain = 1.*

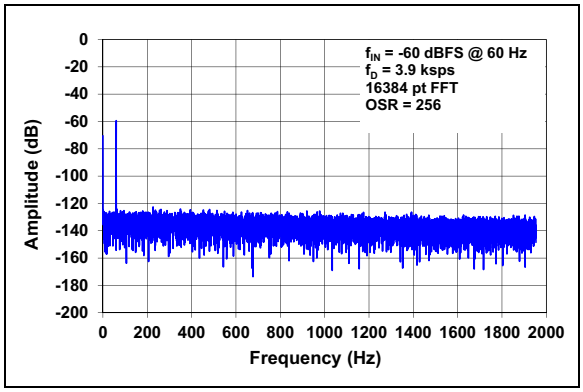


FIGURE 2-4: *Spectral Response.*

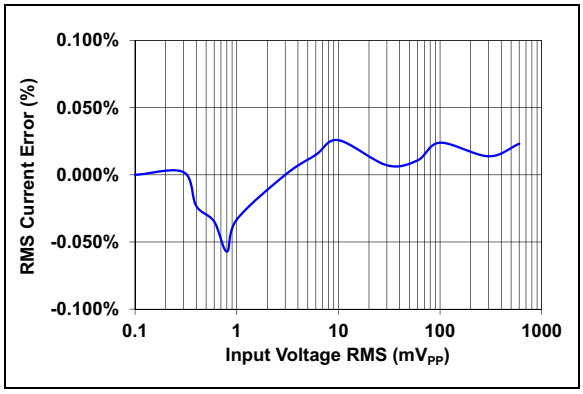


FIGURE 2-2: *RMS Current, Gain = 1.*

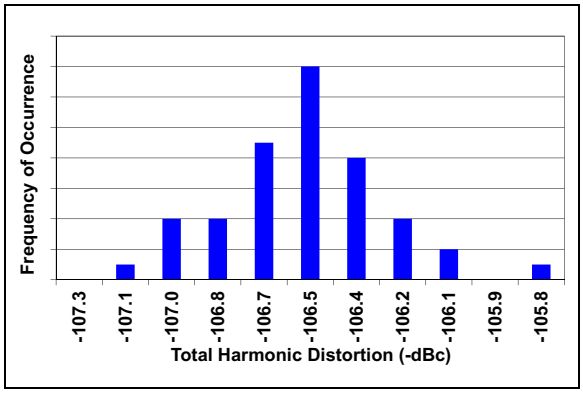


FIGURE 2-5: *THD Histogram.*

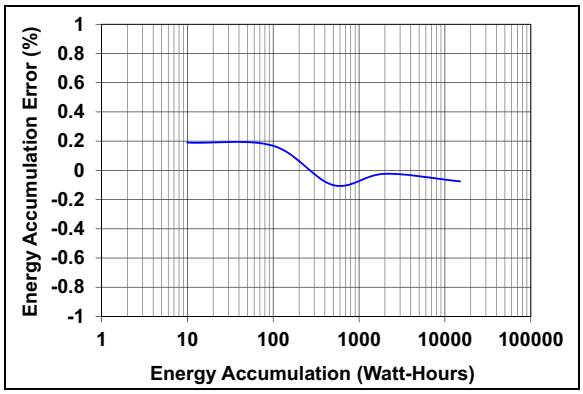


FIGURE 2-3: *Energy, Gain = 8.*

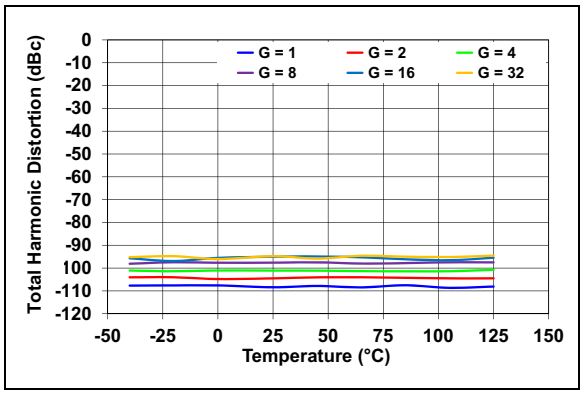


FIGURE 2-6: *THD vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

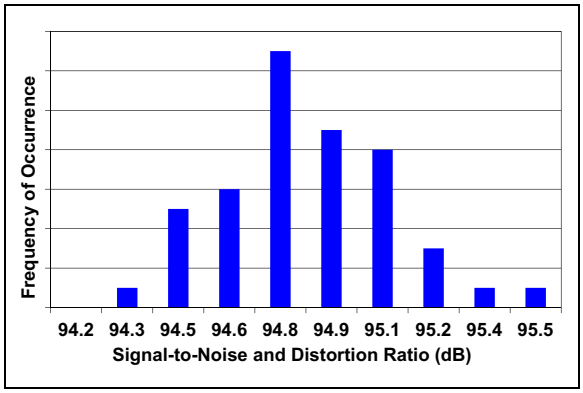


FIGURE 2-7: *SNR Histogram.*

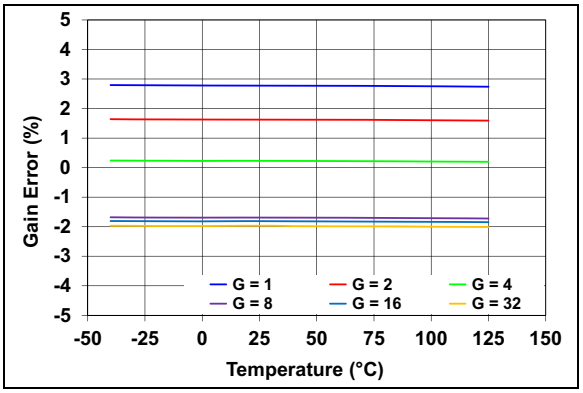


FIGURE 2-9: *Gain Error vs. Temperature.*

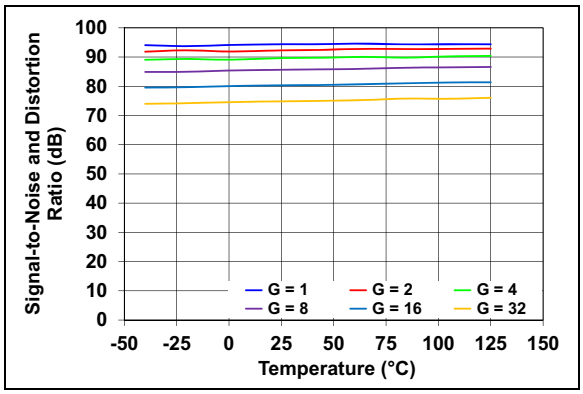


FIGURE 2-8: *SINAD vs. Temperature.*

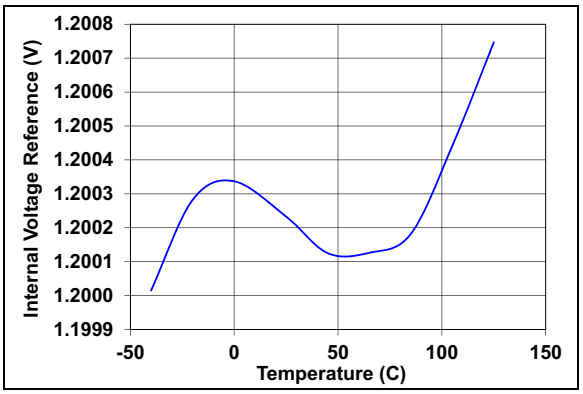


FIGURE 2-10: *Internal Voltage Reference vs. Temperature.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F511A 5x5 QFN	Symbol	Function
1	EVENT1	Event 1 Output pin
2, 3, 8, 9	NC	No Connect (must be left floating)
4	UART_RX	UART Communication RX pin
5	$COMMON_A$	Common pin A, to be connected to pin 13 ($COMMON_B$)
6	OSCI	Oscillator Crystal Connection pin or External Clock Input pin
7	OSCO	Oscillator Crystal Connection pin
10	$\overline{RESET}$	Reset pin for Delta-Sigma ADCs
11	AV_{DD}	Analog Power Supply pin
12	UART_TX	UART Communication TX pin
13	$COMMON_B$	Common pin B, to be connected to pin 5 ($COMMON_A$)
14	PWM	Pulse-Width Modulation (PWM) Output pin
15	EVENT2	Event 2 Output pin
16	I1+	Noninverting Current Channel Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel Input for 24-bit ΔΣ ADC
18	V1-	Inverting Voltage Channel Input for 24-bit ΔΣ ADC
19	V1+	Noninverting Voltage Channel Input for 24-bit ΔΣ ADC
20	AN_IN	Analog Input for SAR ADC
21	A_{GND}	Analog Ground Pin, return path for internal analog circuitry
22	ZCD	Zero Crossing Detection Output
23	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output pin
24, 27	D_{GND}	Digital Ground pin, return path for internal digital circuitry
25	DV_{DD}	Digital Power Supply pin
26	$\overline{MCLR}$	Master Clear for device
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to pins 24 and 27 (D_{GND}))

3.1 Event Output Pins (EVENTn)

These digital output pins can be configured to act as output flags based on various internal raise conditions. Control is modified through the Event Configuration register.

3.2 UART Communication Pins (UART_RX, UART_TX)

The MCP39F511A device contains an asynchronous full-duplex UART. The UART communication is eight bits with Start and Stop bit. See **Section 4.3 "UART Settings"** for more information.

3.3 Common Pins ($COMMON_A$ and $_B$)

$COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F511A. These two pins should be connected together in the application.

3.4 Oscillator Pins (OSCI/OSCO)

OSCI and OSCO provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 4 MHz crystal can be connected to these pins. If a crystal of external clock source is not detected, the device will clock from the internal 4 MHz oscillator.

3.5 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the Delta-Sigma ADCs, PGA, internal V_{REF} and other blocks associated with the Analog Front End (AFE) in a Reset state when pulled low. This input is Schmitt-triggered.

3.6 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F511A.

This pin requires appropriate bypass capacitors and should be maintained to +2.7V and +3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.7 Pulse-Width Modulator (PWM)

This digital output is a dedicated PWM output that can be controlled through the PWM Frequency and PWM Duty Cycle registers. See **Section 8.0 "Pulse Width Modulation (PWM)"** for more information.

3.8 24-Bit Delta-Sigma ADC Differential Current Channel Input Pins (I1+/I1-)

I1- and I1+ are the two fully-differential current-channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.9 24-Bit Delta-Sigma ADC Differential Voltage Channel Inputs (V1-/V1+)

V1- and V1+ are the two fully-differential voltage-channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each V_N+/- input pin is ±1V with no distortion and ±2V with no breaking after continuous voltage.

3.10 Analog Input (AN_IN)

This is the input to the analog-to-digital converter that can be used for temperature measurement and compensation. If temperature compensation is required in the application, it is advised to connect the low-power active thermistor IC MCP9700A to this pin. If temperature compensation is not required, this can be used as a general purpose analog-to-digital converter input.

3.11 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground plane is available on the PCB, it is recommended that this pin be tied to that plane.

3.12 Zero Crossing Detection (ZCD)

This digital output pin is the output of the zero crossing detection circuit of the IC. The output here will be a logic output with edges that transition at each zero crossing of the voltage channel input. For more information see **Section 5.13 "Zero Crossing Detection (ZCD)"**.

3.13 Noninverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for the Delta-Sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.14 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.15 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F511A. This pin requires appropriate bypass capacitors and should be maintained between +2.7V and +3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.16 Data-Ready Pin ($\overline{DR}$)

The data-ready pin indicates if a new Delta-Sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the data-ready pin to indicate the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with the line frequency to ensure an integer number of samples for each line cycle.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.17 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to pin 24 (D_{GND}).

NOTES:

4.0 COMMUNICATION PROTOCOL

The communication protocol for the MCP39F511A device is based on the Simple Sensor Interface (SSI) protocol. This protocol is used for point-to-point communication from a single-host microcontroller (MCU) to a single-slave MCP39F511A device.

All communication to the device occurs in frames. Each frame consists of a header byte, the number of bytes in the frame, command packet (or command packets) and a checksum. It is important to note that the maximum number of bytes in either a receive or transmit frame is 35.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

This approach allows for single, secure transmission from the host processor to the MCP39F511A device with either a single command or multiple commands. No command in a frame is processed until the entire frame is complete and the checksum and number of bytes are validated.

The number of bytes in an individual command packet depend on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

This protocol can also be used to set up transmission from the MCP39F511A device on specific registers. A predetermined single-wire transmission frame is defined for one-wire interfaces. The Auto-Transmit mode can be initiated by setting the SINGLE_WIRE bit in the System Configuration register, allowing for single-wire communication within the application. See **Section 4.8 "Single-Wire Transmission Mode"** for more information on this communication.

4.1 Device Responses

After the reception of a communication frame, the MCP39F511A device has three possible responses, which will be returned with or without data depending on the frame received. These responses are:

- Acknowledge (ACK, 0x06): Frame received with success, commands understood and commands executed with success.
- Negative Acknowledge (NAK, 0x15): Frame received with success, however commands not executed with success, commands not understood or some other error in the command bytes.
- Checksum Fail (CSFAIL, 0x51): Frame received with success, however the checksum of the frame did not match the bytes in the frame.

Note:	There is one unique device ID response that is used to determine which MCP39FXXX device is present: [NAK(0x15) + ID_BYTE]. If the command received is a single byte (0x5A) instead of a command frame, the response is NAK followed by the ID_BYTE. For the MCP39F511A device, the ID_BYTE is 0x04.

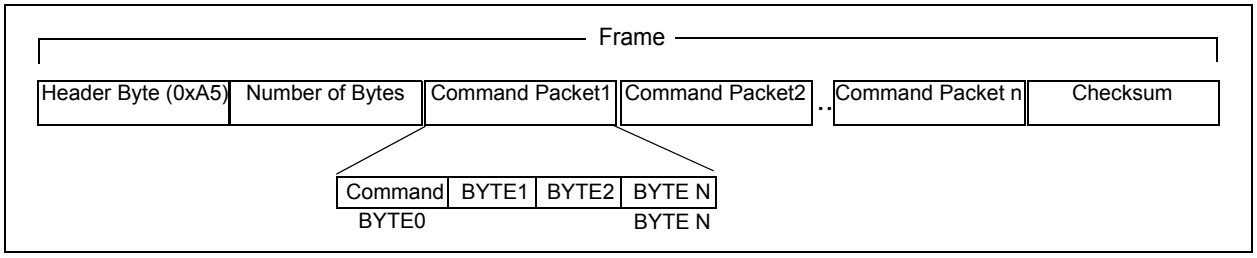


FIGURE 4-1: *Communication Frame MCP39F511A.*

4.2 Checksum

The checksum is generated using simple byte addition and taking the modules to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and the number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F511A device will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F511A device, the frame and checksum are created in the same way, with the header byte becoming an Acknowledge (0x06). Communication examples are given in **Section 4.5 "Example Communication Frames and MCP39F511A Responses"**.

4.3 UART Settings

The default baud rate is 9.6 kbps and can be changed using the UART bits in the **System Configuration Register**. Note that the baud rate is changed at system power-up, so when changing the baud rate, a `Save To Flash` command followed by a power-on cycle is required. The UART operates in 8-bit mode, plus one Start bit and one Stop bit, for a total of 10 bits per byte, as shown in Figure 4-2.

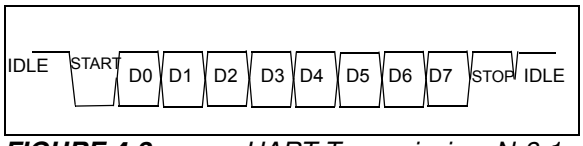


FIGURE 4-2: *UART Transmission, N-8-1.*

4.4 Command List

The following table is a list of all accepted command bytes for the MCP39F511A device. There are 10 possible accepted commands for the MCP39F511A device.

TABLE 4-1: MCP39F511A INSTRUCTION SET

Command #	Command	Command ID	Instruction Parameter	Number of Bytes	Successful Response UART_TX
1	`Register Read, N bytes`	0x4E	NoB(3)	2	ACK, NoB, data, checksum
2	`Register Write, N bytes`	0x4D	NoB(3)	1+N	ACK
3	`Set Address Pointer`	0x41	ADDRESS	3	ACK
4	`Save Registers To Flash`	0x53	None	1	ACK
5	`Page Read EEPROM`	0x42	PAGE	2	ACK, NoB, data, checksum
6	`Page Write EEPROM`	0x50	PAGE	18	ACK
7	`Bulk Erase EEPROM`	0x4F	None	1	ACK
8	`Auto-Calibrate Gain`	0x5A	None	Note 1	
9	`Auto-Calibrate Reactive Gain`	0x7A	None	Note 1, 2	
10	`Auto-Calibrate Frequency`	0x76	None	Note 1, 2	
11	`Save Energy Counters to EEPROM`	0x45	None	1	ACK

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

2: AC mode only

3: NoB represents total number of bytes in frame

4.5 Example Communication Frames and MCP39F511A Responses

Tables 4-2 to 4-11 show exact hexadecimal communication frames as recommended to be sent to the MCP39F511A device from the system MCU. The values here can be used as direct examples for writing the code to communicate to the MCP39F511A device.

TABLE 4-2: REGISTER READ, N BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x08	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0x4E	Command (`Register Read, N Bytes`)	
7	0x20	Number of Bytes to Read (32)	
8	0x5E	Checksum	ACK + NoB (35) + data (32) + checksum

Note 1: This example `Register Read, N bytes` frame, as it is written here, can be used to poll a subset of the output data, starting at the top, address 0x02, and reading 32 data bytes back or 35 bytes total in the frame.

TABLE 4-3: REGISTER WRITE, N BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x0C	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x94	Address Low	
6	0x4D	Command (`Register Write, N Bytes`)	
7	0x04	Number of Bytes to Write (4)	
8–11	*Data*	Data Bytes (4 total data bytes)	
12	Checksum	Checksum	ACK

Note 1: This `Register Write, N Bytes` frame, as it is written here, can be used to write the System Configuration register, which controls the device configuration, including the ADC. See Register 6-2 for more information.

TABLE 4-4: SET ADDRESS POINTER COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x06	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0xF8	Checksum	ACK

Note 1: The `Set Address Pointer` command is typically included inside of a frame that includes a read or write command, as shown in Tables 4-2 and 4-3. There is typically no reason for this command to have its own frame, but is shown here as an example.

TABLE 4-5: SAVE TO FLASH COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x53	Command (`Save To Flash`)	
4	0xFC	Checksum	ACK

TABLE 4-6: PAGE READ EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x42	Command (`Page Read EEPROM`)	
4	0x01	Page Number (example: 1)	
5	0xF8	Checksum	ACK + NoB (19) + EEPROM Page Data (16) + Checksum

TABLE 4-7: PAGE WRITE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x15	Number of Bytes in Frame	
3	0x50	Command (`Page Write EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5-20	*Data*	EEPROM Data (16 bytes/page)	
21	Checksum	Checksum	ACK

TABLE 4-8: BULK ERASE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x4F	Command (`Bulk Erase EEPROM`)	
4	0xF8	Checksum	ACK

TABLE 4-9: AUTO-CALIBRATE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x5A	Command (`Auto-Calibrate Gain`)	
4	0x03	Checksum	ACK (or NAK if unable to calibrate)[1]

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

TABLE 4-10: AUTO-CALIBRATE REACTIVE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x7A	Command (`Auto-Calibrate Reactive Gain`)	
4	0x23	Checksum	ACK (or NAK if unable to calibrate)[1]

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

TABLE 4-11: AUTO-CALIBRATE FREQUENCY COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x76	Command (`Auto-Calibrate Frequency`)	
4	0x1F	Checksum	ACK (or NAK if unable to calibrate)[1]

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

4.6 Command Descriptions

4.6.1 REGISTER READ, N BYTES (0x4E)

The `Register Read, N bytes` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other read commands. An Acknowledge NoB, Data and Checksum is the response for this command. The maximum number of bytes that can be read with this command is 32. If there are other read commands within a frame, the maximum number of bytes that can be read is 32 minus the number of bytes being read in the frame. With this command, the data is returned LSb first.

4.6.2 REGISTER WRITE, N BYTES (0x4D)

The `Register Write, N bytes` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other write commands. An Acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 32. If there are other write commands within a frame, the maximum number of bytes that can be written is 32 minus the number of bytes being written in the frame. With this command, the data is written to the LSb first.

4.6.3 SET ADDRESS POINTER (0x41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes, Address High byte followed by Address Low byte. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an Acknowledge will be returned.

4.6.4 SAVE REGISTERS TO FLASH (0x53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to Flash. This includes all R/W registers in the register set. The response to this command is an Acknowledge.

4.6.5 PAGE READ EEPROM (0x42)

The `Page Read EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F511A. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an Acknowledge NoB, 16-bytes of data and CRC Checksum.

4.6.6 PAGE WRITE EEPROM (0x50)

The `Page Write EEPROM` command is expecting 17 additional bytes in the command parameters, which are EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"** The response to this command is an Acknowledge.

4.6.7 BULK ERASE EEPROM (0x4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. The response to this command is an Acknowledge.

4.6.8 AUTO-CALIBRATE GAIN (0x5A)

The `Auto-Calibrate Gain` command initiates the single-point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and active power based on the target values written in the corresponding registers. See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration. The response to this command is an Acknowledge.

4.6.9 AUTO-CALIBRATE REACTIVE POWER GAIN (0X7A)

The `Auto-Calibrate Reactive Gain` command initiates a single-point calibration to match the measured reactive power to the target reactive power. This is typically done at PF = 0.5. See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration.

4.6.10 AUTO-CALIBRATE FREQUENCY (0x76)

For applications not using an external crystal and running the MCP39F511A device off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency register is set such that the frequency indication matches what is set in the Line Frequency Reference register. See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration.

4.6.11 SAVE ENERGY COUNTERS TO EEPROM (0x45)

The `Save Energy Counters to EEPROM` command makes a copy of the energy counters to EEPROM. Import active and reactive energy counters are saved in PAGE 0. Export active and reactive energy counters are saved in PAGE 1. The bytes are written at incremental addresses, starting with the LSb. The response to this command is an Acknowledge.

4.7 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F511A:

TABLE 4-12: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
u64	Unsigned, 64-bit register
u32	Unsigned, 32-bit register
s32	Signed, 32-bit register
u16	Unsigned, 16-bit register
s16	Signed, 16-bit register
b32	32-bit register containing discrete Boolean bit settings

4.8 Single-Wire Transmission Mode

In Single-Wire Transmission mode, at the end of each computation cycle, the device automatically transmits a frame of power data. This allows for single-wire communication after the device has been configured.

The single-wire transmission frame consists of 20 bytes: three Header bytes, one checksum and 16 bytes of power data (including RMS current, RMS voltage, active power, reactive power and line frequency).

TABLE 4-13: SINGLE-WIRE TRANSMISSION FRAME (Note 1)

#	Byte
1	HEADERBYTE (0xAB)
2	HEADERBYTE2 (0xCD)
3	HEADERBYTE3 (0xEF)
4	CURRENT RMS – Byte 0
5	CURRENT RMS – Byte 1
6	CURRENT RMS – Byte 2
7	CURRENT RMS – Byte 3
8	VOLTAGE RMS – Byte 0
9	VOLTAGE RMS – Byte 1
10	ACTIVE POWER – Byte 0
11	ACTIVE POWER – Byte 1
12	ACTIVE POWER – Byte 2
13	ACTIVE POWER – Byte 3
14	REACTIVE POWER – Byte 0
15	REACTIVE POWER – Byte 1
16	REACTIVE POWER – Byte 2
17	REACTIVE POWER – Byte 3
18	LINE FREQUENCY – Byte 0
19	LINE FREQUENCY – Byte 1
20	CHECKSUM

Note 1: For custom single-wire transmission packets, contact a Microchip sales office.

NOTES:

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F511A device uses a coherent sampling algorithm to phase lock the sampling rate to the line frequency with an integer number of samples per line cycle (56), and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the power outputs.

Assuming that the input frequency is 50 Hz, the sampling speed is 56 * 50 = 2800 samples/second. For the default accumulation interval parameter of 2, the computational cycle is 56 * 4 divided by the sampling speed (the result is 80 ms).

In DC mode, the sampling speed is fixed at approximately 1953 samples/second. For the default value of the accumulation interval parameter (2), the computational cycle is 56 * 4 divided by the sampling speed (the result is approximately 114.7 ms).

5.1.1 LINE FREQUENCY

The coherent sampling algorithm is also used to calculate the Line Frequency Output register, which is updated every computation cycle. The correction factor for line frequency measurement is the Gain Line Frequency register, which is used during the line frequency calibration, see **Section 9.6.1 "Using the Auto-Calibrate Frequency Command"**. Note that the resolution of the Line Frequency Output register is fixed, and the resolution is 1 milliHz.

5.1.2 POWER ON RESET (POR) WITH AC DETECTION BEHAVIOR

At Power-on Reset, the calculation engine must initialize the AFE and also initialize all the peripherals, prior to being able to start the first computation cycle. In addition, the device must detect whether or not an AC signal is present and if so, determine the correct coherent sampling clock values. This process is given sufficient time for correct initialization and the start-up time is 500 ms for a 50 Hz line, and 417 ms for a 60 Hz line.

The high pass filters are turned off to let pass both DC and AC signals. If the number of zero crossings detected during this time on the voltage channel is less than 10 (to filter out false detections), the device will automatically switch to DC mode.

5.1.3 DC DETECTION AND DC MODE

The device uses an internal counter based on the sampling rate of the AFE to determine if an AC signal is not present and if the device should switch to DC mode. If an AC signal is not present for this time period (same as above, based on the number of zero crossings detected on the voltage channel), the device will switch to DC mode, turning off the high pass filters and setting the frequency output to zero.

5.2 Accumulation Interval Parameter

The accumulation interval is defined as an 2^N number of line cycles, where N is the value in the Accumulation Interval Parameter register. N can be as low as 0 (for the fastest update rate), but no bigger than 8.

5.3 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F511A is shown in Figure 5-1. All conditions set in this diagram effect all of the output registers (RMS current, RMS voltage, Active power, Reactive power, Apparent power, etc.). The gain of the PGA, the Shutdown and Reset status of the 24-bit ADCs are all controlled through the System Configuration Register.

For DC applications, offset can be removed by using the OFFCAL_CH0 and OFFCAL_CH1 registers for current offset and voltage offset, respectively. The OFFCAL_MSB register holds the most significant byte (MSB) for both the OFFCAL_CH0 (current) and OFFCAL_CH1 (voltage) calibration values and together add to the full 24-bit value written directly into the internal offset registers of the ADC. The Phase Compensation register is used to compensate for any external phase error between the voltage and current channels.

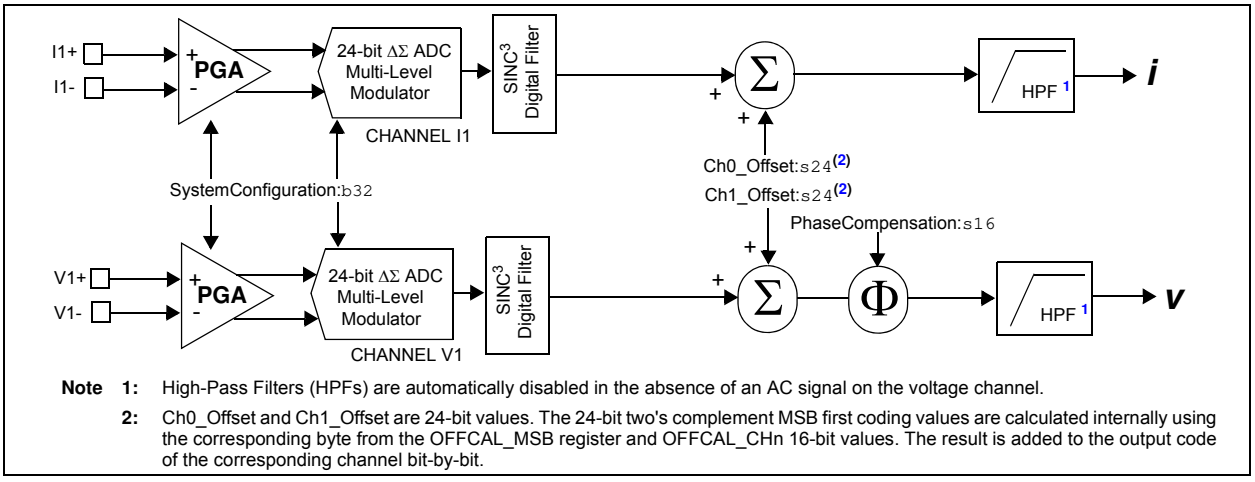
See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration.

5.4 RMS Current and RMS Voltage

The MCP39F511A device provides true RMS measurements. The MCP39F511A device has two simultaneous sampling 24-bit A/D converters for the current and voltage measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$



Note 1: High-Pass Filters (HPFs) are automatically disabled in the absence of an AC signal on the voltage channel.

2: Ch0_Offset and Ch1_Offset are 24-bit values. The 24-bit two's complement MSB first coding values are calculated internally using the corresponding byte from the OFFCAL_MSB register and OFFCAL_CHn 16-bit values. The result is added to the output code of the corresponding channel bit-by-bit.

FIGURE 5-1: *Channel I1 and V1 Signal Flow.*

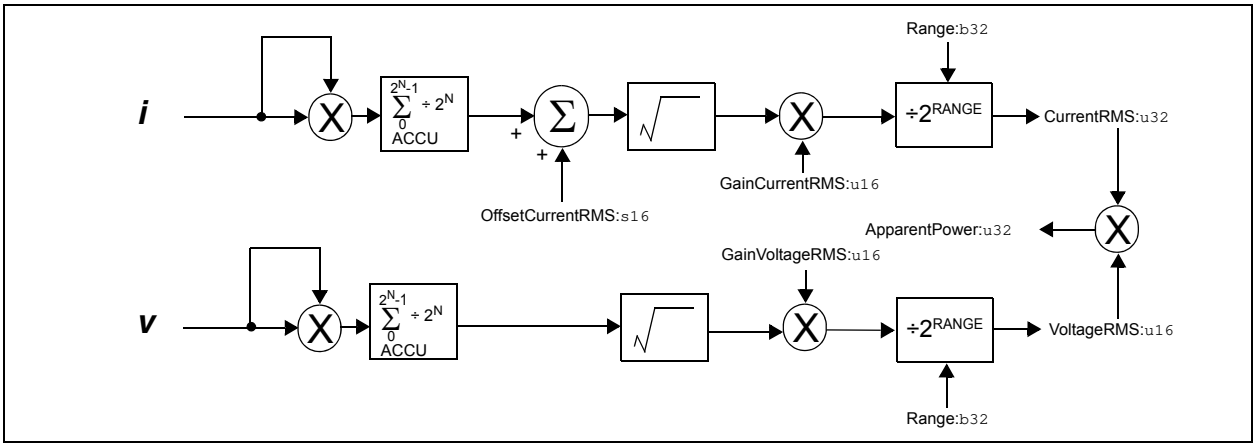


FIGURE 5-2: *RMS Current and Voltage Calculation Signal Flow.*

5.5 Power and Energy

The MCP39F511A offers signed power numbers for active and reactive power, import and export registers for active energy, and four-quadrant reactive power measurement. For this device, import power or energy is considered positive (power or energy being consumed by the load), and export power or energy is considered negative (power or energy being delivered by the load). The following figure represents the measurements obtained by the MCP39F511A.

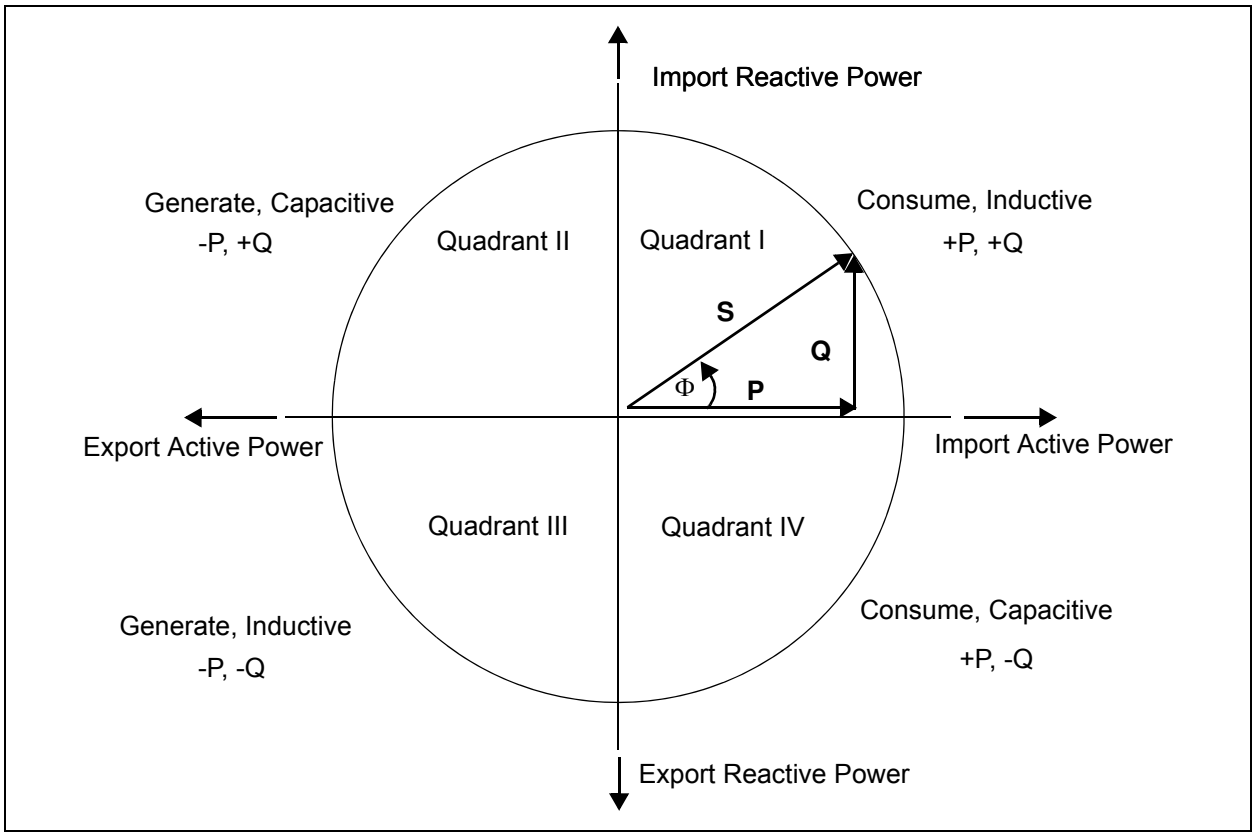


FIGURE 5-3: *The Power Circle and Triangle (S = Apparent, P = Active, Q = Reactive).*