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MCP39F511N

Dual-Channel, Single-Phase Power-Monitoring IC with Calculation

Features

- Power Monitoring of Two Loads with accuracy of 0.5% across 4000:1 Dynamic Range
- Built-in Calculations on Fast 16-Bit Processing Core:
  - Active, Reactive, Apparent Power
  - True RMS Current, RMS Voltage
  - Line Frequency, Power Factor
- 64-bit Wide Import and Export Active Energy Accumulation Registers Per Channel
- 64-bit Four Quadrant Reactive Energy Accumulation Registers Per Channel
- Signed Active and Reactive Power Outputs
- Dedicated Zero Crossing Detection (ZCD) Pin Output with Less than 200 µs Latency
- Dedicated PWM Output Pin with Programmable Frequency and Duty Cycle
- Automatic Event Pin Control through Fast Voltage Surge Detection
  - Less than 5 ms Delay
- Two-Wire Serial Protocol with Selectable Baud Rate up to 115.2 kbps using Universal Asynchronous Receiver/Transmitter (UART)
- Fast Calibration Routines and Simplified Command Protocol
- 512 Bytes User-Accessible EEPROM through Page Read/Write Commands
- Low-Drift Internal Voltage Reference, 10 ppm/°C Typical
- 28-lead 5x5 QFN Package
- Extended Temperature Range: -40°C to +125°C

Applications

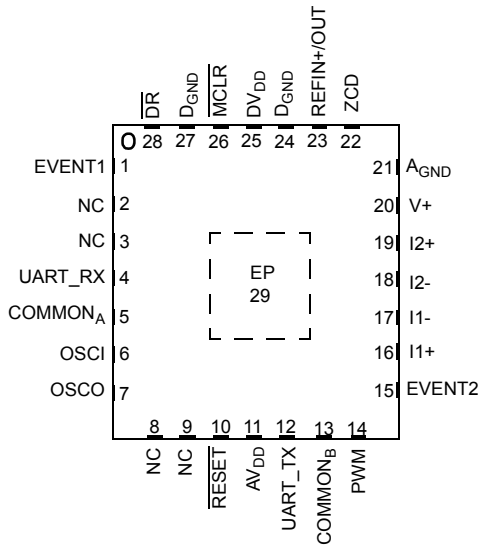
- Wall Socket (Dual Plug) Power Monitoring
- Power Monitoring for Home Automation
- Industrial Lighting Power Monitoring
- Real-Time Measurement of Input Power for AC/DC Supplies
- Intelligent Power Distribution Units

Description

The MCP39F511N is a highly integrated, complete dual-channel single-phase power-monitoring IC designed for real-time measurement of input power for dual-socket wall outlets, power strips, and consumer and industrial applications. It includes dual-channel 24-bit Delta-Sigma ADCs for dual-current measurements, a 10-bit SAR ADC for voltage measurement, a 16-bit calculation engine, EEPROM and a flexible two-wire interface. An integrated low-drift voltage reference with 10 ppm/°C in addition to 94.5 dB of SINAD performance on each measurement channel allows for better than 0.5% accurate designs across a 4000:1 dynamic range.

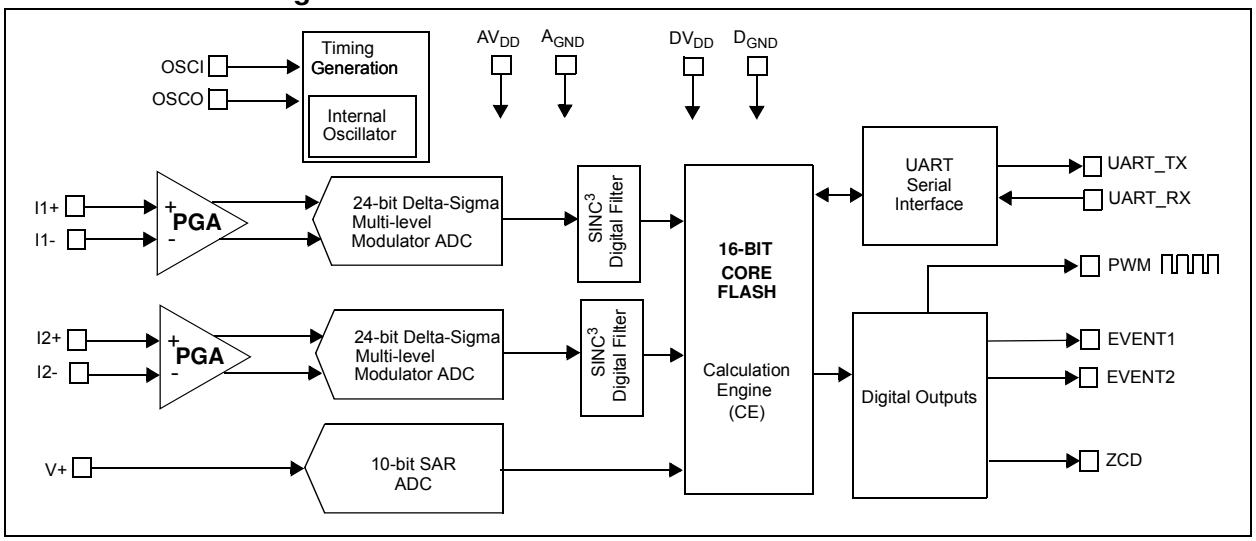
Package Types

MCP39F511N
5x5 QFN*

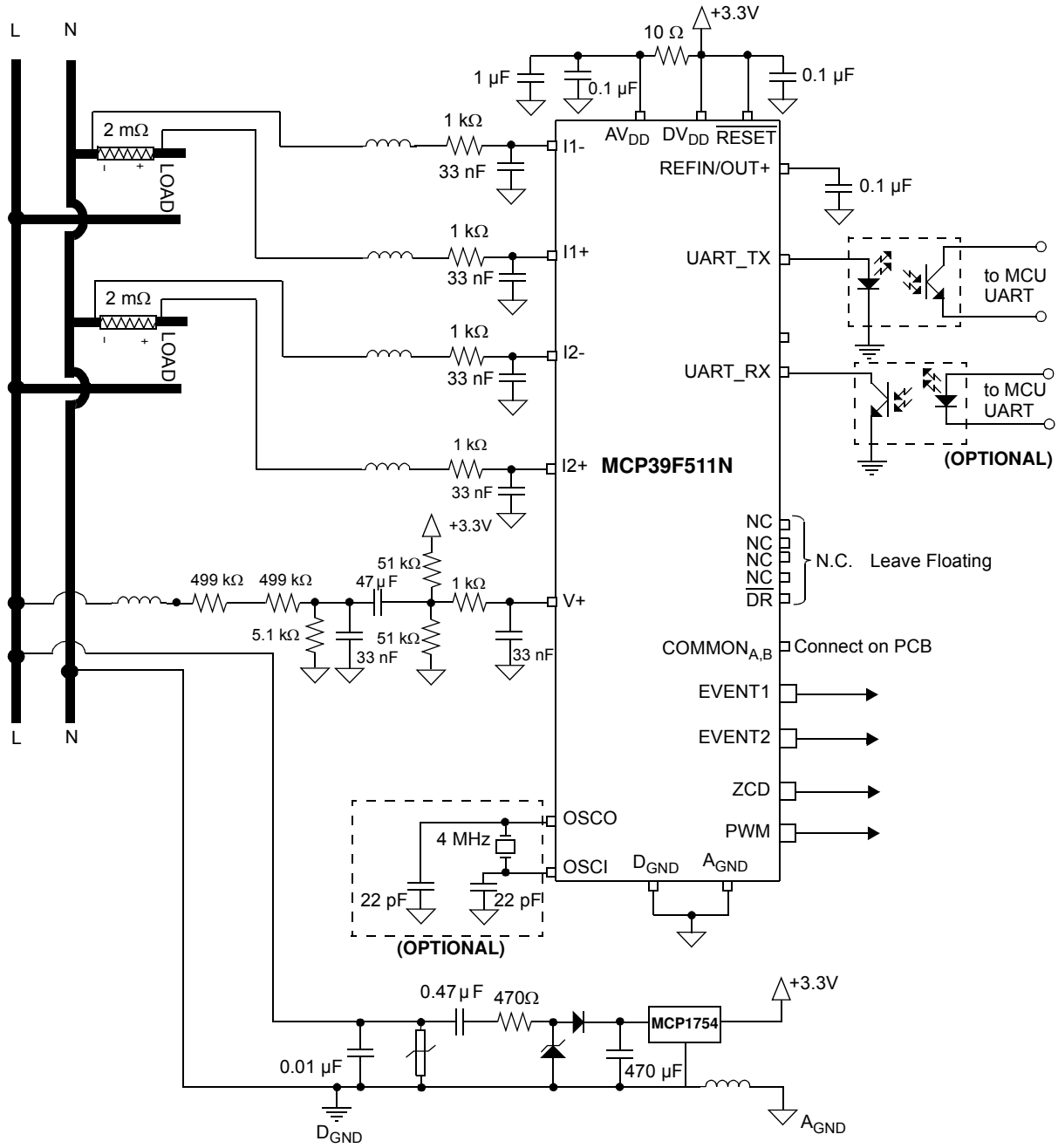


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



Typical Application



Note: The external sensing components shown here, the 2 mΩ shunts, two 499 kΩ and 5.1 kΩ resistor for the 200:1 voltage divider, are specifically chosen to match the default values for the calibration registers defined in **Section 6.0 "Register Descriptions"**. By choosing low-tolerance components of these values (e.g. 1% tolerance), measurement accuracy in the 2-3% range can be achieved with zero calibration. See **Section 9.0 "MCP39F511N Calibration"** for more information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} ..... -0.3 to +4.5V
AV_{DD} ..... -0.3 to +4.0V
Digital inputs and outputs w.r.t. A_{GND} ..... -0.3V to +4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} ..... -2V to +2V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin ..... 300 mA
Maximum Current into DV_{DD} pin ..... 250 mA
Maximum Output Current Sunk by Digital IO ..... 25 mA
Maximum Current Sourced by Digital IO ..... 25 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) ..... 4.0 kV, 200V
ESD on all other pins (HBM,MM) ..... 4.0 kV, 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Measurement						
Active Power (**Note 1**)	P	—	±0.5	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Reactive Power (**Note 1**)	Q	—	±0.5	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Apparent Power (**Note 1**)	S	—	±1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Current RMS (**Note 1**)	I_{RMS}	—	±1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Voltage RMS (**Note 1**)	V_{RMS}	—	±1	—	%	4000:1 Dynamic Range on Voltage Channel (**Note 2**)
Power Factor (**Note 1**)	Φ	—	±1	—	%	
Line Frequency (**Note 1**)	LF	—	±1	—	%	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x ($1/f_{LINE}$)	—	ms	**Note 3**
Minimum Time for Voltage Surge/Sag Detection	t_{AC_SASU}	—	see **Section 7.0**	—	ms	**Note 4**
24-Bit Delta-Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (I2+ – I2-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	**Note 5**
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	**Note 6**
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	**Note 6**
Signal-to-Noise Ratio	SNR	92	95	—	dB	**Note 6**
Spurious Free Dynamic Range	SFDR	—	111	—	dB	**Note 6**
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + 0.6V_{PP}, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.0 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
10-Bit SAR ADC Performance for Voltage Measurement						
Resolution	N_R	—	10	—	bits	
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	DV_{DD} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Nonlinearity	I_{NL}	—	±1	±2	LSb	
Differential Nonlinearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Clock and Timings						
UART Baud Rate	UDB	1.2	—	115.2	kbps	See **Section 3.2** for protocol details
Master Clock and Crystal Frequency	f_{MCLK}	-2%	8	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40°C to +85°C only (**Note 7**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	
Temperature Coefficient	TCV_{REF}	—	10	—	ppm/°C	T_A = -40°C to +85°C, V_{REFEXT} = 0
Output Impedance	$Z_{OUT}V_{REF}$	—	2	—	kΩ	
Current, V_{REF}	$AI_{DD}V_{REF}$	—	40	—	µA	
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.3V	V	
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
DV_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0 – 3.3V in 0.1s, 0 – 2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-on Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms
Operating Current	I_{DD}	—	15	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	Years	Provided no other specifications are violated
Supply Current during Programming	I_{DDPD}	—	7	—	mA	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 DV_{DD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
		—	0.050	0.100	µA	Digital Output pins only (ZCD, PWM, EVENT1, EVENT2)

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistance						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	36.9	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz, channel 1 or channel 2.

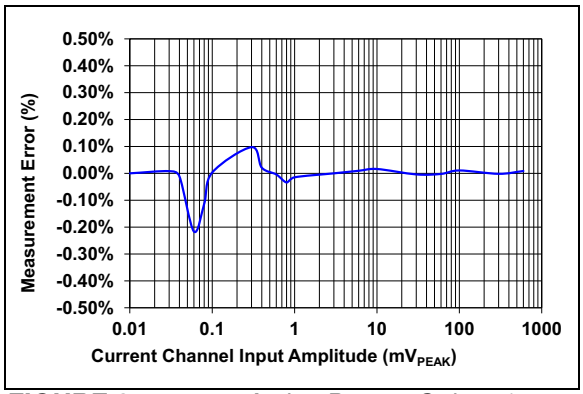


FIGURE 2-1: *Active Power, Gain = 1.*

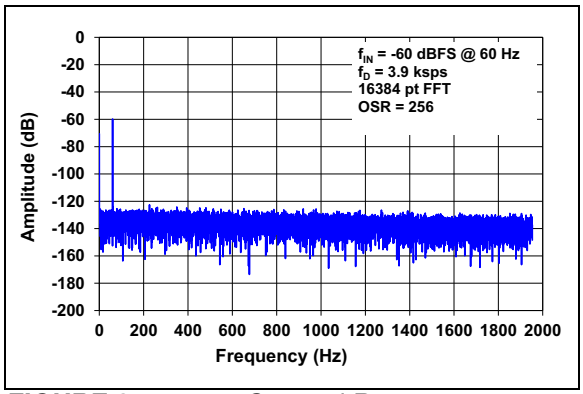


FIGURE 2-4: *Spectral Response.*

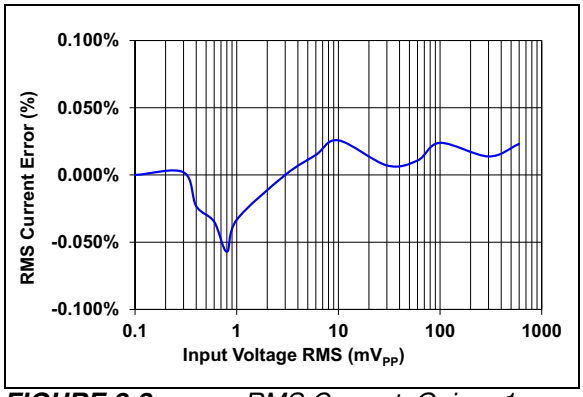


FIGURE 2-2: *RMS Current, Gain = 1.*

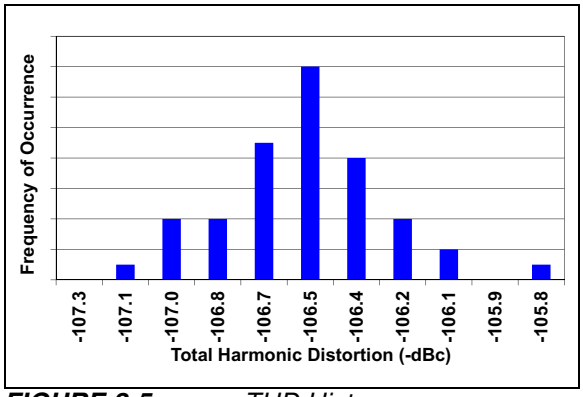


FIGURE 2-5: *THD Histogram.*

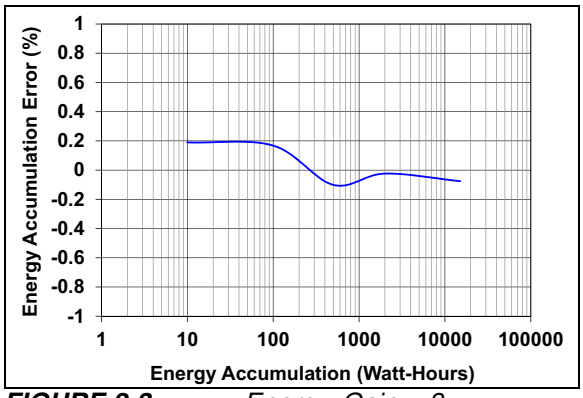


FIGURE 2-3: *Energy, Gain = 8.*

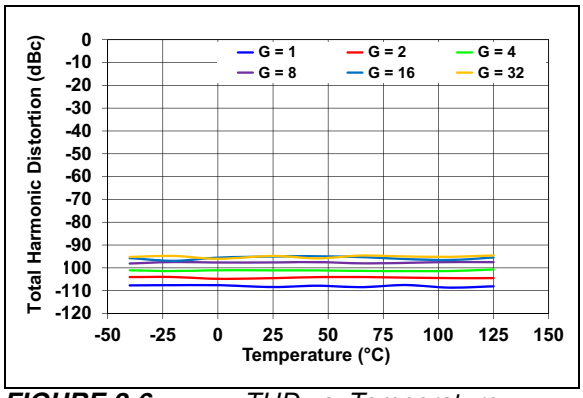


FIGURE 2-6: *THD vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz, channel 1 or channel 2.

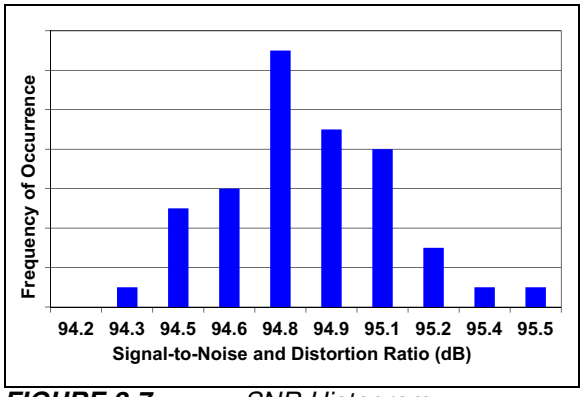


FIGURE 2-7: *SNR Histogram.*

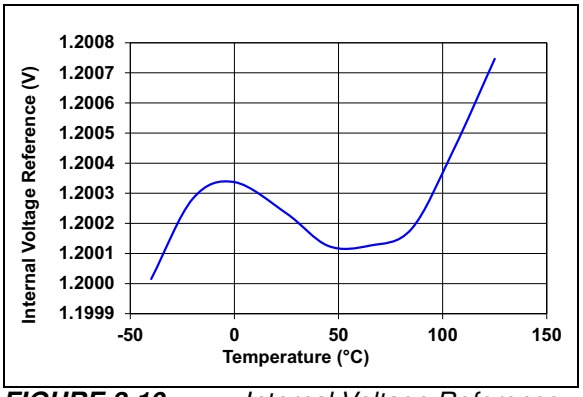


FIGURE 2-10: *Internal Voltage Reference vs. Temperature.*

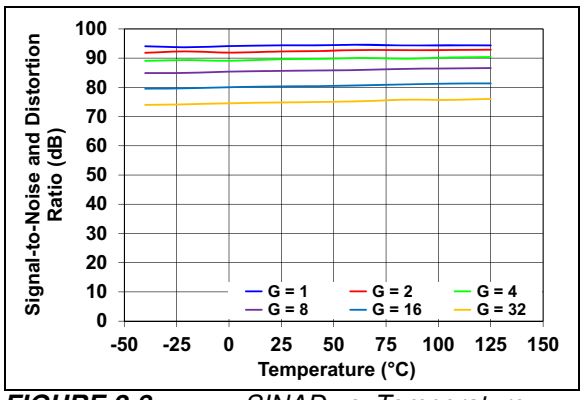


FIGURE 2-8: *SINAD vs. Temperature.*

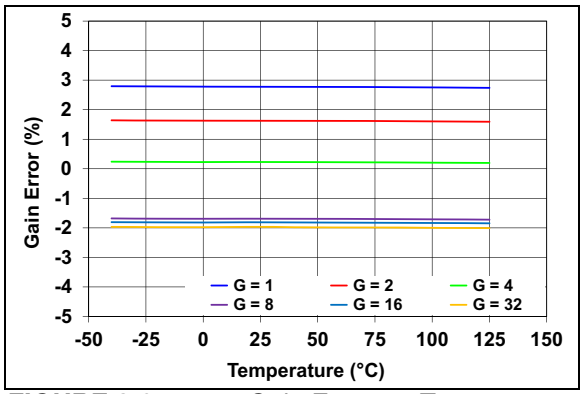


FIGURE 2-9: *Gain Error vs. Temperature.*

3.0 PIN DESCRIPTION

The pin descriptions are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F511N 5x5 QFN	Symbol	Function
1	EVENT1	Event 1 Output pin
2, 3, 8, 9	NC	No Connect (must be left floating)
4	UART_RX	UART Communication RX pin
5	$COMMON_A$	Common pin A, to be connected to pin 13 ($COMMON_B$)
6	OSCI	Oscillator Crystal Connection pin or External Clock Input pin
7	OSCO	Oscillator Crystal Connection pin
10	$\overline{RESET}$	Reset pin for Delta Sigma ADCs
11	AV_{DD}	Analog Power Supply pin
12	UART_TX	UART Communication TX pin
13	$COMMON_B$	Common pin B, to be connected to pin 5 ($COMMON_A$)
14	PWM	Pulse-Width Modulation (PWM) Output pin
15	EVENT2	Event 2 Output pin
16	I1+	Non-Inverting Current Channel 1 Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel 1 Input for 24-bit ΔΣ ADC
18	I2-	Inverting Voltage Channel 2 Input for 24-bit ΔΣ ADC
19	I2+	Non-Inverting Current Channel 2 Input for 24-bit ΔΣ ADC
20	V+	Non-Inverting Voltage Channel Input for 10-bit SAR ADC
21	A_{GND}	Analog Ground pin, return path for internal analog circuitry
22	ZCD	Zero Crossing Detection Output
23	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output pin
24, 27	D_{GND}	Digital Ground pin, return path for internal digital circuitry
25	DV_{DD}	Digital Power Supply pin
26	$\overline{MCLR}$	Master Clear for device
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to pins 24 and 27 (D_{GND}))

3.1 Event Output Pins (EVENTn)

These digital output pins can be configured to act as output flags based on various internal raise conditions. Control is modified through the Event Configuration register.

3.2 UART Communication Pins (UART_RX, UART_TX)

The MCP39F511N device contains an asynchronous full-duplex UART. The UART communication is eight bits with the Start and Stop bits. See **Section 4.3 "UART Settings"** for more information.

3.3 Common Pins (COMMON A and B)

The $COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F511N. These two pins should be connected together in the application.

3.4 Oscillator Pins (OSCI/OSCO)

OSCI and OSCO provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 8 MHz crystal can be connected to these pins. If a crystal or external clock source is not detected, the device will clock from the internal 8 MHz oscillator.

3.5 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the Delta-Sigma ADCs, PGA, internal V_{REF} and other blocks associated with the analog front-end in a Reset state when pulled low. This input is Schmitt-triggered.

3.6 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F511N.

This pin requires appropriate bypass capacitors and should be maintained to 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.7 Pulse-Width Modulator (PWM)

This digital output is a dedicated PWM output that can be controlled through the PWM Frequency and PWM Duty-Cycle Registers. See **Section 8.0 "Pulse-Width modulation (PWM)"** for more information.

3.8 24-Bit Delta Sigma ADC Differential Current Channel Input Pins (I1+/I1-/I2+/I2-)

(I1-, I1+), (I2-, I2+) are the two fully-differential current-channel pair inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.9 Voltage Analog Input (V+)

This is the non-inverting input to the SAR ADC for voltage measurement input. This input is used as the voltage measurement for both channel 1 and channel 2. Care should be taken to limit the voltage input here to within 300 mV of D_{GND}. DC offset of $DV_{DD}/2$ and approximately 1 V_{RMS} AC input signal.

3.10 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground pin is available on the PCB, it is recommended that this pin be tied to that plane.

3.11 Zero Crossing Detection (ZCD)

This digital output pin is the output of the zero crossing detection circuit of the IC. The output here will be a logic output with edges that transition at each zero crossing of the voltage channel input. For more information see **Section 5.10 "Zero Crossing Detection (ZCD)"**.

3.12 Non-Inverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for the delta sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.13 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry components in the system.

3.14 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F511N. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.15 Data Ready Pin ($\overline{DR}$)

The Data Ready pin indicates if a new Delta-Sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the Data Ready pin to indicate the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with the line frequency to ensure an integer number of samples for each line cycle.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.16 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to D_{GND}.

NOTES:

4.0 COMMUNICATION PROTOCOL

All communication to the device occurs in frames. Each frame consists of a header byte, the number of bytes in the frame, a command packet (or command packets) and a checksum. It is important to note that the maximum number of bytes in either a Receive or Transmit frame is 35.

Note: If a custom communication protocol is desired, please contact a Microchip sales office.

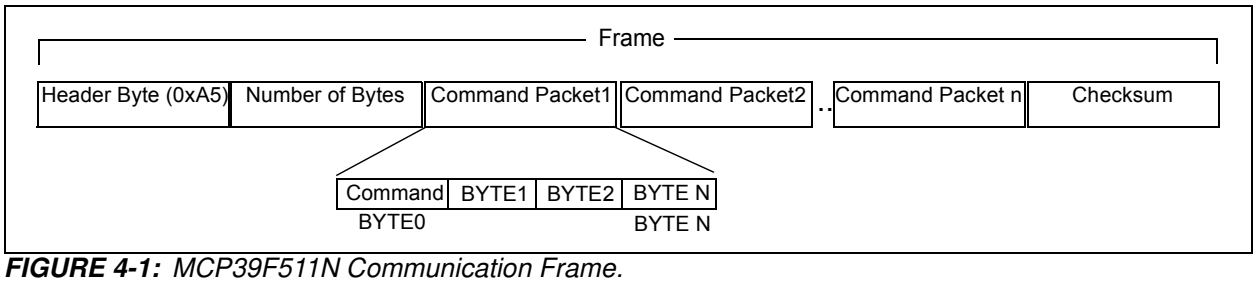


FIGURE 4-1: *MCP39F511N Communication Frame.*

This approach allows for single, secure transmission from the host processor to the MCP39F511N with either a single command or multiple commands. No command in a frame is processed until the entire frame is complete and the checksum and number of bytes are validated.

The number of bytes in an individual *command packet* depends on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

4.1 Device Responses

After the reception of a communication frame, the MCP39F511N has three possible responses, which are returned with or without data, depending on the frame received. These responses are either:

- Acknowledge (ACK, 0x06): Frame received with success, commands understood and commands executed with success.
- Negative Acknowledge (NAK, 0x15): Frame received with success, however commands not executed with success, commands not understood or some other error in the command bytes.
- Checksum Fail (CSFAIL, 0x51): Frame received with success, however the checksum of the frame did not match the bytes in the frame.

Note: There is one unique device ID response which is used to determine which MCP39FXXX device is present: [NAK(0x15) + ID_BYTE].
If the device is interrogated with 0x5A, i.e. it receives 0x5A as the first byte instead of the standard 0xA5 first header byte, a special NAK is returned followed by an ID_BYTE. For the MCP39F511N the ID_BYTE is 0x03.

4.2 Checksum

The checksum is generated using simple byte addition and taking the modulus to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and the number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F511N will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F511N, the frame and checksum are created in the same way, with the header byte becoming an Acknowledge (0x06). Communication examples are given in **Section 4.5 "Example Communication Frames and MCP39F511N Responses"**.

4.3 UART Settings

The default baud rate is 115.2 kbps and can be changed using the UART bits in the System Configuration Register. Note that the baud rate is changed only at system power-up, so when changing the baud rate, a `Save To Flash` command followed by a power-on cycle is required.

The UART operates in 8-bit mode, plus one start bit and one stop bit, for a total of 10 bits per byte, as shown in Figure 4-1.

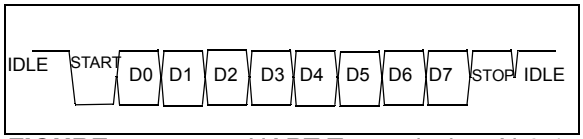


FIGURE 4-1: *UART Transmission, N-8-1.*

4.4 Command List

The following table is a list of all accepted command bytes for the MCP39F511N. There are 10 possible accepted commands for the MCP39F511N.

TABLE 4-1: MCP39F511N INSTRUCTION SET

Command #	Command	Command ID	Instruction Parameter	Number of bytes	Successful Response UART_TX
1	Register Read, N bytes	0x4E	Number of bytes	2	ACK, Data, Checksum
2	Register Write, N bytes	0x4D	Number of bytes	1+N	ACK
3	Set Address Pointer	0x41	ADDRESS	3	ACK
4	Save Registers To Flash	0x53	None	1	ACK
5	Page Read EEPROM	0x42	PAGE	2	ACK, Data, Checksum
6	Page Write EEPROM	0x50	PAGE	18	ACK
7	Bulk Erase EEPROM	0x4F	None	1	ACK
8	Auto-Calibrate Gain	0x5A	Channel Selection (1)	**Note 2**	
9	Auto-Calibrate Reactive Gain	0x7A	Channel Selection (1)	**Note 2**	
10	Auto-Calibrate Frequency	0x76	None	**Note 2**	

Note 1: Each bit in the instruction parameter byte refers to the corresponding channel that is being calibrated with the command. For example, if bits 0 and 1 are high, both channels 1 and 2 will be calibrated. A NAK or ACK will be returned. If a NAK is returned, refer to the Calibration Status bits in the Event Configuration Register for more information.

2: See **Section 9.0 "MCP39F511N Calibration"** for more information on calibration.

4.5 Example Communication Frames and MCP39F511N Responses

Tables 4-2 to 4-11 show exact hexadecimal communication frames as they are recommended to be sent to the MCP39F511N from the system MCU. The values here can be used as direct examples for writing the code to communicate to the MCP39F511N.

TABLE 4-2: REGISTER READ, N BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x08	Number of Bytes in Frame	
3	0x41	Command (Set Address Pointer)	
4	0x00	Address High	
5	0x02	Address Low	
6	0x4E	Command (Register Read, N Bytes)	
7	0x20	Number of Bytes to Read (32)	
8	0x5E	Checksum	ACK + Number of Bytes (35) + 32 bytes + Checksum

Note 1: This example Register Read, N bytes frame, as it is written here, can be used to poll a subset of the output data, starting at the top, address 0x02, and reading 32 data bytes back or 35 bytes total in the frame.

TABLE 4-3: REGISTER WRITE, N- BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x17	Number of Bytes in Frame (23)	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0xB1	Address Low	
6	0x4D	Command (`Register Write, N Bytes`)	
7	0x0F	Number of Bytes to Write (15)	
8-22	*Data*	Data Bytes (15 total data bytes)	
23	Checksum	Checksum	ACK

Note 1: This `Register Write, N Bytes` frame, as shown here, is writing channel 1 range and calibration target values, starting at address 0xB1 (the second byte in the Channel 1 Range register) and then writing 15 bytes of data to consecutive addresses to complete the setup of channel 1 registers prior to calibration. Note these are not the calibration registers, but the calibration targets which need to be written prior to issuing the auto-calibration target commands. See **Section 9.0 "MCP39F511N Calibration"** for more information.

TABLE 4-4: SET ADDRESS POINTER COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x06	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0xEE	Checksum	ACK

Note 1: The `Set Address Pointer` command is typically included inside of a frame that includes a read or write command, as shown in Tables 4-2 and 4-3. There is typically no reason for this command to have its own frame, but is shown here as an example.

TABLE 4-5: SAVE TO FLASH COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x53	Command (`Save To Flash`)	
4	0xFC	Checksum	ACK

TABLE 4-6: PAGE READ EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x42	Command (`Page Read EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5	0xED	Checksum	ACK + EEPROM Page Data + Checksum

TABLE 4-7: PAGE WRITE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x15	Number of Bytes in Frame	
3	0x50	Command (`Page Write EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5-20	*Data*	EEPROM Data (16 bytes/Page)	
21	Checksum	Checksum	ACK

TABLE 4-8: BULK ERASE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x4F	Command (`Bulk Erase EEPROM`)	
4	0xF8	Checksum	ACK

TABLE 4-9: AUTO-CALIBRATE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x5A	Command (`Auto-Calibrate Gain`)	
4	0x03	Instruction Parameter (Channel Instruction, calibrate both channels 1 and 2)	
5	0x07	Checksum	ACK (or NAK if unable to calibrate)(1)

Note 1: See **Section 9.0 "MCP39F511N Calibration"** for more information.

TABLE 4-10: AUTO-CALIBRATE REACTIVE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x7A	Command (`Auto-Calibrate Reactive Gain`)	
4	0x01	Instruction Parameter (Channel Instruction, calibrate channel 1 only)	
5	0x25	Checksum	ACK (or NAK if unable to calibrate)(1)

Note 1: See **Section 9.0 "MCP39F511N Calibration"** for more information.

TABLE 4-11: AUTO-CALIBRATE FREQUENCY COMMAND

Byte #	Value	Description	Response from
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x76	Command (`Auto-Calibrate Frequency`)	
4	0x1F	Checksum	ACK (or NAK if unable to calibrate)(1)

Note 1: See **Section 9.0 "MCP39F511N Calibration"** for more information.

4.6 Command Descriptions

4.6.1 REGISTER READ, N BYTES (0x4E)

The `Register Read, N Bytes` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other read commands. An Acknowledge, Data and Checksum is the response for this command. The maximum number of bytes that can be read with this command is 32. If there are other read commands within a frame, the maximum number of bytes that can be read is 32 minus the number of bytes being read in the frame. With this command, the data is returned LSB first.

4.6.2 REGISTER WRITE, N BYTES (0x4D)

The `Register Write, N Bytes` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other write commands. An Acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 32. If there are other write commands within a frame, the maximum number of bytes that can be written is 32 minus the number of bytes being written in the frame. With this command, the data is written LSB first.

4.6.3 SET ADDRESS POINTER (0x41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes: Address High Byte followed by Address Low Byte. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an Acknowledge will be returned.

4.6.4 SAVE REGISTERS TO FLASH (0x53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to flash. This includes all R/W registers in the register set. The response to this command is an Acknowledge.

4.6.5 PAGE READ EEPROM (0x42)

The `Page Read EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F511N. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an Acknowledge, 16-bytes of data and CRC Checksum.

4.6.6 PAGE WRITE EEPROM (0x50)

The `Page Write EEPROM` command is expecting 17 additional bytes in the command parameters, which are the EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. The response to this command is an Acknowledge.

4.6.7 BULK ERASE EEPROM (0x4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. The response to this command is Acknowledge.

4.6.8 AUTO-CALIBRATE GAIN (0x5A)

The `Auto-Calibrate Gain` command initiates the single-point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and Active power based on the target values written in the corresponding registers. The instruction parameter for this command selects if you are calibrating channel 1, 2 or both. Bit 0 corresponds to channel 1 and bit 1 corresponds to channel 2. See **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration. The response to this command is Acknowledge.

4.6.9 AUTO-CALIBRATE REACTIVE POWER GAIN (0x7A)

The `Auto-Calibrate Reactive Gain` command initiates a single-point calibration to match the measured Reactive power to the target Reactive power. The instruction parameter for this command selects if you are calibrating channel 1, 2, or both. Bit 0 corresponds to channel 1 and bit 1 corresponds to channel 2. This is typically done at PF = 0.5. See section **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration.

4.6.10 AUTO-CALIBRATE FREQUENCY (0x76)

For applications not using an external crystal and running the MCP39F511N off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency register is set such that the frequency indication matches what is set in the Line Frequency Reference register. See **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration.

4.7 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F511N:

TABLE 4-12: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
`u64`	Unsigned, 64-bit register
`u32`	Unsigned, 32-bit register
`s32`	Signed, 32-bit register
`u16`	Unsigned, 16-bit register
`s16`	Signed, 16-bit register
`b32`	32-bit register containing discrete Boolean bit settings

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F511N uses a coherent sampling algorithm to phase lock the sampling rate to the line frequency on the voltage channel input with an integer number of samples per line cycle, and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the power outputs.

There are two separate computation paths, using two currents from two separate channels (channel 1 and channel 2) referenced below as I_N and V. Therefore each current, power, and energy output is duplicated, one for each calculation channel.

In addition, there are duplicate calibration registers (offset, gain, phase, etc.) for each calculation channel.

5.1.1 LINE FREQUENCY

The coherent sampling algorithm is also used to calculate the Line Frequency Output register, which is updated every computation cycle. The correction factor for line frequency measurement is the Gain Line Frequency register which is used during the line frequency calibration (see section **Section 9.6.1 "Using the `Auto-Calibrate Frequency` Command"**. Note that the resolution of the Line Frequency Output register is fixed, and the resolution is 1 mHz.

5.2 Accumulation Interval Parameter

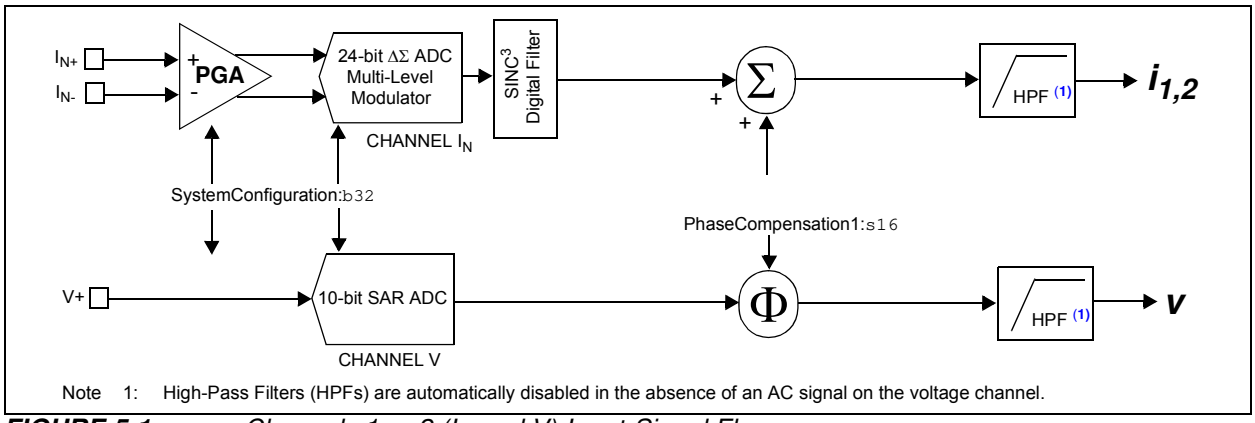
The accumulation interval is defined as a 2^N number of line cycles, where N is the value in the Accumulation Interval Parameter register. This is identical for both calculation channels.

5.3 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F511N is shown in Figure 5-1. All conditions set in this diagram affect all of the output registers (RMS current, RMS voltage, Active power, Reactive power, apparent power, etc.). The gain of the PGA, the Shutdown and Reset status of the 24-bit ADCs are all controlled through the System Configuration Register.

To compensate for any external phase error between the current and voltage channels, the Phase Compensation register can be used.

See **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration.



Note 1: High-Pass Filters (HPFs) are automatically disabled in the absence of an AC signal on the voltage channel.

FIGURE 5-1: *Channels 1 or 2 (I_N and V) Input-Signal Flow.*

5.4 RMS Current, RMS Voltage and Apparent Power (S)

The MCP39F511N device provides true RMS measurements. The MCP39F511N device has two simultaneous sampling 24-bit A/D converters for the current measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$

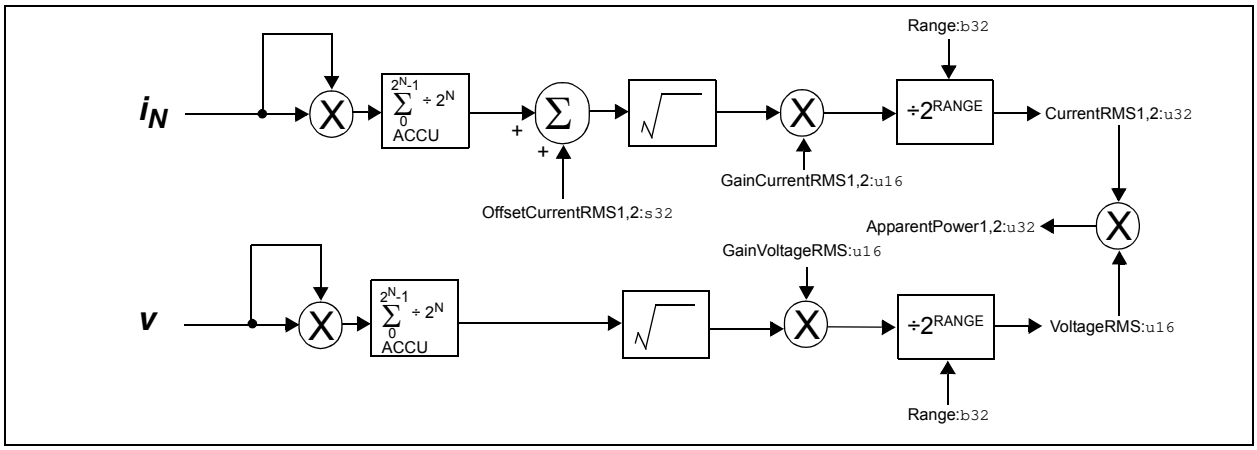


FIGURE 5-2: *RMS Current (Channel 1 or 2), Apparent Power (Channel 1 and 2) and Voltage Calculation Signal Flow.*

5.4.1 APPARENT POWER (S)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER (S)

$$S = I_{RMS} \times V_{RMS}$$

5.4.2 APPARENT POWER DIVISOR DIGITS

The registers AppPowerDivisorDigits1 and AppPowerDivisorDigits2 are configurable by the user depending on the precision of the RMS indications and the desired precision for ApparentPower1 or ApparentPower2.

Because AppPowerDivisorDigits registers can be higher than 4, it may result in a 32-bit divisor. To improve the speed of this part of the calculation engine, a method that uses only multiplications and right-bit shifts was implemented. Therefore the following equation applies:

EQUATION 5-3: APPARENT POWER (S)

$$ApparentPower = \frac{I_{RMS} \times V_{RMS}}{10^{AppPowerDivisorDigits}}$$

5.5 Power and Energy

The MCP39F511N offers signed power numbers for Active and Reactive power, import and export registers for active energy, and four-quadrant Reactive power measurement. For this device, import power or energy is considered positive (power or energy being consumed by the load), and export power or energy is considered negative (power or energy being delivered by the load). The following figure represents the measurements obtained by the MCP39F511N.

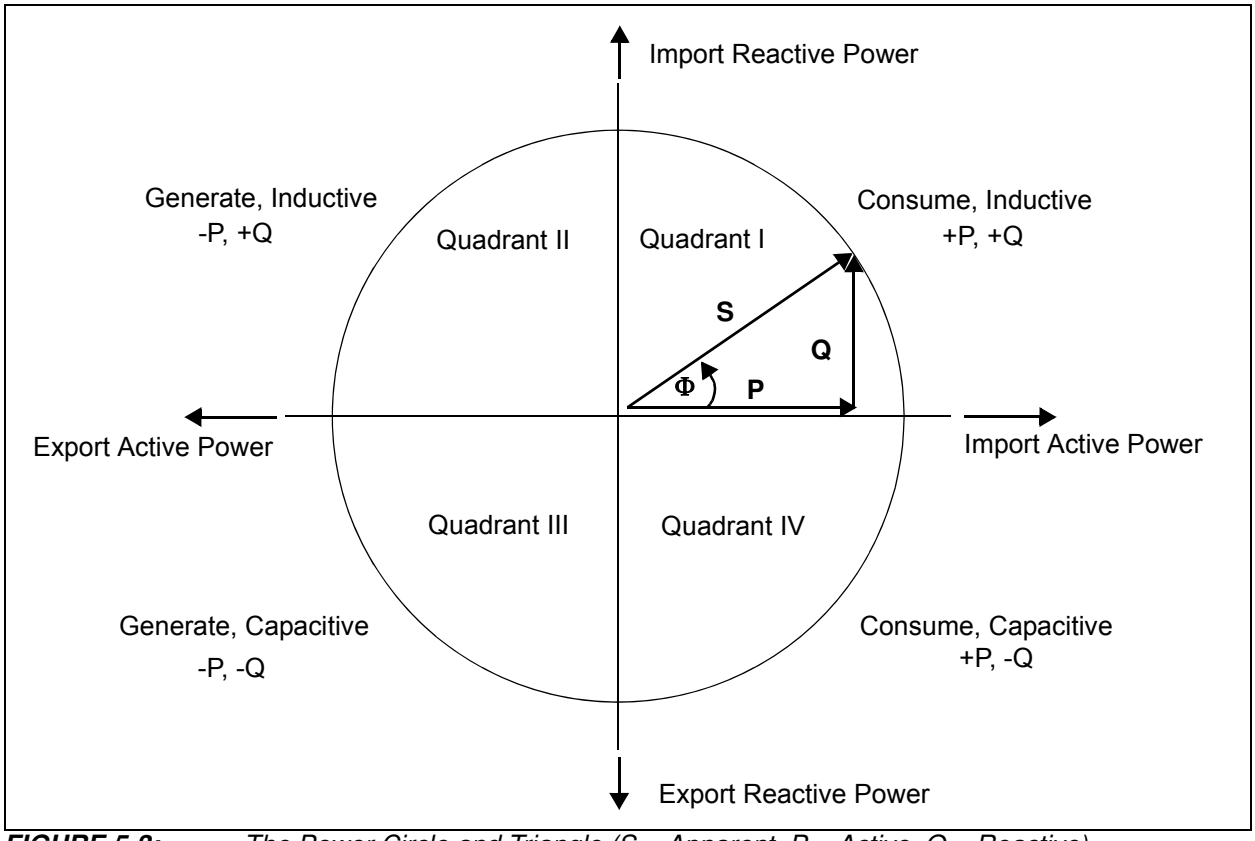


FIGURE 5-3: *The Power Circle and Triangle (S = Apparent, P = Active, Q = Reactive).*

5.6 Energy Accumulation

Energy accumulation for all four energy registers (import/export, active/reactive) occurs at the end of each computation cycle if the energy accumulation has been turned on. See **Section 6.5 "System Configuration Register"** for the energy-control bits. The accumulation of energy occurs in one of eight 64-bit energy counters, four for each channel (import and export counters for both Active and Reactive power).

5.6.1 NO-LOAD THRESHOLD

The no-load threshold is set by modifying the value in the No-Load Threshold register. The unit for this register is power with a default resolution of 0.01W. The default value is 100 or 1.00W. Any power that is below 1W will not be accumulated into any of the energy registers.

For scaling of the Apparent power indication, the calculation engine uses the Apparent Power Divisor register. This is described in the following register operations, per Equation 5-4.

EQUATION 5-4: APPARENT POWER (S)

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{ApparentPowerDivisor}}$$

5.7 Active Power (P)

The MCP39F511N has three simultaneous sampling A/D converters monitoring two individual currents and two individual active powers. For the Active Power calculations, the instantaneous currents and voltage are multiplied together to create instantaneous power. This instantaneous power is then converted to Active Power by averaging or calculating the DC component.

Equation 5-5 controls the number of samples used in this accumulation prior to updating the Active Power output register.

Please note that although this register is unsigned, the direction of the Active power (import or export) can be determined by the Active Power Sign bit located in the System Status Register.

EQUATION 5-5: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

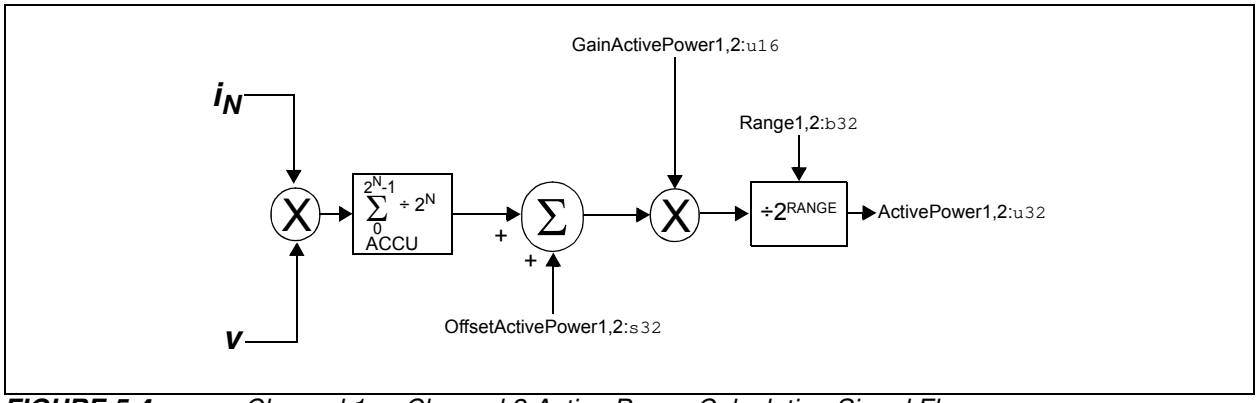


FIGURE 5-4: *Channel 1 or Channel 2 Active Power Calculation Signal Flow.*

5.8 Power Factor (PF)

Power factor is calculated by the ratio of P to S, or Active power divided by Apparent power.

EQUATION 5-6: POWER FACTOR

$$PF = \frac{P}{S}$$

The Power Factor Reading is stored in two signed 16-bit registers (Power Factor), one for each channel. This register is a signed, two's complement register with the MSB representing the polarity of the power factor. Positive power factor means import power, negative power factor means export power. The sign of the Reactive power component can be used to determine if the load is inductive (positive) or capacitive (negative).

Each LSB is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.9 Reactive Power (Q)

In the MCP39F511N, Reactive Power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with Active power where ACCU acts as the accumulator. Any light load or residual power can be removed by using the Offset Reactive Power register. Gain is corrected by the Gain Reactive Power register. The final output is an unsigned 32-bit value located in the Reactive Power register.

Please note that although this register is unsigned, the direction of the power can be determined by the Reactive Power Sign bit in the System Status Register.

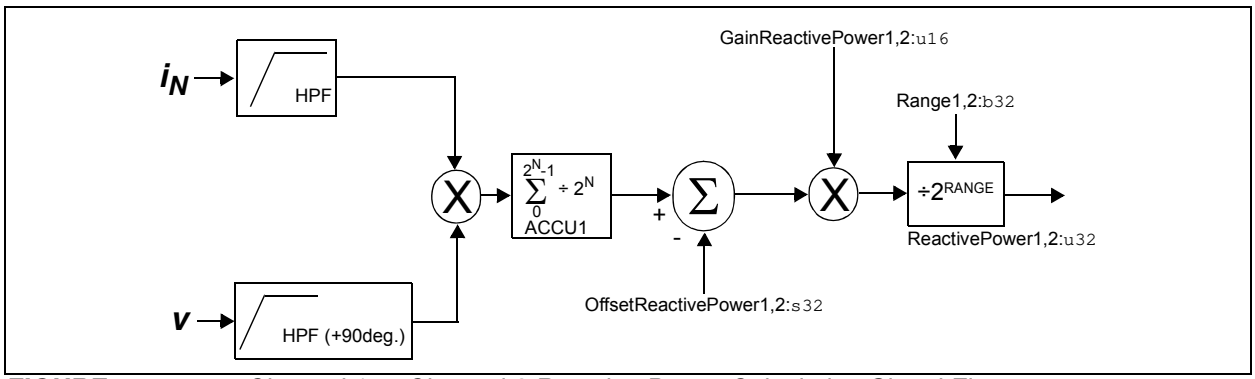


FIGURE 5-5: *Channel 1 or Channel 2 Reactive Power Calculation Signal Flow.*