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MCP39F521

I²C Power Monitor with Calculation and Energy Accumulation

Features

- Power Monitoring Accuracy Capable of 0.1% Error Across 4000:1 Dynamic Range
- Built-In Calculations on Fast 16-bit Processing Core
  - Active, Reactive, Apparent Power
  - True Root Mean Square (RMS) Current, RMS Voltage
  - Line Frequency, Power Factor
- 64-bit Wide Import and Export Active Energy Accumulation Registers
- 64-bit Four Quadrant Reactive Energy Accumulation Registers
- Signed Active and Reactive Power Outputs
- Dedicated Zero Crossing Detection (ZCD) Pin Output with Less than 100 µs Latency
- Automatic Event Pin Control through Fast Voltage Surge Detection, Less than 5 ms Delay
- I²C Interface, up to 400 kHz Clock Rate
- Two Independent Registers for Minimum and Maximum Output Quantity Tracking
- Fast Calibration Routines and Simplified Command Protocol
- 512 Bytes User-Accessible EEPROM through Page Read/Write Commands
- Low-Drift Internal Voltage Reference, 10 ppm/°C Typical
- 28-lead 5 x 5 mm QFN Package
- Extended Temperature Range -40°C to +125°C

Applications

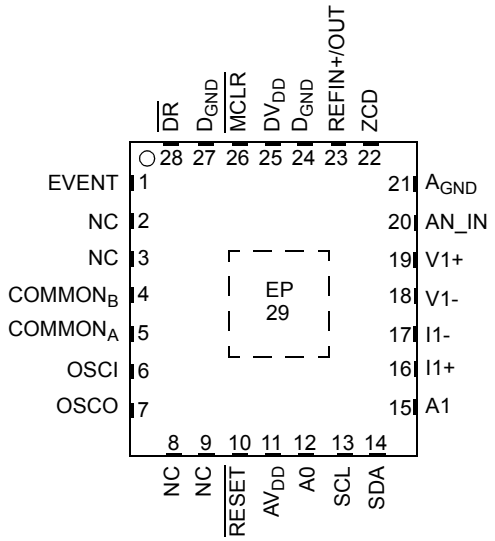
- Power Monitoring for Home Automation
- Industrial Lighting Power Monitoring
- Real-Time Measurement of Input Power for AC/DC Supplies
- Intelligent Power Distribution Units

Description

The MCP39F521 is a highly integrated, complete single-phase power-monitoring device, designed for real-time measurement of input power for AC/DC power supplies, power distribution units, consumer and industrial applications. It includes dual-channel delta-sigma ADCs, a 16-bit calculation engine, EEPROM and a flexible two-wire I²C interface. An integrated low-drift voltage reference with 10 ppm/°C in addition to 94.5 dB of signal-to-noise and distortion ratio (SINAD) performance on each measurement channel allows for better than 0.1% accurate designs across a 4000:1 dynamic range.

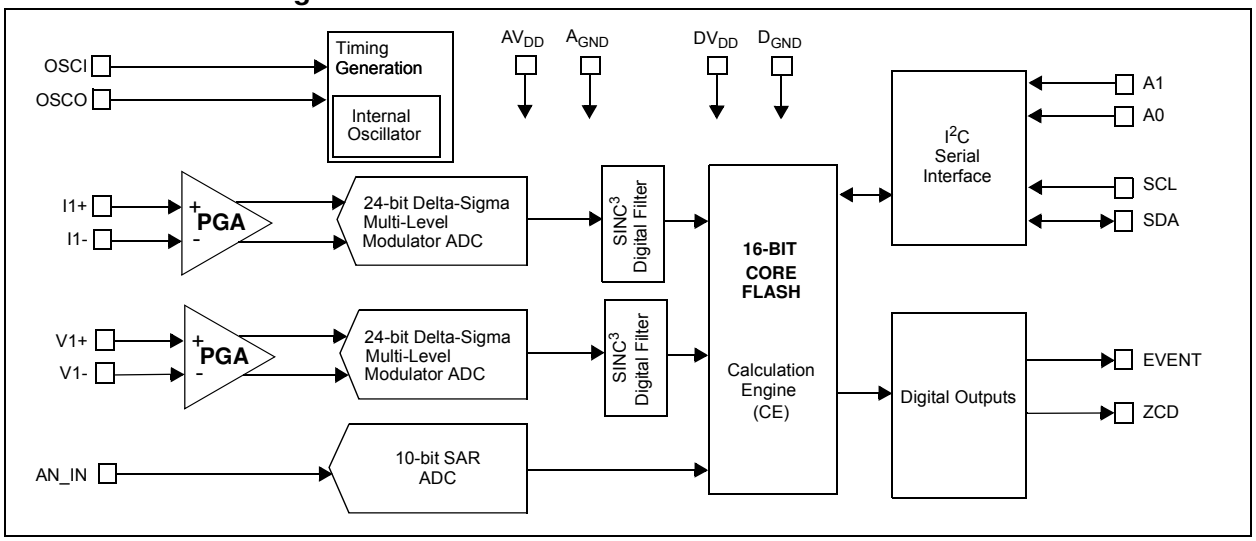
Package Types

MCP39F521
5x5 QFN*

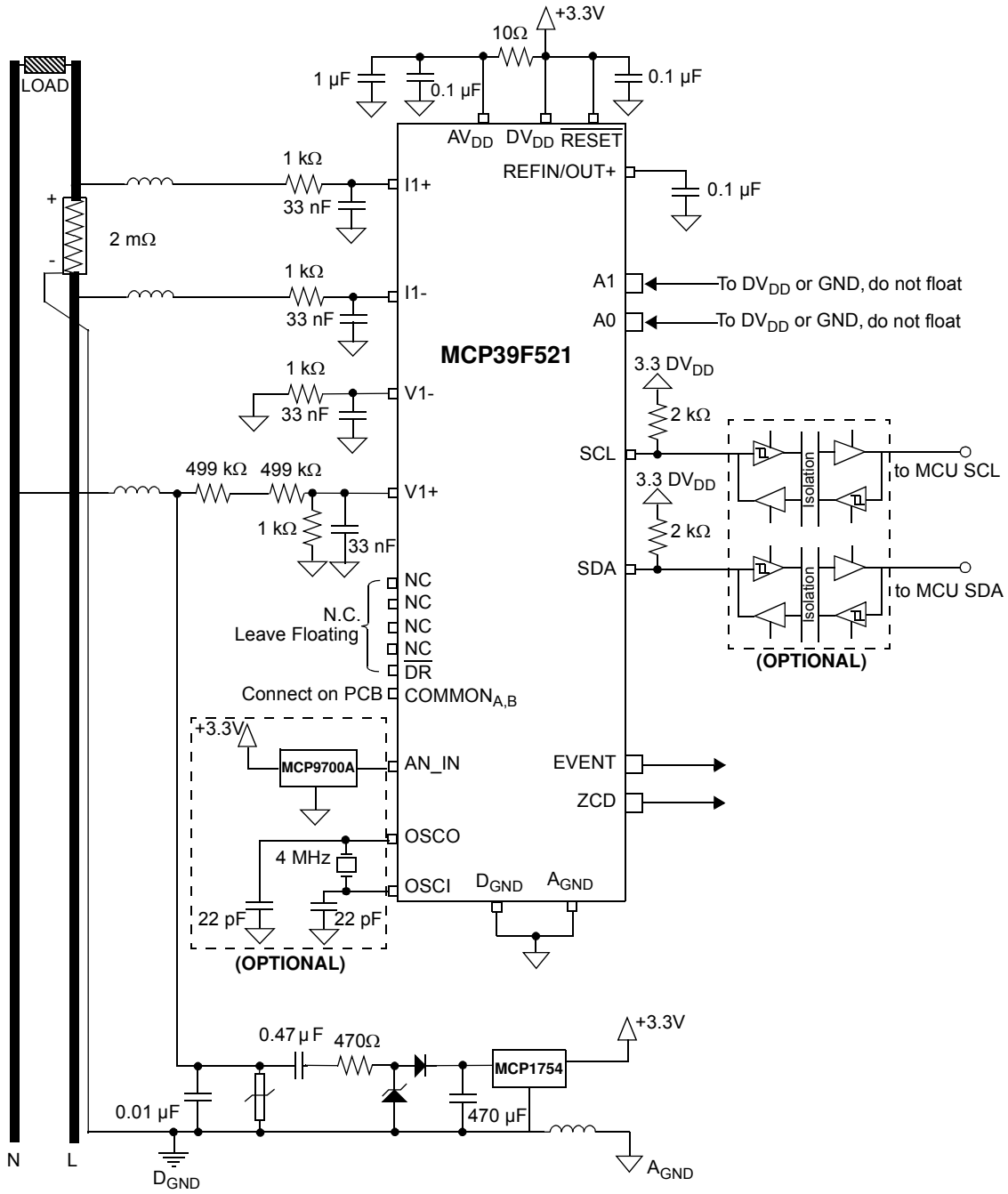


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



MCP39F521 Typical Application – Single-Phase, Two-Wire Application Schematic



Note: The external sensing components shown here, a 2 mΩ shunt, two 499 kΩ and 1 kΩ resistors for the 1000:1 voltage divider, are specifically chosen to match the default values for the calibration registers defined in **Section 6.0, Register Descriptions**. By choosing low-tolerance components of these values (e.g. 1% tolerance), measurement accuracy in the 2-3% range can be achieved with zero calibration. See **Section 8.0, MCP39F521 Calibration** for more information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} ..... -0.3 to +4.5V
AV_{DD} ..... -0.3 to +4.0V
Digital inputs and outputs w.r.t. A_{GND} ..... -0.3V to +4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} ..... -2V to +2V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin ..... 300 mA
Maximum Current into DV_{DD} pin ..... 250 mA
Maximum Output Current Sunk by Digital IO ..... 25 mA
Maximum Current Sourced by Digital IO ..... 25 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) ..... 4.0 kV, 200V
ESD on all other pins (HBM,MM) ..... 4.0 kV, 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Measurement						
Active Power (**Note 1**)	P	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Reactive Power (**Note 1**)	Q	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Apparent Power (**Note 1**)	S	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Current RMS (**Note 1**)	I_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Voltage RMS (**Note 1**)	V_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Voltage Channel (**Note 2**)
Power Factor (**Note 1**)	Φ	—	±0.1	—	%	
Line Frequency (**Note 1**)	LF	—	±0.1	—	%	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.
2: Specification by design and characterization; not production tested.
3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.
4: Applies to Voltage Sag and Voltage Surge events only.
5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.
6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.
7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x ($1/f_{LINE}$)	—	ms	**Note 3**
Minimum Time for Voltage Surge/Sag Detection	t_{AC_SASU}	—	see **Section 7.0**	—	ms	**Note 4**
24-Bit Delta-Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (V1+ – V1-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	**Note 5**
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	**Note 6**
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	**Note 6**
Signal-to-Noise Ratio	SNR	92	95	—	dB	**Note 6**
Spurious Free Dynamic Range	SFDR	—	111	—	dB	**Note 6**
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + $0.6V_{PP}$, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.

6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
10-Bit SAR ADC Performance for Temperature Measurement						
Resolution	N_R	—	10	—	bits	
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	D_{VDD} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Nonlinearity	I_{NL}	—	±1	±2	LSb	
Differential Nonlinearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Temperature Measurement Rate		—	$f_{LINE}/2^N$	—	sps	**Note 3**
Clock and Timings						
I^2C Clock Frequency	f_{SCL}	—	—	400	kHz	100 kHz and 400 kHz I^2C modes supported
Master Clock and Crystal Frequency	f_{MCLK}	-2%	4	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40 to +85°C only (**Note 7**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	
Temperature Coefficient	TCV_{REF}	—	10	—	ppm/°C	T_A = -40°C to +85°C, V_{REFEXT} = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	
Current, V_{REF}	$AI_{DD}V_{REF}$	—	40	—	µA	
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.3V	V	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.

6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	
DV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0 – 3.3V in 0.1s, 0 – 2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power On Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms
Operating Current	I_{DD}	—	13	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	Years	Provided no other specifications are violated
Supply Current during Programming	I_{DDPD}	—	7	—	mA	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0, Typical Performance Curves** for typical performance.

6: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and I^2C only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 DV_{DD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
		—	0.050	0.100	µA	Digital Output pins only (ZCD, EVENT)

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	36.9	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

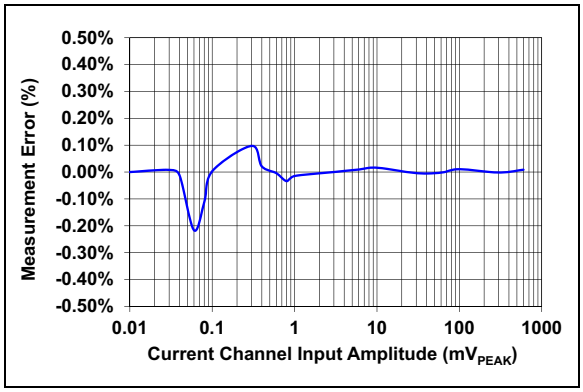


FIGURE 2-1: *Active Power, Gain = 1.*

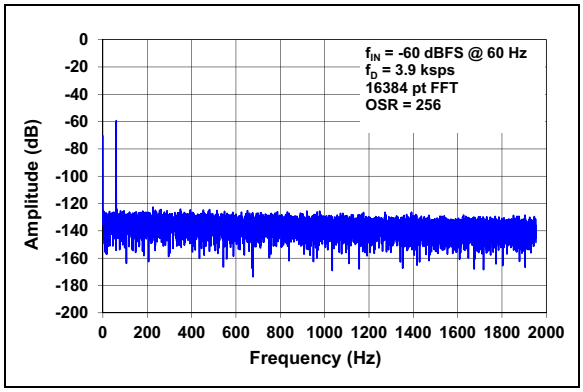


FIGURE 2-4: *Spectral Response.*

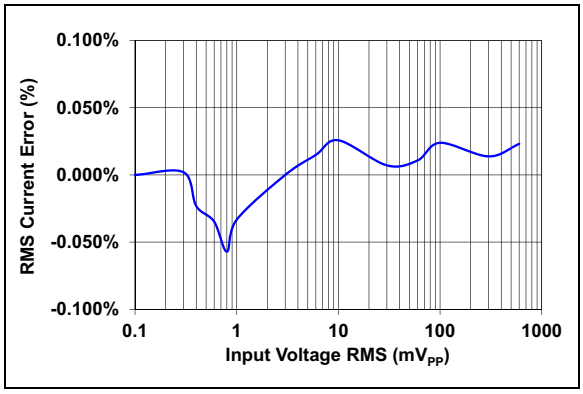


FIGURE 2-2: *RMS Current, Gain = 1.*

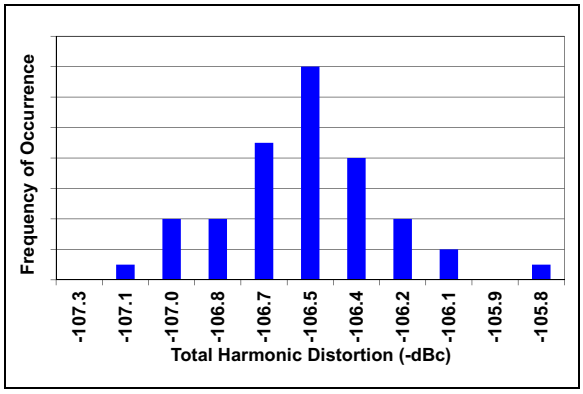


FIGURE 2-5: *THD Histogram.*

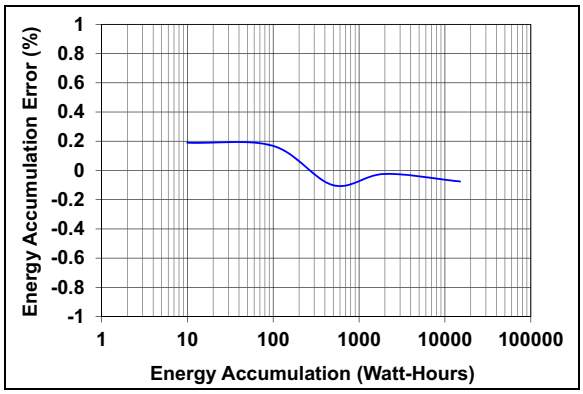


FIGURE 2-3: *Energy, Gain = 8.*

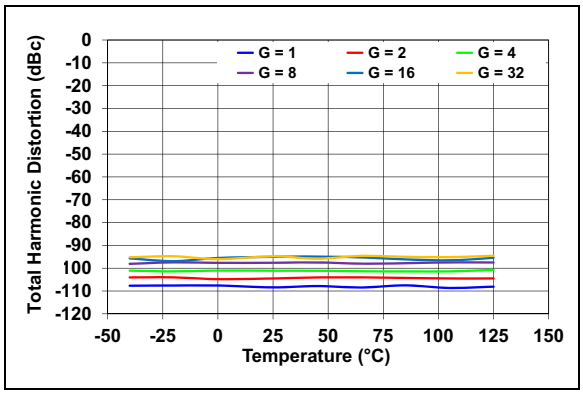


FIGURE 2-6: *THD vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

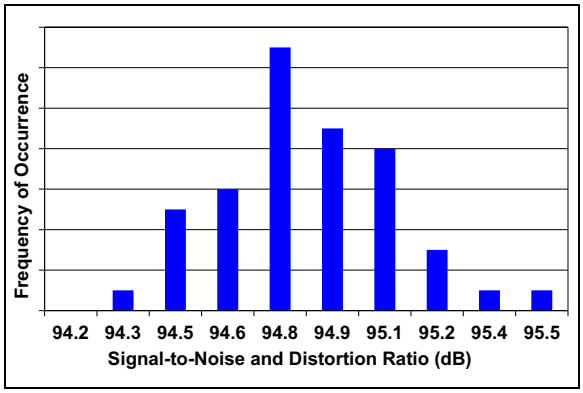


FIGURE 2-7: *SNR Histogram.*

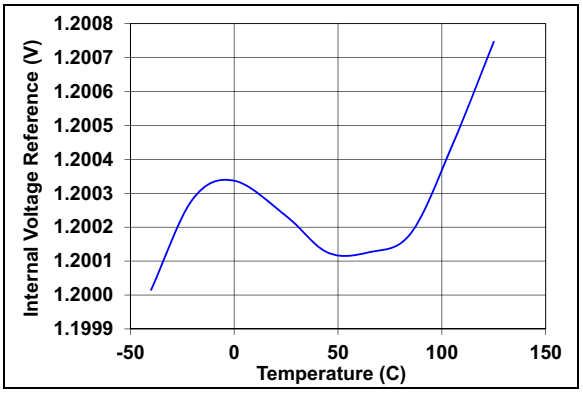


FIGURE 2-10: *Internal Voltage Reference vs. Temperature.*

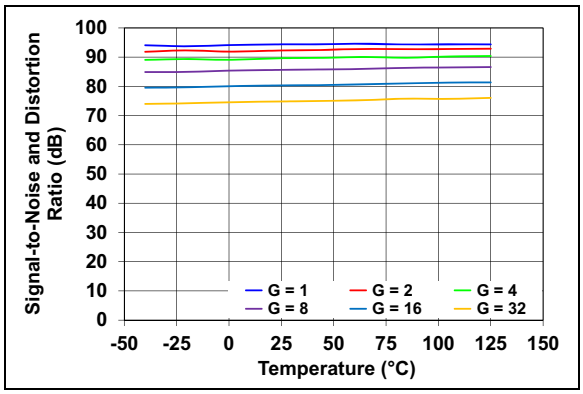


FIGURE 2-8: *SINAD vs. Temperature.*

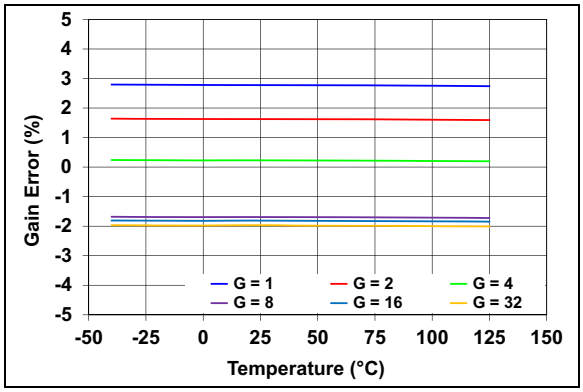


FIGURE 2-9: *Gain Error vs. Temperature.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F521 5x5 QFN	Symbol	Function
1	EVENT	Event Output Pin
2, 3, 8, 9	NC	No Connect (must be left floating)
4	$COMMON_B$	Common pin B, to be connected to $COMMON_A$
5	$COMMON_A$	Common pin A, to be connected to $COMMON_B$
6	OSCI	Oscillator Crystal Connection Pin or External Clock Input Pin
7	OSCO	Oscillator Crystal Connection Pin
10	$\overline{RESET}$	Reset Pin for Delta Sigma ADCs
11	AV_{DD}	Analog Power Supply Pin
12	A0	I^2C Address Select Pin A0
13	SCL	I^2C Serial Clock
14	SDA	I^2C Serial Data
15	A1	I^2C Address Select Pin A1
16	I1+	Noninverting Current Channel Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel Input for 24-bit ΔΣ ADC
18	V1-	Inverting Voltage Channel Input for 24-bit ΔΣ ADC
19	V1+	Noninverting Voltage Channel Input for 24-bit ΔΣ ADC
20	AN_IN	Analog Input for SAR ADC
21	A_{GND}	Analog Ground Pin, Return Path for internal analog circuitry
22	ZCD	Zero Crossing Detection Output
23	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output Pin
24, 27	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
25	DV_{DD}	Digital Power Supply Pin
26	$\overline{MCLR}$	Master Clear for Device
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to D_{GND})

3.1 Event Output Pin (EVENT)

This digital output pin can be configured to act as an output flag based on various internal raise conditions. Control is modified through the Event Configuration register.

3.2 Common Pins ($COMMON_A$ and $COMMON_B$)

The $COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F521. These two pins should be connected together in the application.

3.3 Oscillator Pins (OSCI/OSCO)

OSCI and OSCO provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 4 MHz crystal can be connected to these pins. If a crystal of external clock source is not detected, the device will clock from the internal 4 MHz oscillator.

3.4 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the delta-sigma ADCs, PGA, internal V_{REF} and other blocks associated with the analog front-end in a Reset state when pulled low. This input is Schmitt-triggered.

3.5 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F521.

This pin requires appropriate bypass capacitors and should be maintained to 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.6 Chip Address Inputs (A0, A1)

The A0 and A1 inputs are used by the MCP39F521 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four devices may be connected to the same bus by using different combinations. These inputs must be connected to V_{DD} or GND and cannot be left floating.

In most applications, the chip address inputs are hardwired to logic 0 or logic 1. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic 0 or logic 1 before normal device operation can proceed.

3.7 I^2C Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.8 I^2C Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to DV_{DD} (typical 10kΩ for 100kHz, 2kΩ for 400kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Change during SCL high is reserved for indicating the Start and Stop conditions.

3.9 24-Bit Delta Sigma ADC Differential Current Channel Input Pins (I1+/I1-)

I1- and I1+ are the two fully-differential current channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.10 24-Bit Delta Sigma ADC Differential Voltage Channel Inputs (V1-/V1+)

V1- and V1+ are the two fully-differential voltage channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each V_N+/- input pin is ±1V with no distortion and ±2V, with no breaking after continuous voltage.

3.11 Analog Input (AN_IN)

This is the input to the analog-to-digital converter that can be used for temperature measurement and compensation. If temperature compensation is required in the application, it is advised to connect the low-power active thermistor IC MCP9700A to this pin. If temperature compensation is not required, this can be used as a general purpose analog-to-digital converter input.

3.12 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground pin is available on the PCB, it is recommended that this pin be tied to that plane.

3.13 Zero Crossing Detection (ZCD)

This digital output pin is the output of the Zero Crossing Detection circuit of the IC. The output here will be a logic output with edges that transition at each zero crossing of the voltage channel input. For more information see **Section 5.13, Zero Crossing Detection (ZCD)**.

3.14 Noninverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for the delta sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.15 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.16 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F521. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.17 Data Ready Pin ($\overline{DR}$)

The data ready pin indicates if a new delta-sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the Data Ready pin to indicate that the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with the line frequency to ensure an integer number of samples for each line cycle.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.18 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to D_{GND}.

NOTES:

4.0 COMMUNICATION PROTOCOL

The I^2C communication protocol is a frame-based protocol, with a complete communication frame occurring between the I^2C start and stop bits.

A command frame is a write transmission from the I^2C master to the MCP39F521 device.

A read response frame is read transmission from the I^2C master to the MCP39F521.

Each command frame consists of a header byte, the number of bytes in the frame, command packet (or command packets) and a checksum.

Each response frame consists of either a ACK, NAK, CSFAIL, or ACK+Data with checksum.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

4.1 COMMUNICATION FRAMES

The following two figures represent the command frames and read request frames.

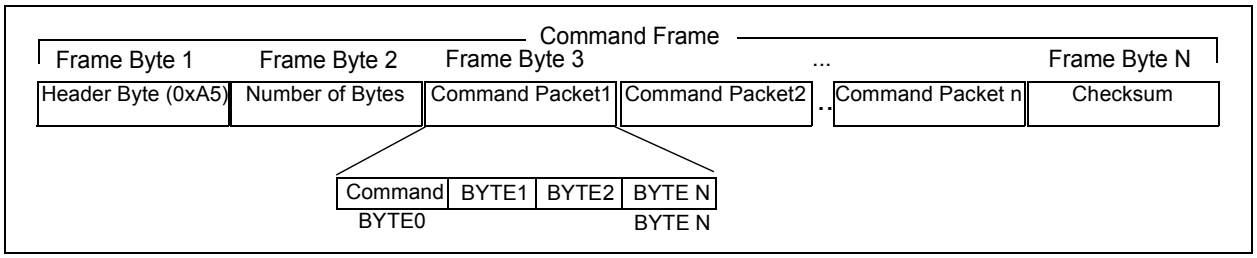


FIGURE 4-1: *MCP39F521 Command Write Frame.*

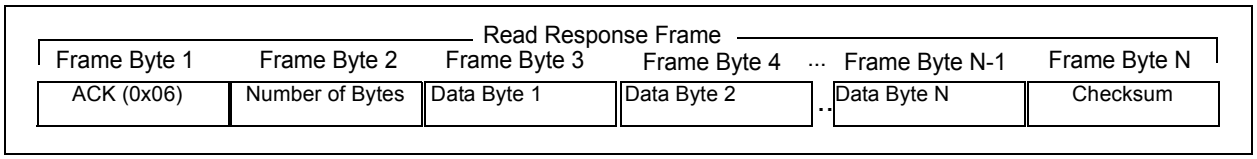


FIGURE 4-2: *MCP39F521 Read Response Frame (ACK with Data).*

The following two figures represent I^2C command frame writes and read frame responses.

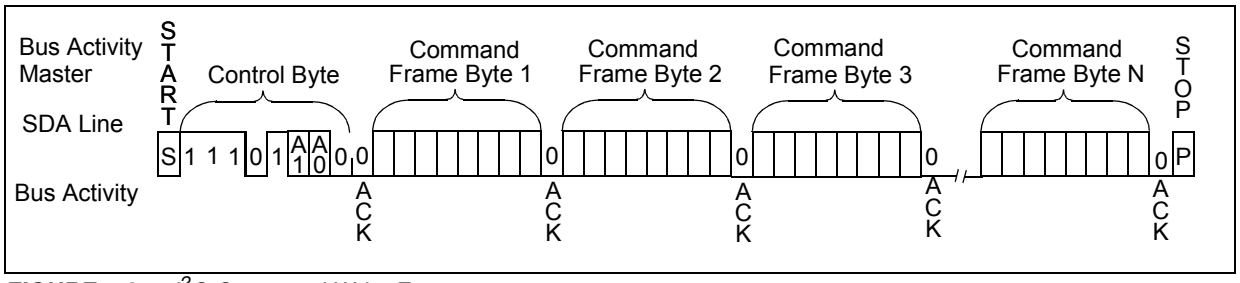


FIGURE 4-3: *I^2C Command Write Frame.*

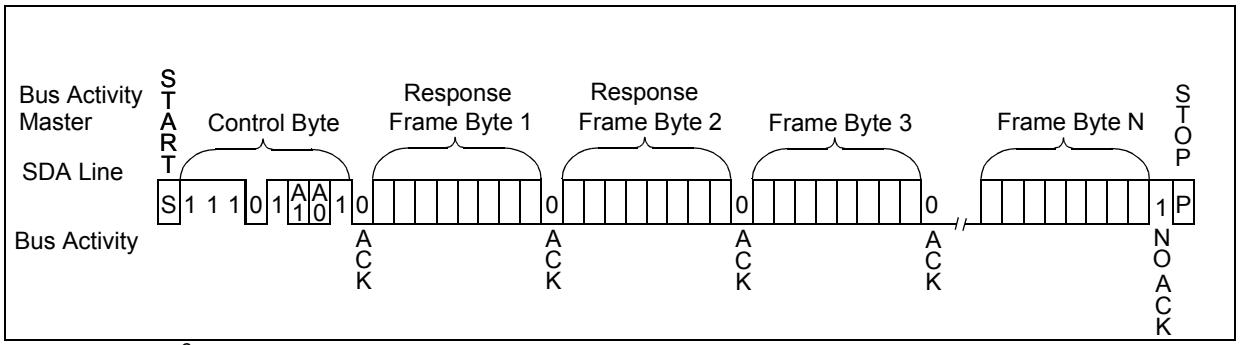


FIGURE 4-4: *I^2C Read Response Frame.*

This approach allows for single, secure transmission from the host processor to the MCP39F521 with either a single command, or multiple commands. No command in a frame is processed until the frame is complete and the checksum and number of bytes are validated after the stop bit.

The number of bytes in an individual *command packet* depends on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

4.2 I²C CONTROL BYTE

A Control byte is the first byte received following the Start condition from the master device. The Control byte consists of a 4-bit control code. For the MCP39F521 the control code is '1110' for all read and write operations. The following three bits are chip-select address bits, A2, A1, and A0. For the MCP39F521, A2 is always set to binary '1'. A1 and A0 are controlled by the logic pins A1 and A0, which allows up to 4 different devices on the I²C bus.

The last bit of the Control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected.

Following a Start condition, the MCP39F521 monitors the SDA bus checking for the 4-bit control code ('1110') and proper address bits. Upon receiving the correct control code and address bits, the slave (MCP39F521) outputs an acknowledge signal on the SDA line, and depending on the state of the R/W bit, will either respond with data or wait to receive additional bytes prior to the Stop condition. The Control byte is defined in the following figure.

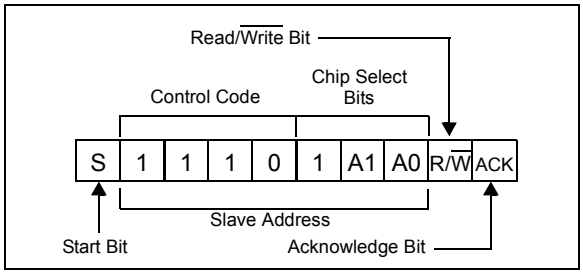


FIGURE 4-5: *MCP39F521 Control Byte Format.*

4.3 I²C Time Out and Clock Stretching

Time out is when an I²C slave resets its interface if the I²C clock is low for longer than a specified time. The MCP39F521 offers a set 2 ms I²C time out that can be disabled through the Time-out Disable bit in the System Configuration Register (Register 6-2).

In addition, the device includes a clock stretching feature which allows the master to know when a frame has been processed. Clock stretching is when a slave device can not cooperate with the clock speed or needs to slow down the bus. In the case of the MCP39F521, after a frame is received, the device will hold the clock low until the frame has been processed. The maximum clock stretching duration is less than 10 milliseconds.

4.4 Checksum

The checksum is generated using simple byte addition and taking the modulus to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F521 will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F521, the frame and checksum are created in the same way, with the header byte becoming an acknowledge (0x06). Communication examples are given in **Section 4.6, Example Communication Frames and MCP39F521 Responses**.

4.5 Command List

The following table is a list of all accepted command bytes for the MCP39F521. There are **10** possible accepted commands for the MCP39F521.

TABLE 4-1: MCP39F521 INSTRUCTION SET

Command #	Command	Command ID	Instruction Parameter	Number of Bytes	Successful Response
1	`Register Read, N bytes`	0x4E	Number of Bytes	2	ACK, Data, Checksum
2	`Register Write, N bytes`	0x4D	Number of Bytes	1+N	ACK
3	`Set Address Pointer`	0x41	ADDRESS	3	ACK
4	`Save Registers To Flash`	0x53	None	2	ACK
5	`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, Checksum
6	`Page Write EEPROM`	0x50	PAGE	18	ACK
7	`Bulk Erase EEPROM`	0x4F	None	2	ACK
8	`Auto-Calibrate Gain`	0x5A	None	**Note 1**	
9	`Auto-Calibrate Reactive Gain`	0x7A	None	**Note 1**	
10	`Auto-Calibrate Frequency`	0x76	None	**Note 1**	

Note 1: See **Section 8.0, MCP39F521 Calibration** for more information on calibration.

4.6 Example Communication Frames and MCP39F521 Responses

Tables 4-2 to 4-11 show exact hexadecimal communication frames as they should be sent to the MCP39F521 from the system MCU. The values here can be used as direct examples for writing your code to communicate to the MCP39F521.

TABLE 4-2: REGISTER READ, N BYTES COMMAND (Note 1)

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x08	Number of Bytes in Frame	
3	0x41	Command (Set Address Pointer)	
4	0x00	Address High	
5	0x02	Address Low	
6	0x4E	Command (`Register Read, N bytes`)	
7	0x20	Number of Bytes to Read (32)	
8	0x5E	Checksum	ACK + Number of Bytes (35) + 32 bytes, + Checksum

Note 1: This example `Register Read, N bytes` frame, as written here, can be used to poll a subset of the output data, starting at the top, address 0x02, and reading 32 data bytes back or 35 bytes total in the frame.

TABLE 4-3: REGISTER WRITE, N- BYTES COMMAND (Note 1)

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x25	Number of Bytes in Frame	
3	0x41	Command (Set Address Pointer)	
4	0x00	Address High	
5	0x48	Address Low	
6	0x4D	Command (`Register Write, N Bytes`)	
7	0x1C	Number of Bytes to Write (28)	
8-36	*Data*	Data Bytes (28 total data bytes)	
37	Checksum	Checksum	ACK

Note 1: This `Register Write, N Bytes` frame, as written here, can be used to write the entire set of calibration target data, starting at the top, address 0x7A, and continuing to write until the end of this set of registers, 28 bytes later, register 0x94. Note these are not the calibration registers, but the calibration targets which need to be written prior to issuing the auto-calibration target commands. See **Section 8.0, MCP39F521 Calibration** for more information.

TABLE 4-4: SET ADDRESS POINTER COMMAND (Note 1)

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x06	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0xEE	Checksum	ACK

Note 1: The `Set Address Pointer` command is typically included inside of a frame that includes a read or write command, as shown in Table 4-2 and Table 4-3. There is typically no reason for this command to have its own frame, but is shown here as an example.

TABLE 4-5: SAVE TO FLASH COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x53	Command (`Save To Flash`)	
4	0xFC	Checksum	ACK

TABLE 4-6: PAGE READ EEPROM COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x42	Command (`Page Read EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5	0xED	Checksum	ACK + EEPROM Page Data + Checksum

TABLE 4-7: PAGE WRITE EEPROM COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x15	Number of Bytes in Frame	
3	0x50	Command (`Page Write EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5-20	*Data*	EEPROM Data (16 bytes/Page)	
21	Checksum	Checksum	ACK

TABLE 4-8: BULK ERASE EEPROM COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x4F	Command (`Bulk Erase EEPROM`)	
4	0xF8	Checksum	ACK

TABLE 4-9: AUTO-CALIBRATE GAIN COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x5A	Command (`Auto-Calibrate Gain`)	
4	0x03	Checksum	ACK (or NAK if unable to calibrate), see **Section 8.0, MCP39F521 Calibration** for more information.

TABLE 4-10: AUTO-CALIBRATE REACTIVE GAIN COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x7A	Command (`Auto-Calibrate Reactive Gain`)	
4	0x23	Checksum	ACK (or NAK if unable to calibrate), see **Section 8.0, MCP39F521 Calibration** for more information.

TABLE 4-11: AUTO-CALIBRATE FREQUENCY COMMAND

Byte #	Value	Byte Description	Response from MCP39F521
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x76	Command (`Auto-Calibrate Frequency`)	
4	0x1F	Checksum	ACK (or NAK if unable to calibrate), see **Section 8.0, MCP39F521 Calibration** for more information.

4.7 Command Descriptions

4.7.1 REGISTER READ, N BYTES (0x4E)

The `Register Read, N bytes` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. The maximum number of bytes that can be read with this command is 32. If there are other read commands within a frame, the maximum number of bytes that can be read is 32 minus the number of bytes being read in the frame. With this command, the data is returned LSB first.

4.7.2 REGISTER WRITE, N BYTES (0x4D)

The `Register Write, N bytes` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other write commands. An acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 32. If there are other write commands within a frame, the maximum number of bytes that can be written is 32 minus the number of bytes being written in the frame. With this command, the data is written LSB first.

4.7.3 SET ADDRESS POINTER (0x41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes, address high byte followed by address low byte. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an acknowledge will be returned.

4.7.4 SAVE REGISTERS TO FLASH (0x53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to flash. This includes all R/W registers in the register set. The response to this command is an acknowledge.

4.7.5 PAGE READ EEPROM (0x42)

The `Read Page EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F521. A more complete description of the memory organization of the EEPROM can be found in **Section 9.0, EEPROM**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an acknowledge, 16-bytes of data and CRC checksum.

4.7.6 PAGE WRITE EEPROM (0x50)

The `Page Write EEPROM` command is expecting 17 additional bytes in the command parameters, which are the EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 9.0, EEPROM** The response to this command is an acknowledge.

4.7.7 BULK ERASE EEPROM (0x4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 9.0, EEPROM**. The response to this command is acknowledge.

4.7.8 AUTO-CALIBRATE GAIN (0x5A)

The `Auto-Calibrate Gain` command initiates the single-point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and active power based on the target values written in the corresponding registers. See **Section 8.0, MCP39F521 Calibration** for more information on device calibration. The response to this command is acknowledge.

4.7.9 AUTO-CALIBRATE REACTIVE GAIN (0X7A)

The `Auto-Calibrate Reactive Gain` command initiates a single-point calibration to match the measured reactive power to the target reactive power. This is typically done at PF = 0.5. See section **Section 8.0, MCP39F521 Calibration** for more information on device calibration.

4.7.10 AUTO-CALIBRATE FREQUENCY (0x76)

For applications not using an external crystal and running the MCP39F521 off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency (0x00AE) register is set such that the frequency indication matches what is set in the Line Frequency Reference (0x0094) register. See **Section 8.0, MCP39F521 Calibration** for more information on device calibration.

4.8 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F521:

TABLE 4-12: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
u64	Unsigned, 64-bit register
u32	Unsigned, 32-bit register
s32	Signed, 32-bit register
u16	Unsigned, 16-bit register
s16	Signed, 16-bit register
b32	32-bit register containing discrete Boolean bit settings

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F521 uses a coherent sampling algorithm to phase lock the sampling rate to the line frequency with an integer number of samples per line cycle, and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the output power quantities.

5.2 Accumulation Interval Parameter

The accumulation interval is defined as an 2^N number of line cycles, where N is the value in the Accumulation Interval Parameter register.

5.3 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F521 is shown in Figure 5-1. All conditions set in this diagram effect all of the output registers (RMS current, RMS voltage, active power, reactive power, apparent power, etc.). The gain of the PGA, the Shutdown and Reset status of the 24-bit ADCs are all controlled through the System Configuration register (Register 6-2).

For DC applications, offset can be removed by using the DC Offset Current register. To compensate for any external phase error between the current and voltage channels, the Phase Compensation register can be used.

See **Section 8.0, MCP39F521 Calibration** for more information on device calibration.

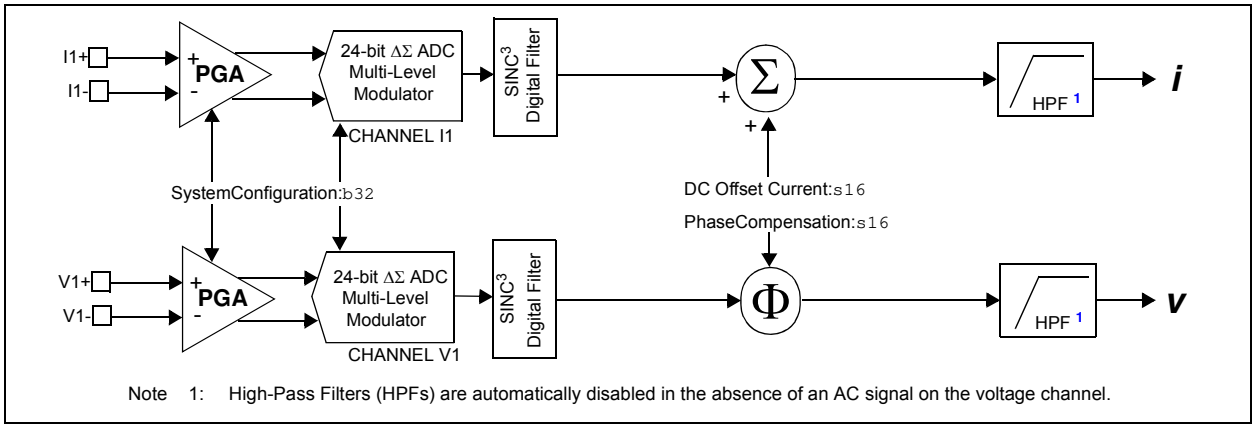


FIGURE 5-1: *Channel I1 and V1 Signal Flow.*

5.4 RMS Current and RMS Voltage

The MCP39F521 device provides true RMS measurements. The MCP39F521 device has two simultaneous sampling 24-bit A/D converters for the current and voltage measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$

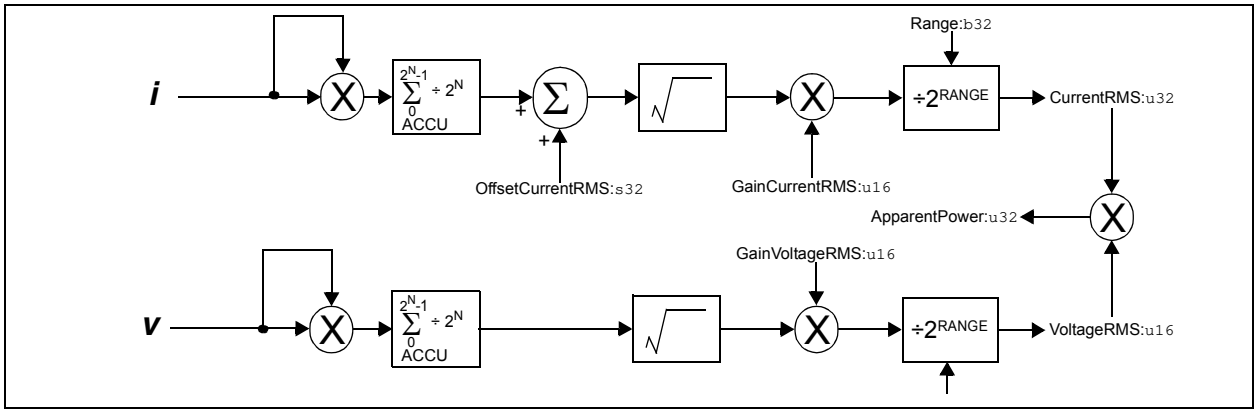


FIGURE 5-2: *RMS Current and Voltage Calculation Signal Flow.*

5.5 Power and Energy

The MCP39F521 offers signed power numbers for active and reactive power, import and export registers for active energy, and four-quadrant reactive power measurement. For this device, import power or energy is considered positive (power or energy being consumed by the load), and export power or energy is considered negative (power or energy being delivered by the load). The following figure represents the measurements obtained by the MCP39F521.

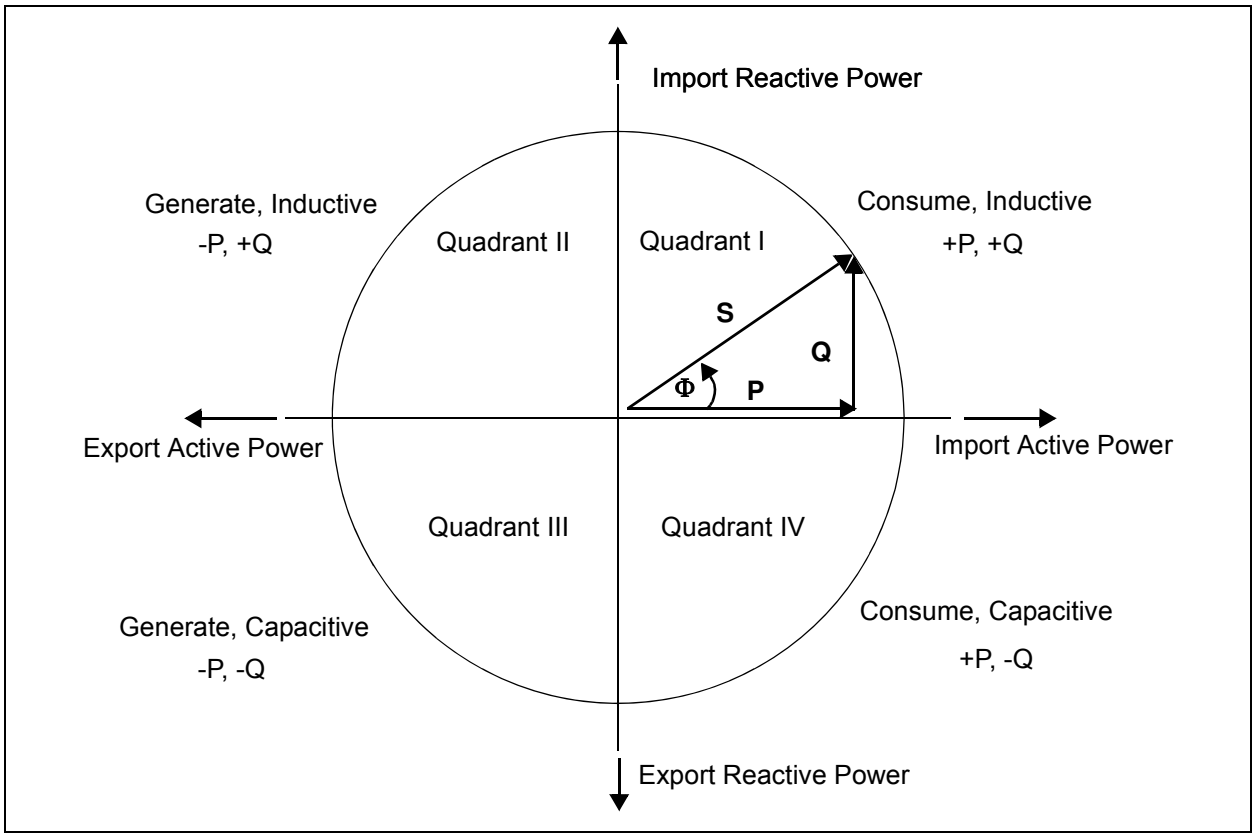


FIGURE 5-3: *The Power Circle and Triangle (S = Apparent, P = Active, Q = Reactive).*

5.6 Energy Accumulation

Energy accumulation for all four energy registers (import/export, active/reactive) occurs at the end of each computation cycle, if the energy accumulation has been turned on. See **Section 6.3, System Status Register** on the Energy Control register. A no-load threshold test is done to make sure the measured energy is not below the no-load threshold; if it is above the no-load threshold, the accumulation occurs with a default energy resolution of 1mWh for all of the energy registers.

5.6.1 NO-LOAD THRESHOLD

The no-load threshold is set by modifying the value in the No-Load Threshold register. The unit for this register is power with a default resolution of 0.01W. The default value is 100 or 1.00W. Any power that is below 1W will not be accumulated into any of the energy registers.

5.7 Apparent Power (S)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER (S)

$$S = I_{RMS} \times V_{RMS}$$

For scaling of the apparent power indication, the calculation engine uses the register Apparent Power Divisor. This is described in the following register operations, per Equation 5-3.

EQUATION 5-3: APPARENT POWER (S)

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{ApparentPowerDivisor}}$$

5.8 Active Power (P)

The MCP39F521 has two simultaneous sampling A/D converters. For the active power calculation, the instantaneous current and instantaneous voltages are multiplied together to create instantaneous power. This instantaneous power is then converted to active power by averaging or calculating the DC component.

Equation 5-4 controls the number of samples used in this accumulation prior to updating the Active Power output register.

Please note that although this register is unsigned, the direction of the active power (import or export) can be determined by the Active Power Sign bit (SIGN_PA) located in the System Status register (Register 6-1).

EQUATION 5-4: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

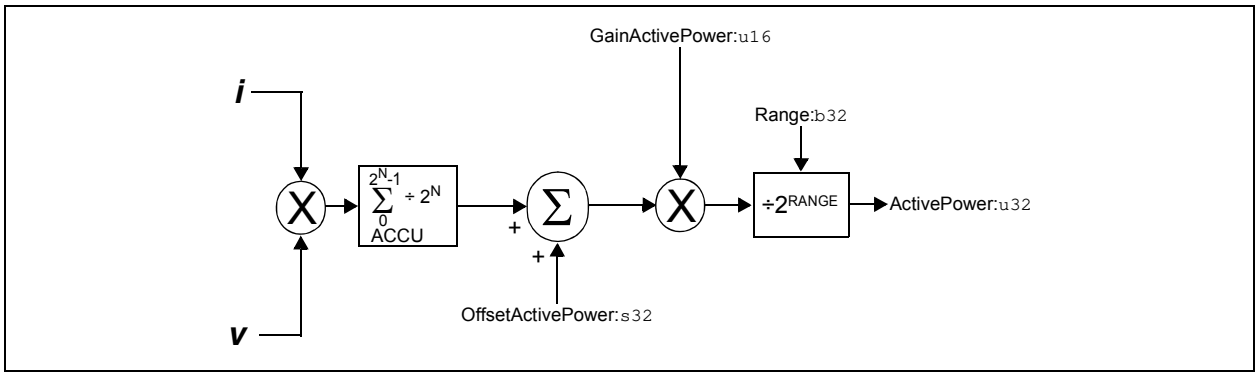


FIGURE 5-4: *Active Power Calculation Signal Flow.*

5.9 Power Factor (PF)

Power factor is calculated by the ratio of P to S or active power divided by apparent power.

EQUATION 5-5: POWER FACTOR

$$PF = \frac{P}{S}$$

The Power Factor Reading is stored in a signed 16-bit register (Power Factor). This register is a signed, two's complement register with the MSB representing the polarity of the power factor. Positive means inductive load, negative means capacitive load. Each LSB is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.10 Reactive Power (Q)

In the MCP39F521, Reactive Power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with active power where ACCU acts as an accumulator. Any light load or residual power can be removed by using the Offset Reactive Power register. Gain is corrected by the Gain Reactive Power register. The final output is an unsigned 32-bit value located in the Reactive Power register.

Please note that although this register is unsigned, the direction of the power can be determined by the Reactive Power Sign bit (SIGN_PR) in the System Status register (Register 6-1).

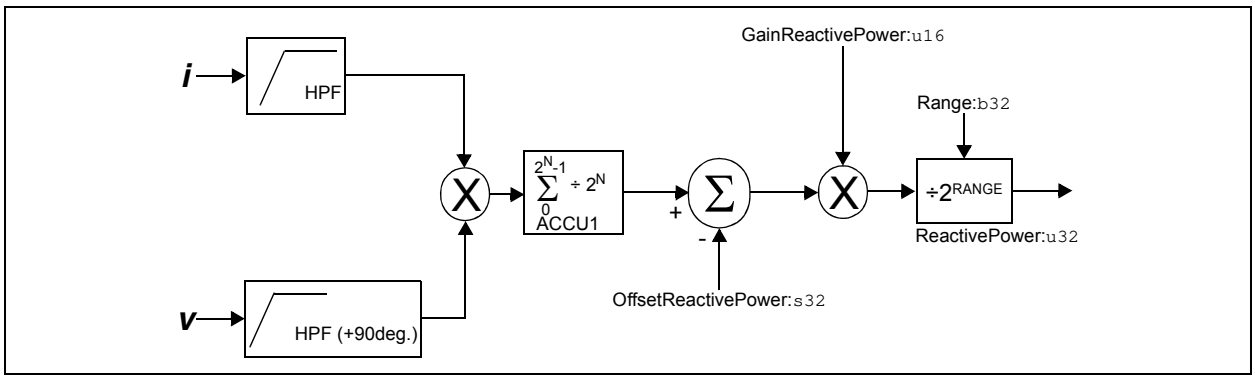


FIGURE 5-5: *Reactive Power Calculation Signal Flow.*