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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP4011/2/3/4

Low-Cost 64-Step Volatile Digital POT

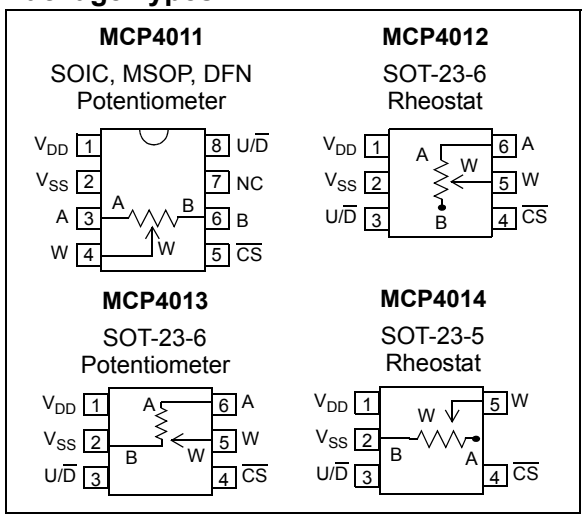
Features

- Volatile Digital Potentiometer in SOT-23, SOIC, MSOP and DFN packages
- 64 Taps: 63 Resistors with Taps to terminal A and terminal B
- Simple Up/$\overline{\text{Down}}$ (U/$\overline{\text{D}}$) Protocol
- Power-on Recall of Default Wiper Setting
  - Custom POR wiper settings available (contact factory)
- Resistance Values: 2.1 kΩ, 5 kΩ, 10 kΩ or 50 kΩ
- Low Tempco:
  - Absolute (Rheostat): 50 ppm (0°C to 70°C typ.)
  - Ratiometric (Potentiometer): 10 ppm (typ.)
- Low Wiper Resistance: 75Ω (typ.)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Low-Power Operation: 1 µA Max Static Current
- Wide Operating Voltage Range:
  - 1.8V to 5.5V - Device Operation
  - 2.7V to 5.5V - Resistor Characteristics Specified
- Extended Temperature Range: -40°C to +125°C
- Wide Bandwidth (-3 dB) Operation:
  - 4 MHz (typ.) for 2.1 kΩ device

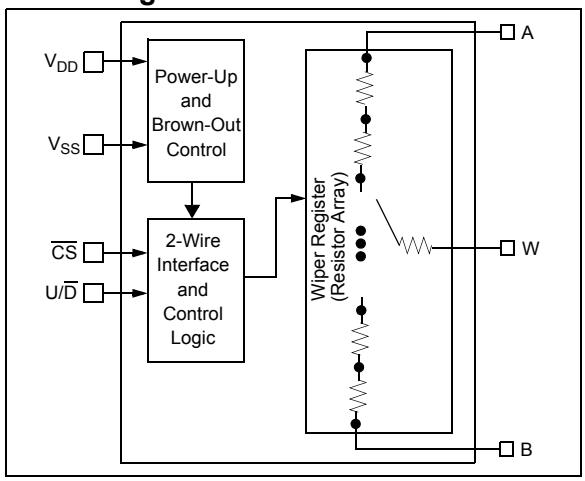
Description

The MCP4011/2/3/4 devices are volatile, 6-bit Digital Potentiometers that can be configured as either a potentiometer or rheostat. The wiper setting is controlled through a simple Up/$\overline{\text{Down}}$ (U/$\overline{\text{D}}$) serial interface.

Package Types



Block Diagram



Device Features

Device	Wiper Configuration	Memory Type	POR Wiper Setting	Resistance (typical)		# of Steps	V_{DD} Operating Range (2)	Control Interface	WiperLock™ Technology
				Options (kΩ)	Wiper (Ω)				
MCP4011	Potentiometer (1)	RAM	Mid-Scale	2.1, 5.0, 10.0, 50.0	75	64	1.8V to 5.5V	U/$\overline{\text{D}}$	No
MCP4012	Rheostat	RAM	Mid-Scale	2.1, 5.0, 10.0, 50.0	75	64	1.8V to 5.5V	U/$\overline{\text{D}}$	No
MCP4013	Potentiometer	RAM	Mid-Scale	2.1, 5.0, 10.0, 50.0	75	64	1.8V to 5.5V	U/$\overline{\text{D}}$	No
MCP4014	Rheostat	RAM	Mid-Scale	2.1, 5.0, 10.0, 50.0	75	64	1.8V to 5.5V	U/$\overline{\text{D}}$	No

Note 1: Floating either terminal (A or B) allows the device to be used in Rheostat mode.

2: Analog characteristics (resistor) tested from 2.7V to 5.5V.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V

$\overline{CS}$ and U/$\overline{D}$ inputs w.r.t V_{SS} ..... -0.3V to 12.5V

A,B and W terminals w.r.t V_{SS} ..... -0.3V to V_{DD} + 0.3V

Current at Input Pins .....±10 mA

Current at Supply Pins .....±10 mA

Current at Potentiometer Pins .....±2.5 mA

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-55°C to +125°C

ESD protection on all pins .....≥ 4 kV (HBM), ≥ 400V (MM)

Maximum Junction Temperature (T_J) .....+150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
	V_{DD}	—	1.8	—	V	V_{DD} = 1.8V, $\overline{CS}$:V_{IHH} = 8.5V, V_{IH} = 1.8V, V_{IL} = 0V, U/$\overline{D}$:V_{IH} = 1.8V, V_{IL} = 0V
$\overline{CS}$ Input Voltage	V_{CS}	V_{SS}	—	12.5	V	The $\overline{CS}$ pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}). (**Note 6**)
Supply Current	I_{DD}	—	45	—	µA	5.5V, $\overline{CS}$ = V_{SS}, $f_{U/D}$ = 1 MHz
		—	15	—	µA	2.7V, $\overline{CS}$ = V_{SS}, $f_{U/D}$ = 1 MHz
		—	0.3	1	µA	Serial Interface Inactive ($\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IH})
Resistance (± 20%)	R_{AB}	1.68	2.1	2.52	kΩ	-202 devices **(Note 1)**
		4.0	5	6.0	kΩ	-502 devices **(Note 1)**
		8.0	10	12.0	kΩ	-103 devices **(Note 1)**
		40.0	50	60.0	kΩ	-503 devices **(Note 1)**

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}. (-202 devices V_A = 4V).

3: **MCP4011/13** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4012/14** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	2.7V	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4012** includes V_{WZSE} **MCP4014** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: For voltages below 2.7V, refer to **Section 2.0 "Typical Performance Curves"**.

9: The **MCP4011** is externally connected to match the configurations of the **MCP4012** and **MCP4014** and then tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions	
Resolution	N		64		Taps	No Missing Codes	
Step Resistance	R_S	—	R_{AB} / 63	—	Ω	**Note 6**	
Wiper Resistance (**Note 3, Note 4)**	R_W	—	70	125	Ω	5.5V	
		—	70	325	Ω	2.7V	
Nominal Resistance Tempco	ΔR/ΔT	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WA}/\Delta T$	—	10	—	ppm/°C	**MCP4011** and **MCP4013** only, code = 1Fh	
Full-Scale Error (**MCP4011/13** only)	V_{WFSE}	-0.5	-0.1	+0.5	LSb	Code 3Fh, 2.7V ≤ V_{DD} ≤ 5.5V	
Zero-Scale Error (**MCP4011/13** only)	V_{WZSE}	-0.5	+0.1	+0.5	LSb	Code 00h, 2.7V ≤ V_{DD} ≤ 5.5V	
Monotonicity	N		Yes		Bits		
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 5**, **Note 6**	
Current through A, W or B	I_W	—	—	2.5	mA	**Note 6**	
Leakage current into A, W or B	I_{WL}	—	100	—	nA	**MCP4011** A = W = B = V_{SS}	
		—	100	—	nA	**MCP4012/13** A = W = V_{SS}	
		—	100	—	nA	**MCP4014** W = V_{SS}	
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, code = 1Fh	
Capacitance (P_W)	C_W	—	120	—	pF	f =1 MHz, code = 1Fh	
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, code = 1Fh	
Bandwidth -3 dB	BW	—	4	—	MHz	-202 devices	Code = 1F, output load = 30 pF
		—	2	—	MHz	-502 devices	
		—	1	—	MHz	-103 devices	
		—	200	—	kHz	-503 devices	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}. (-202 devices V_A = 4V).

3: **MCP4011/13** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4012/14** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	2.7V	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4012** includes V_{WZSE} **MCP4014** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: For voltages below 2.7V, refer to **Section 2.0 "Typical Performance Curves"**.

9: The **MCP4011** is externally connected to match the configurations of the **MCP4012** and **MCP4014** and then tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions	
Potentiometer Integral Non-linearity	INL	-0.5	±0.25	+0.5	LSb	**MCP4011/13** only **(Note 2)**	
Potentiometer Differential Non-linearity	DNL	-0.5	±0.25	+0.5	LSb	**MCP4011/13** only **(Note 2)**	
Rheostat Integral Non-linearity **MCP4011** (**Note 4, Note 9**) **MCP4012** and **MCP4014** **(Note 4)**	R-INL	-0.5	±0.25	+0.5	LSb	-202 devices (2.1 kΩ)	5.5V
		-8.5	+4.5	+8.5	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
		-0.5	±0.25	+0.5	LSb	-502 devices (5 kΩ)	5.5V
		-5.5	+2.5	+5.5	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
		-0.5	±0.25	+0.5	LSb	-103 devices (10 kΩ)	5.5V
		-3	+1	+3	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
		-0.5	±0.25	+0.5	LSb	-503 devices (50 kΩ)	5.5V
		-1	+0.25	+1	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
Rheostat Differential Non-linearity **MCP4011** (**Note 4, Note 9**) **MCP4012** and **MCP4014** **(Note 4)**	R-DNL	-0.5	±0.25	+0.5	LSb	-202 devices (2.1 kΩ)	5.5V
		-1	+0.5	+2	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
		-0.5	±0.25	+0.5	LSb	-502 devices (5 kΩ)	5.5V
		-1	+0.25	+1.25	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
		-0.5	±0.25	+0.5	LSb	-103 devices (10 kΩ)	5.5V
		-1	0	+1	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**
		-0.5	±0.25	+0.5	LSb	-503 devices (50 kΩ)	5.5V
		-0.5	0	+0.5	LSb		2.7V **(Note 7)**
		See **Section 2.0**			LSb		1.8V **(Note 7, Note 8)**

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$. (-202 devices V_A = 4V).

3: **MCP4011/13** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4012/14** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	2.7V	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4012** includes V_{WZSE} **MCP4014** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: For voltages below 2.7V, refer to **Section 2.0 "Typical Performance Curves"**.

9: The **MCP4011** is externally connected to match the configurations of the **MCP4012** and **MCP4014** and then tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Digital Inputs/Outputs ($\overline{CS}$, U/$\overline{D}$)						
Input High Voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.3 V_{DD}	V	
High-Voltage Input Entry Voltage	V_{IHH}	8.5	—	12.5 (6)	V	Threshold for WiperLock™ Technology
High-Voltage Input Exit Voltage	V_{IHH}	—	—	V_{DD}+0.8(6)	V	
$\overline{CS}$ Pull-up/Pull-down Resistance	R_{CS}	—	16	—	kΩ	V_{DD} = 5.5V, V_{CS} = 3V
$\overline{CS}$ Weak Pull-up/Pull-down Current	I_{PU}	—	170	—	µA	V_{DD} = 5.5V, V_{CS} = 3V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD}
$\overline{CS}$ and U/$\overline{D}$ Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 1 MHz, $V_{DD} \geq$ 2.7V
RAM (Wiper) Value						
Value Range	N	0h	—	3Fh	hex	
Default POR Setting	N	1Fh			hex	
Power Requirements						
Power Supply Sensitivity (**MCP4011** and **MCP4013** only)	PSS	—	0.0015	0.0035	%/%	V_{DD} = 4.5V to 5.5V, V_A = 4.5V, Code = 1Fh
		—	0.0015	0.0035	%/%	V_{DD} = 2.7V to 4.5V, V_A = 2.7V, Code = 1Fh

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}. (-202 devices V_A = 4V).

3: **MCP4011/13** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4012/14** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	2.7V	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4012** includes V_{WZSE} **MCP4014** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: For voltages below 2.7V, refer to **Section 2.0 "Typical Performance Curves"**.

9: The **MCP4011** is externally connected to match the configurations of the **MCP4012** and **MCP4014** and then tested.

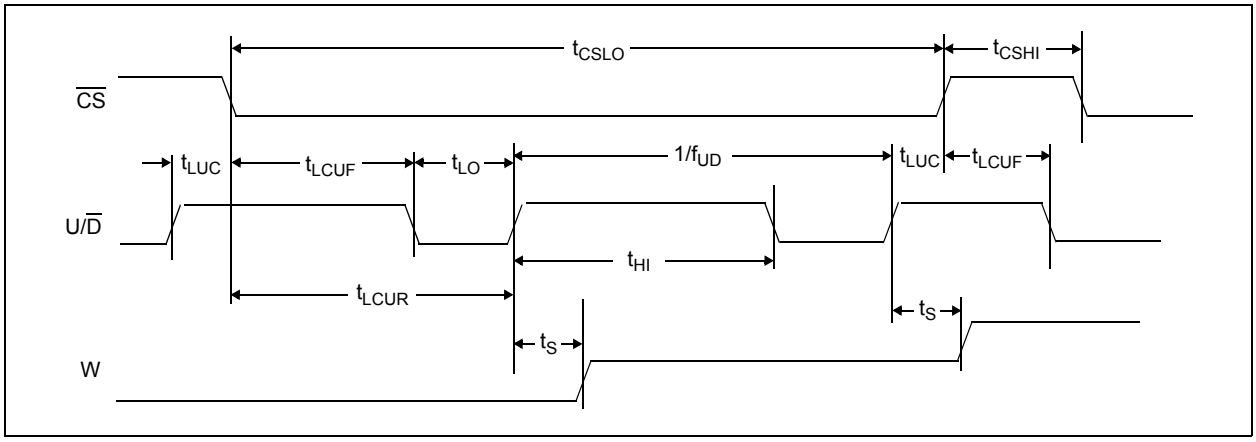


FIGURE 1-1: *Increment Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +1.8V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	2.7V ≤ V_{DD} ≤ 5.5V
		—	—	—	ns	1.8V ≤ V_{DD} < 2.7V
U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{LUC}	500	—	—	ns	2.7V ≤ V_{DD} ≤ 5.5V
		750	—	—	ns	1.8V ≤ V_{DD} < 2.7V
$\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{LCUF}	500	—	—	ns	
$\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{LCUR}	3	—	—	µs	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	

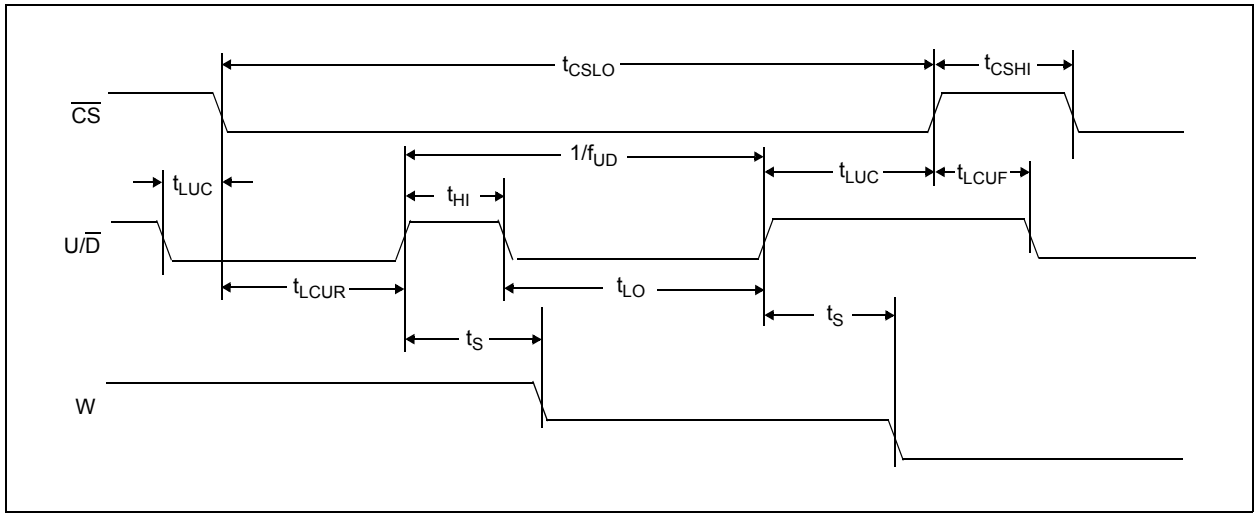


FIGURE 1-2: *Decrement Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +1.8V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	2.7V ≤ V_{DD} ≤ 5.5V
		—	—	—	ns	1.8V ≤ V_{DD} < 2.7V
U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{LUC}	500	—	—	ns	2.7V ≤ V_{DD} ≤ 5.5V
		750	—	—	ns	1.8V ≤ V_{DD} < 2.7V
$\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{LCUF}	500	—	—	ns	
$\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{LCUR}	3	—	—	µs	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	

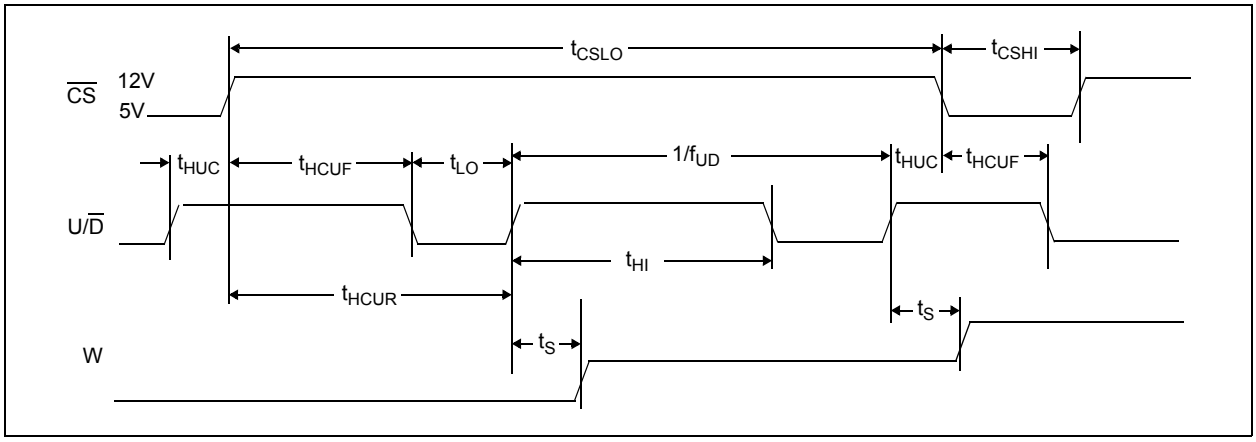


FIGURE 1-3: *High-Voltage Increment Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +1.8V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	2.7V ≤ V_{DD} ≤ 5.5V
		—	—	—	ns	1.8V ≤ V_{DD} < 2.7V
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
HV U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{HUC}	1.5	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{HCUF}	8	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{HCUR}	4.5	—	—	µs	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	

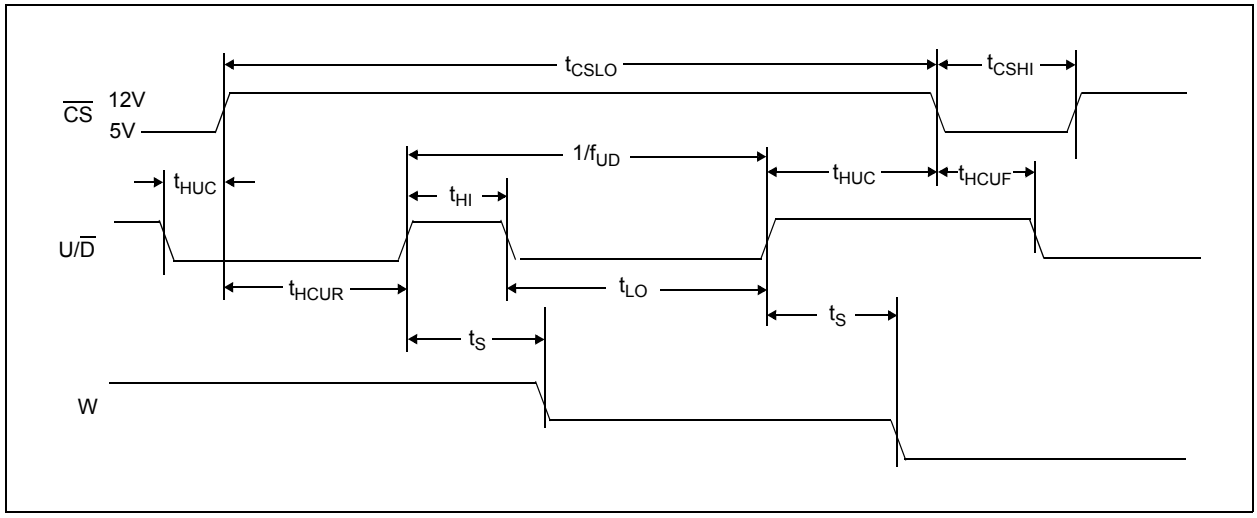


FIGURE 1-4: *High-Voltage Decrement Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +1.8V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	2.7V ≤ V_{DD} ≤ 5.5V
		—	—	—	ns	1.8V ≤ V_{DD} < 2.7V
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
HV U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{HUC}	1.5	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{HCUF}	8	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{HCUR}	4.5	—	—	µs	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 8L-DFN (2x3)	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

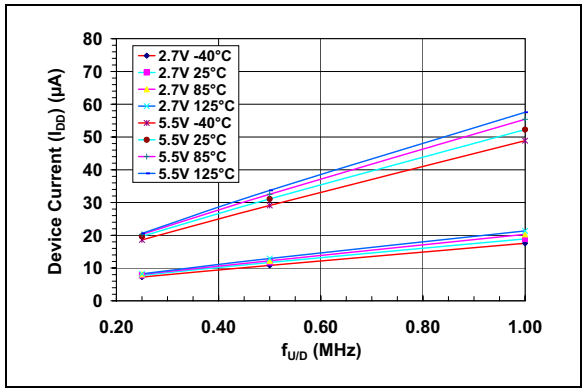


FIGURE 2-1: *Device Current (I_{DD}) vs. U/$\overline{D}$ Frequency ($f_{U/D}$) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

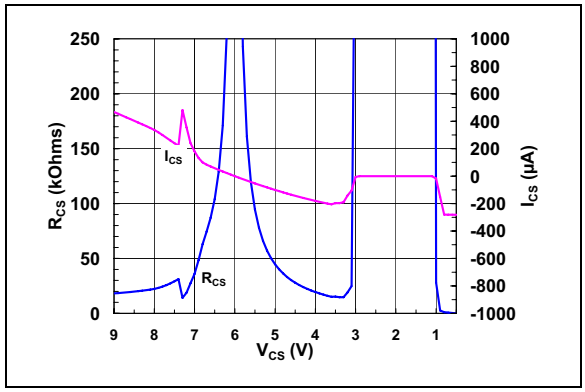


FIGURE 2-3: *$\overline{CS}$ Pull-up/Pull-down Resistance (R_{CS}) and Current (I_{CS}) vs. $\overline{CS}$ Input Voltage (V_{CS}) (V_{DD} = 5.5V).*

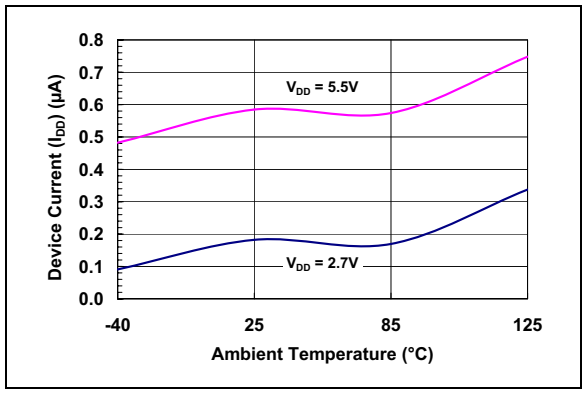


FIGURE 2-2: *Device Current (I_{SHDN}) and V_{DD}. ($\overline{CS}$ = V_{DD}) vs. Ambient Temperature.*

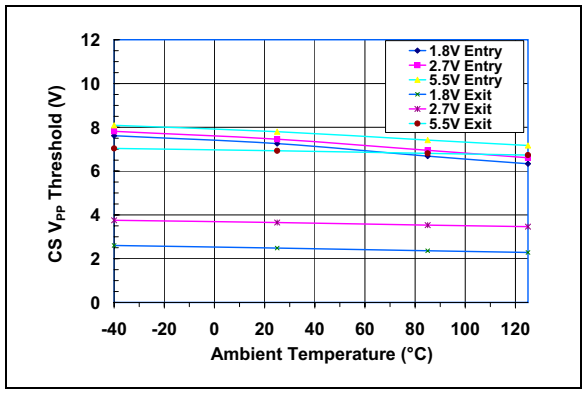


FIGURE 2-4: *$\overline{CS}$ High Input Entry/Exit Threshold vs. Ambient Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

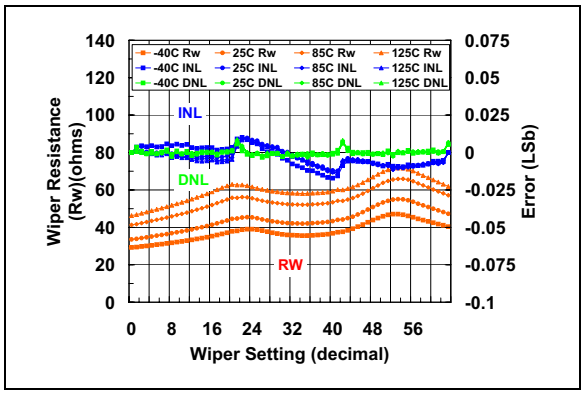


FIGURE 2-5: *2.1 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

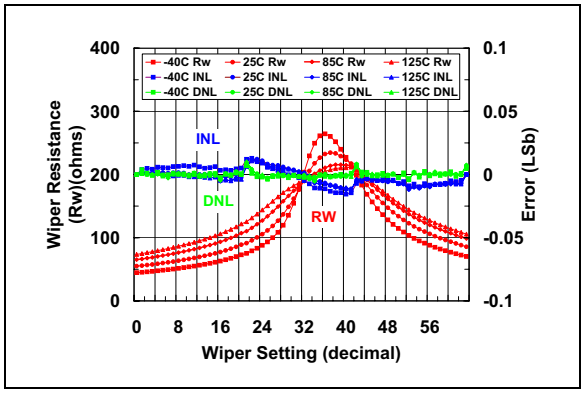


FIGURE 2-6: *2.1 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

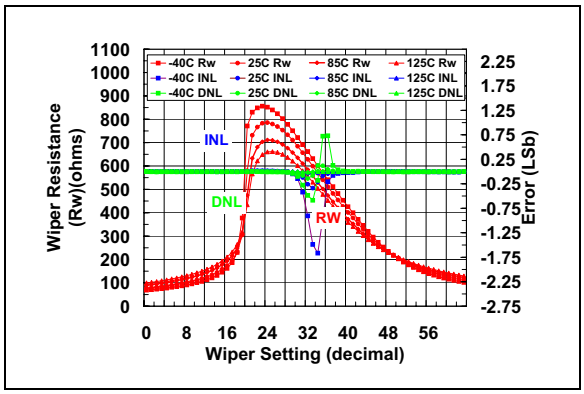


FIGURE 2-7: *2.1 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

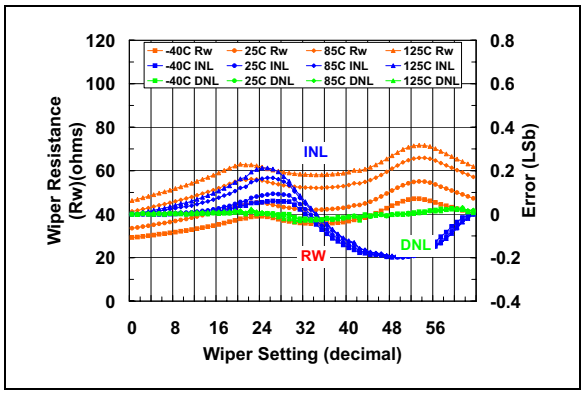


FIGURE 2-8: *2.1 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

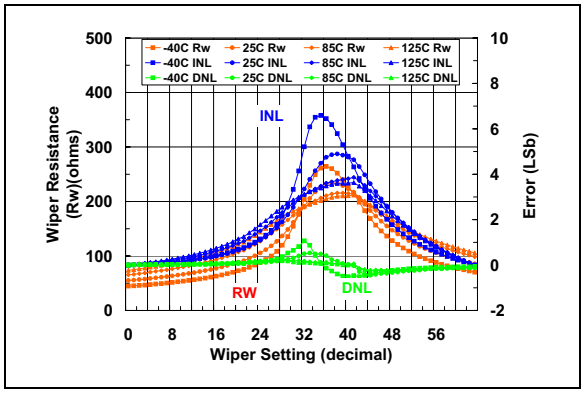


FIGURE 2-9: *2.1 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

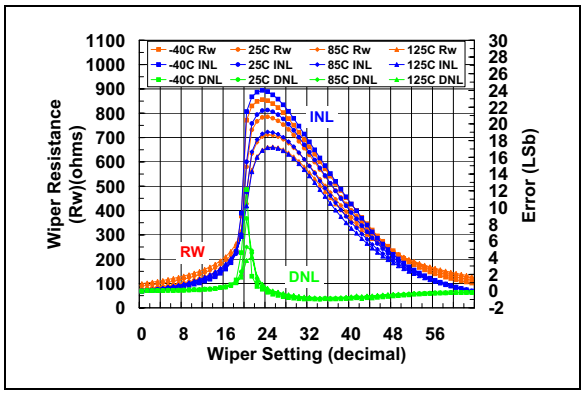


FIGURE 2-10: *2.1 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

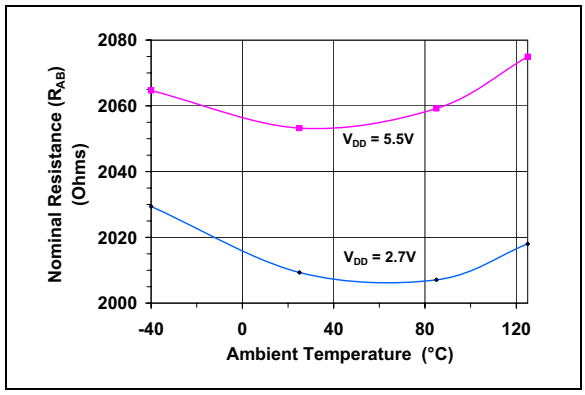


FIGURE 2-11: *2.1 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

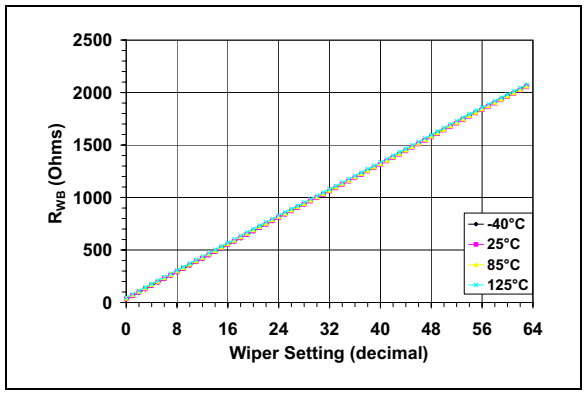


FIGURE 2-12: *2.1 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

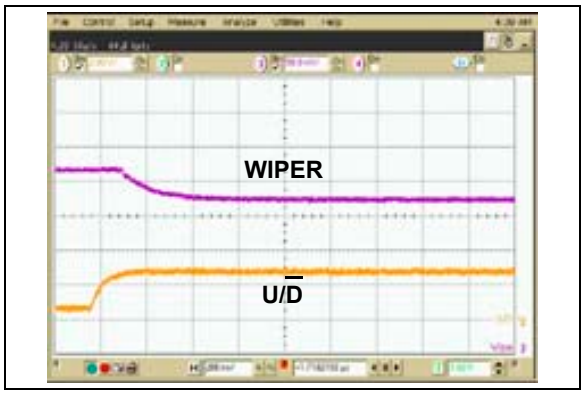


FIGURE 2-13: *2.1 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

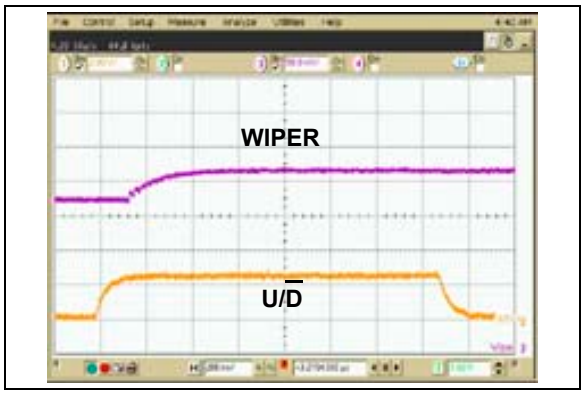


FIGURE 2-16: *2.1 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

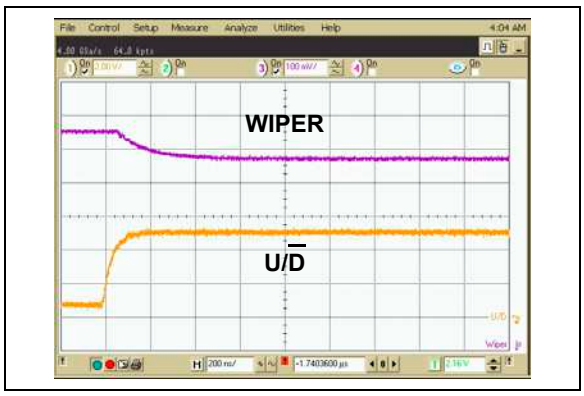


FIGURE 2-14: *2.1 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

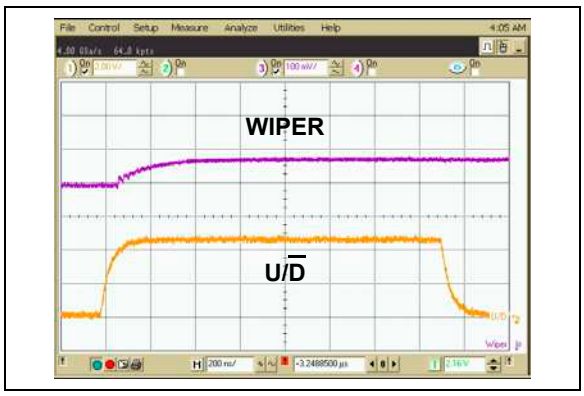


FIGURE 2-17: *2.1 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

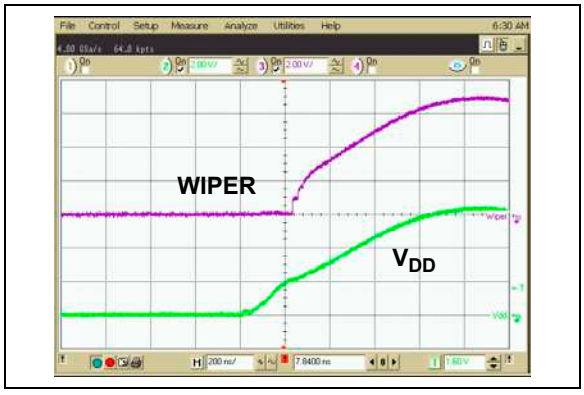


FIGURE 2-15: *2.1 kΩ – Power-Up Wiper Response Time.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

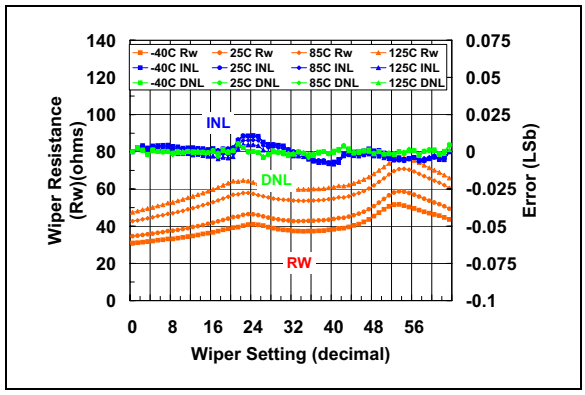


FIGURE 2-18: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

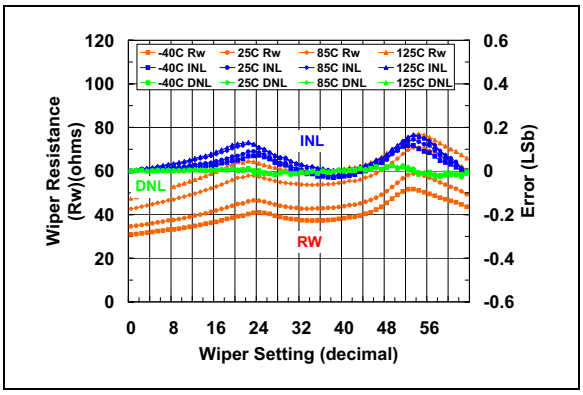


FIGURE 2-21: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

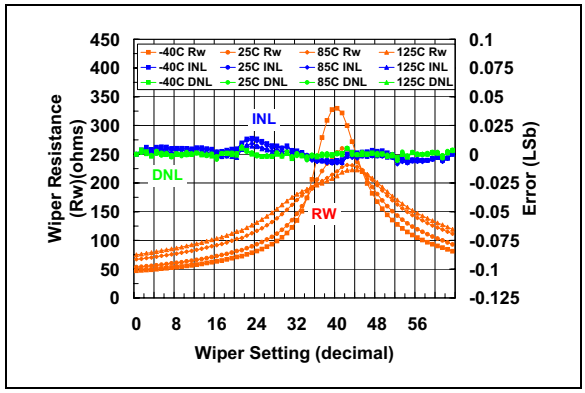


FIGURE 2-19: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

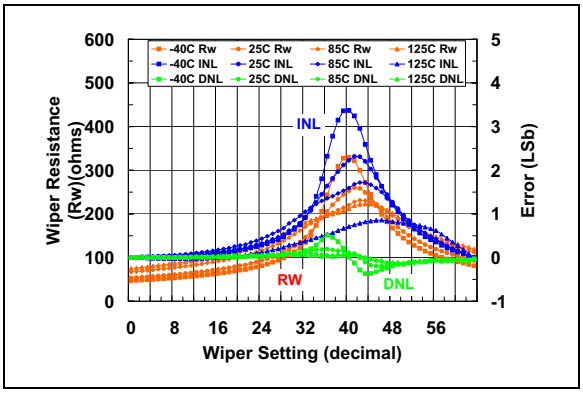


FIGURE 2-22: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

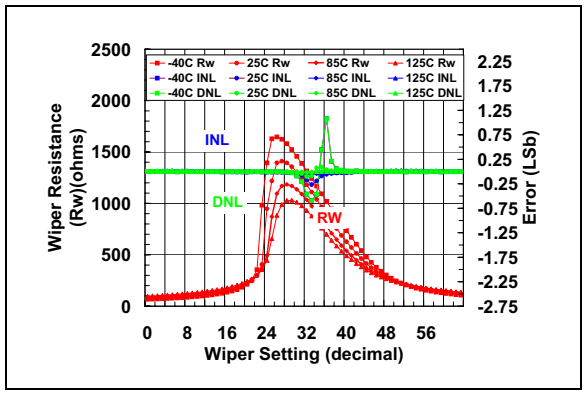


FIGURE 2-20: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

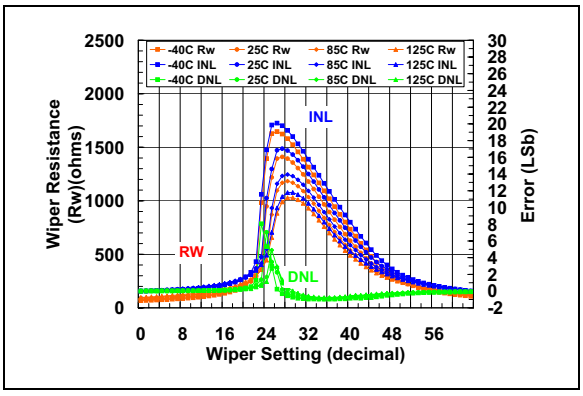


FIGURE 2-23: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

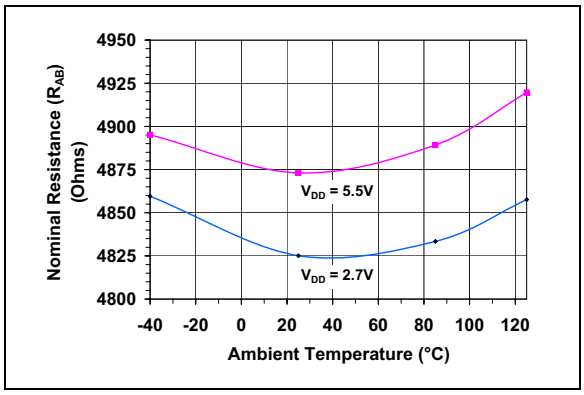


FIGURE 2-24: *5 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

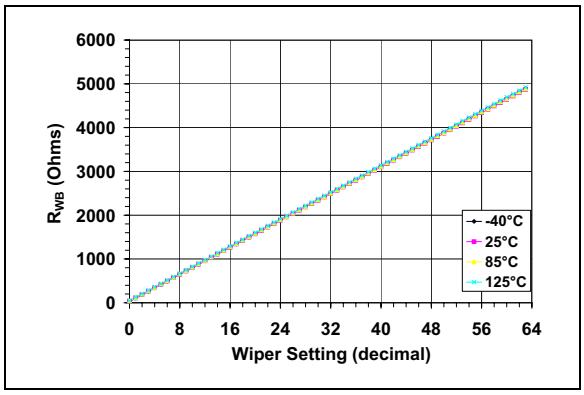


FIGURE 2-25: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

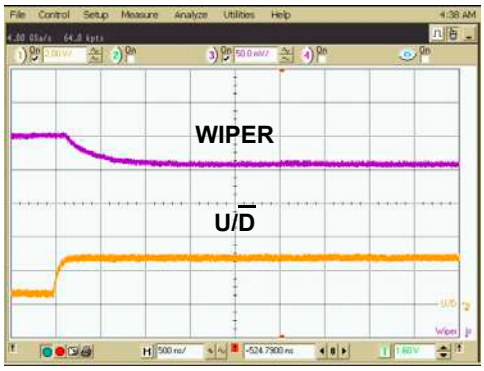


FIGURE 2-26: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

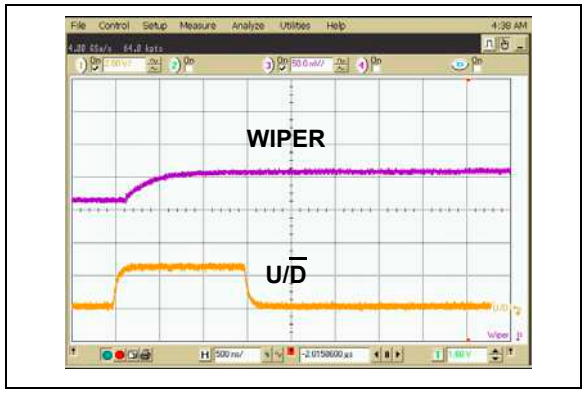


FIGURE 2-28: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

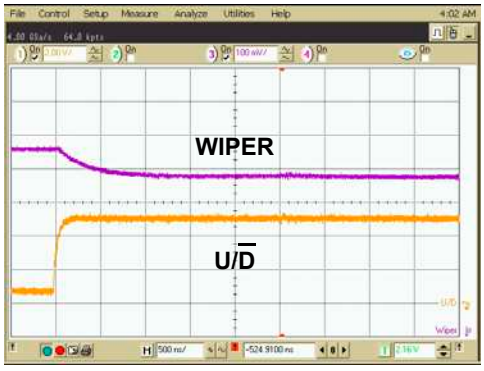


FIGURE 2-27: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

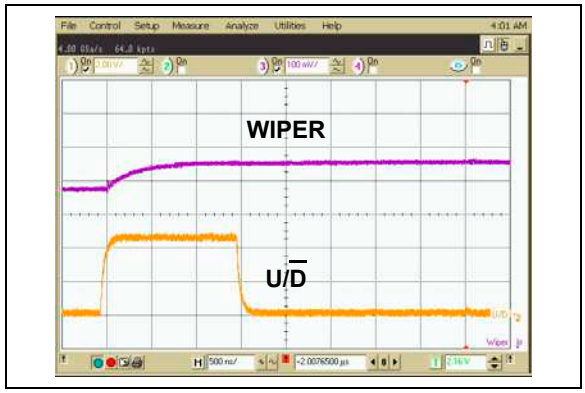


FIGURE 2-29: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

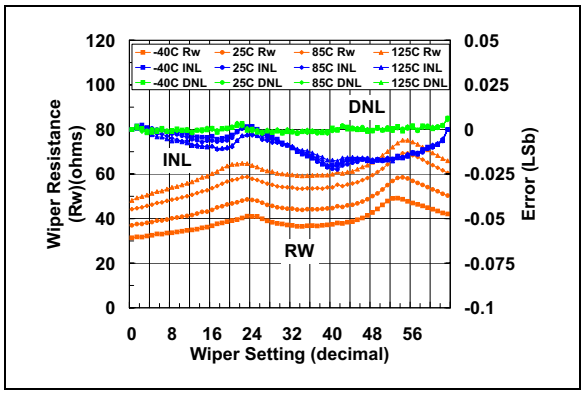


FIGURE 2-30: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

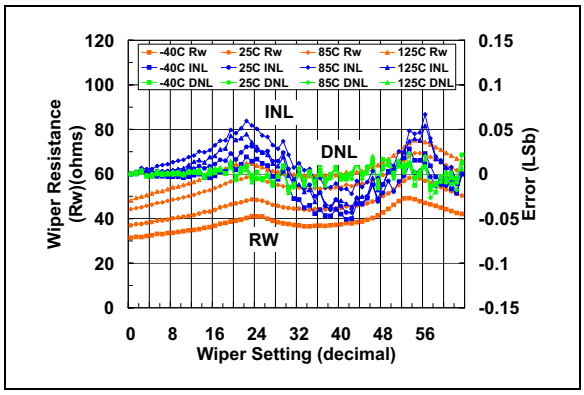


FIGURE 2-33: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

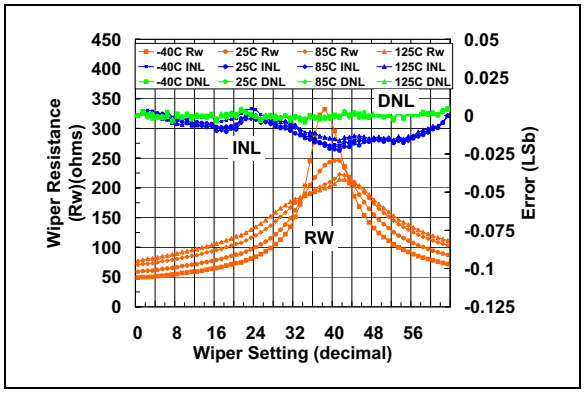


FIGURE 2-31: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

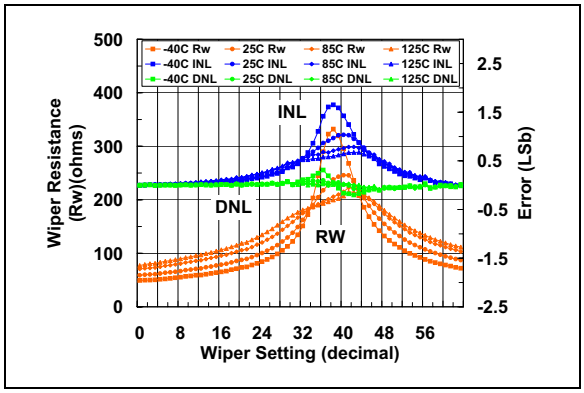


FIGURE 2-34: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

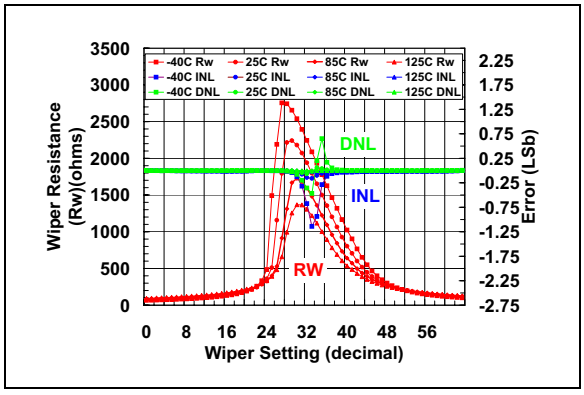


FIGURE 2-32: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

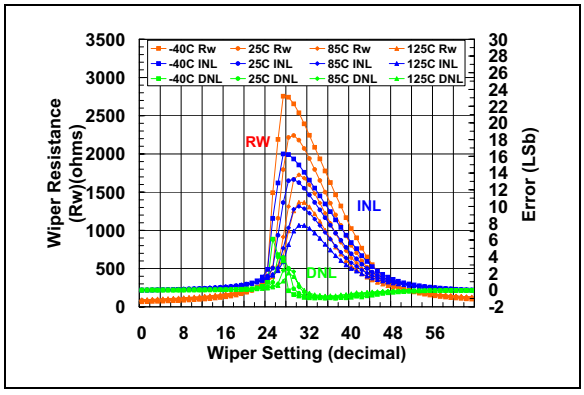


FIGURE 2-35: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

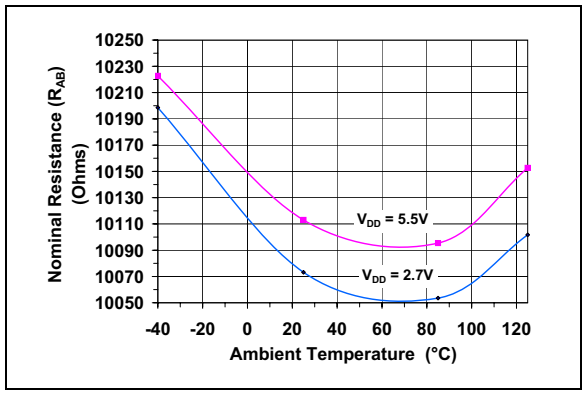


FIGURE 2-36: *10 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

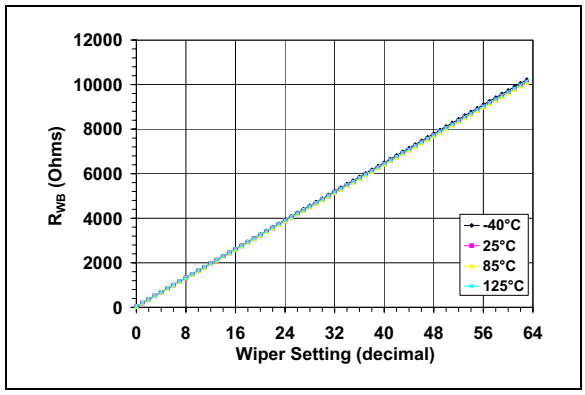


FIGURE 2-37: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

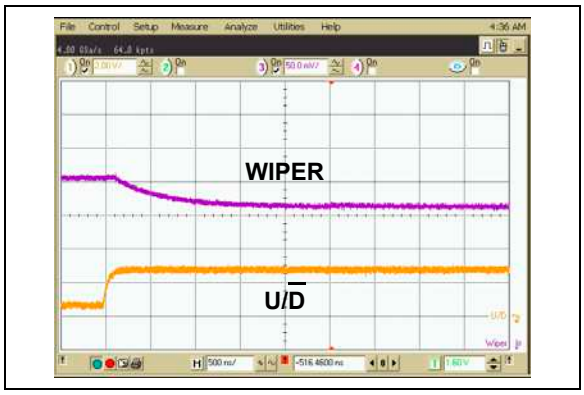


FIGURE 2-38: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

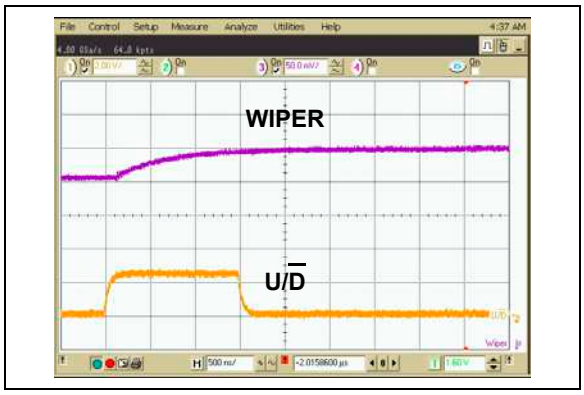


FIGURE 2-40: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

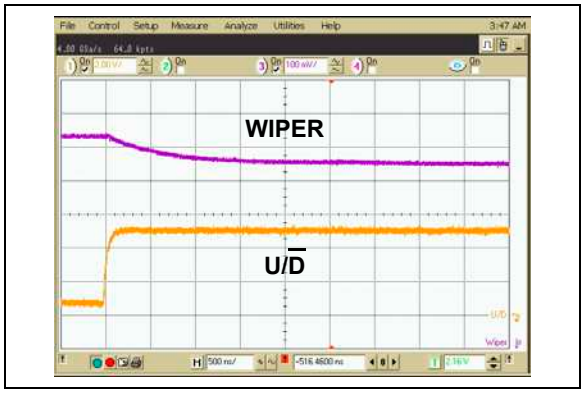


FIGURE 2-39: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

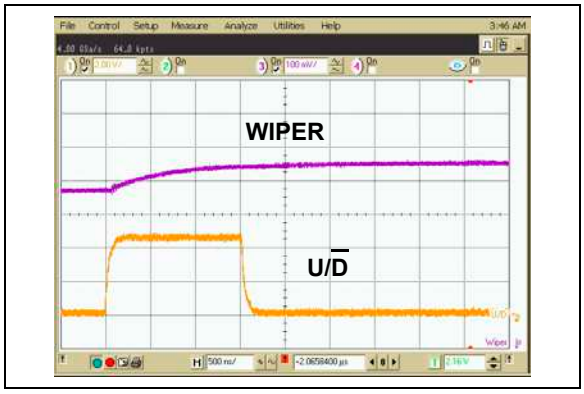


FIGURE 2-41: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

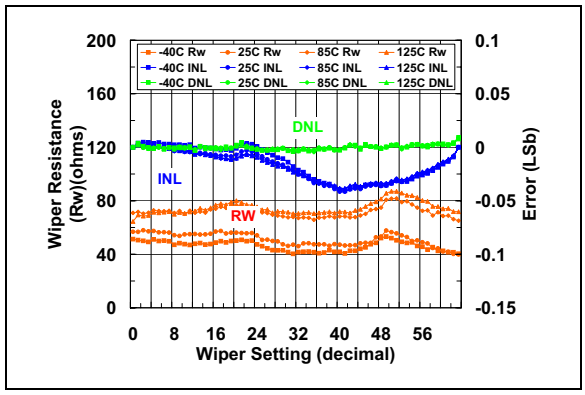


FIGURE 2-42: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

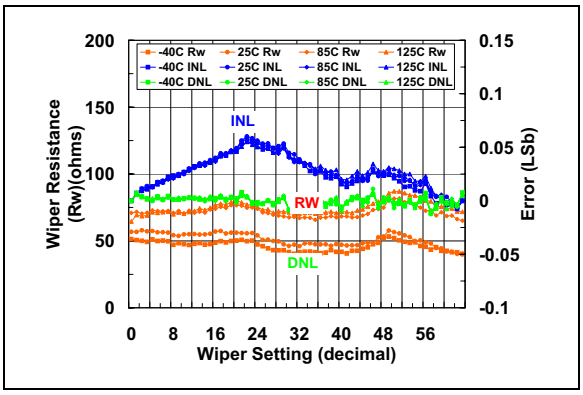


FIGURE 2-45: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

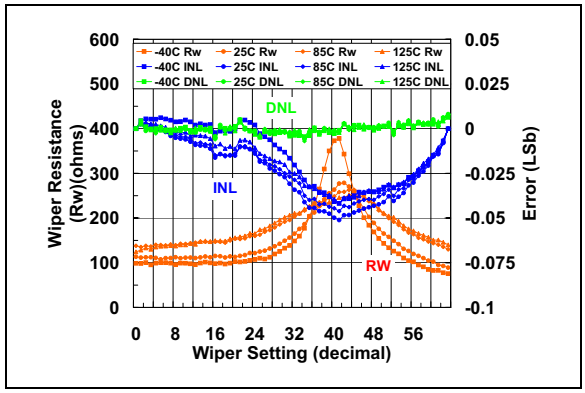


FIGURE 2-43: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

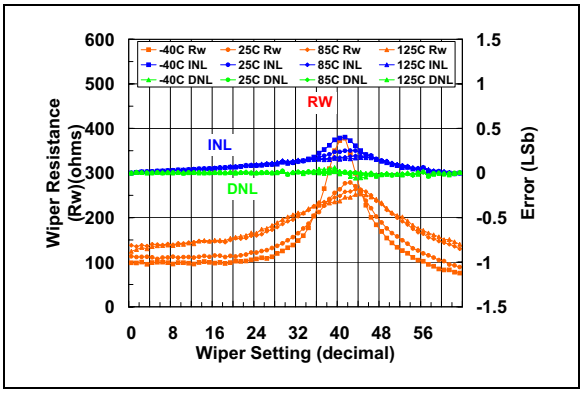


FIGURE 2-46: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

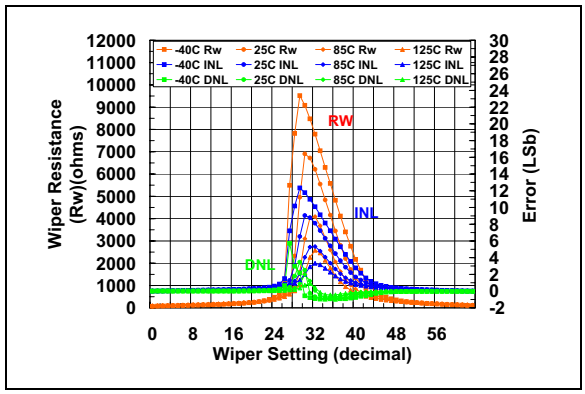


FIGURE 2-44: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

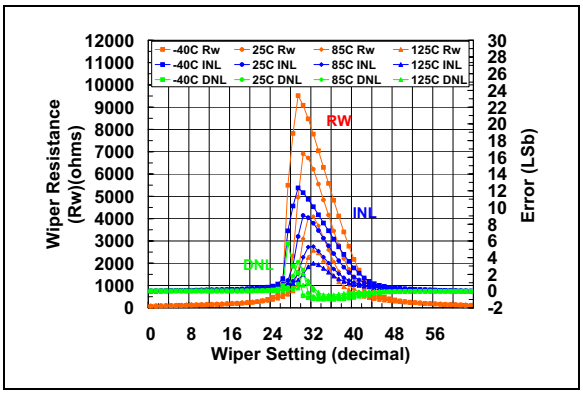


FIGURE 2-47: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

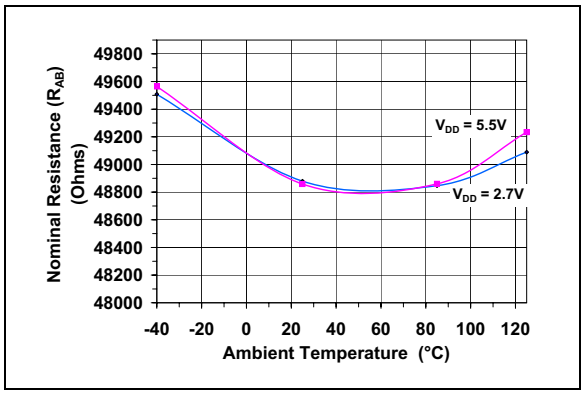


FIGURE 2-48: *50 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

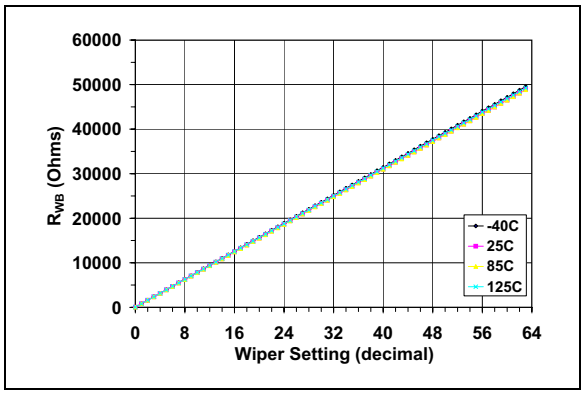


FIGURE 2-49: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

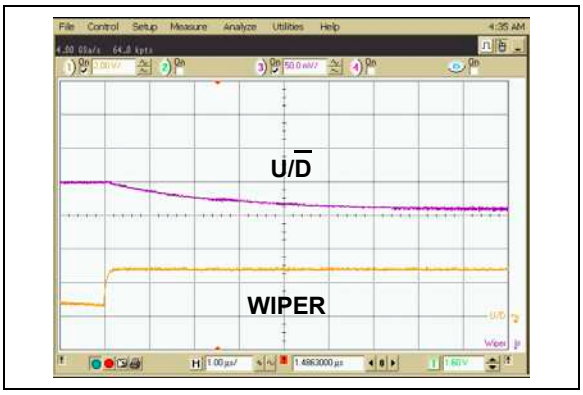


FIGURE 2-50: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

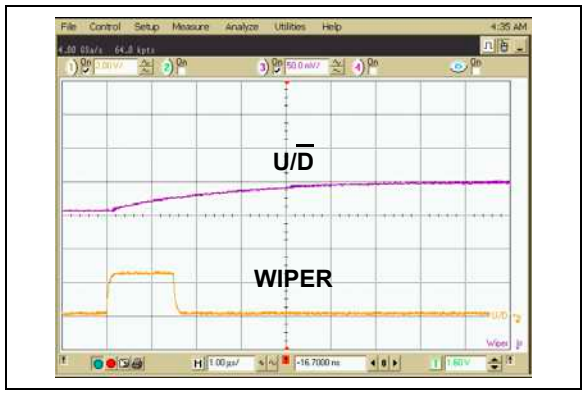


FIGURE 2-53: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

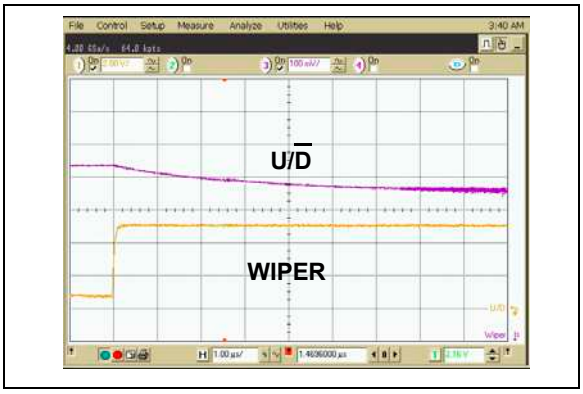


FIGURE 2-51: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

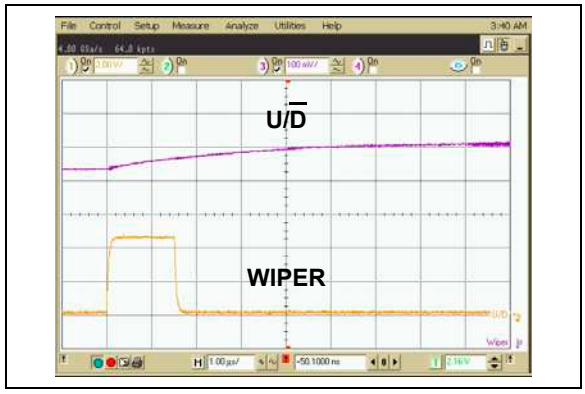


FIGURE 2-54: *50 kΩ - Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

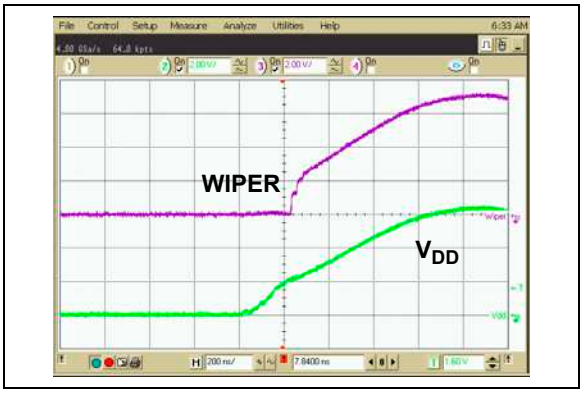


FIGURE 2-52: *50 kΩ – Power-Up Wiper Response Time.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

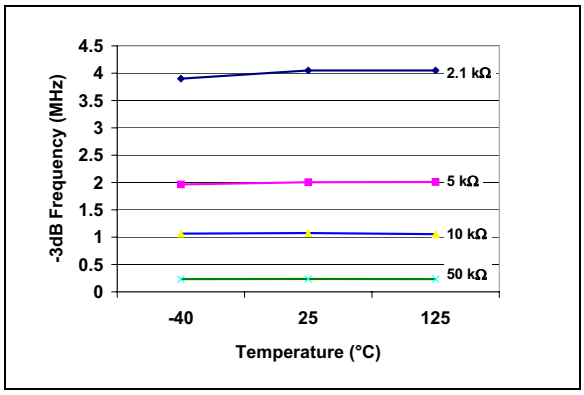


FIGURE 2-55: *-3 dB Bandwidth vs. Temperature.*

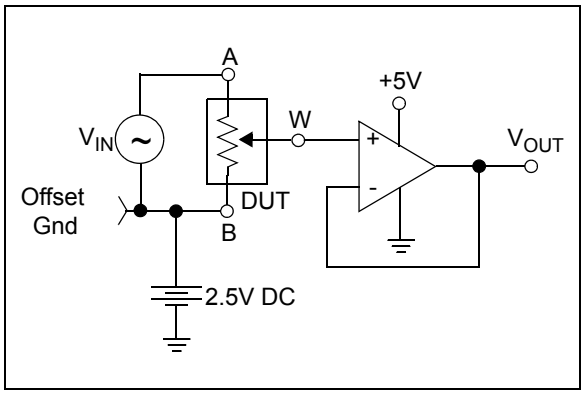


FIGURE 2-56: *-3 dB Bandwidth Test Circuit.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number			Symbol	Pin Type	Buffer Type	Function
MCP4011 (SOIC-8)	MCP4012 MCP4013 (SOT-23-6)	MCP4014 (SOT-23-5)				
1	1	1	V_{DD}	P	—	Positive Power Supply Input
2	2	2	V_{SS}	P	—	Ground
3	6	—	A	I/O	A	Potentiometer Terminal A
4	5	5	W	I/O	A	Potentiometer Wiper Terminal
5	4	4	$\overline{CS}$	I	TTL	Chip Select Input
6	—	—	B	I/O	A	Potentiometer Terminal B
7	—	—	NC	—	—	No Connection
8	3	3	U/$\overline{D}$	I	TTL	Increment/$\overline{\text{Decrement}}$ Input

Legend: TTL = TTL compatible input
A = Analog input
I = Input
O = Output
P = Power

3.1 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device's positive power supply input. The input power supply is relative to V_{SS} and can range from 1.8V to 5.5V. A decoupling capacitor on V_{DD} (to V_{SS}) is recommended to achieve maximum performance.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.3 Potentiometer Terminal A

The terminal A pin is connected to the internal potentiometer's terminal A (available on some devices). The potentiometer's terminal A is the fixed connection to the 0x3F terminal of the digital potentiometer.

The terminal A pin is available on the MCP4011, MCP4012 and MCP4013 devices. The terminal A pin does not have a polarity relative to the terminal W or B pins. The terminal A pin can support both positive and negative current. The voltage on terminal A must be between V_{SS} and V_{DD}.

The terminal A pin is not available on the MCP4014. The potentiometer's terminal A is internally floating.

3.4 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer's terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on terminal W must be between V_{SS} and V_{DD}.

3.5 Potentiometer Terminal B

The terminal B pin is connected to the internal potentiometer's terminal B (available on some devices). The potentiometer's terminal B is the fixed connection to the 0x00 terminal of the digital potentiometer.

The terminal B pin is available on the MCP4011 device. The terminal B pin does not have a polarity relative to the terminal W or A pins. The terminal B pin can support both positive and negative current. The voltage on terminal B must be between V_{SS} and V_{DD}.

The terminal B pin is not available on the MCP4012, MCP4013 and MCP4014 devices.

For the MCP4013 and MCP4014, the internal potentiometer's terminal B is internally connected to V_{SS}. Terminal B does not have a polarity relative to terminals W or A. Terminal B can support both positive and negative current.

For the MCP4012, terminal B is internally floating.