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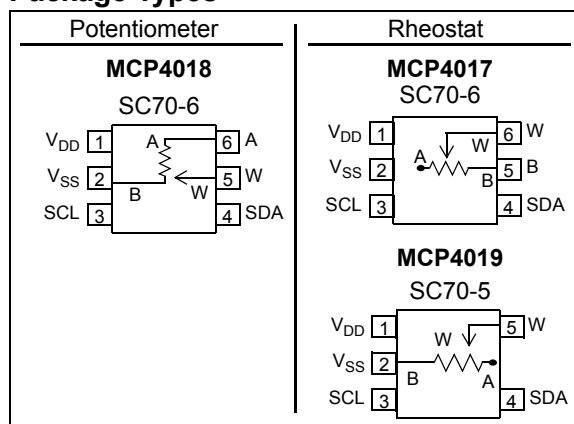


7-Bit Single I²C™ Digital POT with Volatile Memory in SC70

Features

- Potentiometer or Rheostat configuration options
- 7-bit: Resistor Network Resolution
 - 127 Resistors (128 Steps)
- Zero Scale to Full Scale Wiper operation
- R_{AB} Resistances: 5 kΩ, 10 kΩ, 50 kΩ, or 100 kΩ
- Low Wiper Resistance: 100Ω (typical)
- Low Tempo:
 - Absolute (Rheostat): 50 ppm typical (0°C to 70°C)
 - Ratiometric (Potentiometer): 10 ppm typical
- Simple I²C Protocol with read & write commands
- Brown-out reset protection (1.5V typical)
- Power-on Default Wiper Setting (Mid-scale)
- Low-Power Operation:
 - 2.5 μA Static Current (typical)
- Wide Operating Voltage Range:
 - 2.7V to 5.5V - Device Characteristics Specified
 - 1.8V to 5.5V - Device Operation

Package Types



- Wide Bandwidth (-3 dB) Operation:
 - 2 MHz (typical) for 5.0 kΩ device
- Extended temperature range (-40°C to +125°C)
- Very small package (SC70)
- Lead free (Pb-free) package

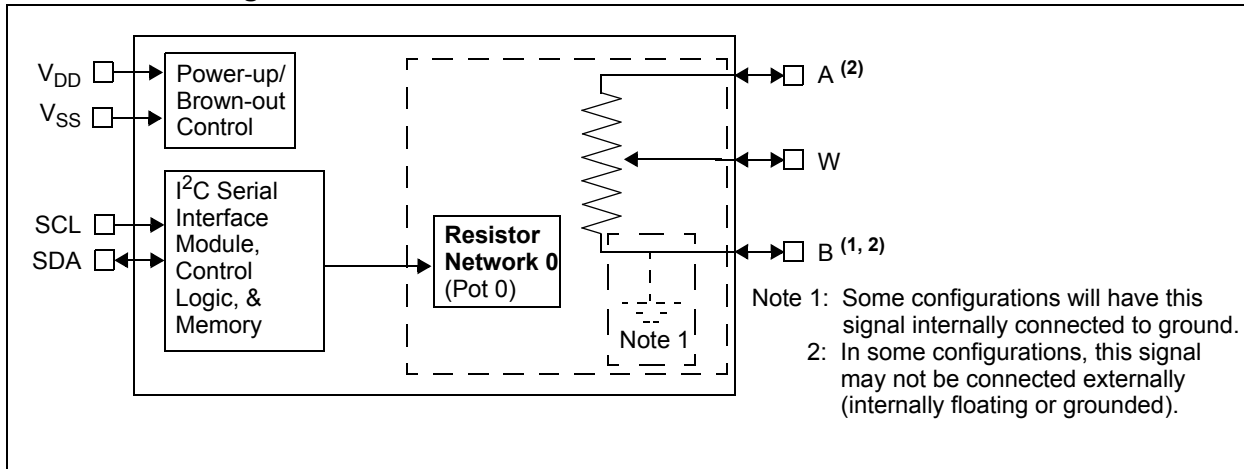
Device Features

Device	Control Interface	# of Steps	Wiper Configuration	Memory Type	Resistance (typical)		VDD Operating Range ⁽¹⁾	Package
					Options (kΩ)	Wiper (Ω)		
MCP4017	I ² C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	75	1.8V to 5.5V	SC70-6
MCP4018	I ² C	128	Potentiometer	RAM	5.0, 10.0, 50.0, 100.0	75	1.8V to 5.5V	SC70-6
MCP4019	I ² C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	75	1.8V to 5.5V	SC70-5

Note 1: Analog characteristics only tested from 2.7V to 5.5V

MCP4017/18/19

Device Block Diagram



Comparison of Similar Microchip Devices ⁽¹⁾

Device	Control Interface	# of Steps	Wiper Configuration	Memory Type	Resistance (typical)	V _{DD} Operating Range ⁽²⁾	HV Interface	WiperLock Technology	Package
					Options (kΩ)				
MCP4017	I ² C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-6
MCP4012	U/D	64	Rheostat	RAM	2.1, 5.0, 10.0, 50.0	1.8V to 5.5V	Yes	No	SOT-23-6
MCP4022	U/D	64	Rheostat	EE	2.1, 5.0, 10.0, 50.0	2.7V to 5.5V	Yes	Yes	SOT-23-6
MCP4132	SPI	129	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	PDIP-8, SOIC-8, MSOP-8, DFN-8
MCP4142	SPI	129	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4152	SPI	257	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	
MCP4162	SPI	257	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4532	I ² C	129	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	MSOP-8, DFN-8
MCP4542	I ² C	129	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4552	I ² C	257	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	Yes	No	
MCP4562	I ² C	257	Rheostat	EE	5.0, 10.0, 50.0, 100.0	2.7V to 5.5V	Yes	Yes	
MCP4018	I ² C	128	Potentiometer	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-6
MCP4013	U/D	64	Potentiometer	RAM	2.1, 5.0, 10.0, 50.0	1.8V to 5.5V	Yes	No	SOT-23-6
MCP4023	U/D	64	Potentiometer	EE	2.1, 5.0, 10.0, 50.0	2.7V to 5.5V	Yes	Yes	SOT-23-6
MCP4019	I ² C	128	Rheostat	RAM	5.0, 10.0, 50.0, 100.0	1.8V to 5.5V	No	No	SC70-5
MCP4014	U/D	64	Rheostat	RAM	2.1, 5.0, 10.0, 50.0	1.8V to 5.5V	Yes	No	SOT-23-5
MCP4024	U/D	64	Rheostat	EE	2.1, 5.0, 10.0, 50.0	2.7V to 5.5V	Yes	Yes	SOT-23-5

Note 1: This table is broken into three groups by a thick line (and color coding). The unshaded devices in this table are the devices described in this data sheet, while the shaded devices offer a comparable resistor network configuration.

2: Analog characteristics only tested from 2.7V to 5.5V

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS}	-0.6V to +7.0V
Voltage on SCL, and SDA with respect to V_{SS}	-0.6V to 12.5V
Voltage on all other pins (A, W, and B) with respect to V_{SS}	-0.3V to $V_{DD} + 0.3V$
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ ON HV pins)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 20 mA
Maximum output current sunk by any Output pin	25 mA
Maximum output current sourced by any Output pin	25 mA
Maximum current out of V_{SS} pin	100 mA
Maximum current into V_{DD} pin	100 mA
Maximum current into A, W and B pins.....	± 2.5 mA
Package power dissipation ($T_A = +50^\circ\text{C}$, $T_J = +150^\circ\text{C}$) SC70-5	302 mW
SC70-6	TBD
Storage temperature	-65°C to $+150^\circ\text{C}$
Ambient temperature with power applied	-40°C to $+125^\circ\text{C}$
ESD protection on all pins	≥ 4 kV (HBM)
.....	≥ 400 V (MM)
Maximum Junction Temperature (T_J)	$+150^\circ\text{C}$

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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AC/DC CHARACTERISTICS

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to 5.5V , $5\text{ k}\Omega$, $10\text{ k}\Omega$, $50\text{ k}\Omega$, $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25^{\circ}\text{C}$.				
Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	Analog Characteristics specified
		1.8	—	5.5	V	Digital Characteristics specified
V_{DD} Start Voltage to ensure Wiper Reset	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(Note 7)			V/ms	
Delay after device exits the reset state ($V_{DD} > V_{BOR}$)	T_{BORD}	—	10	20	μS	
Supply Current (Note 8)	I_{DD}	—	45	80	μA	Serial Interface Active, Write all 0's to Volatile Wiper $V_{DD} = 5.5\text{V}$, $F_{SCL} = 400\text{ kHz}$
		—	2.5	5	μA	Serial Interface Inactive, (Stop condition, $SCL = SDA = V_{IH}$), Wiper = 0, $V_{DD} = 5.5\text{V}$

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4018** device only, includes V_{WZSE} and V_{WFSE} .

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to 5.5V , $5\text{ k}\Omega$, $10\text{ k}\Omega$, $50\text{ k}\Omega$, $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25^{\circ}\text{C}$.					
Parameters	Sym	Min	Typ	Max	Units	Conditions	
Resistance ($\pm 20\%$)	R_{AB}	4.0	5	6.0	$\text{k}\Omega$	-502 devices (Note 1)	
		8.0	10	12.0	$\text{k}\Omega$	-103 devices (Note 1)	
		40.0	50	60.0	$\text{k}\Omega$	-503 devices (Note 1)	
		80.0	100	120.0	$\text{k}\Omega$	-104 devices (Note 1)	
Resolution	N	128			Taps	No Missing Codes	
Step Resistance	R_S	—	$R_{AB} / (127)$	—	Ω	Note 5	
Wiper Resistance	R_W	—	100	170	Ω	$V_{DD} = 5.5\text{ V}$, $I_W = 2.0\text{ mA}$, code = 00h	
		—	155	325	Ω	$V_{DD} = 2.7\text{ V}$, $I_W = 2.0\text{ mA}$, code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB}/\Delta T$	—	50	—	$\text{ppm}/^{\circ}\text{C}$	$T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	
		—	100	—	$\text{ppm}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	
		—	150	—	$\text{ppm}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	
Ratiometric Tempco	$\Delta V_{WB}/\Delta T$	—	15	—	$\text{ppm}/^{\circ}\text{C}$	Code = Midscale (3Fh)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	V_{SS}	—	V_{DD}	V	Note 4, Note 5	
Maximum current through Terminal (A, W or B) Note 5	I_T	—	—	2.5	mA	Terminal A	I_{AW} , W = Full Scale (FS)
		—	—	2.5	mA	Terminal B	I_{BW} , W = Zero Scale (ZS)
		—	—	2.5	mA	Terminal W	I_{AW} or I_{BW} , W = FS or ZS
		—	—	1.38	mA	Terminal A and Terminal B	I_{AB} , $V_B = 0\text{V}$, $V_A = 5.5\text{V}$, $R_{AB(MIN)} = 4000$
		—	—	0.688	mA		I_{AB} , $V_B = 0\text{V}$, $V_A = 5.5\text{V}$, $R_{AB(MIN)} = 8000$
		—	—	0.138	mA		I_{AB} , $V_B = 0\text{V}$, $V_A = 5.5\text{V}$, $R_{AB(MIN)} = 40000$
		—	—	0.069	mA		I_{AB} , $V_B = 0\text{V}$, $V_A = 5.5\text{V}$, $R_{AB(MIN)} = 80000$

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
- 3:** **MCP4018** device only, includes V_{WZSE} and V_{WFSE} .
- 4:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 5:** This specification by design.
- 6:** Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
- 7:** POR/BOR is not rate dependent.
- 8:** Supply current is independent of current through the resistor network

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to 5.5V , $5\text{ k}\Omega$, $10\text{ k}\Omega$, $50\text{ k}\Omega$, $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25^{\circ}\text{C}$.					
Parameters	Sym	Min	Typ	Max	Units	Conditions	
Full Scale Error (MCP4018 only) (code = 7Fh)	V_{WFSE}	-3.0	-0.1	—	LSb	5 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-2.0	-0.1	—	LSb	10 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-0.5	-0.1	—	LSb	50 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-0.5	-0.1	—	LSb	100 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
Zero Scale Error (MCP4018 only) (code = 00h)	V_{WZSE}	—	+0.1	+3.0	LSb	5 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+2.0	LSb	10 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+0.5	LSb	50 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+0.5	LSb	100 k Ω	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$
Potentiometer Integral Non-linearity	INL	-0.5	± 0.25	+0.5	LSb	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$ MCP4018 device only (Note 2)	
Potentiometer Differential Non- linearity	DNL	-0.25	± 0.125	+0.25	LSb	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$ MCP4018 device only (Note 2)	
Bandwidth -3 dB (See Figure 2-83, load = 30 pF)	BW	—	2	—	MHz	5 k Ω	Code = 3Fh
		—	1	—	MHz	10 k Ω	Code = 3Fh
		—	260	—	kHz	50 k Ω	Code = 3Fh
		—	100	—	kHz	100 k Ω	Code = 3Fh

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: MCP4018 device only, includes V_{WZSE} and V_{WFSE} .

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified)							
		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)							
		All parameters apply across the specified operating ranges unless noted.							
		$V_{DD} = +2.7\text{V to } 5.5\text{V}$, 5 k Ω , 10 k Ω , 50 k Ω , 100 k Ω devices.							
		Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25^{\circ}\text{C}$.							
Parameters	Sym	Min	Typ	Max	Units	Conditions			
Rheostat Integral Non-linearity MCP4018 (Note 3) MCP4017 and MCP4019 devices only (Note 3)	R-INL	-2.0	± 0.5	+2.0	LSb	5 k Ω	5.5V, $I_W = 900 \mu\text{A}$		
		-5.0	+3.5	+5.0	LSb		2.7V, $I_W = 430 \mu\text{A}$ (Note 6)		
		See Section 2.0			LSb		1.8V (Note 6)		
				-2.0	± 0.5	+2.0	LSb	10 k Ω	5.5V, $I_W = 450 \mu\text{A}$
				-4.0	+2.5	+4.0	LSb		2.7V, $I_W = 215 \mu\text{A}$ (Note 6)
				See Section 2.0			LSb		1.8V (Note 6)
				-1.125	± 0.5	+1.125	LSb	50 k Ω	5.5V, $I_W = 90 \mu\text{A}$
				-1.5	+1	+1.5	LSb		2.7V, $I_W = 43 \mu\text{A}$ (Note 6)
				See Section 2.0			LSb		1.8V (Note 6)
				-0.8	± 0.5	+0.8	LSb	100 k Ω	5.5V, $I_W = 45 \mu\text{A}$
				-1.125	+0.25	+1.125	LSb		2.7V, $I_W = 21.5 \mu\text{A}$ (Note 6)
				See Section 2.0			LSb		1.8V (Note 6)
Rheostat Differential Non-linearity MCP4018 (Note 3) MCP4017 and MCP4019 devices only (Note 3)	R-DNL	-0.5	± 0.25	+0.5	LSb	5 k Ω	5.5V, $I_W = 900 \text{mA}$		
		-0.75	+0.5	+0.75	LSb		2.7V, $I_W = 430 \mu\text{A}$ (Note 6)		
		See Section 2.0			LSb		1.8V (Note 6)		
				-0.5	± 0.25	+0.5	LSb	10 k Ω	5.5V, $I_W = 450 \mu\text{A}$
				-0.75	+0.5	+0.75	LSb		2.7V, $I_W = 215 \mu\text{A}$ (Note 6)
				See Section 2.0			LSb		1.8V (Note 6)
				-0.375	± 0.25	+0.375	LSb	50 k Ω	5.5V, $I_W = 90 \mu\text{A}$
				-0.375	± 0.25	+0.375	LSb		2.7V, $I_W = 43 \mu\text{A}$ (Note 6)
				See Section 2.0			LSb		1.8V (Note 6)
				-0.375	± 0.25	+0.375	LSb	100 k Ω	5.5V, $I_W = 45 \mu\text{A}$
				-0.375	± 0.25	+0.375	LSb		2.7V, $I_W = 21.5 \mu\text{A}$ (Note 6)
				See Section 2.0			LSb		1.8V (Note 6)
Capacitance (P_A)	C_{AW}	—	75	—	pF	f = 1 MHz, Code = Full Scale			
Capacitance (P_W)	C_W	—	120	—	pF	f = 1 MHz, Code = Full Scale			
Capacitance (P_B)	C_{BW}	—	75	—	pF	f = 1 MHz, Code = Full Scale			

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
- 3:** **MCP4018** device only, includes V_{WZSE} and V_{WFSE} .
- 4:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 5:** This specification by design.
- 6:** Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
- 7:** POR/BOR is not rate dependent.
- 8:** Supply current is independent of current through the resistor network

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified)						
		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)						
		All parameters apply across the specified operating ranges unless noted.						
		$V_{DD} = +2.7\text{V}$ to 5.5V , $5\text{ k}\Omega$, $10\text{ k}\Omega$, $50\text{ k}\Omega$, $100\text{ k}\Omega$ devices.						
		Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25^{\circ}\text{C}$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions		
Digital Inputs/Outputs (SDA, SCK)								
Schmitt Trigger High Input Threshold	V_{IH}	$0.7 V_{DD}$	—	—	V	$1.8\text{V} \leq V_{DD} \leq 5.5\text{V}$		
Schmitt Trigger Low Input Threshold	V_{IL}	-0.5	—	$0.3V_{DD}$	V			
Hysteresis of Schmitt Trigger Inputs (Note 5)	V_{HYS}	—	$0.1V_{DD}$	—	V	All inputs except SDA and SCL		
		N.A.	—	—	V			
		N.A.	—	—	V		SDA and SCL	
		$0.1 V_{DD}$	—	—	V			100 kHz
		$0.05 V_{DD}$	—	—	V			
Output Low Voltage (SDA)	V_{OL}	V_{SS}	—	$0.2V_{DD}$	V	$V_{DD} < 2.0\text{V}$, $I_{OL} = 1\text{ mA}$		
		V_{SS}	—	0.4	V	$V_{DD} \geq 2.0\text{V}$, $I_{OL} = 3\text{ mA}$		
Input Leakage Current	I_{IL}	-1	—	1	μA	$V_{IN} = V_{DD}$ and $V_{IN} = V_{SS}$		
Pin Capacitance	C_{IN} , C_{OUT}	—	10	—	pF	$f_C = 400\text{ kHz}$		
RAM (Wiper) Value								
Value Range	N	0h	—	7Fh	hex			
Wiper POR/BOR Value	$N_{POR/BOR}$	3Fh			hex			
Power Requirements								
Power Supply Sensitivity (MCP4018 only)	PSS	—	0.0005	0.0035	%/%	$V_{DD} = 2.7\text{V}$ to 5.5V , $V_A = 2.7\text{V}$, Code = 3Fh		

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4018** device only, includes V_{WZSE} and V_{WFSE} .

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This specification by design.

6: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

7: POR/BOR is not rate dependent.

8: Supply current is independent of current through the resistor network

1.1 I²C Mode Timing Waveforms and Requirements

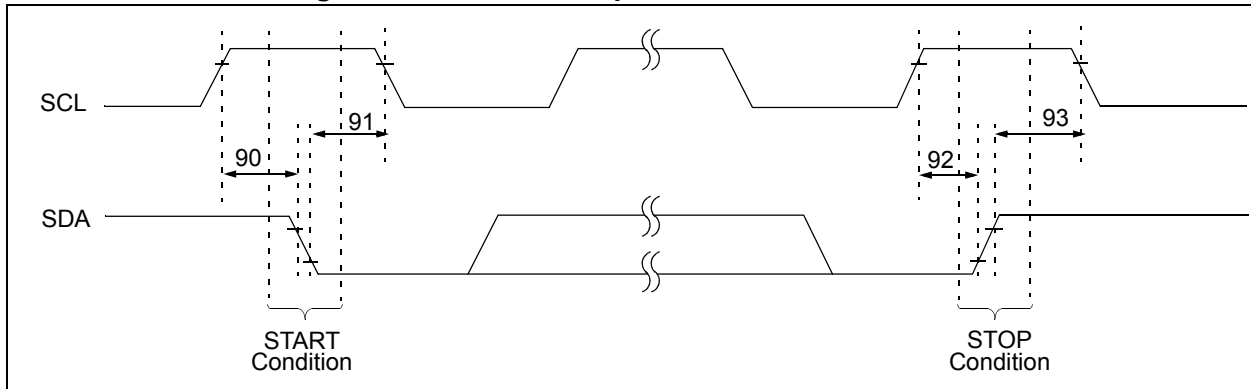


FIGURE 1-1: I²C Bus Start/Stop Bits Timing Waveforms.

TABLE 1-1: I²C BUS START/STOP BITS REQUIREMENTS

I ² C AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (Extended) Operating Voltage V_{DD} range is described in Section 2.0 "Typical Performance Curves"					
Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions	
	F_{SCL}						
		Standard Mode	0	100	kHz	$C_b = 400 \text{ pF}$, 1.8V - 5.5V	
		Fast Mode	0	400	kHz	$C_b = 400 \text{ pF}$, 2.7V - 5.5V	
D102	C_b	Bus capacitive loading					
		100 kHz mode	—	400	pF		
		400 kHz mode	—	400	pF		
90	$T_{SU:STA}$	START condition Setup time	100 kHz mode 400 kHz mode	4700 600	— —	ns ns	Only relevant for repeated START condition
91	$T_{HD:STA}$	START condition Hold time	100 kHz mode 400 kHz mode	4000 600	— —	ns ns	After this period the first clock pulse is generated
92	$T_{SU:STO}$	STOP condition Setup time	100 kHz mode 400 kHz mode	4000 600	— —	ns ns	
93	$T_{HD:STO}$	STOP condition Hold time	100 kHz mode 400 kHz mode	4000 600	— —	ns ns	

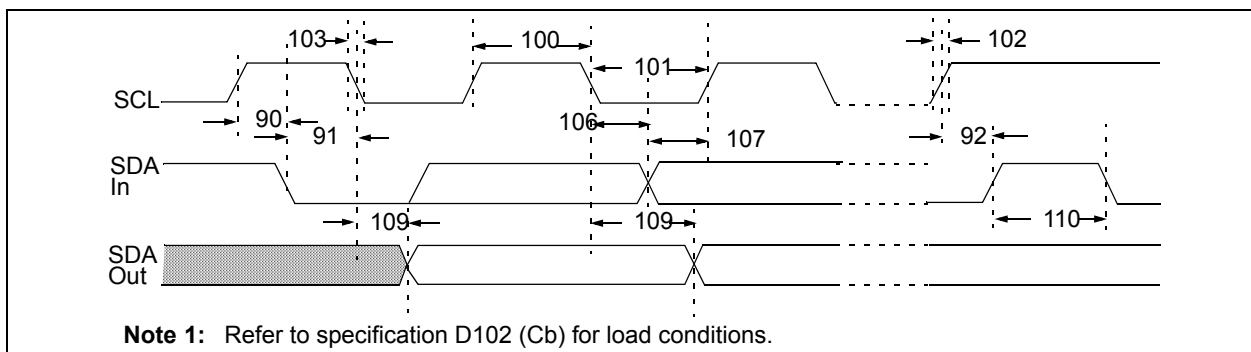


FIGURE 1-2: I²C Bus Data Timing.

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TABLE 1-2: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

I ² C AC Characteristics			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (Extended)				
			Operating Voltage VDD range is described in AC/DC characteristics				
Parameter No.	Sym	Characteristic	Min	Max	Units	Conditions	
100	T _{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
101	T _{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
102A (5)	T _{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
102B (5)	T _{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
103A (5)	T _{FSCL}	SCL fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	40	ns	
103B (5)	T _{FSDA}	SDA fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb (4)	300	ns	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V, Note 6
			400 kHz mode	0	—	ns	2.7V-5.5V, Note 6
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	(2)
			400 kHz mode	100	—	ns	
109	T _{AA}	Output valid from clock	100 kHz mode	—	3450	ns	(1)
			400 kHz mode	—	900	ns	
110	T _{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
	T _{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	Philips Spec states N.A.
			400 kHz mode	—	50	ns	

- Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- 2:** A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu; DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
 $T_R \text{ max.} + t_{su}; \text{DAT} = 1000 + 250 = 1250 \text{ ns}$ (according to the standard-mode I²C bus specification) before the SCL line is released.
- 3:** The MCP4018/MCP4019 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to guarantee that the output data will meet the setup and hold specifications for the receiving device.
- 4:** Use Cb in pF for the calculations.
- 5:** Not Tested.
- 6:** A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70 (Note 1)	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 6L-SC70	θ_{JA}	—	TBD	—	°C/W	

Note 1: Package Power Dissipation (PDIS) is calculated as follows:

$$P_{DIS} = (T_J - T_A) / \theta_{JA}$$

where: T_J = Junction Temperature, T_A = Ambient Temperature.

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NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

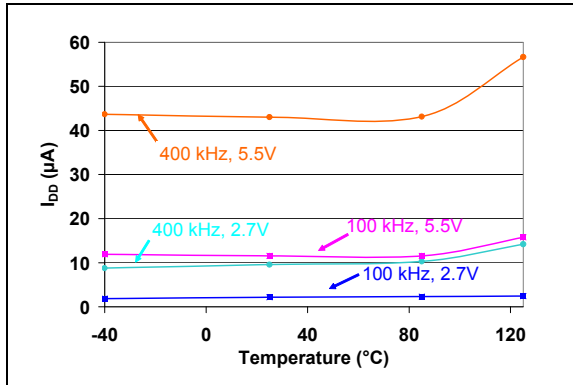


FIGURE 2-1: Interface Active Current (I_{DD}) vs. SCL Frequency (f_{SCL}) and Temperature ($V_{DD} = 1.8\text{V}$, 2.7V and 5.5V).

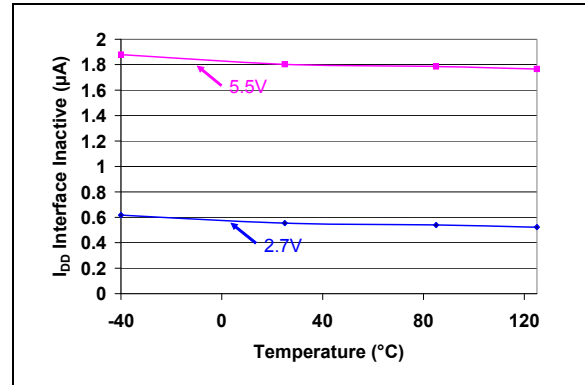


FIGURE 2-2: Interface Inactive Current (I_{SHDN}) vs. Temperature and V_{DD} . ($V_{DD} = 1.8\text{V}$, 2.7V and 5.5V).

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

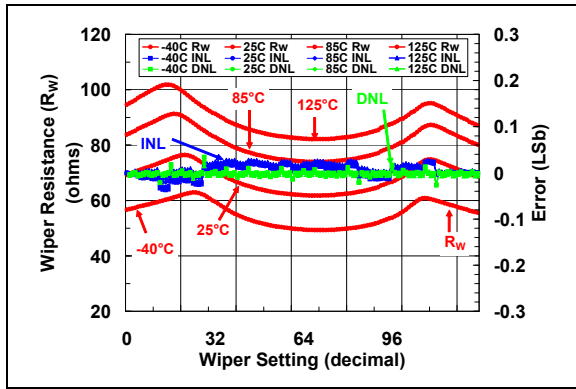


FIGURE 2-3: 5.0 kΩ: Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$). ($A = V_{DD}$, $B = V_{SS}$).

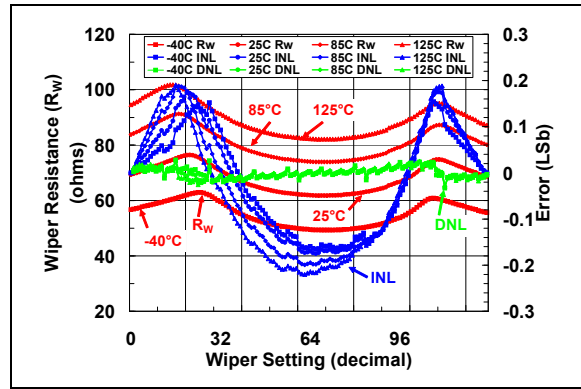


FIGURE 2-6: 5.0 kΩ: Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$). ($I_W = 1.4\text{mA}$, $B = V_{SS}$).

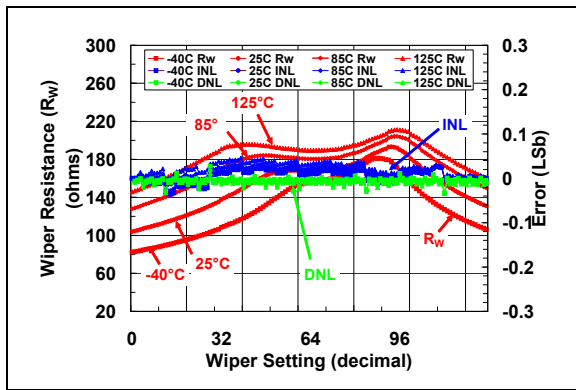


FIGURE 2-4: 5.0 kΩ: Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$). ($A = V_{DD}$, $B = V_{SS}$).

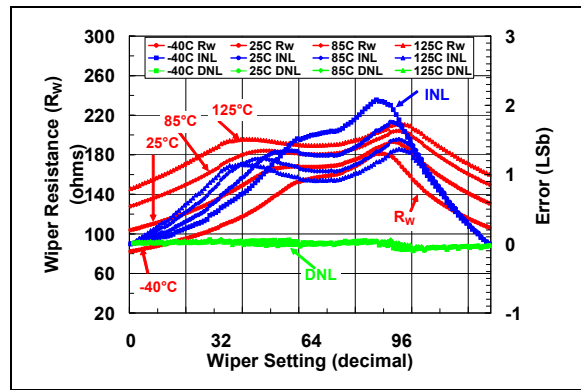


FIGURE 2-7: 5.0 kΩ: Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$). ($I_W = 450\mu\text{A}$, $B = V_{SS}$).

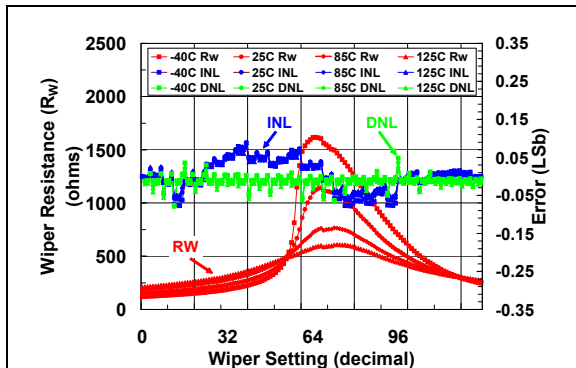


FIGURE 2-5: 5.0 kΩ: Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$). ($A = V_{DD}$, $B = V_{SS}$)

Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

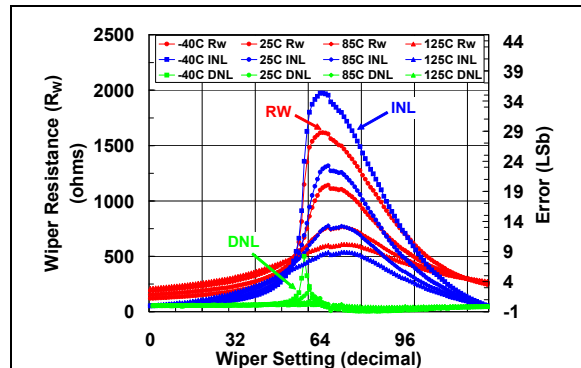


FIGURE 2-8: 5.0 kΩ: Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$). ($I_W = \text{TBD}$, $B = V_{SS}$)

Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

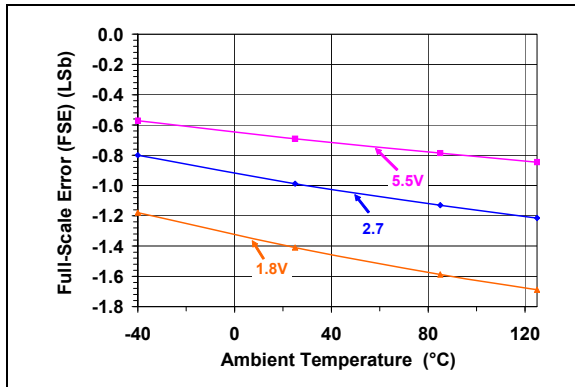


FIGURE 2-9: 5.0 k Ω : Full Scale Error (FSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

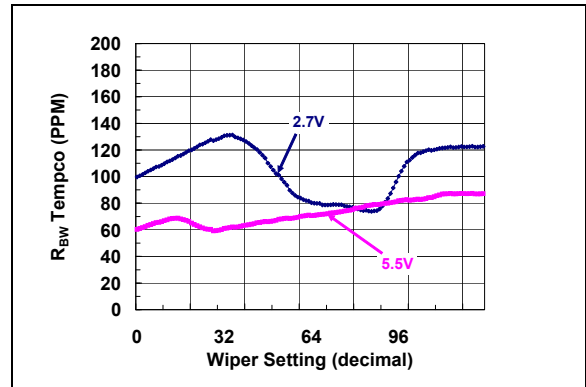


FIGURE 2-12: 5.0 k Ω : R_{BW} Tempco $\Delta R_{WB} / \Delta T$ vs. Code.

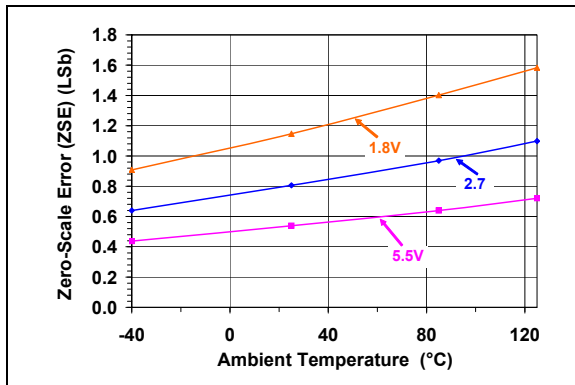


FIGURE 2-10: 5.0 k Ω : Zero Scale Error (ZSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

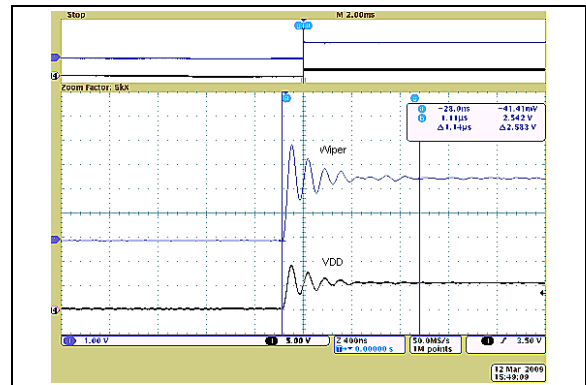


FIGURE 2-13: 5.0 k Ω : Power-Up Wiper Response Time.

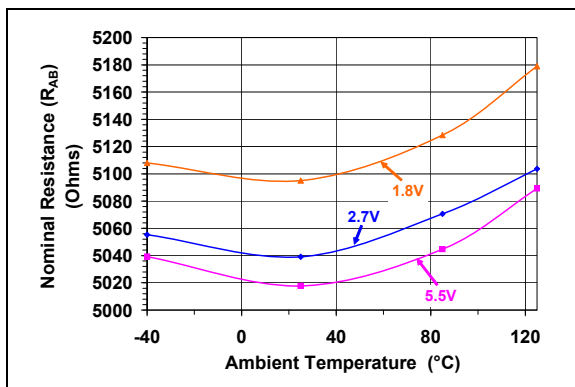


FIGURE 2-11: 5.0 k Ω : Nominal Resistance (Ω) vs. Temperature and V_{DD} .

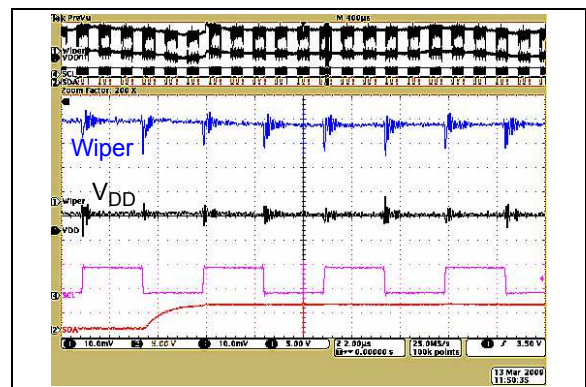


FIGURE 2-14: 5.0 k Ω : Digital Feedthrough (SCL signal coupling to Wiper pin).

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

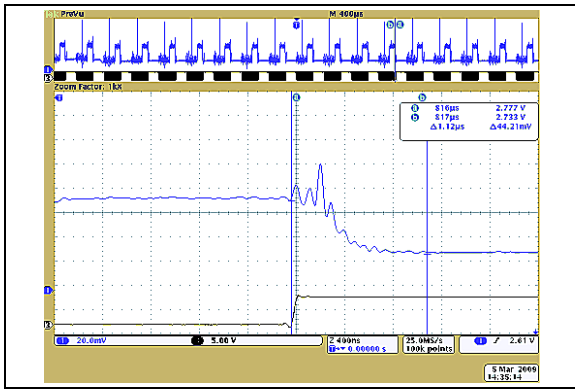


FIGURE 2-15: 5.0 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=5.5\text{V}$).

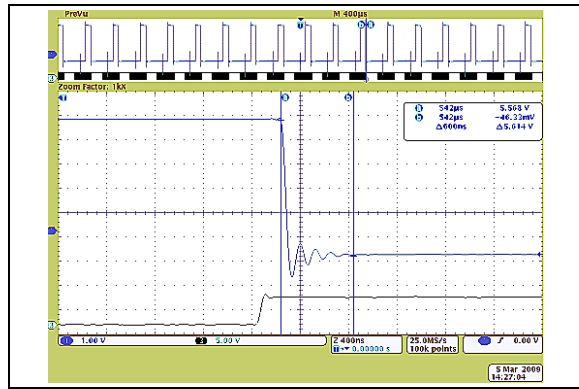


FIGURE 2-18: 5.0 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=5.5\text{V}$).

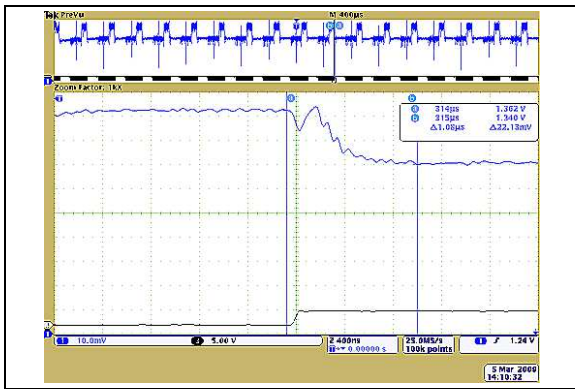


FIGURE 2-16: 5.0 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=2.7\text{V}$).

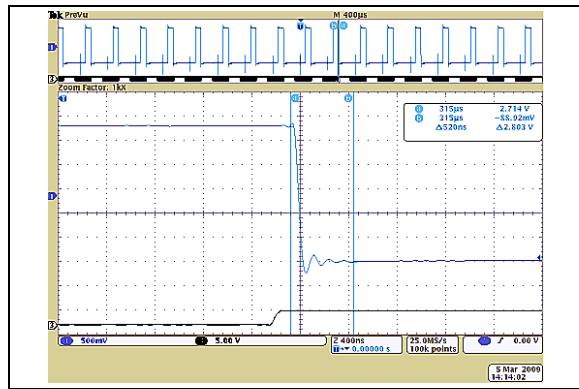


FIGURE 2-19: 5.0 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=2.7\text{V}$).

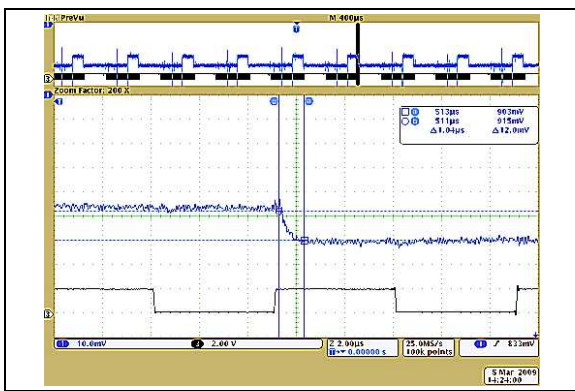


FIGURE 2-17: 5.0 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=1.8\text{V}$).

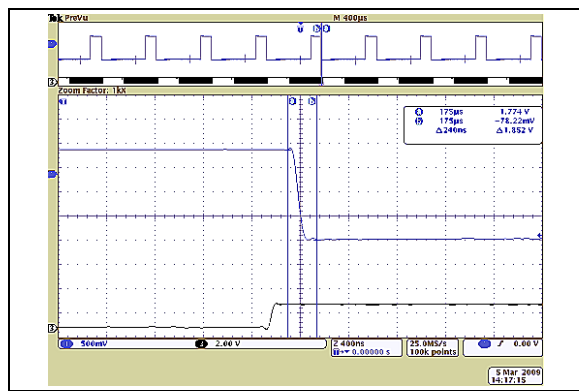


FIGURE 2-20: 5.0 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=1.8\text{V}$).

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

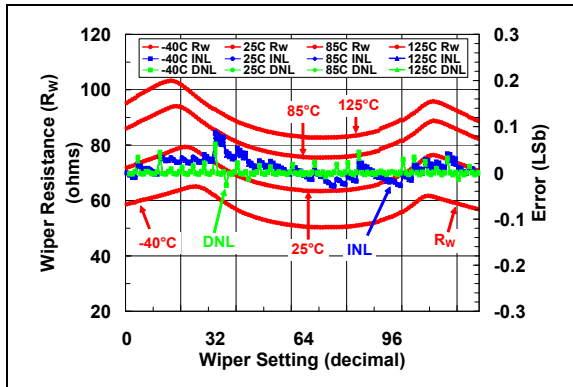


FIGURE 2-21: 10 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$). ($A = V_{DD}$, $B = V_{SS}$)

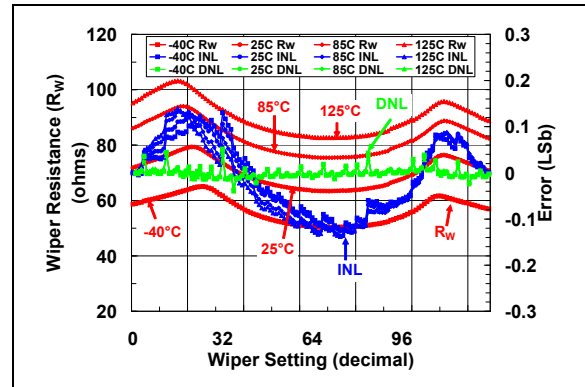


FIGURE 2-24: 10 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$). ($I_W = 450\mu\text{A}$, $B = V_{SS}$)

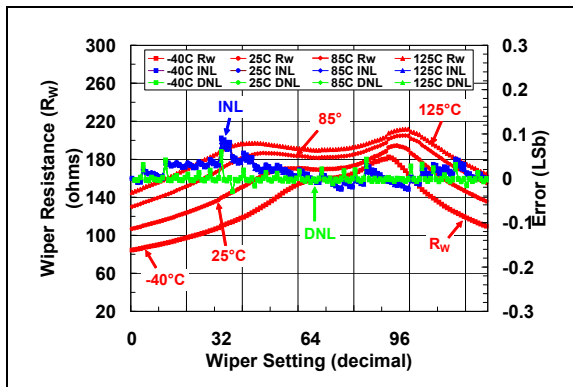


FIGURE 2-22: 10 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$). ($A = V_{DD}$, $B = V_{SS}$)

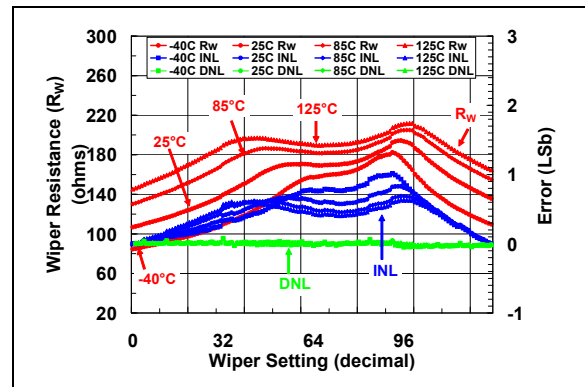
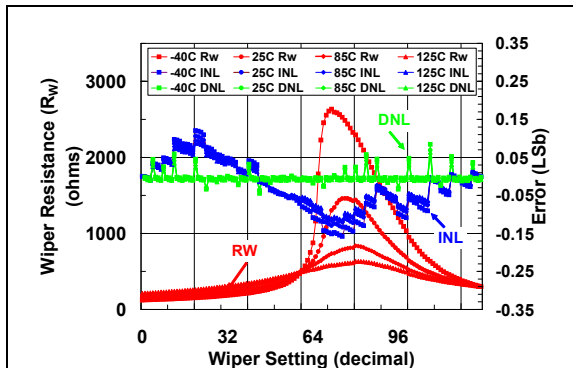
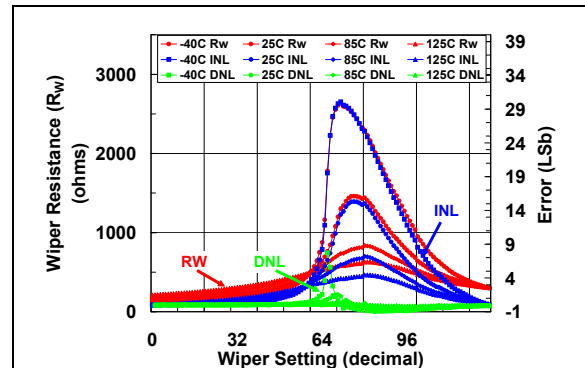


FIGURE 2-25: 10 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$). ($I_W = 210\mu\text{A}$, $B = V_{SS}$)



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-23: 10 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$). ($A = V_{DD}$, $B = V_{SS}$)



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-26: 10 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$). ($I_W = \text{TBD}$, $B = V_{SS}$)

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

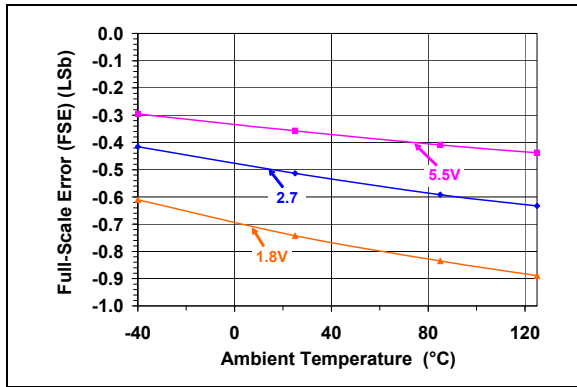


FIGURE 2-27: 10 kΩ : Full Scale Error (FSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

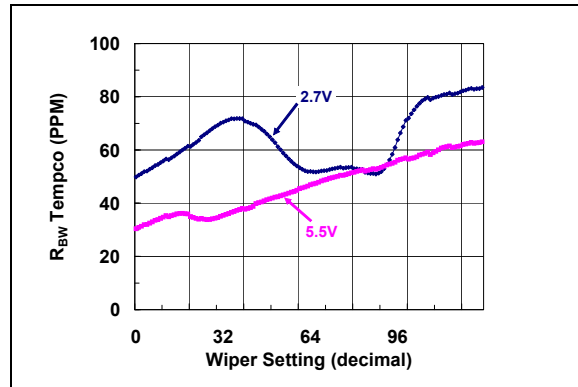


FIGURE 2-30: 10 kΩ : R_{BW} Tempco $\Delta R_{WB} / \Delta T$ vs. Code.

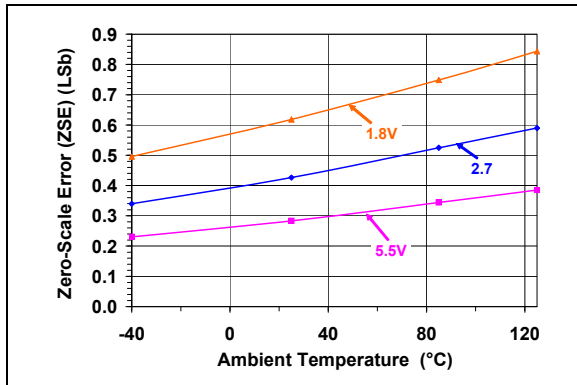


FIGURE 2-28: 10 kΩ : Zero Scale Error (ZSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

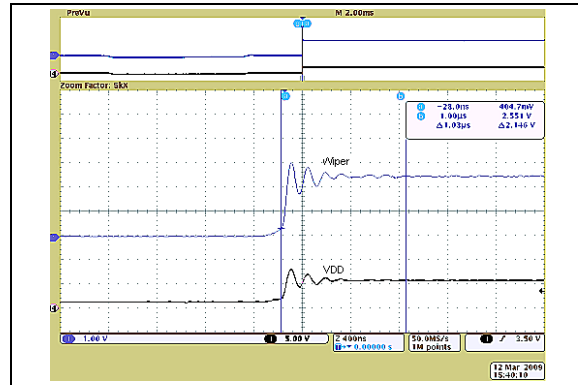


FIGURE 2-31: 10 kΩ : Power-Up Wiper Response Time.

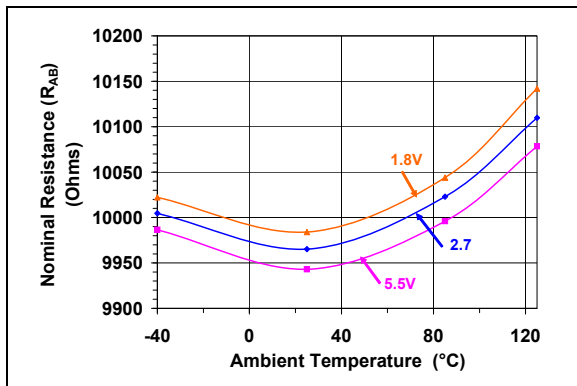


FIGURE 2-29: 10 kΩ : Nominal Resistance (Ω) vs. Temperature and V_{DD} .

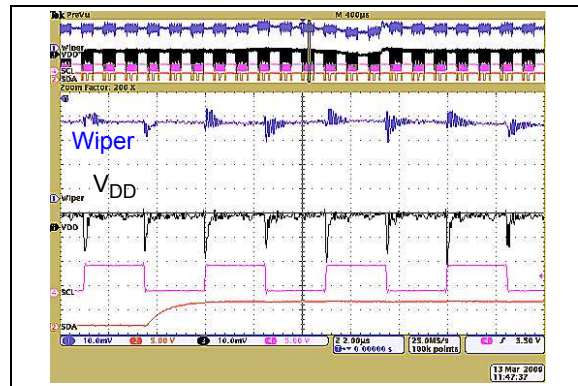


FIGURE 2-32: 10 kΩ : Digital Feedthrough (SCL signal coupling to Wiper pin).

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

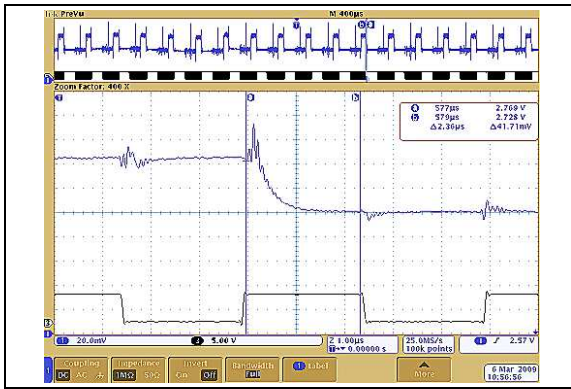


FIGURE 2-33: 10 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=5.5\text{V}$).

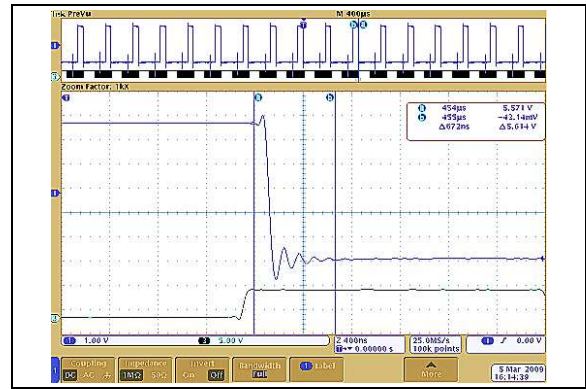


FIGURE 2-36: 10 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=5.5\text{V}$).

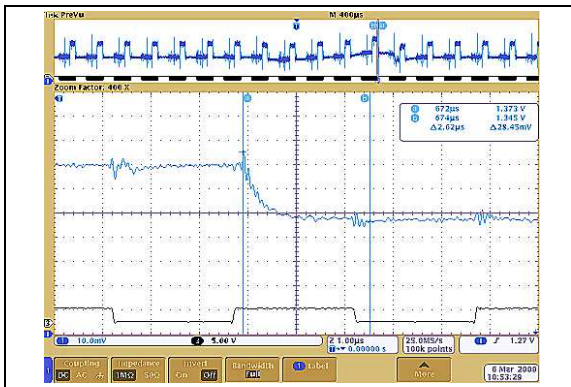


FIGURE 2-34: 10 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=2.7\text{V}$).

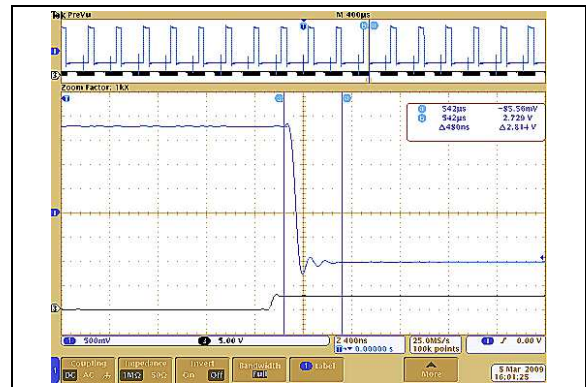


FIGURE 2-37: 10 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=2.7\text{V}$).

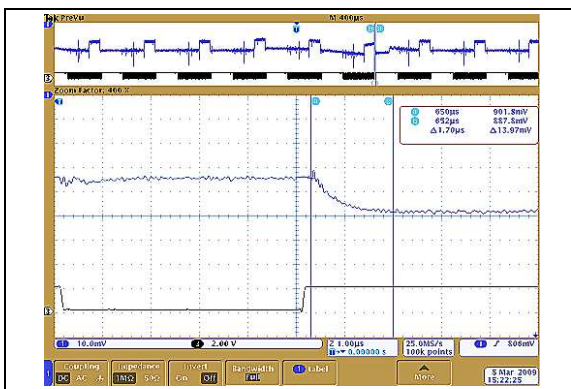


FIGURE 2-35: 10 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=1.8\text{V}$).

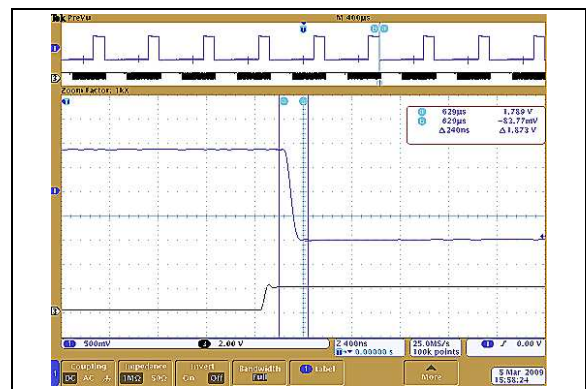


FIGURE 2-38: 10 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=1.8\text{V}$).

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

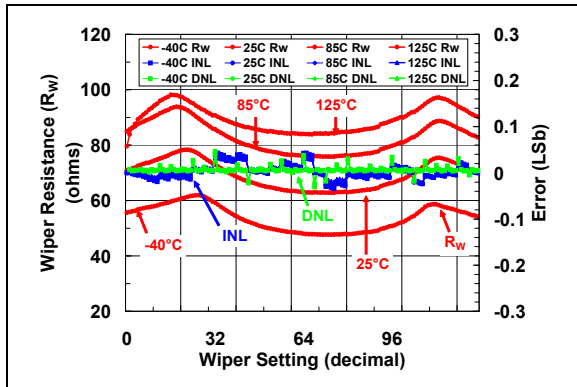


FIGURE 2-39: 50 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$).

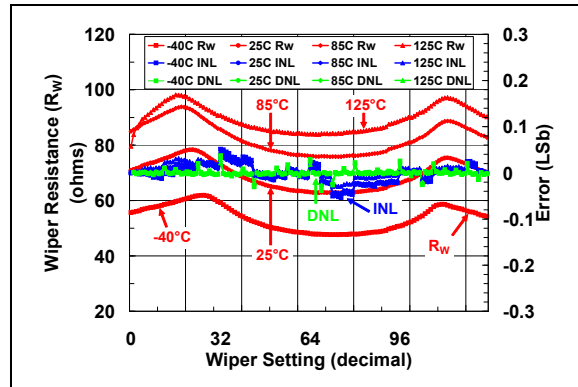


FIGURE 2-42: 50 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$). ($I_W = 90\mu\text{A}$, $B = V_{SS}$)

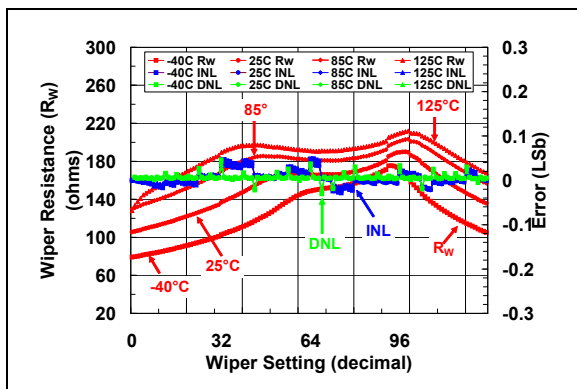


FIGURE 2-40: 50 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$).

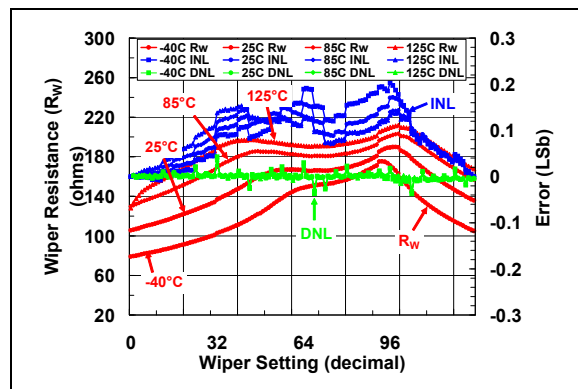
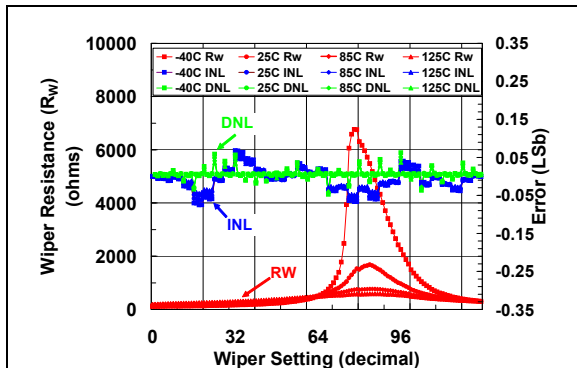
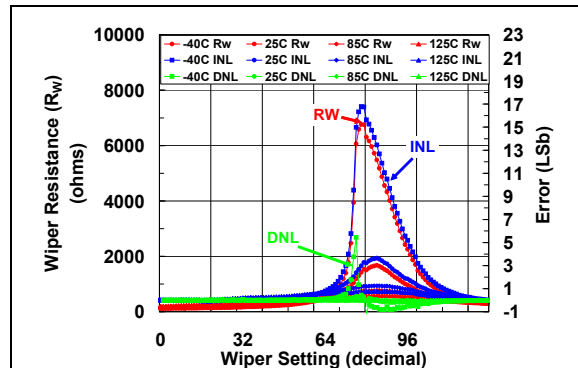


FIGURE 2-43: 50 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$). ($I_W = 45\mu\text{A}$, $B = V_{SS}$)



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-41: 50 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$).



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-44: 50 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$). ($I_W = \text{TBD}$, $B = V_{SS}$)

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

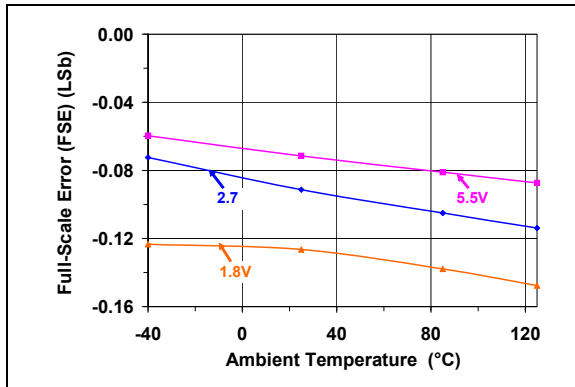


FIGURE 2-45: 50 k Ω : Full Scale Error (FSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

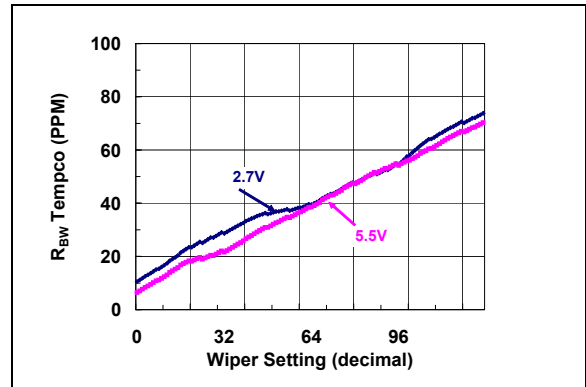


FIGURE 2-48: 50 k Ω : R_{BW} Tempco $\Delta R_{WB} / \Delta T$ vs. Code.

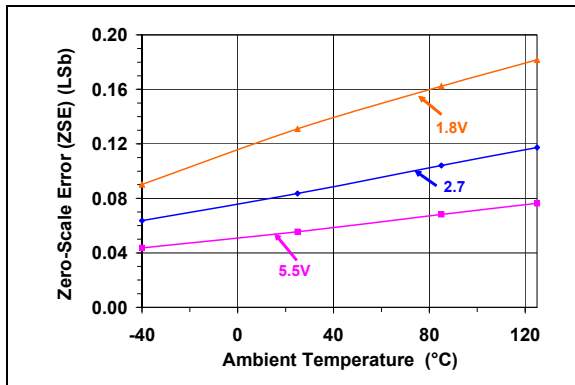


FIGURE 2-46: 50 k Ω : Zero Scale Error (ZSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

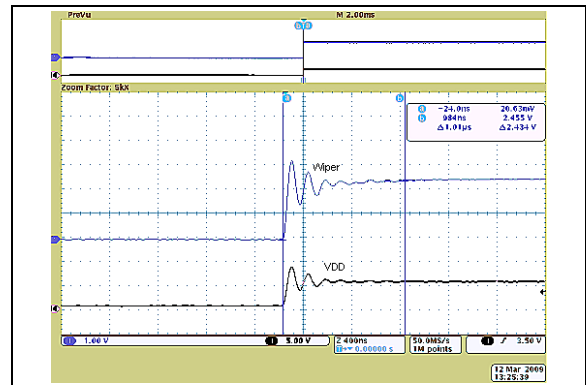


FIGURE 2-49: 50 k Ω : Power-Up Wiper Response Time.

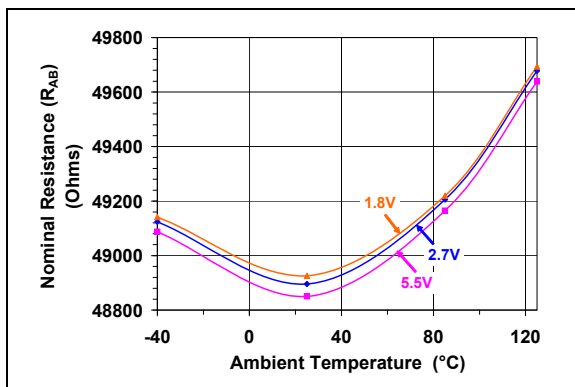


FIGURE 2-47: 50 k Ω : Nominal Resistance (Ω) vs. Temperature and V_{DD} .

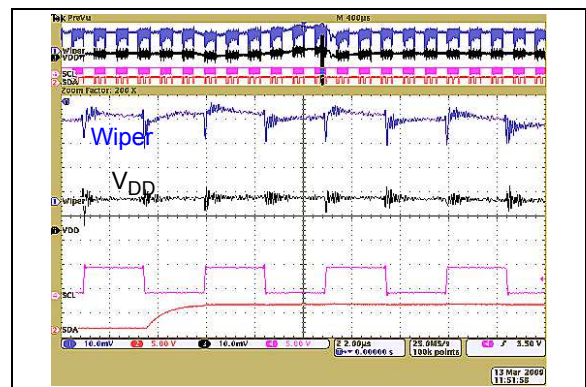


FIGURE 2-50: 50 k Ω : Digital Feedthrough (SCL signal coupling to Wiper pin).

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

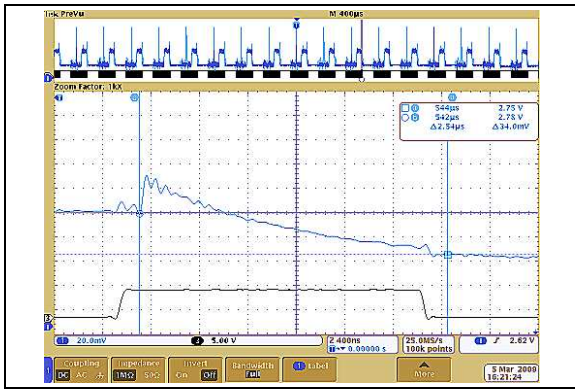


FIGURE 2-51: 50 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=5.5\text{V}$).

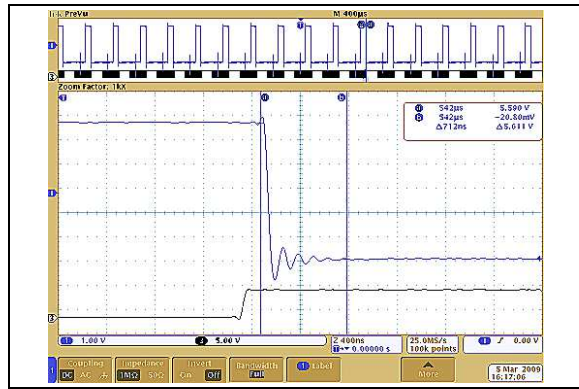


FIGURE 2-54: 50 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=5.5\text{V}$).

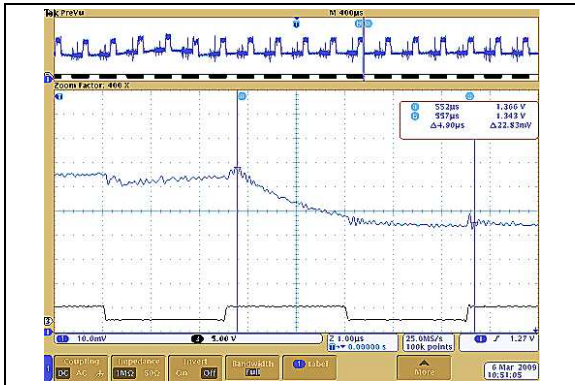


FIGURE 2-52: 50 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=2.7\text{V}$).

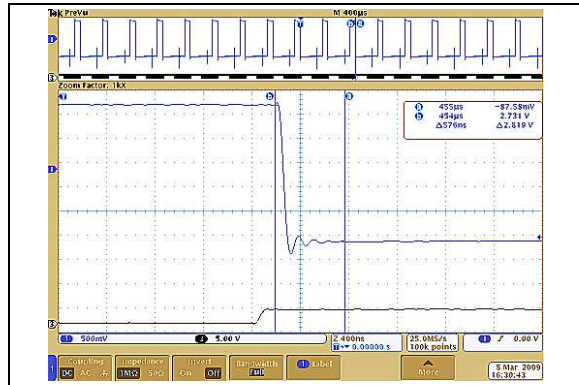


FIGURE 2-55: 50 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=2.7\text{V}$).

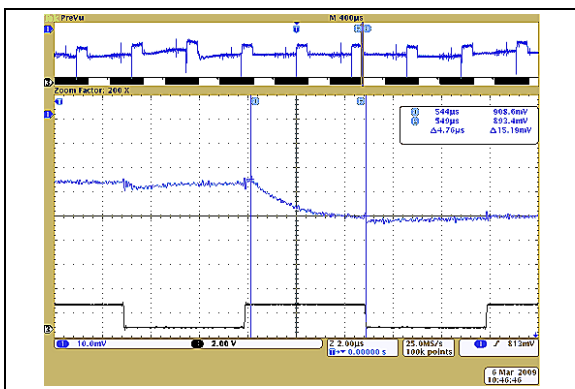


FIGURE 2-53: 50 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD}=1.8\text{V}$).

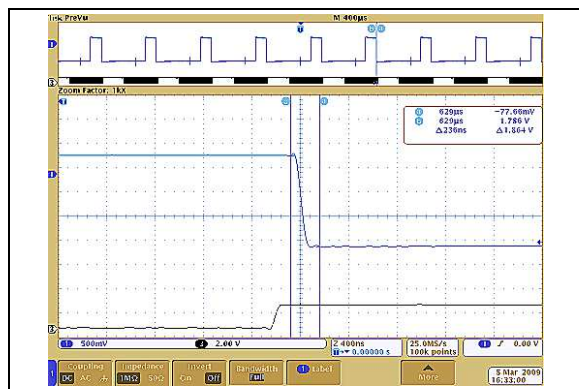


FIGURE 2-56: 50 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD}=1.8\text{V}$).

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

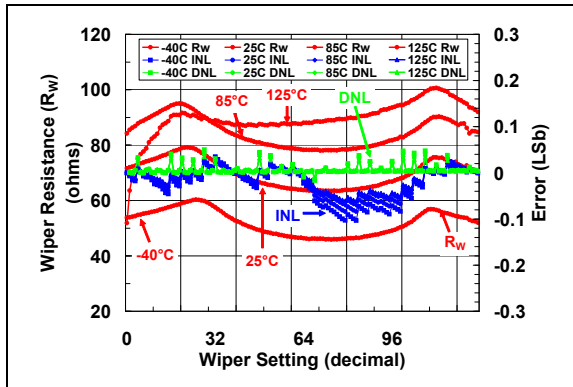


FIGURE 2-57: 100 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$).

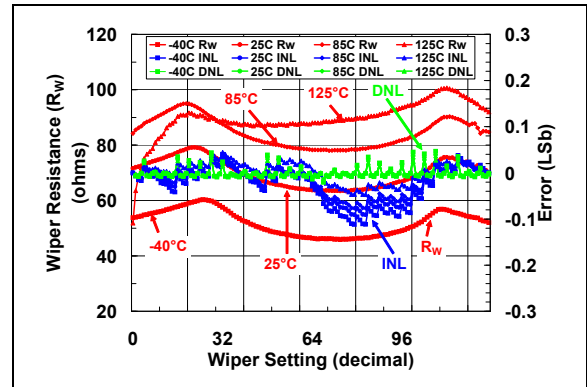


FIGURE 2-60: 100 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 5.5\text{V}$). ($I_W = 45\mu\text{A}$, $B = V_{SS}$)

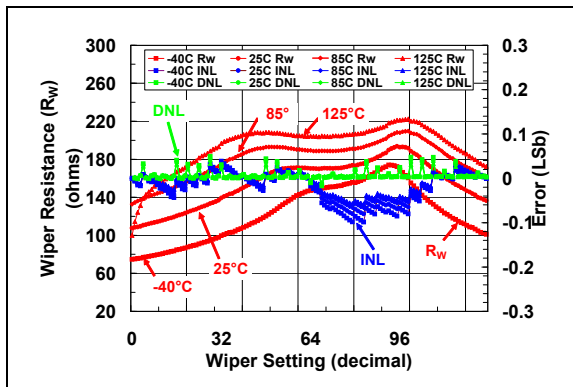


FIGURE 2-58: 100 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$).

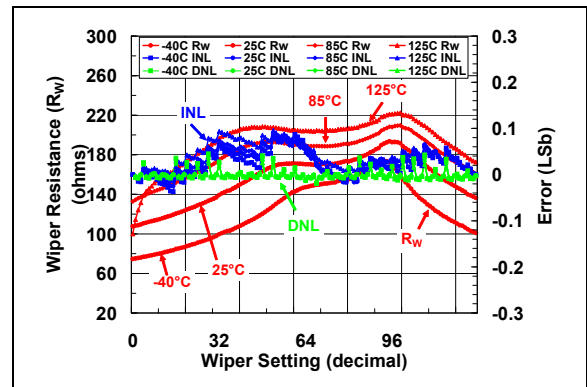
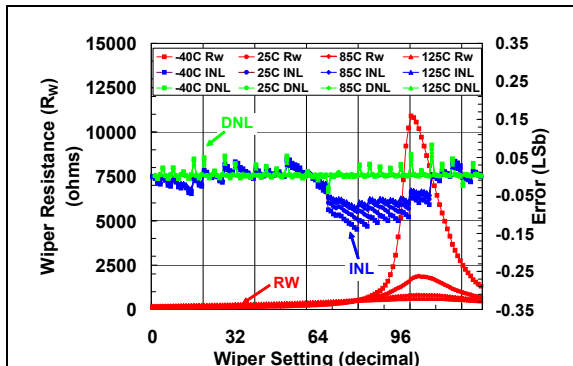
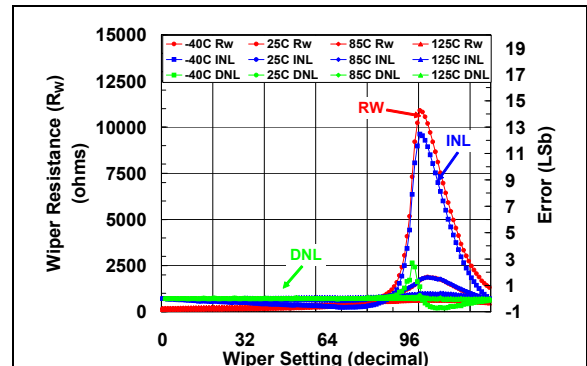


FIGURE 2-61: 100 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 2.7\text{V}$). ($I_W = 21\mu\text{A}$, $B = V_{SS}$)



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-59: 100 kΩ Pot Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$).



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-62: 100 kΩ Rheo Mode : R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Temperature ($V_{DD} = 1.8\text{V}$). ($I_W = \text{TBD}$, $B = V_{SS}$)

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

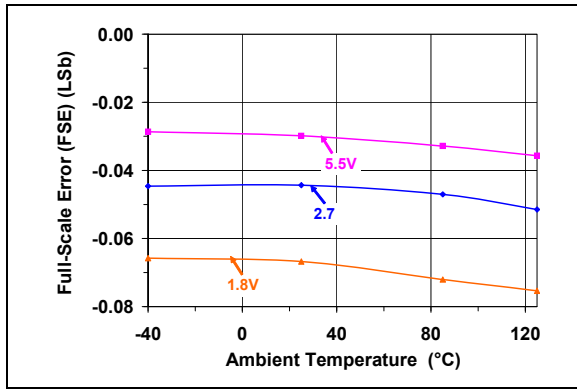


FIGURE 2-63: 100 kΩ : Full Scale Error (FSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

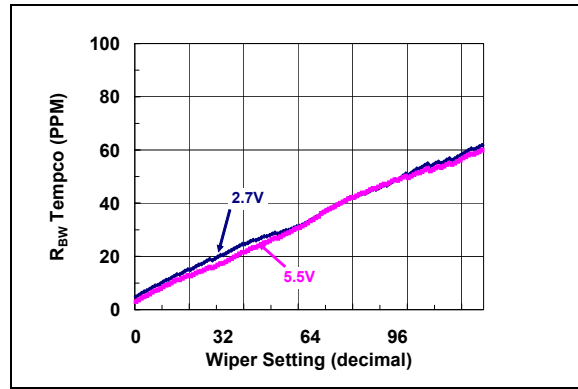


FIGURE 2-66: 100 kΩ : R_{BW} Tempco $\Delta R_{WB} / \Delta T$ vs. Code.

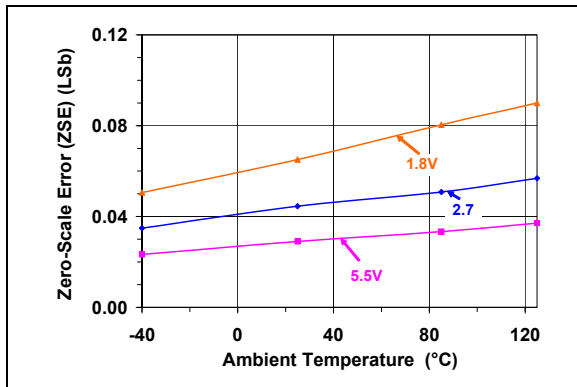


FIGURE 2-64: 100 kΩ : Zero Scale Error (ZSE) vs. Temperature ($V_{DD} = 5.5\text{V}, 2.7\text{V}, 1.8\text{V}$).

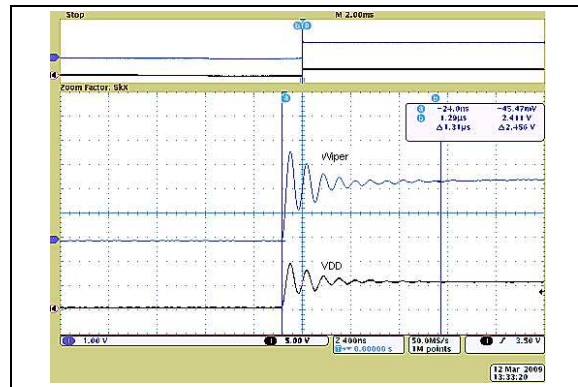


FIGURE 2-67: 100 kΩ : Power-Up Wiper Response Time.

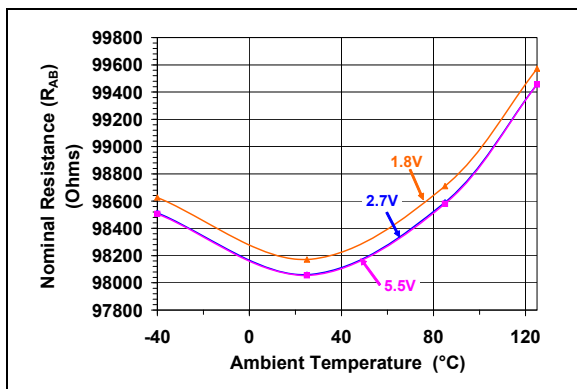


FIGURE 2-65: 100 kΩ : Nominal Resistance (Ω) vs. Temperature and V_{DD} .

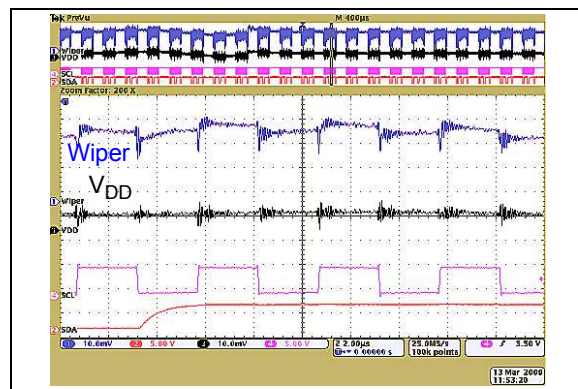


FIGURE 2-68: 100 kΩ : Digital Feedthrough (SCL signal coupling to Wiper pin).

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$.

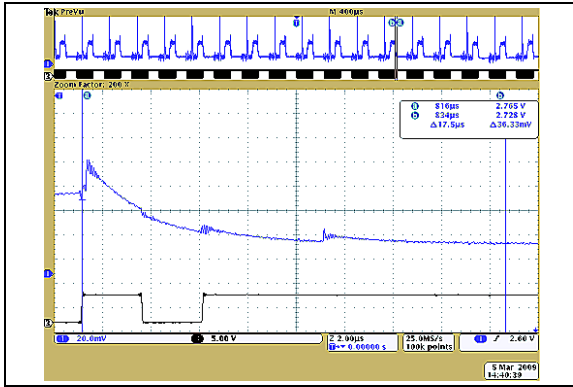


FIGURE 2-69: 100 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD} = 5.5\text{V}$).

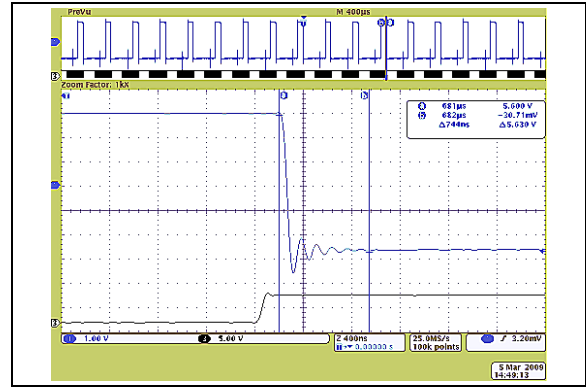


FIGURE 2-72: 100 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD} = 5.5\text{V}$).

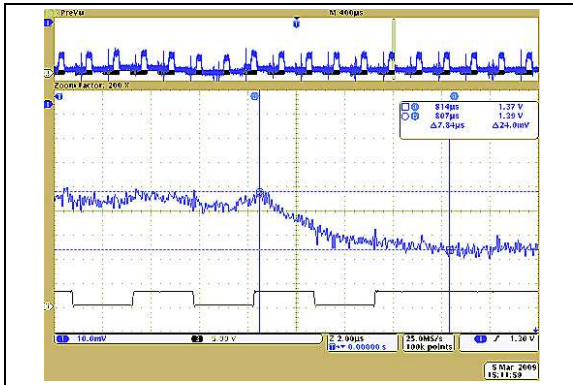


FIGURE 2-70: 100 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD} = 2.7\text{V}$).

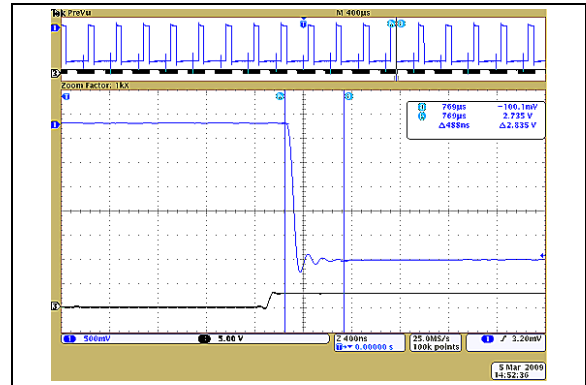


FIGURE 2-73: 100 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD} = 2.7\text{V}$).

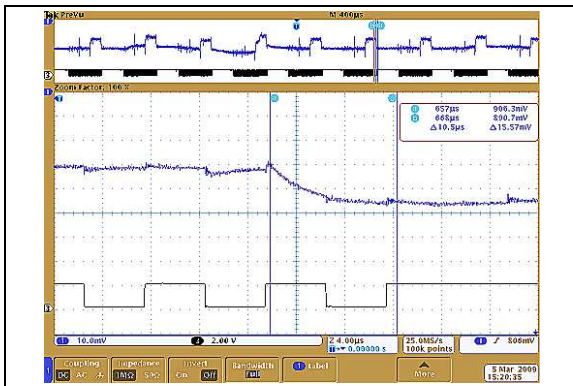


FIGURE 2-71: 100 k Ω : Write Wiper (40h \rightarrow 3Fh) Settling Time ($V_{DD} = 1.8\text{V}$).

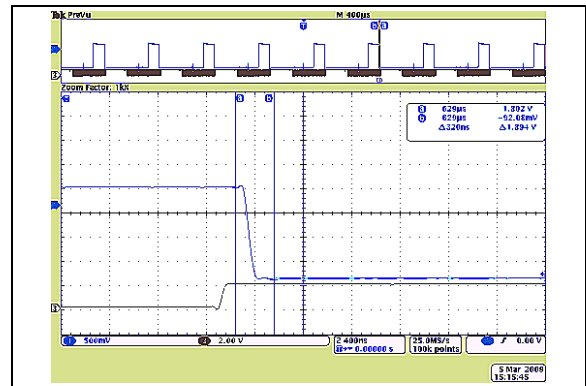


FIGURE 2-74: 100 k Ω : Write Wiper (FFh \rightarrow 00h) Settling Time ($V_{DD} = 1.8\text{V}$).