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MCP414X/416X/424X/426X

7/8-Bit Single/Dual SPI Digital POT with Non-Volatile Memory

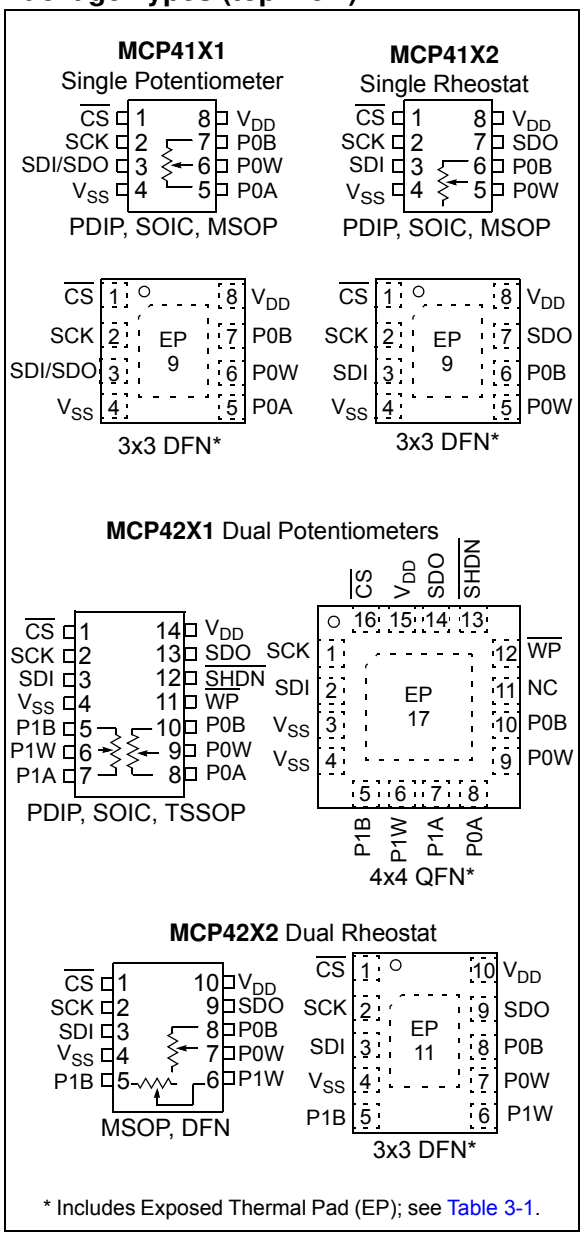
Features

- Single or Dual Resistor Network options
- Potentiometer or Rheostat configuration options
- Resistor Network Resolution
  - 7-bit: 128 Resistors (129 Steps)
  - 8-bit: 256 Resistors (257 Steps)
- R_{AB} Resistances options of:
  - 5 kΩ
  - 10 kΩ
  - 50 kΩ
  - 100 kΩ
- Zero-Scale to Full-Scale Wiper operation
- Low Wiper Resistance: 75Ω (typical)
- Low Tempco:
  - Absolute (Rheostat): 50 ppm typical (0°C to 70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- Non-volatile Memory
  - Automatic Recall of Saved Wiper Setting
  - WiperLock™ Technology
- SPI serial interface (10 MHz, modes 0,0 & 1,1)
  - High-Speed Read/Writes to wiper registers
  - Read/Write to Data EEPROM registers
  - Serially enabled EEPROM write protect
  - SDI/SDO multiplexing (MCP41X1 only)
- Resistor Network Terminal Disconnect Feature via:
  - Shutdown pin ($\overline{SHDN}$)
  - Terminal Control (TCON) Register
- Write Protect Feature:
  - Hardware Write Protect ($\overline{WP}$) Control pin
  - Software Write Protect (WP) Configuration bit
- Brown-out reset protection (1.5V typical)
- Serial Interface Inactive current (2.5 uA typical)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Supports Split Rail Applications
- Internal weak pull-up on all digital inputs
- Wide Operating Voltage:
  - 2.7V to 5.5V - Device Characteristics Specified
  - 1.8V to 5.5V - Device Operation
- Wide Bandwidth (-3dB) Operation:
  - 2 MHz (typical) for 5.0 kΩ device
- Extended temperature range (-40°C to +125°C)

Description

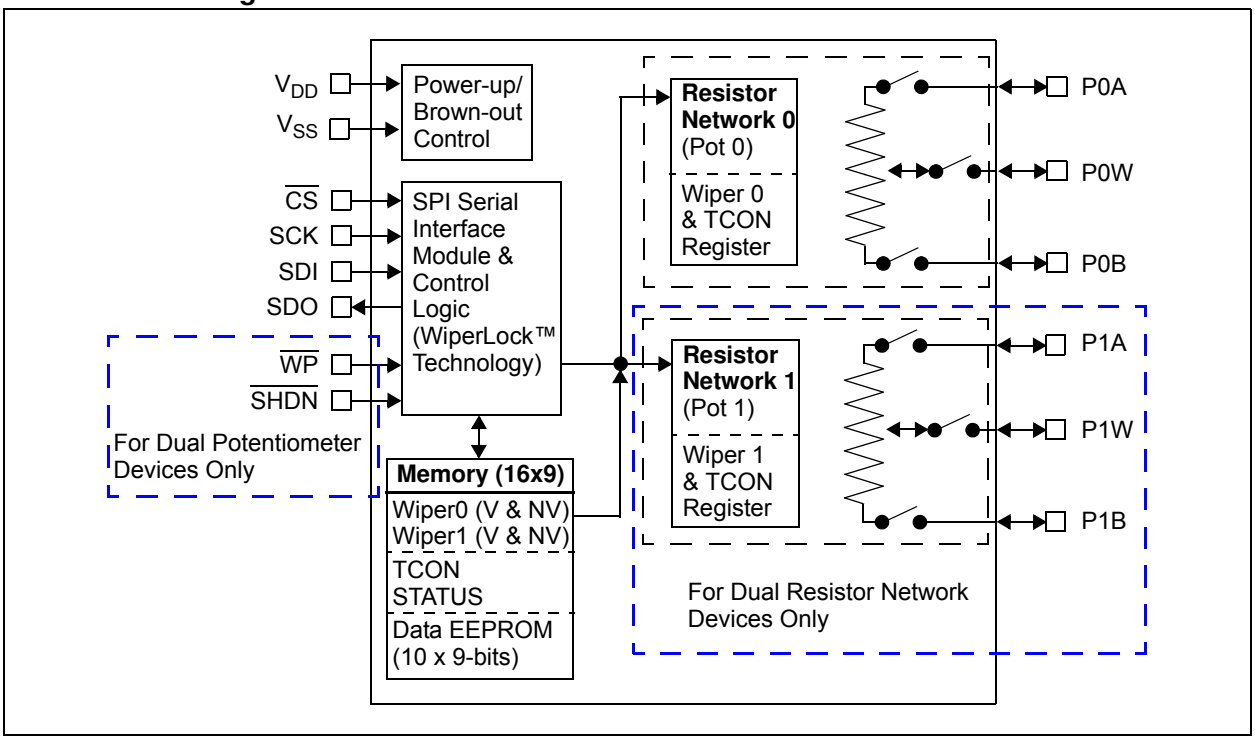
The MCP41XX and MCP42XX devices offer a wide range of product offerings using an SPI interface. WiperLock Technology allows application-specific calibration settings to be secured in the EEPROM.

Package Types (top view)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control Interface	Memory Type	WiperLock Technology	POR Wiper Setting	Resistance (typical)		# of Steps	V_{DD} Operating Range (2)
							R_{AB} Options (kΩ)	Wiper - R_W (Ω)		
MCP4131 (3)	1	Potentiometer (1)	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4132 (3)	1	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4141	1	Potentiometer (1)	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4142	1	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4151 (3)	1	Potentiometer (1)	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4152 (3)	1	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4161	1	Potentiometer (1)	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4162	1	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4231 (3)	2	Potentiometer (1)	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4232 (3)	2	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4241	2	Potentiometer (1)	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4242	2	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4251 (3)	2	Potentiometer (1)	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4252 (3)	2	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4261	2	Potentiometer (1)	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4262	2	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

2: Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.

3: Please check Microchip web site for device release and availability

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +7.0V
Voltage on CS, SCK, SDI, SDI/SDO, WP, and SHDN with respect to V_{SS} ..... -0.6V to 12.5V
Voltage on all other pins (PxA, PxW, PxB, and SDO) with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} (V_I < 0, V_I > V_{DD}, V_I > V_{PP} ON HV pins) .....±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .....±20 mA
Maximum output current sunk by any Output pin .....25 mA
Maximum output current sourced by any Output pin .....25 mA
Maximum current out of V_{SS} pin .....100 mA
Maximum current into V_{DD} pin .....100 mA
Maximum current into PxA, PxW & PxB pins .....±2.5 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied .....-40°C to +125°C
Total power dissipation (**Note 1**) .....400 mW
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV (HBM), ... ≥ 300V (MM)
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD}-V_{OH}) \times I_{OH}\} + \Sigma(V_{OI} \times I_{OL})$$

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Supply Voltage	V_{DD}	2.7	—	5.5	V		
		1.8	—	2.7	V	Serial Interface only.	
$\overline{CS}$, SDI, SDO, SCK, WP, SHDN pin Voltage Range	V_{HV}	V_{SS}	—	12.5V	V	$V_{DD} \geq$ 4.5V	The $\overline{CS}$ pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}). (**Note 6**)
		V_{SS}	—	V_{DD} + 8.0V	V	V_{DD} < 4.5V	
VDD Start Voltage to ensure Wiper Reset	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}	
VDD Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 9**)			V/ms		
Delay after device exits the reset state (V_{DD} > V_{BOR})	T_{BORD}	—	10	20	µs		
Supply Current **(Note 10)**	I_{DD}	—	—	450	µA	Serial Interface Active, V_{DD} = 5.5V, $\overline{CS}$ = V_{IL}, SCK @ 5 MHz, write all 0's to volatile Wiper 0 (address 0h)	
		—	—	1	mA	EE Write Current, V_{DD} = 5.5V, $\overline{CS}$ = V_{IL}, SCK @ 5 MHz, write all 0's to non-volatile Wiper 0 (address 2h)	
		—	2.5	5	µA	Serial Interface Inactive, $\overline{CS}$ = V_{IH}, V_{DD} = 5.5V	
		—	0.55	1	mA	Serial Interface Active, V_{DD} = 5.5V, $\overline{CS}$ = V_{IHH}, SCK @ 5 MHz, decrement non-volatile Wiper 0 (address 2h)	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Resistance (± 20%)	R_{AB}	4.0	5	6.0	kΩ	-502 devices **(Note 1)**	
		8.0	10	12.0	kΩ	-103 devices **(Note 1)**	
		40.0	50	60.0	kΩ	-503 devices **(Note 1)**	
		80.0	100	120.0	kΩ	-104 devices **(Note 1)**	
Resolution	N	257			Taps	8-bit	No Missing Codes
		129			Taps	7-bit	No Missing Codes
Step Resistance	R_S	—	R_{AB} / (256)	—	Ω	8-bit	**Note 6**
		—	R_{AB} / (128)	—	Ω	7-bit	**Note 6**
Nominal Resistance Match	$\|R_{AB0} - R_{AB1}\| / R_{AB}$	—	0.2	1.25	%	**MCP42X1** devices only	
	$\|R_{BW0} - R_{BW1}\| / R_{BW}$	—	0.25	1.5	%	**MCP42X2** devices only, Code = Full-Scale	
Wiper Resistance (**Note 3, Note 4**)	R_W	—	75	160	Ω	V_{DD} = 5.5 V, I_W = 2.0 mA, code = 00h	
		—	75	300	Ω	V_{DD} = 2.7 V, I_W = 2.0 mA, code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (80h or 40h)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 5, Note 6**	
Maximum current through A, W or B	I_W	—	—	2.5	mA	**Note 6**, Worst case current through wiper when wiper is either Full-Scale or Zero Scale.	
Leakage current into A, W or B	I_{WL}	—	100	—	nA	**MCP4XX1** PxA = PxW = PxB = V_{SS}	
		—	100	—	nA	**MCP4XX2** PxB = PxW = V_{SS}	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Full-Scale Error (**MCP4XX1** only) (8-bit code = 100h, 7-bit code = 80h)	V_{WFSE}	-6.0	-0.1	—	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-4.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-3.5	-0.1	—	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-2.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.8	-0.1	—	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Zero-Scale Error (**MCP4XX1** only) (8-bit code = 00h, 7-bit code = 00h)	V_{WZSE}	—	+0.1	+6.0	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.5	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+2.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.8	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Potentiometer Integral Non-linearity	INL	-1	±0.5	+1	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP4XX1** devices only **(Note 2)**	
		-0.5	±0.25	+0.5	LSb	7-bit		
Potentiometer Differential Non-linearity	DNL	-0.5	±0.25	+0.5	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP4XX1** devices only **(Note 2)**	
		-0.25	±0.125	+0.25	LSb	7-bit		
Bandwidth -3 dB (See Figure 2-58, load = 30 pF)	BW	—	2	—	MHz	5 kΩ	8-bit	Code = 80h
		—	2	—	MHz		7-bit	Code = 40h
		—	1	—	MHz	10 kΩ	8-bit	Code = 80h
		—	1	—	MHz		7-bit	Code = 40h
		—	200	—	kHz	50 kΩ	8-bit	Code = 80h
		—	200	—	kHz		7-bit	Code = 40h
		—	100	—	kHz	100 kΩ	8-bit	Code = 80h
		—	100	—	kHz		7-bit	Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Integral Non-linearity **MCP41X1** (**Note 4, Note 8**) **MCP4XX2** devices only **(Note 4)**	R-INL	-1.5	±0.5	+1.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-8.25	+4.5	+8.25	LSb			3.0V, I_W = 480 µA (**Note 7**)
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 900 µA
		-6.0	+4.5	+6.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		-1.5	±0.5	+1.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-5.5	+2.5	+5.5	LSb			3.0V, I_W = 240 µA (**Note 7**)
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 450 µA
		-4.0	+2.5	+4.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		-1.5	±0.5	+1.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-2.0	+1	+2.0	LSb			3.0V, I_W = 48 µA (**Note 7**)
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 90 µA
		-1.5	+1	+1.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		-1.0	±0.5	+1.0	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-1.5	+0.25	+1.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		-0.8	±0.5	+0.8	LSb		7-bit	5.5V, I_W = 45 µA
		-1.125	+0.25	+1.125	LSb			3.0V, I_W = 24 µA (**Note 7**)

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Differential Non-linearity **MCP41X1** (**Note 4, Note 8**) **MCP4XX2** devices only **(Note 4)**	R-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-1.0	+0.5	+1.0	LSb			3.0V (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 900 µA
		-0.75	+0.5	+0.75	LSb			3.0V (**Note 7**)
		-0.5	±0.25	+0.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-1.0	+0.25	+1.0	LSb			3.0V (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 450 µA
		-0.75	+0.5	+0.75	LSb			3.0V (**Note 7**)
		-0.5	±0.25	+0.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-0.5	±0.25	+0.5	LSb			3.0V (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 90 µA
		-0.375	±0.25	+0.375	LSb			3.0V (**Note 7**)
		-0.5	±0.25	+0.5	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-0.5	±0.25	+0.5	LSb			3.0V (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 45 µA
		-0.375	±0.25	+0.375	LSb			3.0V (**Note 7**)
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, Code = Full-Scale		
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, Code = Full-Scale		
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, Code = Full-Scale		

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Digital Inputs/Outputs (CS, SDI, SDO, SCK, WP, SHDN)						
Schmitt Trigger High Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V (Allows 2.7V Digital V_{DD} with 5V Analog V_{DD})
		0.5 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	0.2V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1V_{DD}	—	V	
High Voltage Input Entry Voltage	V_{IHH}	8.5	—	12.5 (6)	V	Threshold for WiperLock™ Technology
High Voltage Input Exit Voltage	V_{IHH}	—	—	V_{DD} + 0.8V (6)	V	
High Voltage Limit	V_{MAX}	—	—	12.5 (6)	V	Pin can tolerate V_{MAX} or less.
Output Low Voltage (SDO)	V_{OL}	V_{SS}	—	0.3V_{DD}	V	I_{OL} = 5 mA, V_{DD} = 5.5V
		V_{SS}	—	0.3V_{DD}	V	I_{OL} = 1 mA, V_{DD} = 1.8V
Output High Voltage (SDO)	V_{OH}	0.7V_{DD}	—	V_{DD}	V	I_{OH} = -2.5 mA, V_{DD} = 5.5V
		0.7V_{DD}	—	V_{DD}	V	I_{OL} = -1 mA, V_{DD} = 1.8V
Weak Pull-up / Pull-down Current	I_{PU}	—	—	1.75	mA	Internal V_{DD} pull-up, V_{IHH} pull-down, V_{DD} = 5.5V, $V_{\overline{CS}}$ = 12.5V
		—	170	—	µA	$\overline{CS}$ pin, V_{DD} = 5.5V, $V_{\overline{CS}}$ = 3V
$\overline{CS}$ Pull-up / Pull-down Resistance	R_{CS}	—	16	—	kΩ	V_{DD} = 5.5V, $V_{\overline{CS}}$ = 3V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 20 MHz

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
RAM (Wiper) Value							
Value Range	N	0h	—	1FFh	hex	8-bit device	
		0h	—	1FFh	hex	7-bit device	
EEPROM							
Endurance	$E_{ndurance}$	—	1M	—	Cycles		
EEPROM Range	N	0h	—	1FFh	hex		
Initial Factory Setting	N	80h			hex	8-bit	WiperLock Technology = Off
		40h			hex	7-bit	WiperLock Technology = Off
EEPROM Programming Write Cycle Time	t_{WC}	—	5	10	ms		
Power Requirements							
Power Supply Sensitivity (**MCP41X2** and **MCP42X2** only)	PSS	—	0.0015	0.0035	%/%	8-bit	V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 80h
		—	0.0015	0.0035	%/%	7-bit	V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

1.1 SPI Mode Timing Waveforms and Requirements

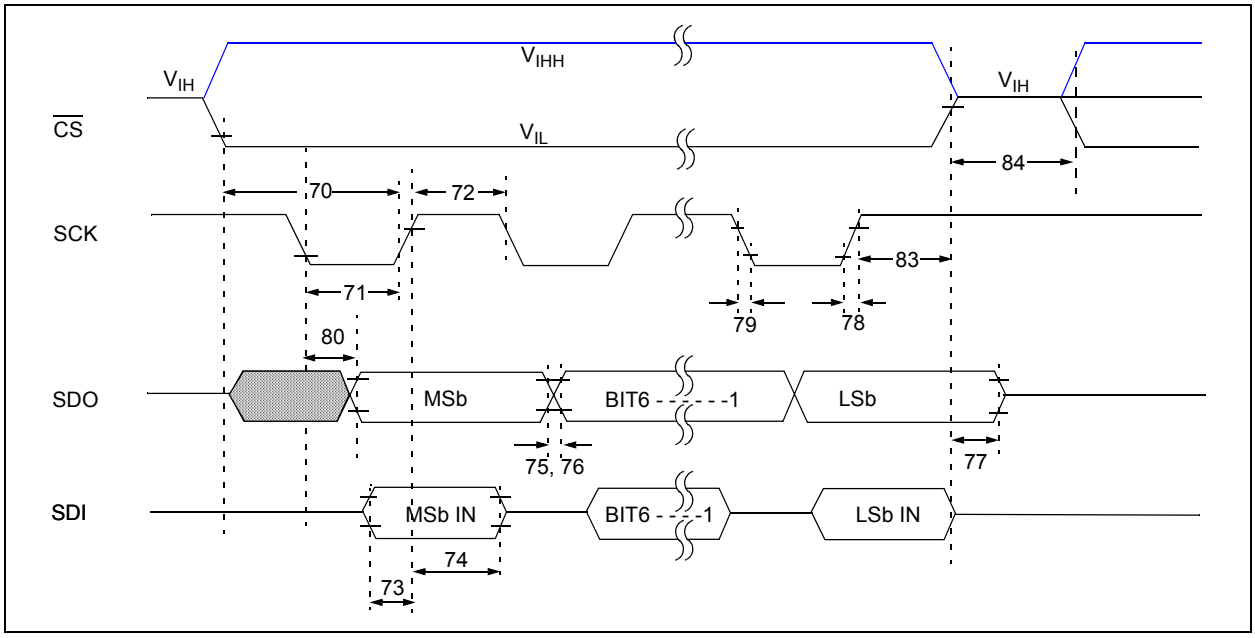


FIGURE 1-1: *SPI Timing Waveform (Mode = 11).*

TABLE 1-1: SPI REQUIREMENTS (MODE = 11)

#	Characteristic	Symbol	Min	Max	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_{DD} = 2.7V to 5.5V
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ input	TcsA2scH	60	—	ns	
71	SCK input high time	TscH	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK input low time	TscL	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
73	Setup time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	70	ns	V_{DD} = 2.7V to 5.5V
				170	ns	V_{DD} = 1.8V to 2.7V
83	$\overline{CS}$ Inactive (V_{IH}) after SCK↑ edge	TscH2csI	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		ms	V_{DD} = 1.8V to 2.7V
84	Hold time of $\overline{CS}$ Inactive (V_{IH}) to $\overline{CS}$ Active (V_{IL} or V_{IHH})	TcsA2csI	50	—	ns	

Note 1: This specification by design.

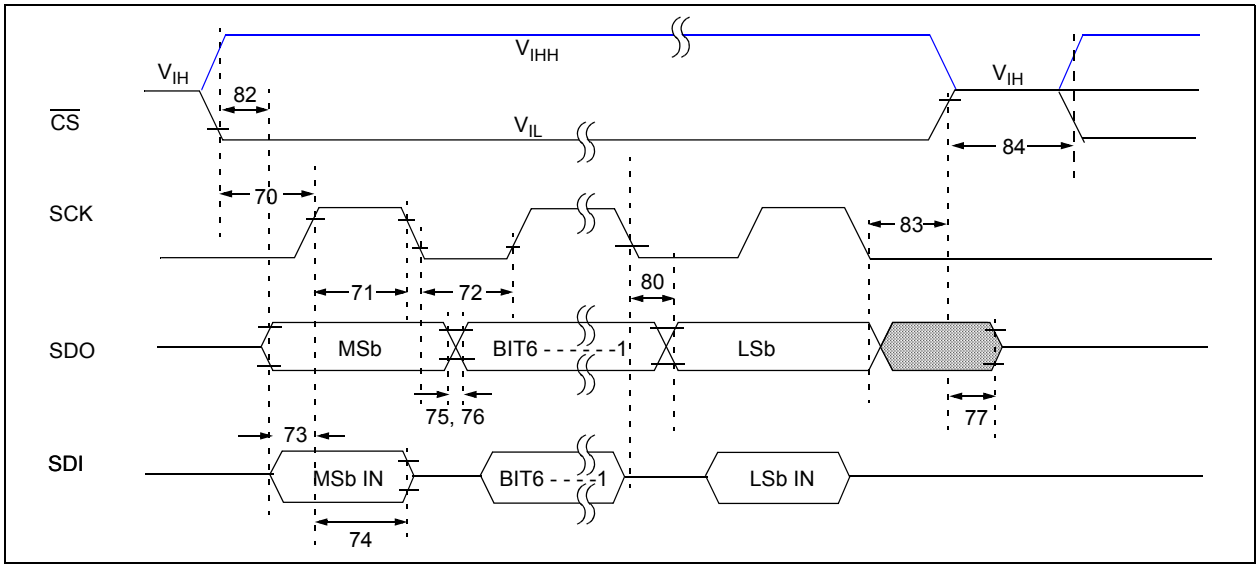


FIGURE 1-2: *SPI Timing Waveform (Mode = 00).*

TABLE 1-2: SPI REQUIREMENTS (MODE = 00)

#	Characteristic	Symbol	Min	Max	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_{DD} = 2.7V to 5.5V
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ input	TcsA2scH	60	—	ns	
71	SCK input high time	TscH	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK input low time	TscL	45	—	ns	V_{DD} = 2.7V to 5.5V
			500	—	ns	V_{DD} = 1.8V to 2.7V
73	Setup time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	70	ns	V_{DD} = 2.7V to 5.5V
				170	ns	V_{DD} = 1.8V to 2.7V
82	SDO data output valid after $\overline{CS}$ Active (V_{IL} or V_{IHH})	TssL2doV	—	70	ns	
83	$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	TscH2csI	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		ms	V_{DD} = 1.8V to 2.7V
84	Hold time of $\overline{CS}$ Inactive (V_{IH}) to $\overline{CS}$ Active (V_{IL} or V_{IHH})	TcsA2csI	50	—	ns	

Note 1: This specification by design.

TABLE 1-3: SPI REQUIREMENTS FOR SDI/SDO MULTIPLEXED (READ OPERATION ONLY) (2)

Characteristic	Symbol	Min	Max	Units	Conditions
SCK Input Frequency	F_{SCK}	—	250	kHz	V_{DD}= 2.7V to 5.5V
$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ input	TcsA2scH	60	—	ns	
SCK input high time	TscH	1.8	—	us	
SCK input low time	TscL	1.8	—	ns	
Setup time of SDI input to SCK↑ edge	TDIV2scH	40	—	ns	
Hold time of SDI input from SCK↑ edge	TscH2DIL	40	—	ns	
$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	TcsH2DOZ	—	50	ns	**Note 1**
SDO data output valid after SCK↓ edge	TscL2DOV	—	1.6	us	
SDO data output valid after $\overline{CS}$ Active (V_{IL} or V_{IHH})	TssL2doV	—	50	ns	
$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	TscH2csI	100	—	ns	
Hold time of $\overline{CS}$ Inactive (V_{IH}) to $\overline{CS}$ Active (V_{II} or V_{IHH})	TcsA2csI	50	—	ns	

Note 1: This specification by design

2: This table is for the devices where the SPI's SDI and SDO pins are multiplexed (SDI/SDO) and a Read command is issued. This is NOT required for SDI/SDO operation with the Increment, Decrement, or Write commands. This data rate can be increased by having external pull-up resistors to increase the rising edges of each bit.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-DFN (3x3)	θ_{JA}	—	60	—	°C/W	
Thermal Resistance, 10L-DFN (3x3)	θ_{JA}	—	57	—	°C/W	
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-QFN	θ_{JA}	—	43	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

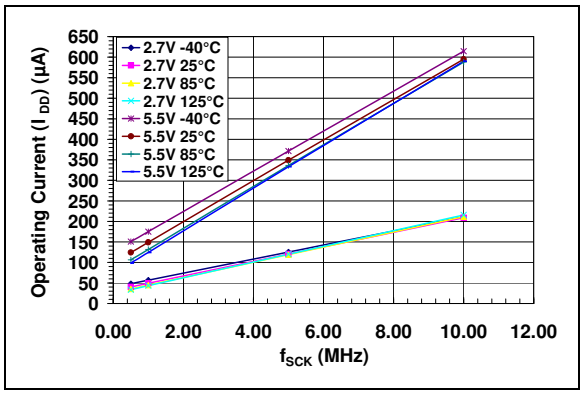


FIGURE 2-1: *Device Current (I_{DD}) vs. SPI Frequency (f_{SCK}) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

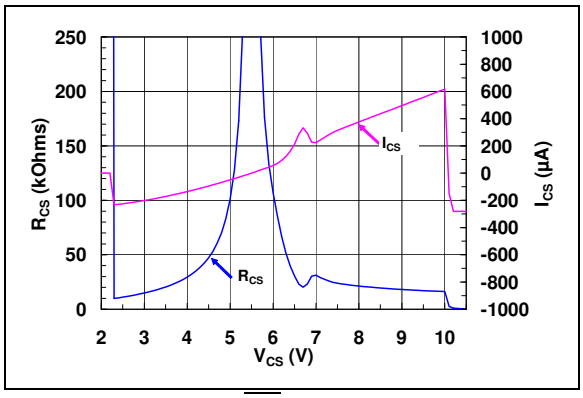


FIGURE 2-4: *$\overline{CS}$ Pull-up/Pull-down Resistance ($R_{\overline{CS}}$) and Current ($I_{\overline{CS}}$) vs. $\overline{CS}$ Input Voltage ($V_{\overline{CS}}$) (V_{DD} = 5.5V).*

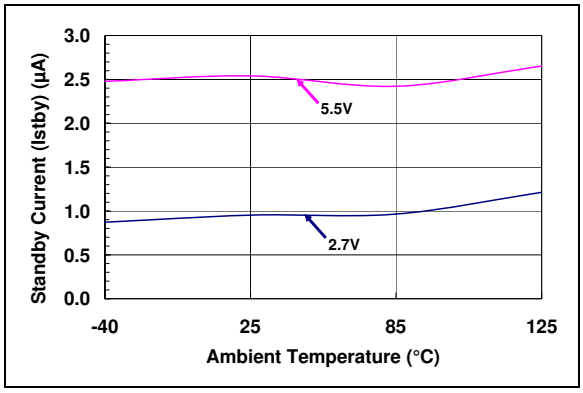


FIGURE 2-2: *Device Current (I_{SHDN}) and V_{DD}. ($\overline{CS}$ = V_{DD}) vs. Ambient Temperature.*

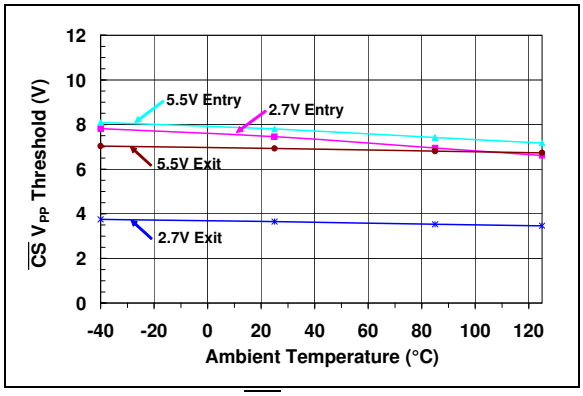


FIGURE 2-5: *$\overline{CS}$ High Input Entry/Exit Threshold vs. Ambient Temperature and V_{DD}.*

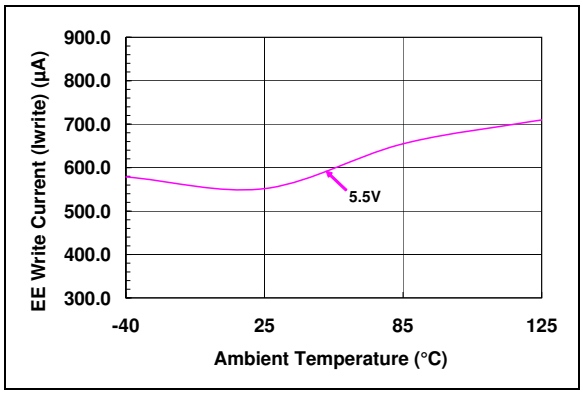


FIGURE 2-3: *Write Current (I_{WRITE}) vs. Ambient Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

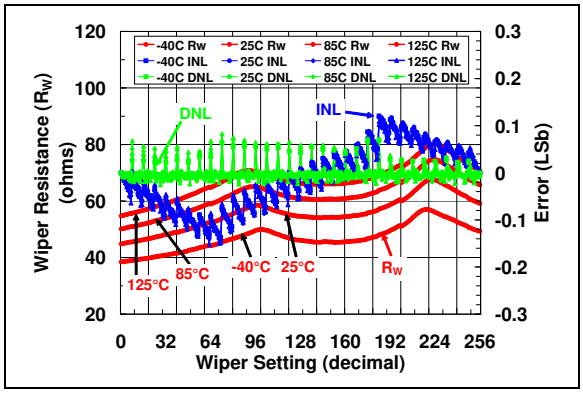


FIGURE 2-6: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

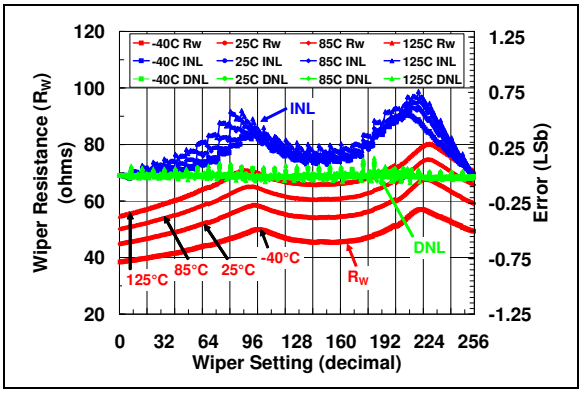


FIGURE 2-9: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

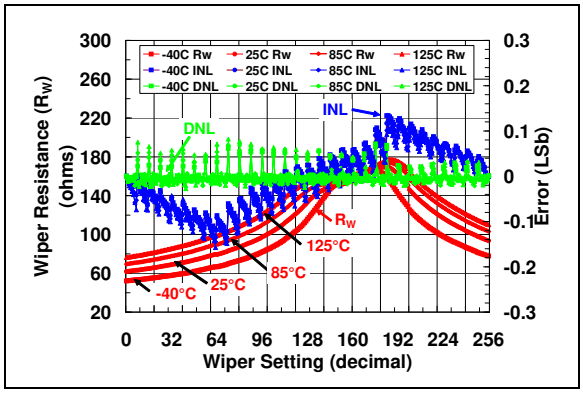


FIGURE 2-7: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

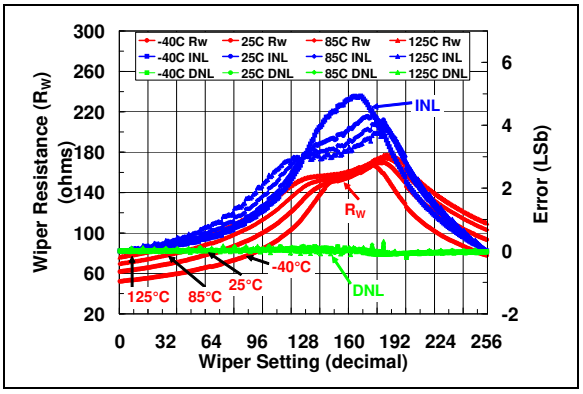


FIGURE 2-10: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

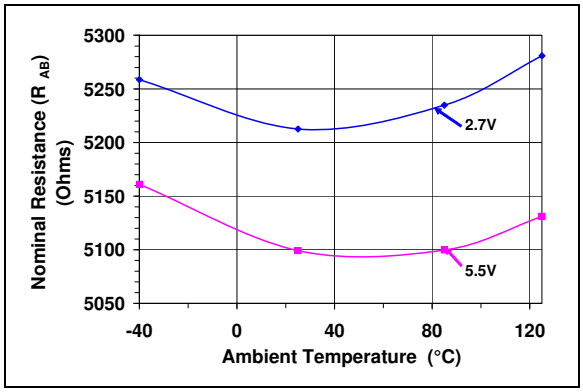


FIGURE 2-8: *5 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

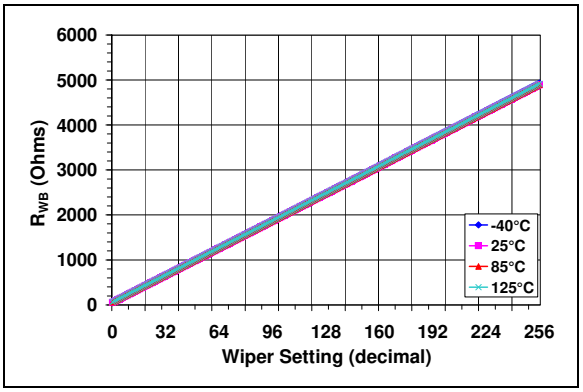


FIGURE 2-11: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

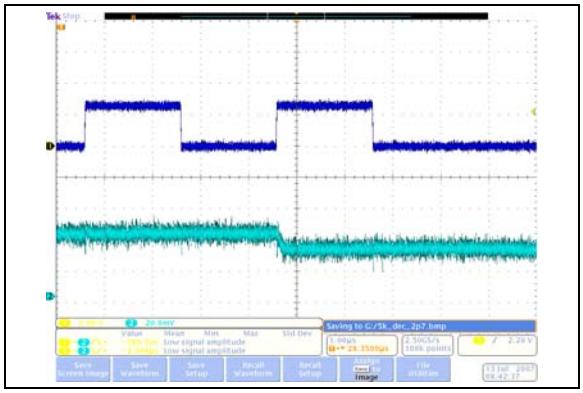


FIGURE 2-12: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

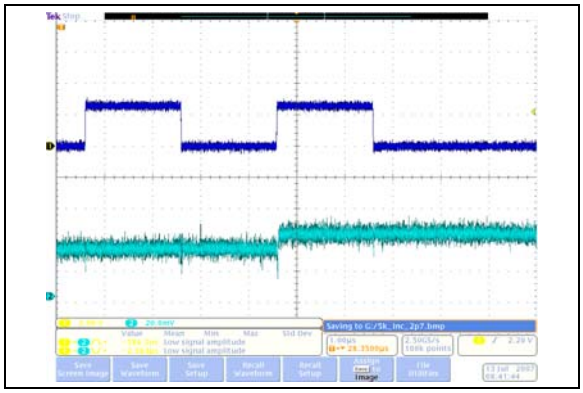


FIGURE 2-15: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

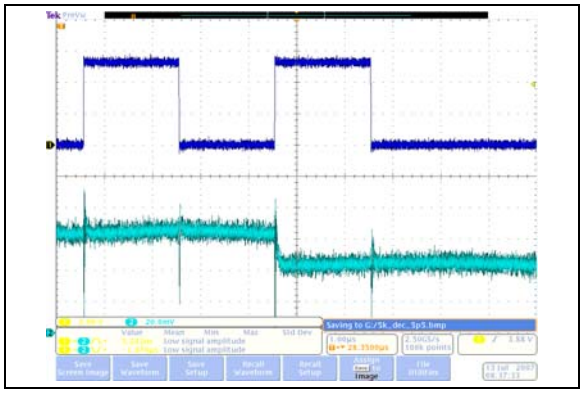


FIGURE 2-13: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

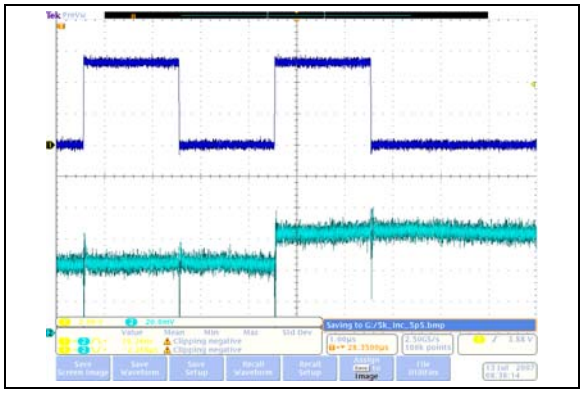


FIGURE 2-16: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

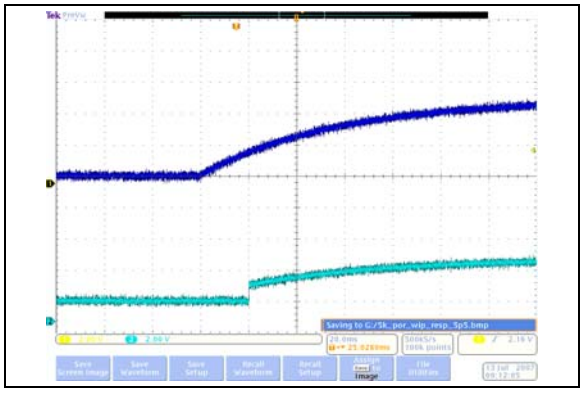


FIGURE 2-14: *5 kΩ – Power-Up Wiper Response Time (20 ms/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

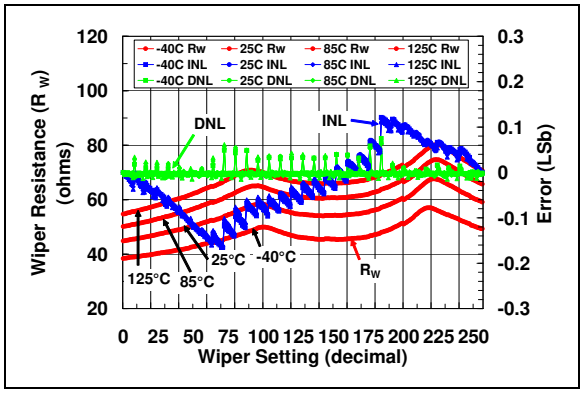


FIGURE 2-17: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

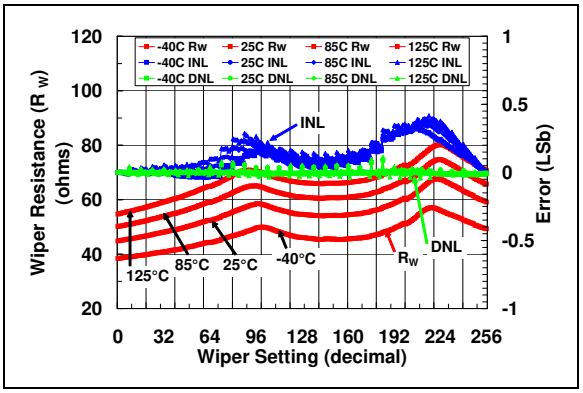


FIGURE 2-20: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

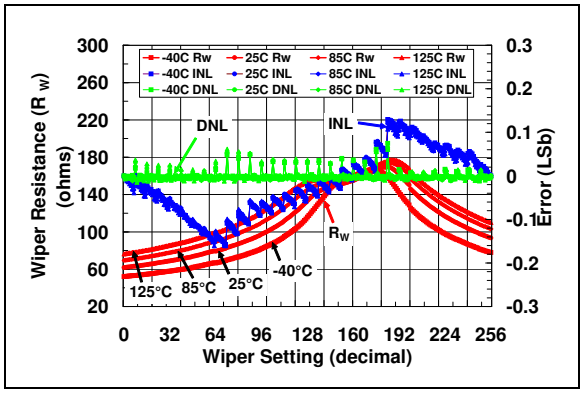


FIGURE 2-18: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

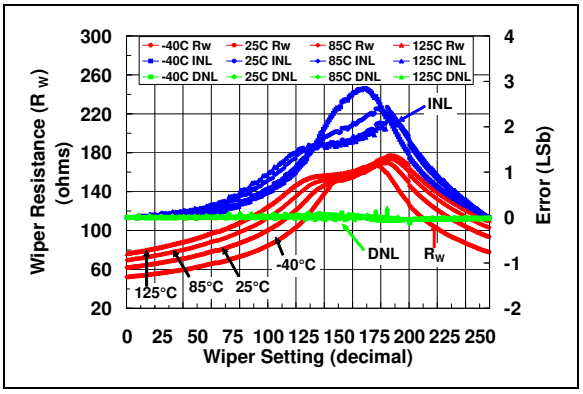


FIGURE 2-21: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

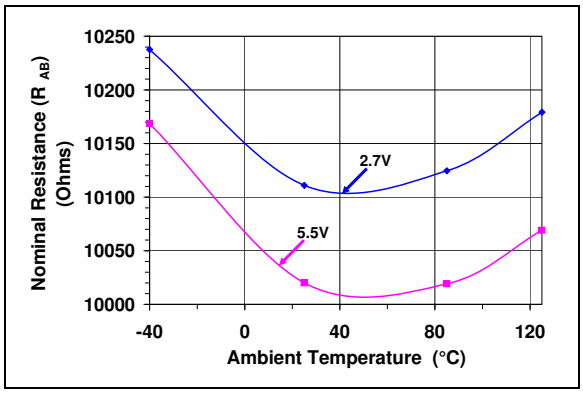


FIGURE 2-19: *10 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

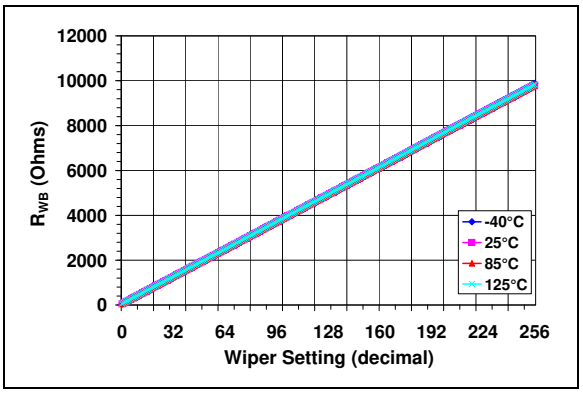


FIGURE 2-22: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

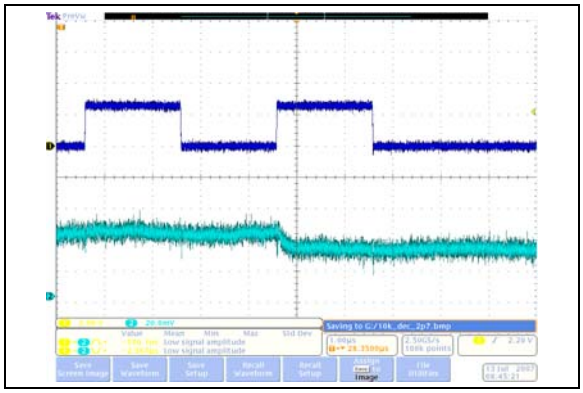


FIGURE 2-23: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

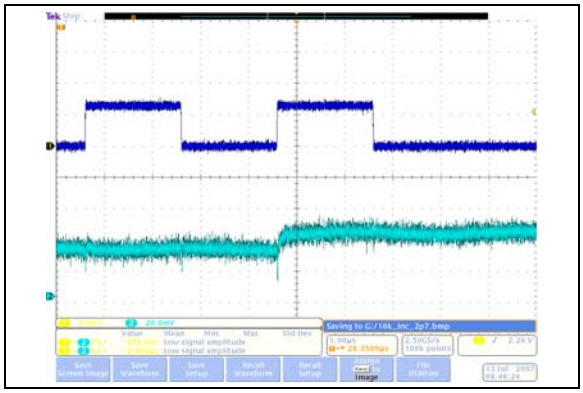


FIGURE 2-25: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

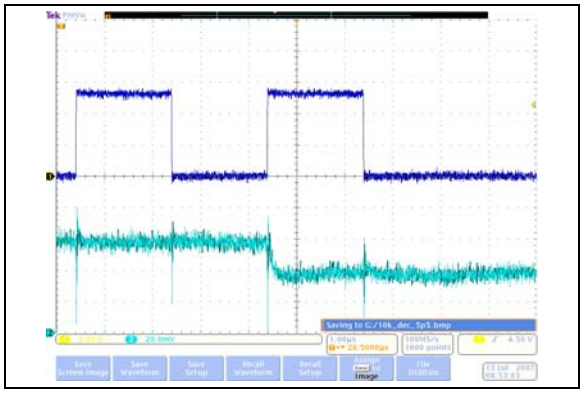


FIGURE 2-24: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

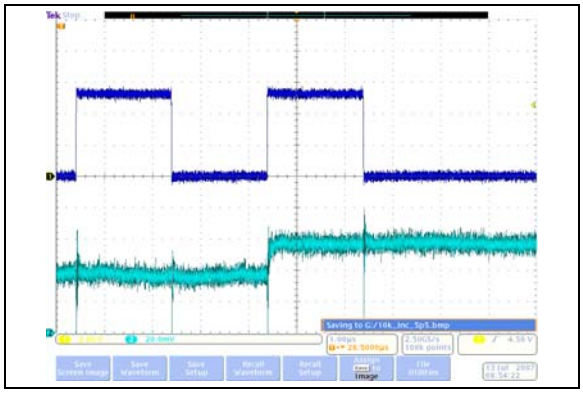


FIGURE 2-26: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

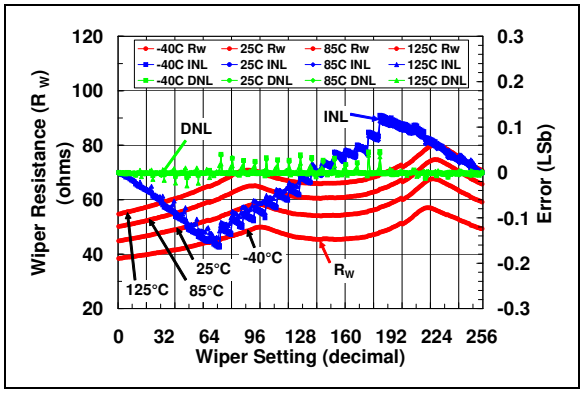


FIGURE 2-27: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

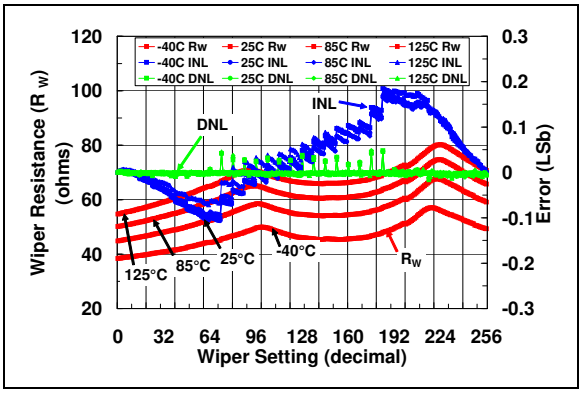


FIGURE 2-30: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

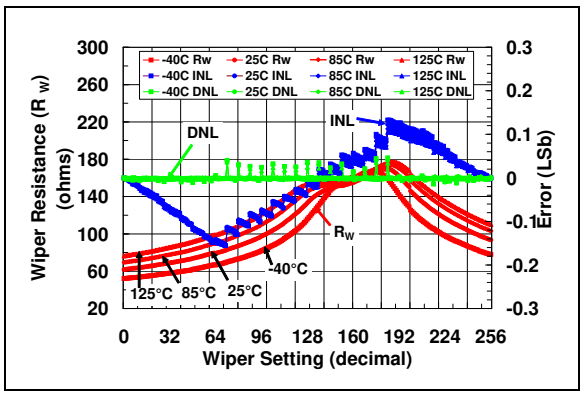


FIGURE 2-28: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

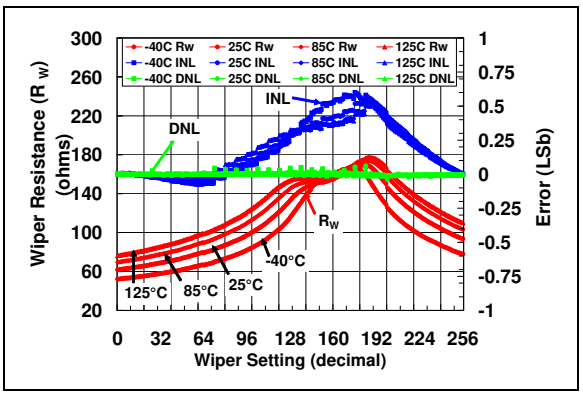


FIGURE 2-31: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

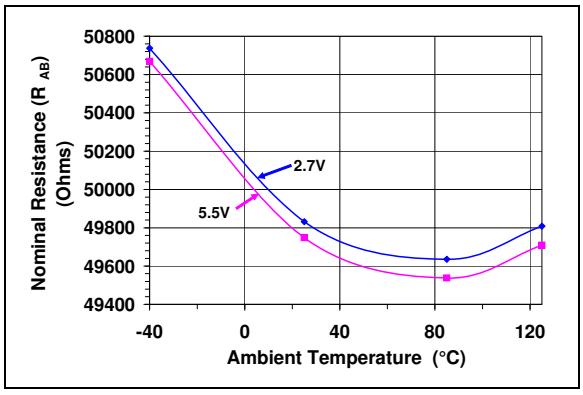


FIGURE 2-29: *50 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

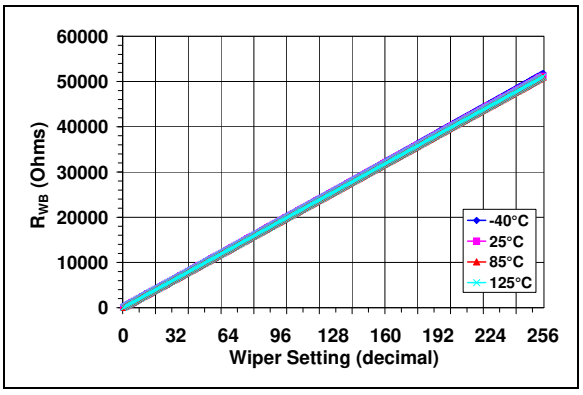


FIGURE 2-32: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

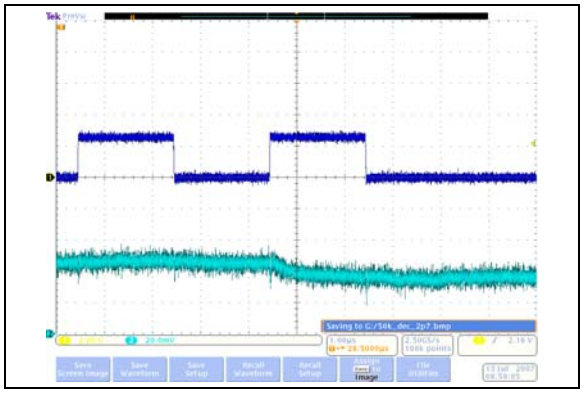


FIGURE 2-33: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

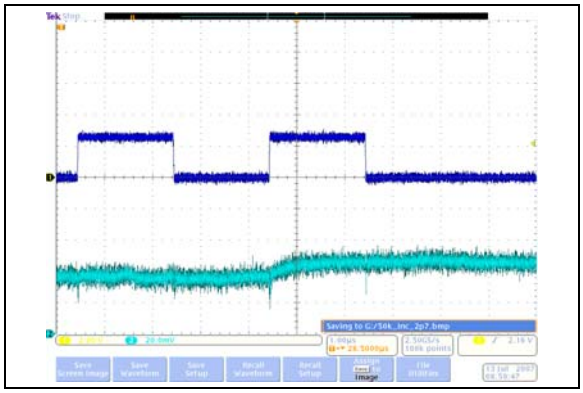


FIGURE 2-35: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

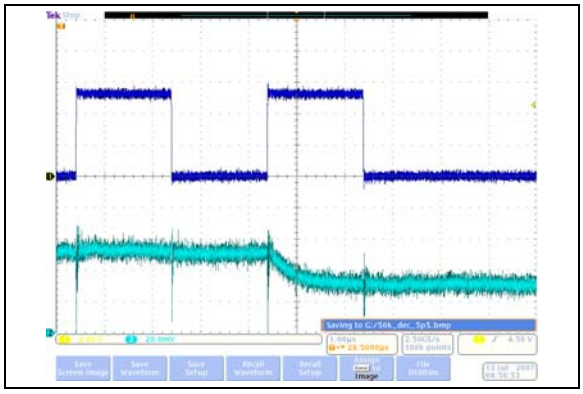


FIGURE 2-34: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

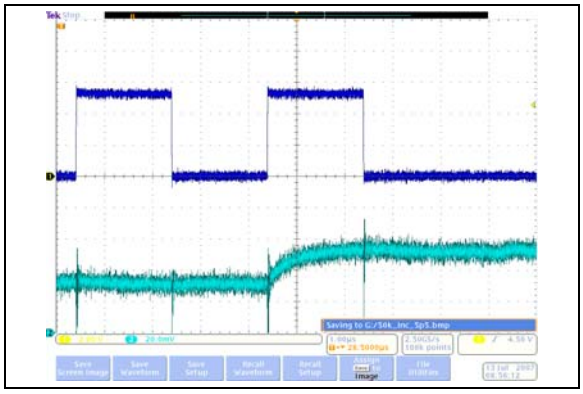


FIGURE 2-36: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

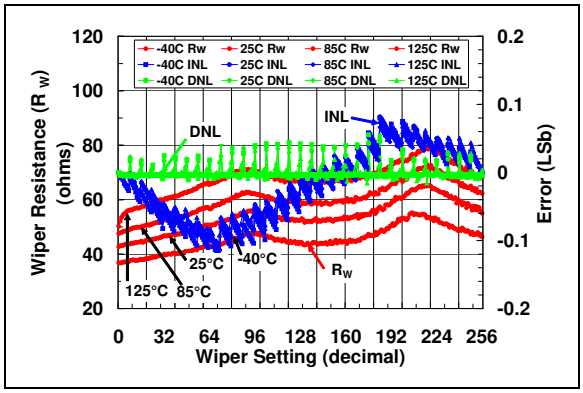


FIGURE 2-37: *100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

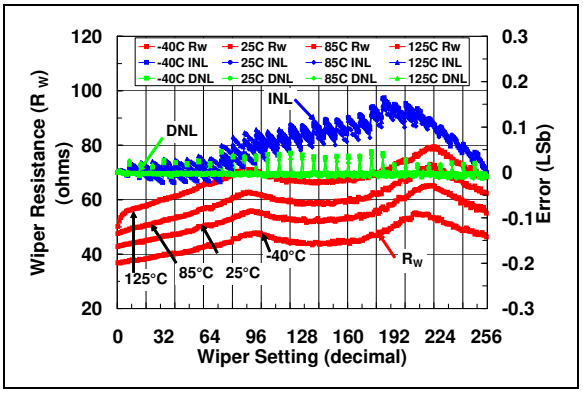


FIGURE 2-40: *100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

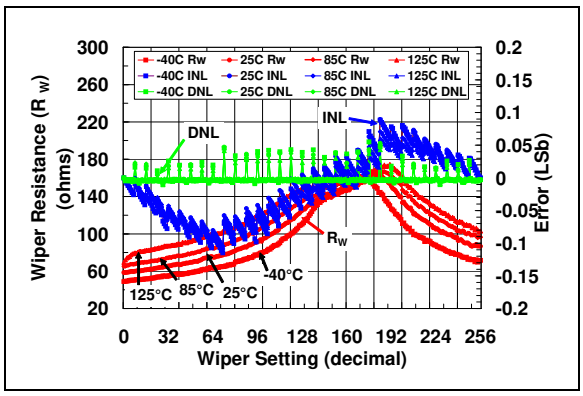


FIGURE 2-38: *100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

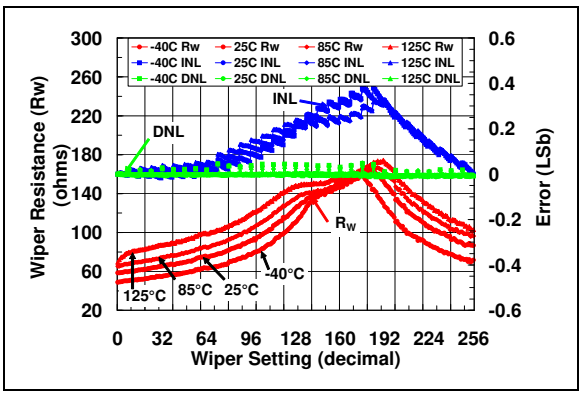


FIGURE 2-41: *100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

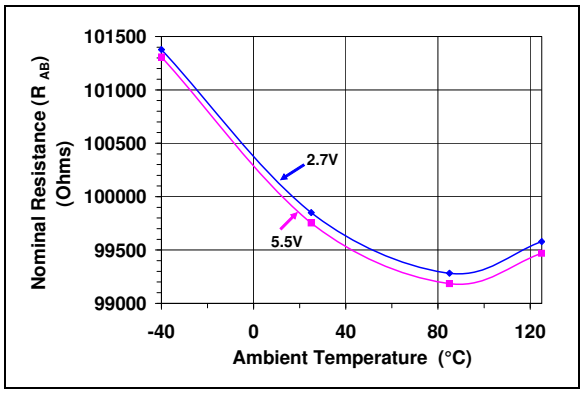


FIGURE 2-39: *100 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

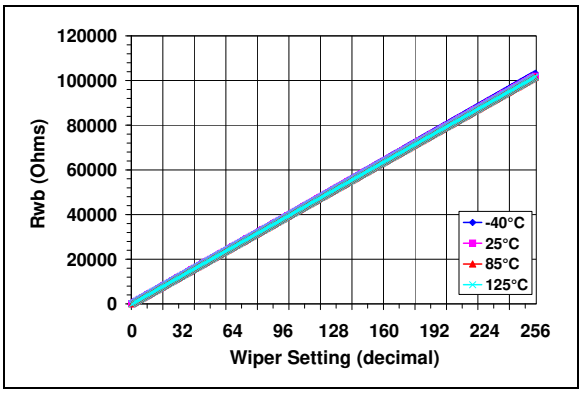


FIGURE 2-42: *100 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

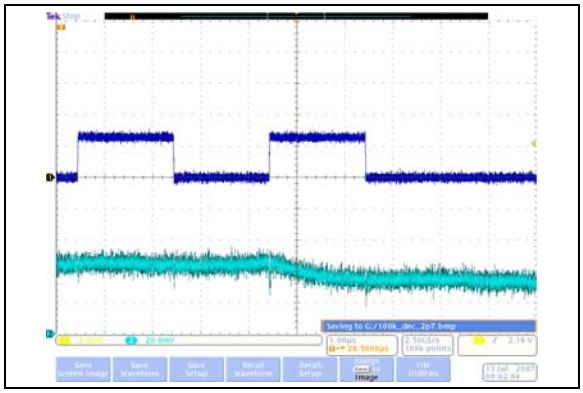


FIGURE 2-43: *100 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

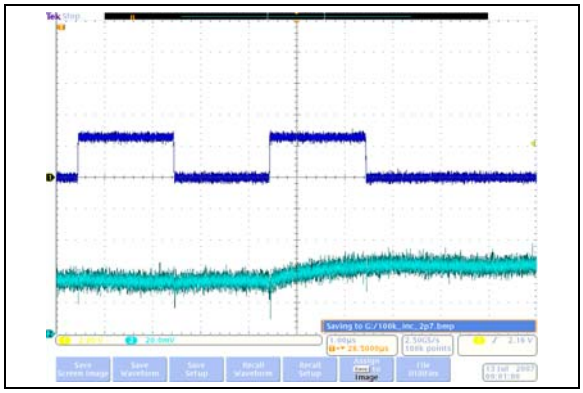


FIGURE 2-45: *100 kΩ – Power-Up Wiper Response Time (1 µs/Div).*

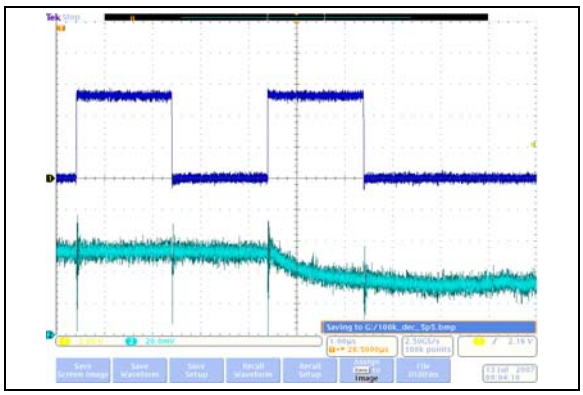


FIGURE 2-44: *100 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

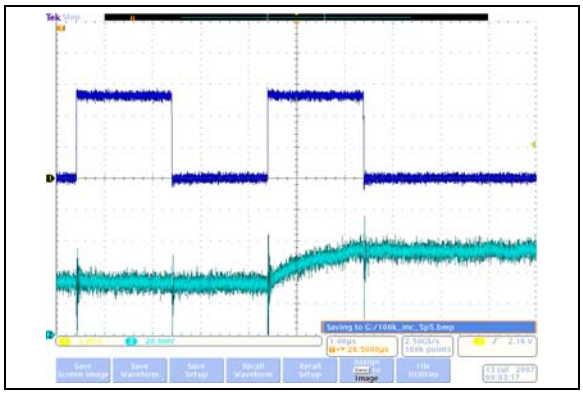


FIGURE 2-46: *100 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

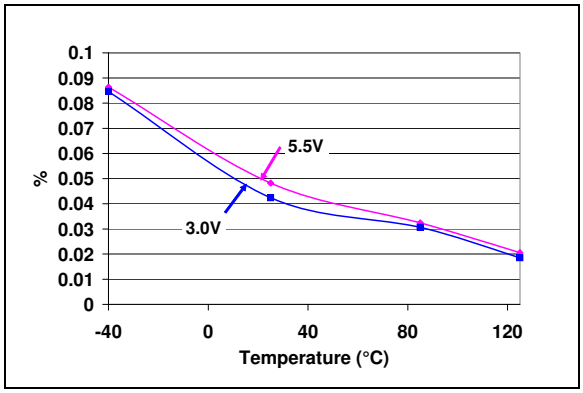


FIGURE 2-47: *Resistor Network 0 to Resistor Network 1 R_{AB} (5 kΩ) Mismatch vs. V_{DD} and Temperature.*

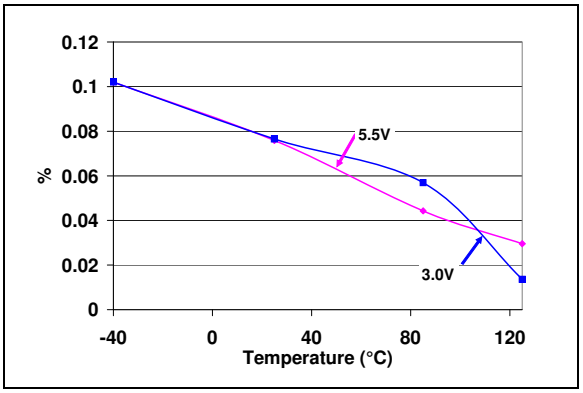


FIGURE 2-49: *Resistor Network 0 to Resistor Network 1 R_{AB} (50 kΩ) Mismatch vs. V_{DD} and Temperature.*

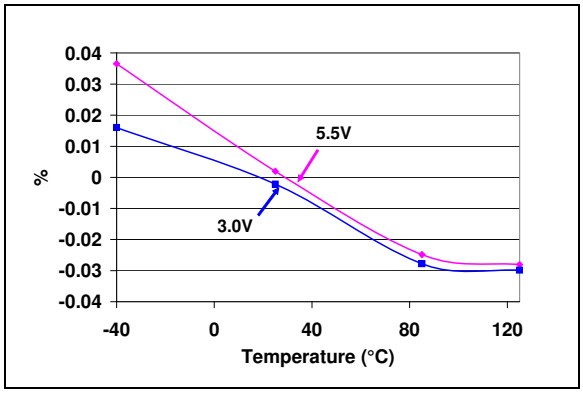


FIGURE 2-48: *Resistor Network 0 to Resistor Network 1 R_{AB} (10 kΩ) Mismatch vs. V_{DD} and Temperature.*

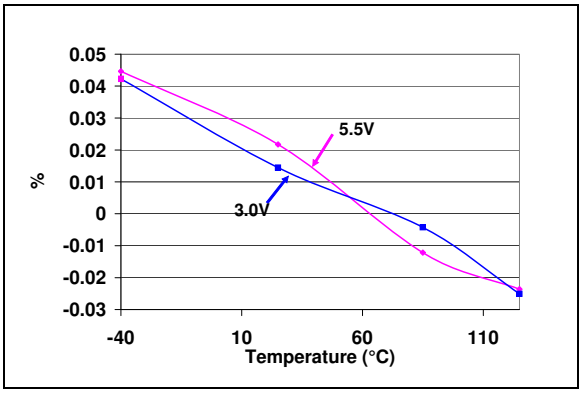


FIGURE 2-50: *Resistor Network 0 to Resistor Network 1 R_{AB} (100 kΩ) Mismatch vs. V_{DD} and Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

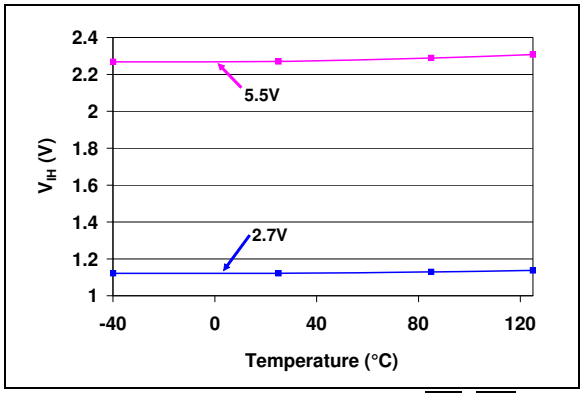


FIGURE 2-51: *V_{IH} (SDI, SCK, $\overline{CS}$, $\overline{WP}$, and $\overline{SHDN}$) vs. V_{DD} and Temperature.*

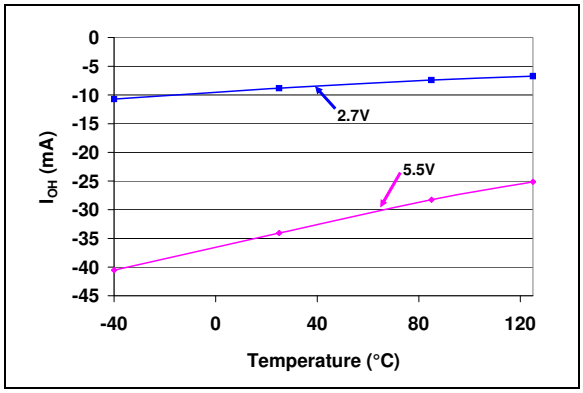


FIGURE 2-53: *I_{OH} (SDO) vs. V_{DD} and Temperature.*

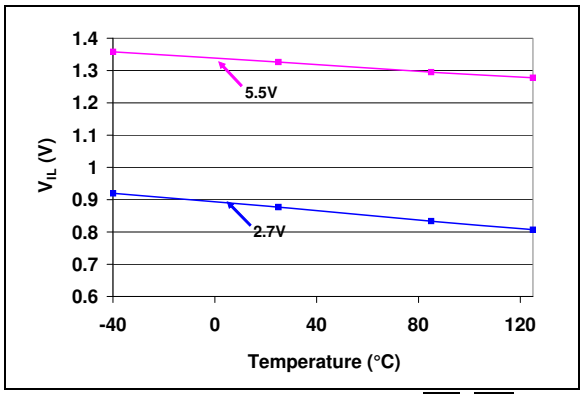


FIGURE 2-52: *V_{IL} (SDI, SCK, $\overline{CS}$, $\overline{WP}$, and $\overline{SHDN}$) vs. V_{DD} and Temperature.*

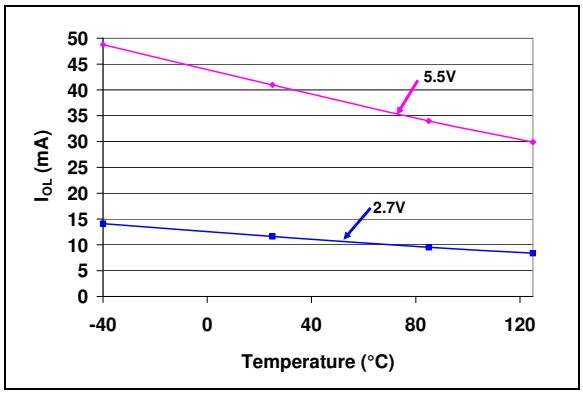


FIGURE 2-54: *I_{OL} (SDO) vs. V_{DD} and Temperature.*