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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP41HVX1

7/8-Bit Single, +36V (±18V) Digital POT with SPI Serial Interface and Volatile Memory

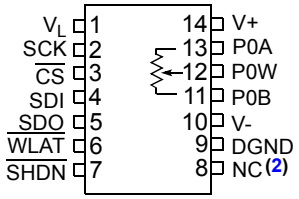
Features

- High-Voltage Analog Support:
  - +36V Terminal Voltage Range (DGND = V-)
  - ±18V Terminal Voltage Range (DGND = V- + 18V)
- Wide Operating Voltage:
  - Analog: 10V to 36V (specified performance)
  - Digital: 2.7V to 5.5V
    1.8V to 5.5V (DGND ≥ V- + 0.9V)
- Single Resistor Network
- Potentiometer Configuration Options
- Resistor Network Resolution
  - 7-bit: 127 resistors (128 Taps)
  - 8-bit: 255 resistors (256 Taps)
- R_{AB} Resistance Options:
  - 5 kΩ – 10 kΩ
  - 50 kΩ – 100 kΩ
- High Terminal/Wiper Current (I_W) Support:
  - 25 mA (for 5 kΩ)
  - 12.5 mA (for 10 kΩ)
  - 6.5 mA (for 50 kΩ and 100 kΩ)
- Zero-Scale to Full-Scale Wiper Operation
- Low Wiper Resistance: 75 Ω (Typical)
- Low Temperature Coefficient:
  - Absolute (Rheostat): 50 ppm typical (0°C to +70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- SPI Serial Interface (10 MHz, Modes 0,0 and 1,1)
- Resistor Network Terminal Disconnect Via:
  - Shutdown pin ($\overline{SHDN}$)
  - Terminal Control (TCON) register
- Write Latch ($\overline{WLAT}$) Pin to Control Update of Volatile Wiper Register (such as Zero Crossing)
- Power-on Reset/Brown-out Reset for Both:
  - Digital supply (V_L/DGND); 1.5V typical
  - Analog supply (V+/V-); 3.5V typical
- Serial Interface Inactive Current (3 µA Typical)
- 500 kHz Typical Bandwidth (-3 dB) Operation (5.0 kΩ Device)
- Extended Temperature Range (-40°C to +125°C)
- Package Types: TSSOP-14 and VQFN-20 (5x5)

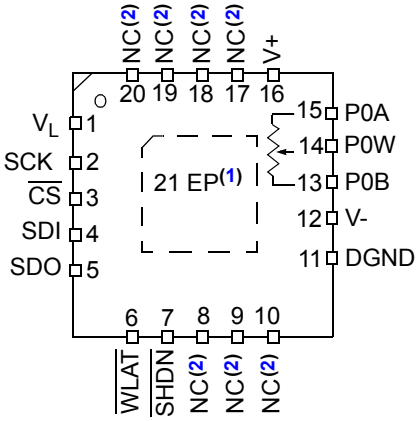
Package Types

MCP41HVX1 Single Potentiometer

TSSOP (ST)



5 x 5 VQFN (MQ)



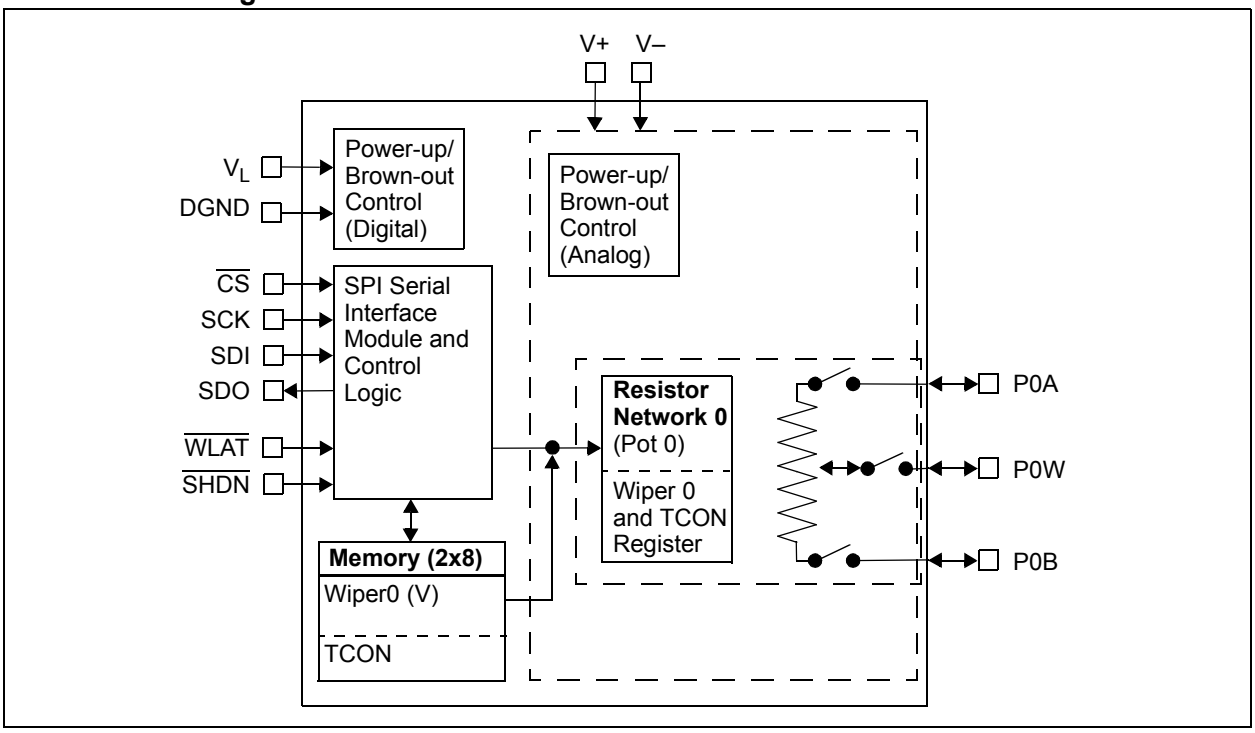
Note 1: Exposed Pad (EP)
2: NC = Not Internally Connected

Description

The MCP41HVX1 family of devices have dual power rails (analog and digital). The analog power rail allows high voltage on the resistor network terminal pins. The analog voltage range is determined by the V+ and V- voltages. The maximum analog voltage is +36V, while the operating analog output minimum specifications are specified from either 10V or 20V. As the analog supply voltage becomes smaller, the analog switch resistances increase, which affects certain performance specifications. The system can be implemented as dual rail (±18V) relative to the digital logic ground (DGND).

The device also has a Write Latch ($\overline{WLAT}$) function, which will inhibit the volatile wiper register from being updated (latched) with the received data until the $\overline{WLAT}$ pin is low. This allows the application to specify a condition where the volatile wiper register is updated (such as zero crossing).

Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control Interface	POR Wiper Setting	Resistance (Typical)		Number of:		Specified Operating Range	
					R_{AB} Options (kΩ)	Wiper - R_W (Ω)	R_S	Taps	V_L (2)	V+ (3)
MCP41HV31	1	Potentiometer (1)	SPI	3Fh	5.0, 10.0, 50.0, 100.0	75	127	128	1.8V to 5.5V	10V (4) to 36V
MCP41HV51	1	Potentiometer (1)	SPI	7Fh	5.0, 10.0, 50.0, 100.0	75	255	256	1.8V to 5.5V	10V (4) to 36V
MCP45HV31 (5)	1	Potentiometer (1)	I²C™	3Fh	5.0, 10.0, 50.0, 100.0	75	127	128	1.8V to 5.5V	10V (4) to 36V
MCP45HV51 (5)	1	Potentiometer (1)	I²C	7Fh	5.0, 10.0, 50.0, 100.0	75	255	256	1.8V to 5.5V	10V (4) to 36V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

2: This is relative to the DGND signal. There is a separate requirement for the V+/V- voltages: $V_L \geq V- + 2.7V$.

3: Relative to V-, the V_L and DGND signals must be between (inclusive) V- and V+.

4: Analog operation will continue while the V+ voltage is above the device's analog Power-on Reset (POR)/Brown-out Reset (BOR) voltage. Operational characteristics may exceed specified limits while the V+ voltage is below the specified minimum voltage.

5: For additional information on these devices, refer to DS20005304.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V- with respect to DGND ..... DGND + 0.6V to -40.0V
Voltage on V+ with respect to DGND ..... DGND - 0.3V to 40.0V
Voltage on V+ with respect to V- ..... DGND - 0.3V to 40.0V
Voltage on V_L with respect to V+ ..... -0.6V to -40.0V
Voltage on V_L with respect to V- ..... -0.6V to +40.0V
Voltage on V_L with respect to DGND ..... -0.6V to +7.0V
Voltage on $\overline{CS}$, SCK, SDI, $\overline{WLAT}$, and $\overline{SHDN}$ with respect to DGND ..... -0.6V to V_L + 0.6V
Voltage on all other pins (PxA, PxW, and PxB) with respect to V- .....-0.3V to V+ + 0.3V
Input clamp current, I_{IK} (V_I < 0, V_I > V_L, V_I > V_{PP} on HV pins) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_L) ..... ±20 mA
Maximum current out of DGND pin ..... 100 mA
Maximum current into V_L pin ..... 100 mA
Maximum current out of V- pin ..... 100 mA
Maximum current into V+ pin .....100 mA
Maximum current into PxA, PxW, & PxB pins (Continuous)
- R_{AB} = 5 kΩ ..... ±25 mA
- R_{AB} = 10 kΩ ..... ±12.5 mA
- R_{AB} = 50 kΩ ..... ±6.5 mA
- R_{AB} = 100 kΩ ..... ±6.5 mA

Maximum current into PxA, PxW, & PxB pins (Pulsed)
- F_{PULSE} > 10 kHz ..... (Max $I_{Continuous}$)/(Duty Cycle)
- F_{PULSE} ≤ 10 kHz ..... (Max $I_{Continuous}$)/√ (Duty Cycle)

Maximum output current sunk by any Output pin ..... 25 mA
Maximum output current sourced by any Output pin ..... 25 mA
Package Power Dissipation (T_A = + 50°C, T_J = +150°C)
- TSSOP-14 ..... 1000 mW
- VQFN-20 (5x5) ..... 2800 mW

Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins
- Human Body Model (HBM) ..... ≥ ±4 kV
- Machine Model (MM) ..... ≥ ±400V
- Charged Device Model (CDM) for TSSOP-14 ..... ≥ ±1 kV

Maximum Junction Temperature (T_J) ..... 150°C
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Positive Supply Voltage (V_L)	V_L	2.7	—	5.5	V	With respect to DGND(4)
		1.8	—	5.5	V	DGND = V- + 0.9V (referenced to V-)(1,4)
		—	—	0	V	With respect to V+
Analog Positive Supply Voltage (V+)	V+	V_L(16)	—	36.0	V	With respect to V-(4)
Digital Ground Voltage (DGND)	V_{DGND}	V-	—	V+ - V_L	V	With respect to V-(4,5)
Analog Negative Supply Voltage (V-)	V-	-36.0 + V_L	—	0	V	With respect to DGND and V_L = 1.8V
Resistor Network Supply Voltage	V_{RN}	—	—	36V	V	Delta voltage between V+ and V-(4)
V_L Start Voltage to ensure Wiper Reset	V_{DPOR}	—	—	1.8	V	With respect to DGND, V+ > 6.0V RAM retention voltage (V_{RAM}) < V_{DBOR}
V+ Voltage to ensure Wiper Reset	V_{APOR}	—	—	6.0	V	With respect to V-, V_L = 0V RAM retention voltage (V_{RAM}) < V_{BOR}
Digital to Analog Level Shifter Operational Voltage	V_{LS}	—	—	2.3	V	V_L to V- voltage. DGND = V-
Power Rail Voltages during Power-Up(1)	V_{LPOR}	—	—	5.5	V	Digital Powers (V_L/DGND) up 1st: V+ and V- floating or as V+/V- powers up (V+ must be ≥ to DGND)(18)
	$V+_{POR}$	—	—	36	V	Analog Powers (V+/V-) up 1st: V_L and DGND floating or as V_L/DGND powers up (DGND must be between V- and V+)(18)
V_L Rise Rate to ensure Power-on Reset	V_{LRR}	**Note 6**			V/ms	With respect to DGND

Note 1 This specification is by design.

Note 4 V+ voltage is dependent on V- voltage. The maximum delta voltage between V+ and V- is 36V. The digital logic DGND potential can be anywhere between V+ and V-. The V_L potential must be ≥ DGND and ≤ V+.

Note 5 The minimum value determined by maximum V- to V+ potential equals 36V, and the minimum value for operation equals 1.8V. So, 36V - 1.8V = 34.2V.

Note 6 POR/BOR is not rate dependent.

Note 16 For specified analog performance, V+ must be 20V or greater (unless otherwise noted).

Note 18 During the power-up sequence, to ensure expected Analog POR operation, the two power systems (Analog and Digital) should have a common reference to ensure that the driven DGND voltage is not at a higher potential than the driven V+ voltage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Delay after device exits the reset state (V_L > V_{BOR})	T_{BORD}	—	10	20	µs		
Supply Current[7]	I_{DDD}	—	45	300	µA	Serial Interface Active, Write all 0's to Volatile Wiper 0 (address 0h) V_L = 5.5V, $\overline{CS}$ = V_{IL}, F_{SCK} = 5 MHz, V- = DGND	
		—	—	7	µA	Serial Interface Inactive, V_L = 5.5V, SCK = V_{IH}, $\overline{CS}$ = V_{IH}, Wiper = 0, V- = DGND	
	I_{DDA}	—	—	5	µA	Current V+ to V-, PxA = PxB = PxW, DGND = V- +(V+/2)	
Resistance (± 20%)[8]	R_{AB}	4.0	5	6.0	kΩ	-502 devices, V+/V- = 10V to 36V	
		8.0	10	12.0	kΩ	-103 devices, V+/V- = 10V to 36V	
		40.0	50	60.0	kΩ	-503 devices, V+/V- = 10V to 36V	
		80.0	100	120.0	kΩ	-104 devices, V+/V- = 10V to 36V	
R_{AB} Current	I_{AB}	—	—	9.00	mA	-502 devices	36V / $R_{AB(MIN)}$, V- = -18V, V+ = +18V[9]
		—	—	4.50	mA	-103 devices	
		—	—	0.90	mA	-503 devices	
		—	—	0.45	mA	-104 devices	
Resolution	N	256			Taps	8-bit	No Missing Codes
		128			Taps	7-bit	No Missing Codes
Step Resistance (see **Appendix B.4**)	R_S	—	R_{AB}/(255)	—	Ω	8-bit	**Note 1**
		—	R_{AB}/(127)	—	Ω	7-bit	**Note 1**

Note 1 This specification is by design.

Note 7 Supply current (IDDD and IDDA) is independent of current through the resistor network.

Note 8 Resistance (RAB) is defined as the resistance between Terminal A to Terminal B.

Note 9 Guaranteed by the R_{AB} specification and Ohms Law.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Wiper Resistance (see **Appendix B.5**)	R_W	—	75	170	Ω	I_W = 1 mA	V+ = +18V, V- = -18V, code = 00h, PxA = floating, PxB = V-.
		—	145	200	Ω	I_W = 1 mA	V+ = +5.0V, V- = -5.0V, code = 00h, PxA = floating, PxB = V-(2)
Nominal Resistance Temperature Coefficient (see **Appendix B.23**)	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -40°C to +85°C	
		—	100	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco (see **Appendix B.22**)	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (80h or 40h)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	V-	—	V+	V	**Note 1**, **Note 11**	
Current through Terminals (A, B, and Wiper)(1)	I_T, I_W	—	—	25	mA	-502 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	12.5	mA	-103 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	6.5	mA	-503 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	6.5	mA	-104 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	36	mA	$I_{BW(W = ZS)}$, or $I_{AW(W = FS)}$	
Leakage current into A, W or B	I_{TL}	—	5	—	nA	A = W = B = V-	

Note 1 This specification is by design.

Note 2 This parameter is not tested, but specified by characterization.

Note 11 Resistor terminals A, W and B's polarity with respect to each other is not restricted.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Full-Scale Error (Potentiometer) (8-bit code = FFh, 7-bit code = 7Fh)(10,17) (V_A = V+, V_B = V-) (see **Appendix B.10**)	V_{WFSE}	-10.5	—	—	LSb	5 kΩ	8-bit	V_{AB} = 20V to 36V
		-8.5	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-13.5	—	—	LSb			V_{AB} = 10V to 36V
		-5.5	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-4.5	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-7.0	—	—	LSb			V_{AB} = 10V to 36V
		-4.5	—	—	LSb	10 kΩ	8-bit	V_{AB} = 20V to 36V
		-6.0	—	—	LSb			V_{AB} = 10V to 36V
		-2.65	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-2.25	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-3.5	—	—	LSb			V_{AB} = 10V to 36V
		-1.0	—	—	LSb	50 kΩ	8-bit	V_{AB} = 20V to 36V
		-0.9	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-1.4	—	—	LSb			V_{AB} = 10V to 36V
		-1.25	—	—	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-0.95	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-1.2	—	—	LSb			V_{AB} = 10V to 36V
		-1.1	—	—	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-0.7	—	—	LSb	100 kΩ	8-bit	V_{AB} = 20V to 36V
		-0.95	—	—	LSb			V_{AB} = 10V to 36V
		-0.7	—	—	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		-0.85	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-0.9	—	—	LSb			V_{AB} = 10V to 36V

Note 2 This parameter is not tested, but specified by characterization.

Note 10 Measured at V_W with V_A = V+ and V_B = V-.

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Zero-Scale Error (Potentiometer) (8-bit code = 00h, 7-bit code = 00h)(10,17) (V_A = V+, V_B = V-) (see **Appendix B.11**)	V_{WZSE}	—	—	+8.5	LSb	5 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+13.5	LSb			V_{AB} = 10V to 36V
		—	—	+4.5	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+7.0	LSb			V_{AB} = 10V to 36V
		—	—	+4.0	LSb	10 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+6.5	LSb			V_{AB} = 10V to 36V
		—	—	+6.0	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+2.0	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+3.25	LSb			V_{AB} = 10V to 36V
		—	—	+3.0	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+0.9	LSb	50 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+0.8	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+1.3	LSb			V_{AB} = 10V to 36V
		—	—	+1.2	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+0.5	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+0.7	LSb			V_{AB} = 10V to 36V
		—	—	+0.5	LSb	100 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+0.95	LSb			V_{AB} = 10V to 36V
		—	—	+0.7	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+0.25	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+0.4	LSb			V_{AB} = 10V to 36V

Note 2 This parameter is not tested, but specified by characterization.

Note 10 Measured at V_W with V_A = V+ and V_B = V-.

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Potentiometer Integral Nonlinearity[10, 17] (see **Appendix B.12**)	P-INL	-1	±0.5	+1	LSb	5 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb		7-bit	V_{AB} = 10V to 36V
		-1	±0.5	+1	LSb	10 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb		7-bit	V_{AB} = 10V to 36V
		-1.1	±0.5	+1.1	LSb	50 kΩ	8-bit	V_{AB} = 10V to 36V
		-1	±0.5	+1	LSb			V_{AB} = 20V to 36V[2]
		-1	±0.5	+1	LSb			V_{AB} = 10V to 36V, -40°C ≤ T_A ≤ +85°C[2]
		-0.6	±0.25	+0.6	LSb		7-bit	V_{AB} = 10V to 36V
		-1.85	±0.5	+1.85	LSb	100 kΩ	8-bit	V_{AB} = 10V to 36V
		-1.2	±0.5	+1.2	LSb			V_{AB} = 20V to 36V[2]
		-1	±0.5	+1	LSb			V_{AB} = 10V to 36V, -40°C ≤ T_A ≤ +85°C[2]
		-1	±0.5	+1	LSb		7-bit	V_{AB} = 10V to 36V
Potentiometer Differential Nonlinearity[10, 17] (see **Appendix B.13**)	P-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb		7-bit	V_{AB} = 10V to 36V
		-0.375	±0.125	+0.375	LSb	10 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	±0.1	+0.125	LSb		7-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb	50 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	±0.1	+0.125	LSb		7-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb	100 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	-0.15	+0.125	LSb		7-bit	V_{AB} = 10V to 36V

Note 2 This parameter is not tested, but specified by characterization.

Note 10 Measured at V_W with V_A = V+ and V_B = V-.

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Bandwidth -3 dB (load = 30 pF) (see **Appendix B.24**)	BW	—	480	—	kHz	5 kΩ	8-bit	Code = 7Fh
		—	480	—	kHz		7-bit	Code = 3Fh
		—	240	—	kHz	10 kΩ	8-bit	Code = 7Fh
		—	240	—	kHz		7-bit	Code = 3Fh
		—	48	—	kHz	50 kΩ	8-bit	Code = 7Fh
		—	48	—	kHz		7-bit	Code = 3Fh
		—	24	—	kHz	100 kΩ	8-bit	Code = 7Fh
		—	24	—	kHz		7-bit	Code = 3Fh
V_W Settling Time (V_A = 10V, V_B = 0V, ±1LSb error band, C_L = 50 pF) (see **Appendix B.17**)	t_S	—	1	—	µs	5 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	
		—	1	—	µs	10 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	
		—	2.5	—	µs	50 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	
		—	5	—	µs	100 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Rheostat Integral Nonlinearity[12,13,14,17] (see **Appendix B.5**)	R-INL	-1.75	—	+1.75	LSb	5 kΩ	8-bit	I_W = 6.0 mA, (V+ - V-) = 36V[2]
		-2.5	—	+2.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V[2]
		-4.0	—	+4.0	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb		7-bit	I_W = 6.0 mA, (V+ - V-) = 36V[2]
		-1.5	—	+1.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V[2]
		-2.0	—	+2.0	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	10 kΩ	8-bit	I_W = 3.0 mA, (V+ - V-) = 36V[2]
		-1.75	—	+1.75	LSb			I_W = 1.7 mA, (V+ - V-) = 20V[2]
		-2.0	—	+2.0	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.6	—	+0.6	LSb		7-bit	I_W = 3.0 mA, (V+ - V-) = 36V[2]
		-0.8	—	+0.8	LSb			I_W = 1.7 mA, (V+ - V-) = 20V[2]
		-1.0	—	+1.0	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	50 kΩ	8-bit	I_W = 600 µA, (V+ - V-) = 36V[2]
		-1.0	—	+1.0	LSb			I_W = 330 µA, (V+ - V-) = 20V[2]
		-1.2	—	+1.2	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb		7-bit	I_W = 600 µA, (V+ - V-) = 36V[2]
		-0.5	—	+0.5	LSb			I_W = 330 µA, (V+ - V-) = 20V[2]
		-0.6	—	+0.6	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	100 kΩ	8-bit	I_W = 300 µA, (V+ - V-) = 36V[2]
		-1.0	—	+1.0	LSb			I_W = 170 µA, (V+ - V-) = 20V[2]
		-1.2	—	+1.2	LSb			I_W = 83 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb		7-bit	I_W = 300 µA, (V+ - V-) = 36V[2]
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 20V[2]
		-0.6	—	+0.6	LSb			I_W = 83 µA, (V+ - V-) = 10V

Note 2 This parameter is not tested, but specified by characterization.

Note 12 Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

Note 13 Externally connected to a Rheostat configuration (RBW), and then tested.

Note 14 Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Rheostat Differential Nonlinearity (12,13,14,17) (see Appendix B.5)	R-DNL	-0.5	—	+0.5	LSb	5 kΩ	8-bit	I_W = 6.0 mA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V(2)
		-0.8	—	+0.8	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-0.6	—	+0.6	LSb			I_W = 1.7 mA, (V+ - V-) = 10V -40°C ≤ T_A ≤ +85°C(2)
		-0.25	—	+0.25	LSb		7-bit	I_W = 6.0 mA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 3.3 mA, (V+ - V-) = 20V(2)
		-0.3	—	+0.3	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	10 kΩ	8-bit	I_W = 3.0 mA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 1.7 mA, (V+ - V-) = 20V(2)
		-0.5	—	+0.5	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 3.0 mA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 1.7 mA, (V+ - V-) = 20V(2)
		-0.25	—	+0.25	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	50 kΩ	8-bit	I_W = 600 µA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 330 µA, (V+ - V-) = 20V(2)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 600 µA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 330 µA, (V+ - V-) = 20V(2)
		-0.25	—	+0.25	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	100 kΩ	8-bit	I_W = 300 µA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 20V(2)
		-0.5	—	+0.5	LSb			I_W = 83 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 300 µA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 170 µA, (V+ - V-) = 20V(2)
		-0.25	—	+0.25	LSb			I_W = 83 µA, (V+ - V-) = 10V

Note 2 This parameter is not tested, but specified by characterization.

Note 12 Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

Note 13 Externally connected to a Rheostat configuration (RBW), and then tested.

Note 14 Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Capacitance (P_A)	C_A	—	75	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid-Scale
Capacitance (P_w)	C_W	—	120	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid-Scale
Capacitance (P_B)	C_B	—	75	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid-Scale
Common-Mode Leakage	I_{CM}	—	5	—	nA	$V_A = V_B = V_W$
Digital Interface Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 400 kHz
Digital Inputs/Outputs ($\overline{CS}$, SDI, SDO, SCK, $\overline{SHDN}$, $\overline{WLAT}$)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_L	—	V_L + 0.3V	V	2.7V ≤ V_L ≤ 5.5V
		0.5 V_L	—	V_L + 0.3V	V	1.8V ≤ V_L ≤ 2.7V
Schmitt Trigger Low-Input Threshold	V_{IL}	DGND - 0.5V	—	0.2 V_L	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_L	—	V	
Output Low Voltage (SDO)	V_{OL}	DGND	—	0.2 V_L	V	V_L = 5.5V, I_{OL} = 5 mA
		DGND	—	0.2 V_L	V	V_L = 1.8V, I_{OL} = 800 µA
Output High Voltage (SDO)	V_{OH}	0.8 V_L	—	V_L	V	V_L = 5.5V, I_{OH} = -2.5 mA
		0.8 V_L	—	V_L	V	V_L = 1.8V, I_{OL} = -800 µA
Input Leakage Current	I_{IL}	-1		1	uA	$V_{IN} = V_L$ and V_{IN} = DGND

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max**	**Units**	**Conditions**	
RAM (Wiper, TCON) Value							
Wiper Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	7Fh	hex	7-bit	
Wiper POR/BOR Value	$N_{POR/BOR}$	7Fh			hex	8-bit	
		3Fh			hex	7-bit	
TCON Value Range	N	0h	—	FFh	hex		
TCON POR/BOR Value	N_{TCON}	FF			hex	All Terminals connected	
Power Requirements							
Power Supply Sensitivity (see **Appendix B.20**)	PSS	—	0.0015	0.0035	%/%	8-bit	V_L = 2.7V to 5.5V, V+ = 18V, V- = -18V, Code = 7Fh
		—	0.0015	0.0035	%/%	7-bit	V_L = 2.7V to 5.5V, V+ = 18V, V- = -18V, Code = 3Fh
Power Dissipation	P_{DISS}	—	260	—	mW	5 kΩ	V_L = 5.5V, V+ = 18V, V- = -18V(15)
		—	130	—	mW	10 kΩ	
		—	26	—	mW	50 kΩ	
		—	13	—	mW	100 kΩ	

Note 15 $P_{DISS} = I * V$, or $((I_{DDD} * 5.5V) + (I_{DDA} * 36V) + (I_{AB} * 36V))$.

AC/DC Notes:

1. This specification is by design.
2. This parameter is not tested, but specified by characterization.
3. See Absolute Maximum Ratings.
4. V+ voltage is dependent on V- voltage. The maximum delta voltage between V+ and V- is 36V. The digital logic DGND potential can be anywhere between V+ and V-. The V_L potential must be ≥ DGND and ≤ V+.
5. The minimum value determined by maximum V- to V+ potential equals 36V, and the minimum value for operation equals 1.8V. So, 36V - 1.8V = 34.2V.
6. POR/BOR is not rate dependent.
7. Supply current (I_{DDD} and I_{DDA}) is independent of current through the resistor network.
8. Resistance (R_{AB}) is defined as the resistance between Terminal A to Terminal B.
9. Guaranteed by the R_{AB} specification and Ohms Law.
10. Measured at V_W with V_A = V+ and V_B = V-.
11. Resistor terminals A, W and B's polarity with respect to each other is not restricted.
12. Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
13. Externally connected to a Rheostat configuration (R_{BW}), and then tested.
14. Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).
15. $P_{DISS} = I * V$, or $((I_{DDD} * 5.5V) + (I_{DDA} * 36V) + (I_{AB} * 36V))$.
16. For specified analog performance, V+ must be 20V or greater (unless otherwise noted).
17. Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.
18. During the power-up sequence, to ensure expected Analog POR operation, the two power systems (Analog and Digital) should have a common reference to ensure that the driven DGND voltage is not at a higher potential than the driven V+ voltage.

1.1 SPI Mode Timing Waveforms and Requirements

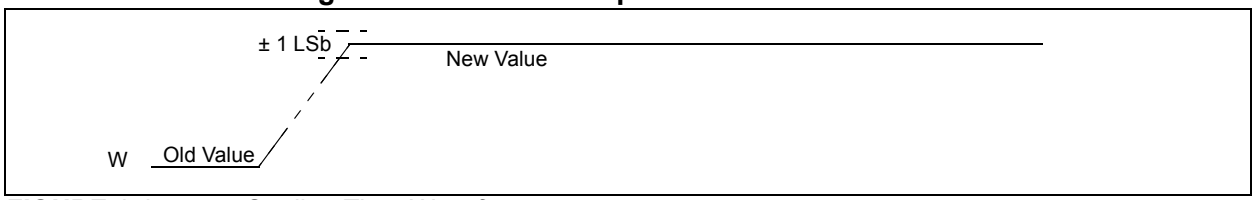


FIGURE 1-1: *Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_W Settling Time (V_A = 10V, V_B = 0V, ±1LSb error band, C_L = 50 pF) (see **Appendix B.17**)	t_S	—	1	—	µs	5 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h
		—	1	—	µs	10 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h
		—	2.5	—	µs	50 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h
		—	5	—	µs	100 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h

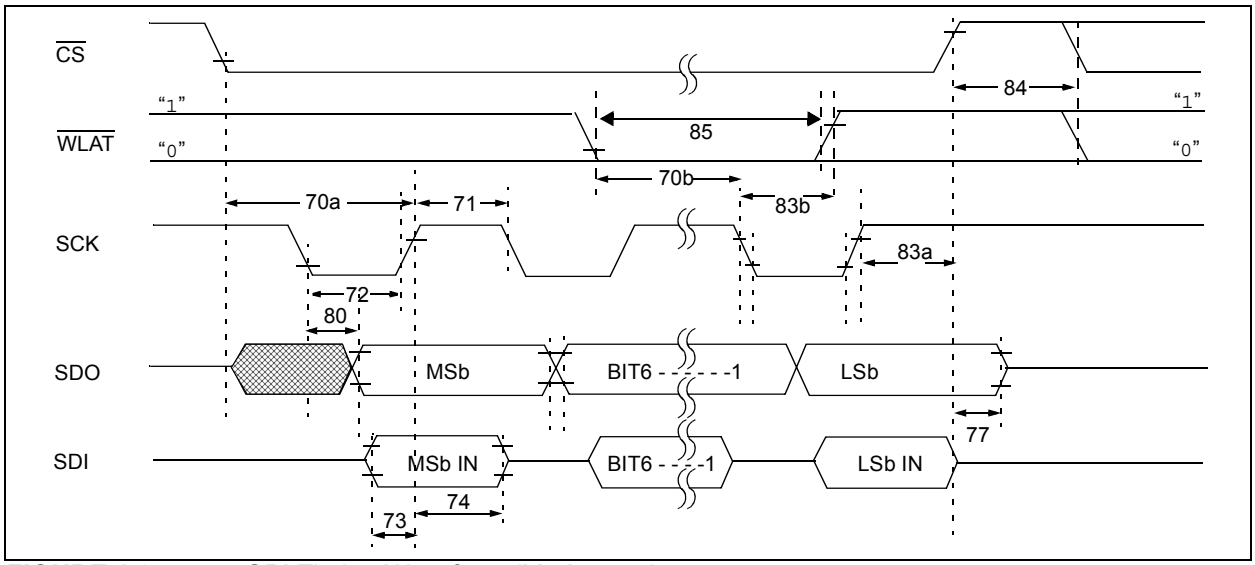


FIGURE 1-2: *SPI Timing Waveform (Mode = 11).*

TABLE 1-2: SPI REQUIREMENTS (MODE = 11)

#	Characteristic	Symbol	Min.	Max.	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_L = 2.7V to 5.5V
			—	1	MHz	V_L = 1.8V to 2.7V
70a	$\overline{CS}$ Active (V_{IL}) to SCK↑ input	TcsA2scH	25	—	ns	
70b	$\overline{WLAT}$ Active (V_{IL}) to eighth (or sixteenth) SCK↓ of the Serial Command to ensure previous data is latched (set-up time)	TwlA2scH	20	—	ns	
71	SCK input high time	TscH	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
72	SCK input low time	TscL	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
73	Set-up time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output high-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	55	ns	V_L = 2.7V to 5.5V
				90	ns	V_L = 1.8V to 2.7V
83a	$\overline{CS}$ Inactive (V_{IH}) after SCK↑ edge	TscH2csI	100	—	ns	
83b	$\overline{WLAT}$ Inactive (V_{IH}) after eighth (or sixteenth) SCK↓ edge (hold time)	TscH2wlatI	50	—	ns	
84	Hold time of $\overline{CS}$ (or $\overline{WLAT}$) Inactive (V_{IH}) to $\overline{CS}$ (or $\overline{WLAT}$) Active (V_{IL})	TcsA2csI	20	—	ns	
85	$\overline{WLAT}$ input low time	T_{WLAT}L	25	—	ns	

Note 1: This specification is by design.

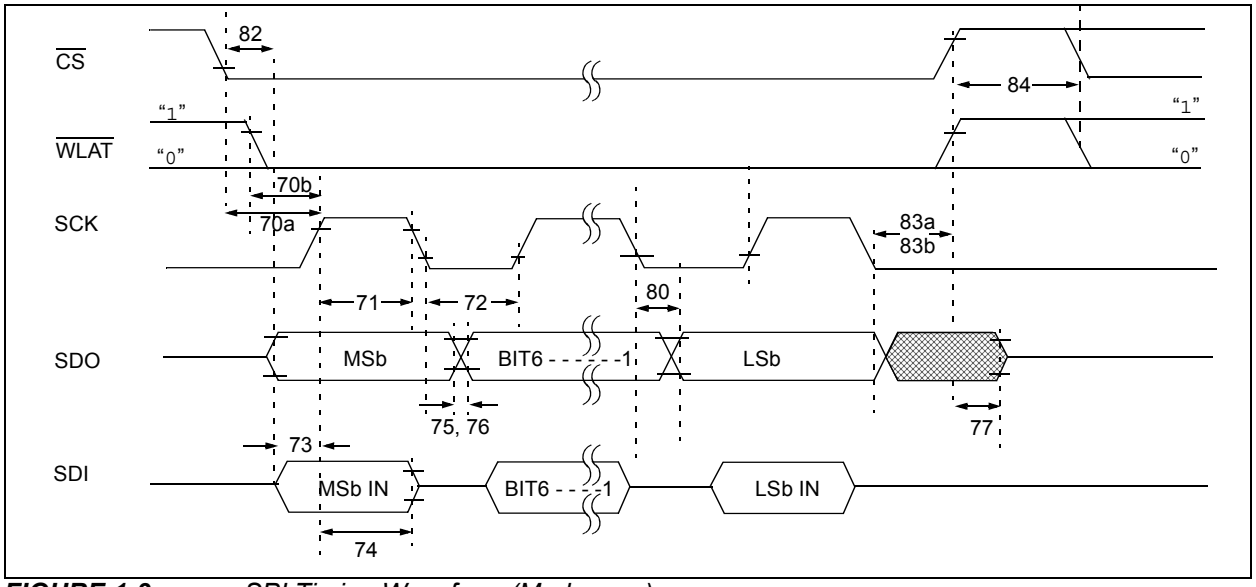


FIGURE 1-3: *SPI Timing Waveform (Mode = 00).*

TABLE 1-3: SPI REQUIREMENTS (MODE = 00)

#	Characteristic	Symbol	Min.	Max.	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_L = 2.7V to 5.5V
			—	1	MHz	V_L = 1.8V to 2.7V
70a	$\overline{CS}$ Active (V_{IL}) to SCK↑ input	TcsA2scH	25	—	ns	
70b	$\overline{WLAT}$ Active (V_{IL}) to eighth (or sixteenth) SCK↓ of the Serial Command to ensure previous data is latched (setup time)	TwlA2scH	20	—	ns	
71	SCK input high time	TscH	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
72	SCK input low time	TscL	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
73	Set-up time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output high-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	55	ns	V_L = 2.7V to 5.5V
				90	ns	V_L = 1.8V to 2.7V
82	SDO data output valid after $\overline{CS}$ Active (V_{IL})	TscL2DOV	—	70	ns	
83a	$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	TscL2csI	100	—	ns	
83b	$\overline{WLAT}$ Inactive (V_{IH}) after SCK↓ edge	TscL2wlatI	50	—	ns	
84	Hold time of $\overline{CS}$ (or $\overline{WLAT}$) Inactive (V_{IH}) to $\overline{CS}$ (or $\overline{WLAT}$) Active (V_{IL})	TcsA2csI	20	—	ns	
85	$\overline{WLAT}$ input low time	$T_{WLAT}L$	25	—	ns	

Note 1: This specification is by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-TSSOP (ST)	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 20L-VQFN (MQ)	θ_{JA}	—	38.3	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The device Performance Curves are available in a separate document. This is done to keep the file size of this PDF document less than the 10 MB file attachment limit of many mail servers.
The MCP41HVX1 Performance Curves document is literature number DS20005209, and can be found on the Microchip website. Look at the MCP41HVX1 Product Page under Documentation and Software, in the Data Sheets category.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.
Additional descriptions of the device pins follows.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP41HVX1

Pin		Symbol	Type	Buffer Type	Function
TSSOP 14L	VQFN 20L				
1	1	V_L	P	—	Positive Digital Power Supply Input
2	2	SCK	I	ST	SPI Serial Clock pin
3	3	$\overline{CS}$	I	ST	Chip Select
4	4	SDI	I	ST	SPI Serial Data In pin
5	5	SDO	O	—	SPI Serial Data Out
6	6	$\overline{WLAT}$	I	ST	Wiper Latch Enable 0 = Received SPI Shift Register Buffer (SPIBUF) value is transferred to Wiper register 1 = Received SPI data value is held in SPI Shift Register Buffer (SPIBUF)
7	7	$\overline{SHDN}$	I	ST	Shutdown
8	11	DGND	P	—	Ground
9	8, 9, 10, 17, 18, 19, 20	NC	—	—	Pin not internally connected to die. To reduce noise coupling, connect pin either to DGND or V_L.
10	12	V-	P	—	Analog Negative Potential Supply
11	13	P0B	I/O	A	Potentiometer 0 Terminal B
12	14	P0W	I/O	A	Potentiometer 0 Wiper Terminal
13	15	P0A	I/O	A	Potentiometer 0 Terminal A
14	16	V+	P	—	Analog Positive Potential Supply
—	21	EP	P	—	Exposed Pad, connect to V- signal or Not Connected (floating)(1)

Legend: A = Analog, ST = Schmitt Trigger, I = Input, O = Output, I/O = Input/Output, P = Power

Note 1: The VQFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device's V- pin.

3.1 Positive Power Supply Input (V_L)

The V_L pin is the device's positive power supply input. The input power supply is relative to DGND and can range from 1.8V to 5.5V. A decoupling capacitor on V_L (to DGND) is recommended to achieve maximum performance.

While the device's $V_L < V_{min}$ (2.7V), the electrical performance of the device may not meet the data sheet specifications.

3.2 Serial Clock (SCK)

The SCK pin is the serial interface's Serial Clock pin. This pin is connected to the host controllers' SCK pin. The MCP41HVX1 is an SPI slave device, so its SCK pin is an input-only pin.

3.3 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is the serial interface's chip select input. Forcing the $\overline{CS}$ pin to V_{IL} enables the serial commands.

3.4 Serial Data In (SDI)

The SDI pin is the serial interface's Serial Data In pin. This pin is connected to the host controller's SDO pin.

3.5 Serial Data Out (SDO)

The SDO pin is the serial interface's Serial Data Out pin. This pin is connected to the host controller's SDI pin. This pin allows the host controller to read the digital potentiometer registers (Wiper and TCON), or monitor the state of the command error bit.

3.6 Wiper Latch ($\overline{WLAT}$)

The $\overline{WLAT}$ pin is used to delay the transfer of the received wiper value (in the shift register) to the wiper register. This allows this transfer to be synchronized to an external event (such as zero crossing). See **Section 4.3.2 "Wiper Latch"**.

3.7 Shutdown ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is used to force the resistor network terminals into the hardware shutdown state. See **Section 4.3.1 "Shutdown"**.

3.8 Digital Ground (DGND)

The DGND pin is the device's digital ground reference.

3.9 Not Connected (NC)

This pin is not internally connected to the die. To reduce noise coupling, these pins should be connected to either V_L or DGND.

3.10 Analog Negative Voltage (V-)

Analog circuitry negative supply voltage. Must **not** have a higher potential then the DGND pin.

3.11 Potentiometer Terminal B

The Terminal B pin is connected to the internal potentiometer's terminal B.

The potentiometer's terminal B is the fixed connection to the zero-scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The Terminal B pin does not have a polarity relative to the Terminal W or A pins. The Terminal B pin can support both positive and negative current. The voltage on Terminal B must be between V+ and V-.

3.12 Potentiometer Wiper (W) Terminal

The Terminal W pin is connected to the internal potentiometer's Terminal W (the Wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The Terminal W pin does not have a polarity relative to terminal's A or B pins. The Terminal W pin can support both positive and negative current. The voltage on Terminal W must be between V+ and V-.

If the V+ voltage powers-up before the V_L voltage, the wiper is forced to mid-scale once the Analog POR voltage is crossed.

If the V+ voltage powers-up after the V_L voltage is greater than the Digital POR voltage, the wiper is forced to the value in the wiper register once the Analog POR voltage is crossed.

3.13 Potentiometer Terminal A

The Terminal A pin is connected to the internal potentiometer's Terminal A.

The potentiometer's Terminal A is the fixed connection to the full-scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0xFF for 8-bit devices or 0x7F for 7-bit devices.

The Terminal A pin does not have a polarity relative to the Terminal W or B pins. The Terminal A pin can support both positive and negative current. The voltage on Terminal A must be between V+ and V-.

3.14 Analog Positive Voltage (V+)

The analog circuitry's positive supply voltage. The V+ pin must have a higher potential then the V- pin.

3.15 Exposed Pad (EP)

This pad is only on the bottom of the VQFN packages. This pad is conductively connected to the device substrate. The EP pin must be connected to the V- signal or left floating. This pad could be connected to a Printed Circuit Board (PCB) heat sink to assist as a heat sink for the device.

4.0 FUNCTIONAL OVERVIEW

This data sheet covers a family of two volatile digital potentiometer devices that will be referred to as MCP41HVX1.

As the **Device Block Diagram** shows, there are six main functional blocks. These are:

- **Operating Voltage Range**
- **POR/BOR Operation**
- **Memory Map**
- **Control Module**
- **Resistor Network**
- **Serial Interface (SPI)**

The POR/BOR operation and the Memory Map are discussed in this section, and the Resistor Network and SPI operation are described in their own sections. The Device Commands are discussed in **Section 7.0 "Device Commands"**.

4.1 Operating Voltage Range

The MCP41HVX1 devices have four voltage signals. These are:

- V+ - Analog power
- V_L - Digital power
- DGND - Digital ground
- V- - Analog ground

Figure 4-1 shows the two possible power-up sequences: analog power rails power-up first, or digital power rails power-up first. The device has been designed so that either power rail may power-up first. The device has a POR circuit for both digital power circuitry and analog power circuitry.

If the V+ voltage powers-up before the V_L voltage, the wiper is forced to mid-scale once the analog POR voltage is crossed.

If the V+ voltage powers-up after the V_L voltage is greater than the digital POR voltage, the wiper is forced to the value in the wiper register once the analog POR voltage is crossed.

Figure 4-2 shows the three cases of the digital power signals (V_L/DGND) with respect to the analog power signals (V+/V-). The device implements level shifts between the digital and analog power systems, which allows the digital interface voltage to be anywhere in the V+/V- voltage window.

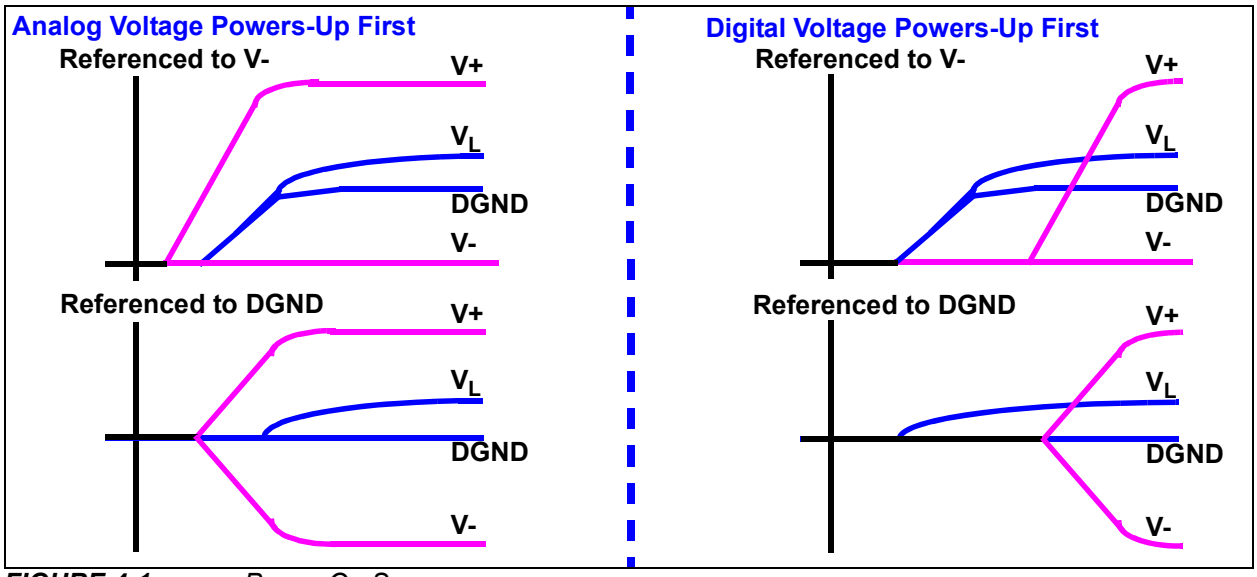


FIGURE 4-1: *Power-On Sequences.*

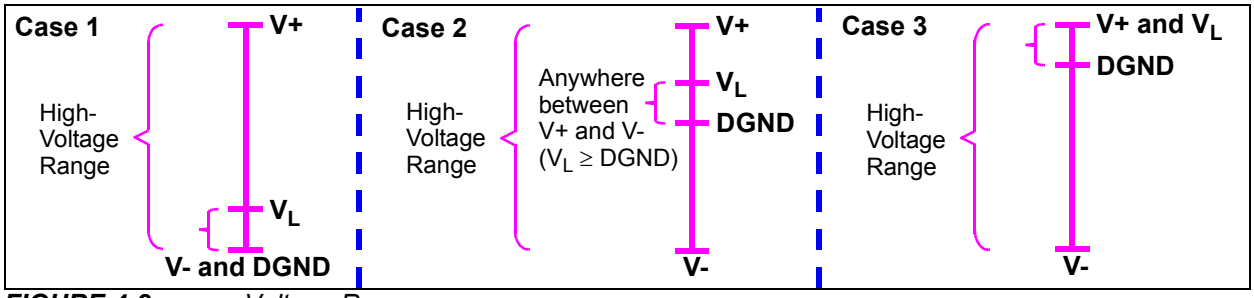


FIGURE 4-2: *Voltage Ranges.*

4.2 POR/BOR Operation

The resistor network's devices are powered by the analog power signals (V+/V-), but the digital logic (including the wiper registers) is powered by the digital power signals (V_L/DGND). So, both the digital circuitry and analog circuitry have independent POR/BOR circuits.

The wiper position will be forced to the default state when the V+ voltage (relative to V-) is above the analog POR/BOR trip point. The wiper register will be in the default state when the V_L voltage (relative to DGND) is above the digital POR/BOR trip point.

The digital-signal-to-analog-signal voltage level shifters require a minimum voltage between the V_L and V- signals. This voltage requirement is below the operating supply voltage specifications. The wiper output may fluctuate while the V_L voltage is less than the level shifter operating voltage, since the analog values may not reflect the digital value. Output issues may be reduced by powering-up the digital supply voltages to their operating voltage before powering the analog supply voltage.

4.2.1 POWER-ON RESET

Each power system has its own independent Power-on Reset circuitry. This is done so that regardless of the power-up sequencing of the analog and digital power rails, the wiper output will be forced to a default value after minimum conditions are met for either power supply.

Table 4-1 shows the interaction between the analog and digital PORs for the V+ and V_L voltages on the wiper pin state.

TABLE 4-1: WIPER PIN STATE BASED ON POR CONDITIONS

V_L Voltage	V+ Voltage		Comments
	V+ < V_{APOR}	V+ ≥ V_{APOR}	
$V_L < V_{DPOR}$	Unknown	Mid-Scale	
$V_L \geq V_{DPOR}$	Unknown	Wiper Register Value(1)	Wiper Register can be updated

Note 1: The default POR state of the wiper register value is the mid-scale value.

4.2.1.1 Digital Circuitry

A Digital Power-on Reset (DPOR) occurs when the device's V_L signal has power applied (referenced from DGND) and the voltage rises above the trip point. A Brown-out Reset (BOR) occurs when a device has power applied to it, and the voltage drops below the trip point.

The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less then 1.8V.

When the device powers-up, the device V_L will cross the V_{POR}/V_{BOR} voltage. Once the V_L voltage crosses the V_{POR}/V_{BOR} voltage, the following happens:

- The volatile wiper registers are loaded with the POR/BOR value
- The TCON registers are loaded with the default values
- The device is capable of digital operation

Table 4-2 shows the default POR/BOR wiper register setting selection.

When V_{POR}/V_{BOR} < V_{DD} < 2.7V, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of incrementing, decrementing, reading and writing to its volatile memory if the proper serial command is executed.

TABLE 4-2: DEFAULT POR/BOR WIPER REGISTER SETTING (DIGITAL)

Typical R_{AB} Value	Package Code	Default POR Wiper Register Setting	Device Resolution	Wiper Code
5.0 kΩ	-502	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
10.0 kΩ	-103	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
50.0 kΩ	-503	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
100.0 kΩ	-104	Mid-Scale	8-bit	7Fh
			7-bit	3Fh

Note 1: Register setting independent of analog power voltage.