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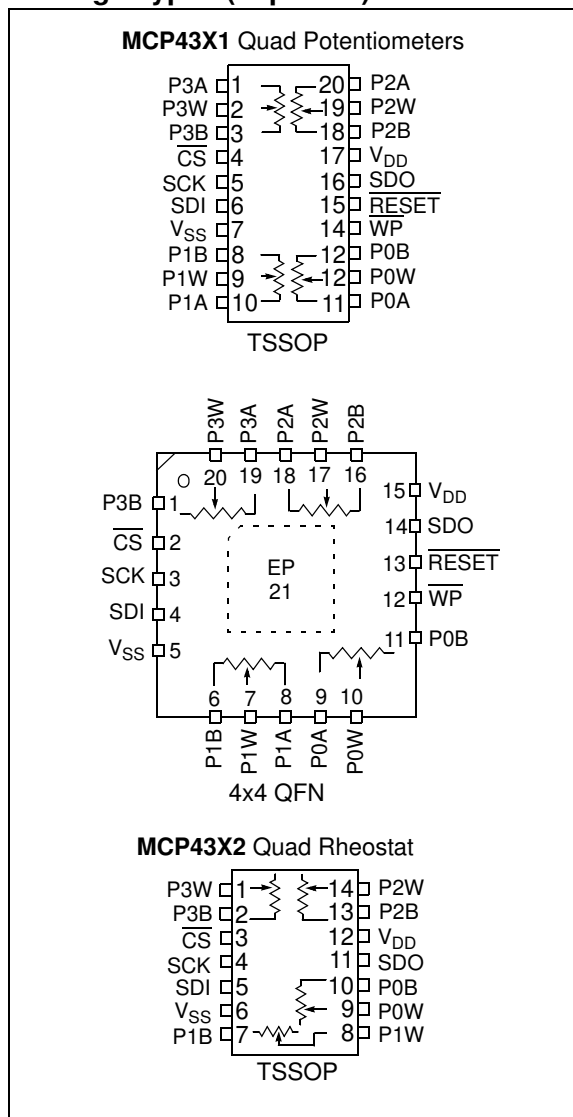


## 7/8-Bit Quad SPI Digital POT with Non-Volatile Memory

### Features

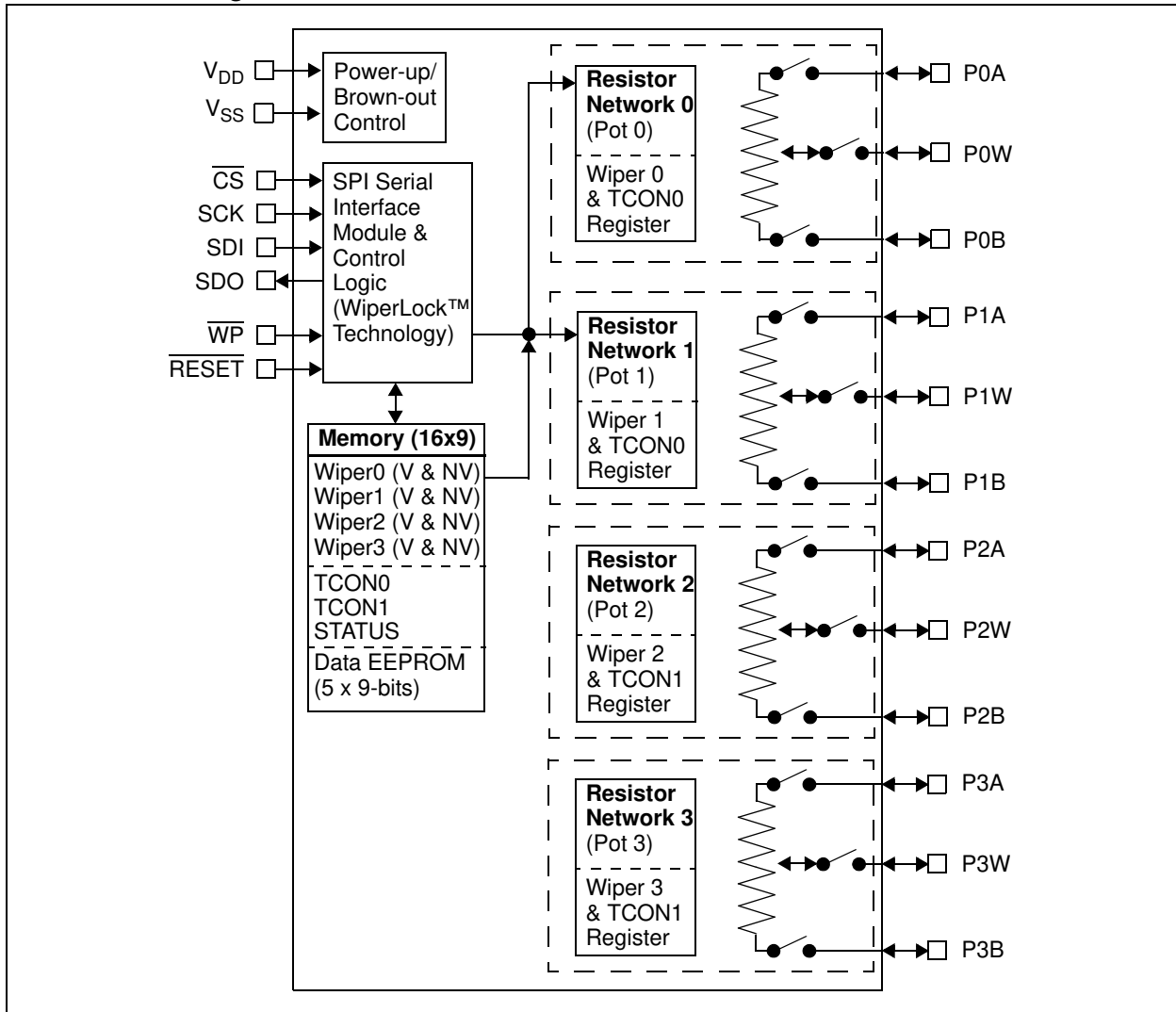
- Quad Resistor Network
- Potentiometer or Rheostat configuration options
- Resistor Network Resolution
  - 7-bit: 128 Resistors (129 Taps)
  - 8-bit: 256 Resistors (257 Taps)
- $R_{AB}$  Resistances options of:
  - 5 k $\Omega$
  - 10 k $\Omega$
  - 50 k $\Omega$
  - 100 k $\Omega$
- Zero Scale to Full Scale Wiper operation
- Low Wiper Resistance: 75  $\Omega$  (typical)
- Low Tempco:
  - Absolute (Rheostat): 50 ppm typical (0°C to 70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- Non-volatile Memory
  - Automatic Recall of Saved Wiper Setting
  - WiperLock™ Technology
- SPI serial interface (10 MHz, modes 0,0 & 1,1)
  - High-Speed Read/Writes to wiper registers
  - Read/Write to Data EEPROM registers
  - Serially enabled EEPROM write protect
- Resistor Network Terminal Disconnect Feature via Terminal Control (TCON) Register
- Reset input pin
- Write Protect Feature:
  - Hardware Write Protect ( $\overline{WP}$ ) Control pin
  - Software Write Protect (WP) Configuration bit
- Brown-out reset protection (1.5V typical)
- Serial Interface Inactive current (2.5  $\mu$ A typical)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Supports Split Rail Applications
- Internal weak pull-up on all digital inputs
- Wide Operating Voltage:
  - 2.7V to 5.5V - Device Characteristics Specified
  - 1.8V to 5.5V - Device Operation
- Wide Bandwidth (-3 dB) Operation:
  - 2 MHz (typical) for 5.0 k $\Omega$  device
- Extended temperature range (-40°C to +125°C)

### Package Types (Top View)



# MCP434X/436X

## Device Block Diagram



## Device Features

Device	# of POTs	Wiper Configuration	Control Interface	Memory Type	WiperLock Technology	POR Wiper Setting	Resistance (typical)		# of Taps	V <sub>DD</sub> Operating Range <sup>(2)</sup>
							R <sub>AB</sub> Options (kΩ)	Wiper - R <sub>W</sub> (Ω)		
MCP4331 <sup>(3)</sup>	4	Potentiometer <sup>(1)</sup>	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4332 <sup>(3)</sup>	4	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4341	4	Potentiometer <sup>(1)</sup>	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4342	4	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4351 <sup>(3)</sup>	4	Potentiometer <sup>(1)</sup>	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4352 <sup>(3)</sup>	4	Rheostat	SPI	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4361	4	Potentiometer <sup>(1)</sup>	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4362	4	Rheostat	SPI	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V

**Note 1:** Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

**2:** Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.

**3:** Please check Microchip web site for device release and availability.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Voltage on $V_{DD}$ with respect to $V_{SS}$	-0.6V to +7.0V
Voltage on $\overline{CS}$ , SCK, SDI, SDI/SDO, $\overline{WP}$ , and RESET with respect to $V_{SS}$	-0.6V to 12.5V
Voltage on all other pins (PxA, PxW, PxB, and SDO) with respect to $V_{SS}$	-0.3V to $V_{DD} + 0.3V$
Input clamp current, $I_{IK}$ ( $V_I < 0$ , $V_I > V_{DD}$ , $V_I > V_{PP}$ ON HV pins)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 20$ mA
Maximum output current sunk by any Output pin	25 mA
Maximum output current sourced by any Output pin	25 mA
Maximum current out of $V_{SS}$ pin	100 mA
Maximum current into $V_{DD}$ pin	100 mA
Maximum current into PxA, PxW & PxB pins	$\pm 2.5$ mA
Storage temperature	-65°C to +150°C
Ambient temperature with power applied	-40°C to +125°C
Package power dissipation ( $T_A = +50^\circ\text{C}$ , $T_J = +150^\circ\text{C}$ )	
TSSOP-14	1000 mW
TSSOP-20	1110 mW
QFN-20 (4x4)	2320 mW
Soldering temperature of leads (10 seconds)	+300°C
ESD protection on all pins	$\geq 4$ kV (HBM), $\geq 300$ V (MM)
Maximum Junction Temperature ( $T_J$ )	+150°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# MCP434X/436X

## AC/DC CHARACTERISTICS

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .				
Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	$V_{DD}$	2.7	—	5.5	V	
		1.8	—	2.7	V	Serial Interface only.
$\overline{\text{CS}}$ , $\text{SDI}$ , $\text{SDO}$ , $\text{SCK}$ , $\text{WP}$ , $\text{RESET}$ pin Voltage Range	$V_{HV}$	$V_{SS}$	—	12.5V	V	$V_{DD} \geq 4.5\text{V}$ The $\overline{\text{CS}}$ pin will be at one of three input levels ( $V_{IL}$ , $V_{IH}$ or $V_{IHH}$ ). (Note 6)
		$V_{SS}$	—	$V_{DD} + 8.0\text{V}$	V	$V_{DD} < 4.5\text{V}$
$V_{DD}$ Start Voltage to ensure Wiper Reset	$V_{BOR}$	—	—	1.65	V	RAM retention voltage ( $V_{RAM}$ ) $< V_{BOR}$
$V_{DD}$ Rise Rate to ensure Power-on Reset	$V_{DDRR}$	(Note 9)			V/ms	
Delay after device exits the reset state ( $V_{DD} > V_{BOR}$ )	$T_{BORD}$	—	10	20	$\mu\text{s}$	
Supply Current (Note 10)	$I_{DD}$	—	—	450	$\mu\text{A}$	Serial Interface Active, $V_{DD} = 5.5\text{V}$ , $\overline{\text{CS}} = V_{IL}$ , $\text{SCK} @ 5\text{ MHz}$ , write all 0's to volatile Wiper 0 (address 0h)
		—	—	1	mA	EE Write Current, $V_{DD} = 5.5\text{V}$ , $\overline{\text{CS}} = V_{IL}$ , $\text{SCK} @ 5\text{ MHz}$ , write all 0's to non-volatile Wiper 0 (address 2h)
		—	2.5	5	$\mu\text{A}$	Serial Interface Inactive, $\overline{\text{CS}} = V_{IH}$ , $V_{DD} = 5.5\text{V}$
		—	0.55	1	mA	Serial Interface Active, $V_{DD} = 5.5\text{V}$ , $\overline{\text{CS}} = V_{IHH}$ , $\text{SCK} @ 5\text{ MHz}$ , decrement non-volatile Wiper 0 (address 2h)

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** **MCP43X1** only.
- 4:** **MCP43X2** only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.

## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .					
Parameters	Sym	Min	Typ	Max	Units	Conditions	
Resistance ( $\pm 20\%$ )	$R_{AB}$	4.0	5	6.0	$\text{k}\Omega$	-502 devices ( <b>Note 1</b> )	
		8.0	10	12.0	$\text{k}\Omega$	-103 devices ( <b>Note 1</b> )	
		40.0	50	60.0	$\text{k}\Omega$	-503 devices ( <b>Note 1</b> )	
		80.0	100	120.0	$\text{k}\Omega$	-104 devices ( <b>Note 1</b> )	
Resolution	N	257			Taps	8-bit No Missing Codes	
		129			Taps	7-bit No Missing Codes	
Step Resistance	$R_S$	—	$R_{AB} / (256)$	—	$\Omega$	8-bit <b>Note 6</b>	
		—	$R_{AB} / (128)$	—	$\Omega$	7-bit <b>Note 6</b>	
Nominal Resistance Match	$( R_{ABWC} - R_{ABMEAN} ) / R_{ABMEAN}$	—	0.2	1.50	%	<b>MCP43X1</b> devices only	
		—	0.2	1.25	%		
		—	0.2	1.0	%		
		—	0.2	1.0	%		
	$( R_{BWWC} - R_{BWMEAN} ) / R_{BWMEAN}$	—	0.25	1.75	%	Code = Full Scale	
		—	0.25	1.50	%		
		—	0.25	1.25	%		
		—	0.25	1.25	%		
Wiper Resistance ( <b>Note 3, Note 4</b> )	$R_W$	—	75	160	$\Omega$	$V_{DD} = 5.5\text{ V}$ , $I_W = 2.0\text{ mA}$ , code = 00h	
		—	75	300	$\Omega$	$V_{DD} = 2.7\text{ V}$ , $I_W = 2.0\text{ mA}$ , code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB} / \Delta T$	—	50	—	$\text{ppm}/^{\circ}\text{C}$	$T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	
		—	100	—	$\text{ppm}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	
		—	150	—	$\text{ppm}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	
Ratiometric Tempco	$\Delta V_{WB} / \Delta T$	—	15	—	$\text{ppm}/^{\circ}\text{C}$	Code = Midscale (80h or 40h)	

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** **MCP43X1** only.
- 4:** **MCP43X2** only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.

# MCP434X/436X

## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .				
Parameters	Sym	Min	Typ	Max	Units	Conditions
Resistor Terminal Input Voltage Range (Terminals A, B and W)	$V_A, V_W, V_B$	$V_{SS}$	—	$V_{DD}$	V	<b>Note 5, Note 6</b>
Maximum current through A, W or B	$I_W$	—	—	2.5	mA	<b>Note 6</b> , Worst case current through wiper when wiper is either Full Scale or Zero Scale.
Leakage current into A, W or B	$I_{WL}$	—	100	—	nA	<b>MCP43X1</b> $PxA = PxW = PxB = V_{SS}$
		—	100	—	nA	<b>MCP43X2</b> $PxB = PxW = V_{SS}$

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** **MCP43X1** only.
- 4:** **MCP43X2** only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.

## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions		
Full Scale Error (MCP43X1 only) (8-bit code = 100h, 7-bit code = 80h)	$V_{WFSE}$	-6.0	-0.1	—	LSb	5 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-4.0	-0.1	—	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-3.5	-0.1	—	LSb	10 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-2.0	-0.1	—	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-0.8	-0.1	—	LSb	50 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-0.5	-0.1	—	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-0.5	-0.1	—	LSb	100 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		-0.5	-0.1	—	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
Zero Scale Error (MCP43X1 only) (8-bit code = 00h, 7-bit code = 00h)	$V_{WZSE}$	—	+0.1	+6.0	LSb	5 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+3.0	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+3.5	LSb	10 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+2.0	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+0.8	LSb	50 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+0.5	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+0.5	LSb	100 k $\Omega$	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
		—	+0.1	+0.5	LSb		7-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$
Potentiometer Integral Non-linearity	INL	-1	$\pm 0.5$	+1	LSb	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$	
		-0.5	$\pm 0.25$	+0.5	LSb	7-bit	MCP43X1 devices only (Note 2)	
Potentiometer Differential Non-linearity	DNL	-0.5	$\pm 0.25$	+0.5	LSb	8-bit	$3.0\text{V} \leq V_{DD} \leq 5.5\text{V}$	
		-0.25	$\pm 0.125$	+0.25	LSb	7-bit	MCP43X1 devices only (Note 2)	
Bandwidth -3 dB (See Figure 2-54, load = 30 pF)	BW	—	2	—	MHz	5 k $\Omega$	8-bit	Code = 80h
		—	2	—	MHz		7-bit	Code = 40h
		—	1	—	MHz	10 k $\Omega$	8-bit	Code = 80h
		—	1	—	MHz		7-bit	Code = 40h
		—	200	—	kHz	50 k $\Omega$	8-bit	Code = 80h
		—	200	—	kHz		7-bit	Code = 40h
		—	100	—	kHz	100 k $\Omega$	8-bit	Code = 80h
		—	100	—	kHz		7-bit	Code = 40h

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** MCP43X1 only.
- 4:** MCP43X2 only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The MCP43X1 is externally connected to match the configurations of the MCP43X2, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.



# MCP434X/436X

## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions		
Rheostat Integral Non-linearity <b>MCP43X1</b> (Note 4, Note 8) <b>MCP43X2</b> devices only (Note 4)	R-INL	-1.5	$\pm 0.5$	+1.5	LSb	5 k $\Omega$	8-bit	5.5V, $I_W = 900\text{ }\mu\text{A}$
		-8.25	+4.5	+8.25	LSb			3.0V, $I_W = 480\text{ }\mu\text{A}$ (Note 7)
		-1.125	$\pm 0.5$	+1.125	LSb	5 k $\Omega$	7-bit	5.5V, $I_W = 900\text{ }\mu\text{A}$
		-6.0	+4.5	+6.0	LSb			3.0V, $I_W = 480\text{ }\mu\text{A}$ (Note 7)
		-1.5	$\pm 0.5$	+1.5	LSb	10 k $\Omega$	8-bit	5.5V, $I_W = 450\text{ }\mu\text{A}$
		-5.5	+2.5	+5.5	LSb			3.0V, $I_W = 240\text{ }\mu\text{A}$ (Note 7)
		-1.125	$\pm 0.5$	+1.125	LSb	10 k $\Omega$	7-bit	5.5V, $I_W = 450\text{ }\mu\text{A}$
		-4.0	+2.5	+4.0	LSb			3.0V, $I_W = 240\text{ }\mu\text{A}$ (Note 7)
		-1.5	$\pm 0.5$	+1.5	LSb	50 k $\Omega$	8-bit	5.5V, $I_W = 90\text{ }\mu\text{A}$
		-2.0	+1	+2.0	LSb			3.0V, $I_W = 48\text{ }\mu\text{A}$ (Note 7)
		-1.125	$\pm 0.5$	+1.125	LSb	50 k $\Omega$	7-bit	5.5V, $I_W = 90\text{ }\mu\text{A}$
		-1.5	+1	+1.5	LSb			3.0V, $I_W = 48\text{ }\mu\text{A}$ (Note 7)
		-1.0	$\pm 0.5$	+1.0	LSb	100 k $\Omega$	8-bit	5.5V, $I_W = 45\text{ }\mu\text{A}$
		-1.5	+0.25	+1.5	LSb			3.0V, $I_W = 24\text{ }\mu\text{A}$ (Note 7)
		-0.8	$\pm 0.5$	+0.8	LSb	100 k $\Omega$	7-bit	5.5V, $I_W = 45\text{ }\mu\text{A}$
		-1.125	+0.25	+1.125	LSb			3.0V, $I_W = 24\text{ }\mu\text{A}$ (Note 7)

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- Note 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- Note 3:** **MCP43X1** only.
- Note 4:** **MCP43X2** only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- Note 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- Note 6:** This specification by design.
- Note 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- Note 8:** The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
- Note 9:** POR/BOR is not rate dependent.
- Note 10:** Supply current is independent of current through the resistor network.

## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions		
Rheostat Differential Non-linearity <b>MCP43X1</b> ( <b>Note 4</b> , <b>Note 8</b> ) <b>MCP43X2</b> devices only ( <b>Note 4</b> )	R-DNL	-0.5	$\pm 0.25$	+0.5	LSb	5 k $\Omega$	8-bit	5.5V, $I_W = 900\text{ }\mu\text{A}$
		-1.0	+0.5	+1.0	LSb			3.0V ( <b>Note 7</b> )
		-0.375	$\pm 0.25$	+0.375	LSb	10 k $\Omega$	7-bit	5.5V, $I_W = 900\text{ }\mu\text{A}$
		-0.75	+0.5	+0.75	LSb			3.0V ( <b>Note 7</b> )
		-0.5	$\pm 0.25$	+0.5	LSb	10 k $\Omega$	8-bit	5.5V, $I_W = 450\text{ }\mu\text{A}$
		-1.0	+0.25	+1.0	LSb			3.0V ( <b>Note 7</b> )
		-0.375	$\pm 0.25$	+0.375	LSb	10 k $\Omega$	7-bit	5.5V, $I_W = 450\text{ }\mu\text{A}$
		-0.75	+0.5	+0.75	LSb			3.0V ( <b>Note 7</b> )
		-0.5	$\pm 0.25$	+0.5	LSb	50 k $\Omega$	8-bit	5.5V, $I_W = 90\text{ }\mu\text{A}$
		-0.5	$\pm 0.25$	+0.5	LSb			3.0V ( <b>Note 7</b> )
		-0.375	$\pm 0.25$	+0.375	LSb	50 k $\Omega$	7-bit	5.5V, $I_W = 90\text{ }\mu\text{A}$
		-0.375	$\pm 0.25$	+0.375	LSb			3.0V ( <b>Note 7</b> )
		-0.5	$\pm 0.25$	+0.5	LSb	100 k $\Omega$	8-bit	5.5V, $I_W = 45\text{ }\mu\text{A}$
		-0.5	$\pm 0.25$	+0.5	LSb			3.0V ( <b>Note 7</b> )
		-0.375	$\pm 0.25$	+0.375	LSb	100 k $\Omega$	7-bit	5.5V, $I_W = 45\text{ }\mu\text{A}$
		-0.375	$\pm 0.25$	+0.375	LSb			3.0V ( <b>Note 7</b> )
Capacitance ( $P_A$ )	$C_{AW}$	—	75	—	pF	f = 1 MHz, Code = Full Scale		
Capacitance ( $P_W$ )	$C_W$	—	120	—	pF	f = 1 MHz, Code = Full Scale		
Capacitance ( $P_B$ )	$C_{BW}$	—	75	—	pF	f = 1 MHz, Code = Full Scale		

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** **MCP43X1** only.
- 4:** **MCP43X2** only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.

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## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .				
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Digital Inputs/Outputs (<math>\overline{\text{CS}}</math>, <math>\overline{\text{SDI}}</math>, <math>\overline{\text{SDO}}</math>, <math>\overline{\text{SCK}}</math>, <math>\overline{\text{WP}}</math>, <math>\overline{\text{RESET}}</math>)</b>						
Schmitt Trigger High Input Threshold	$V_{IH}$	$0.45 V_{DD}$	—	—	V	$2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$ (Allows $2.7\text{V}$ Digital $V_{DD}$ with $5\text{V}$ Analog $V_{DD}$ )
		$0.5 V_{DD}$	—	—	V	$1.8\text{V} \leq V_{DD} \leq 2.7\text{V}$
Schmitt Trigger Low Input Threshold	$V_{IL}$	—	—	$0.2V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	$V_{HYS}$	—	$0.1V_{DD}$	—	V	
High Voltage Input Entry Voltage	$V_{IHH}$	8.5	—	$12.5^{(6)}$	V	Threshold for WiperLock™ Technology
High Voltage Input Exit Voltage	$V_{IHH}$	—	—	$V_{DD} + 0.8\text{V}$	V	
High Voltage Limit	$V_{MAX}$	—	—	$12.5^{(6)}$	V	Pin can tolerate $V_{MAX}$ or less.
Output Low Voltage (SDO)	$V_{OL}$	$V_{SS}$	—	$0.3V_{DD}$	V	$I_{OL} = 5\text{ mA}$ , $V_{DD} = 5.5\text{V}$
		$V_{SS}$	—	$0.3V_{DD}$	V	$I_{OL} = 1\text{ mA}$ , $V_{DD} = 1.8\text{V}$
Output High Voltage (SDO)	$V_{OH}$	$0.7V_{DD}$	—	$V_{DD}$	V	$I_{OH} = -2.5\text{ mA}$ , $V_{DD} = 5.5\text{V}$
		$0.7V_{DD}$	—	$V_{DD}$	V	$I_{OL} = -1\text{ mA}$ , $V_{DD} = 1.8\text{V}$

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** **MCP43X1** only.
- 4:** **MCP43X2** only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The **MCP43X1** is externally connected to match the configurations of the **MCP43X2**, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.

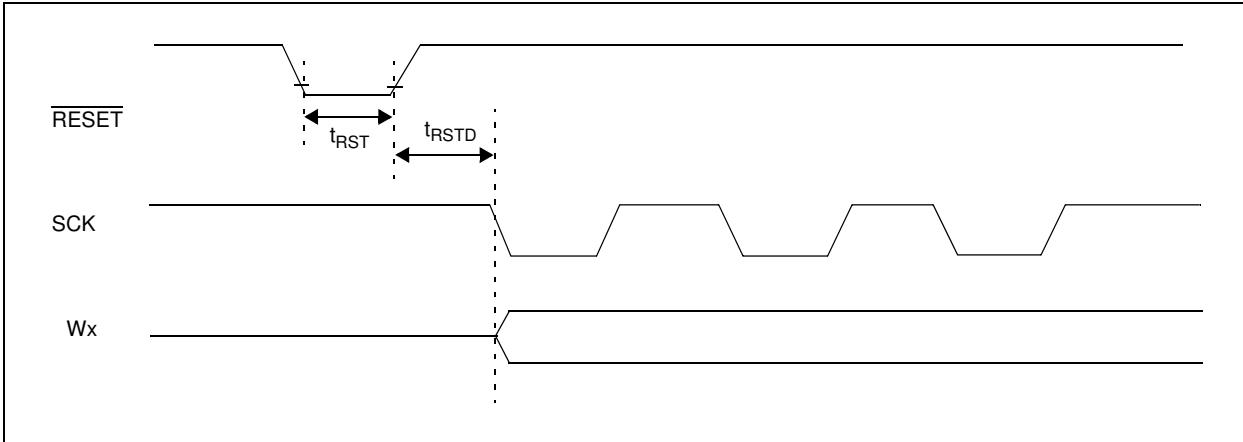
## AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
		All parameters apply across the specified operating ranges unless noted.					
		$V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices.					
		Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .					
Parameters	Sym	Min	Typ	Max	Units	Conditions	
Weak Pull-up Current	$I_{PU}$	—	—	1.75	mA	Internal $V_{DD}$ pull-up, $V_{IHH}$ pull-down, $V_{DD} = 5.5\text{V}$ , $V_{\overline{CS}} = 12.5\text{V}$	
		—	170	—	$\mu\text{A}$	$\overline{CS}$ pin, $V_{DD} = 5.5\text{V}$ , $V_{\overline{CS}} = 3\text{V}$	
$\overline{CS}$ Pull-up / Pull-down Resistance	$R_{CS}$	—	16	—	$\text{k}\Omega$	$V_{DD} = 5.5\text{V}$ , $V_{\overline{CS}} = 3\text{V}$	
$\overline{RESET}$ Pull-up Resistance	$R_{RESET}$	—	16	—	$\text{k}\Omega$	$V_{DD} = 5.5\text{V}$ , $V_{\overline{RESET}} = 0\text{V}$	
Input Leakage Current	$I_{IL}$	-1	—	1	$\mu\text{A}$	$V_{IN} = V_{DD}$ (all pins) and $V_{IN} = V_{SS}$ (all pins except $\overline{RESET}$ )	
Pin Capacitance	$C_{IN}, C_{OUT}$	—	10	—	pF	$f_C = 20\text{ MHz}$	
<b>RAM (Wiper, TCON) Value</b>							
Value Range	N	0h	—	1FFh	hex	8-bit device	
		0h	—	1FFh	hex	7-bit device	
TCON POR/BOR Setting		1FF			hex	All Terminals connected	
<b>EEPROM</b>							
Endurance	$E_{endurance}$	—	1M	—	Cycles		
EEPROM Range	N	0h	—	1FFh	hex		
Initial NV Wiper POR/BOR Setting	N	080h			hex	8-bit	WiperLock Technology = Off
		040h			hex	7-bit	WiperLock Technology = Off
Initial EEPROM POR/BOR Setting	N	000h			hex		
EEPROM Programming Write Cycle Time	$t_{WC}$	—	3	10	ms		
<b>Power Requirements</b>							
Power Supply Sensitivity (MCP43X1)	PSS	—	0.0015	0.0035	%/%	8-bit	$V_{DD} = 2.7\text{V}$ to $5.5\text{V}$ , $V_A = 2.7\text{V}$ , Code = 80h
		—	0.0015	0.0035	%/%	7-bit	$V_{DD} = 2.7\text{V}$ to $5.5\text{V}$ , $V_A = 2.7\text{V}$ , Code = 40h

- Note 1:** Resistance is defined as the resistance between terminal A to terminal B.
- 2:** INL and DNL are measured at  $V_W$  with  $V_A = V_{DD}$  and  $V_B = V_{SS}$ .
- 3:** MCP43X1 only.
- 4:** MCP43X2 only, includes  $V_{WZSE}$  and  $V_{WFSE}$ .
- 5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.
- 6:** This specification by design.
- 7:** Non-linearity is affected by wiper resistance ( $R_W$ ), which changes significantly over voltage and temperature.
- 8:** The MCP43X1 is externally connected to match the configurations of the MCP43X2, and then tested.
- 9:** POR/BOR is not rate dependent.
- 10:** Supply current is independent of current through the resistor network.

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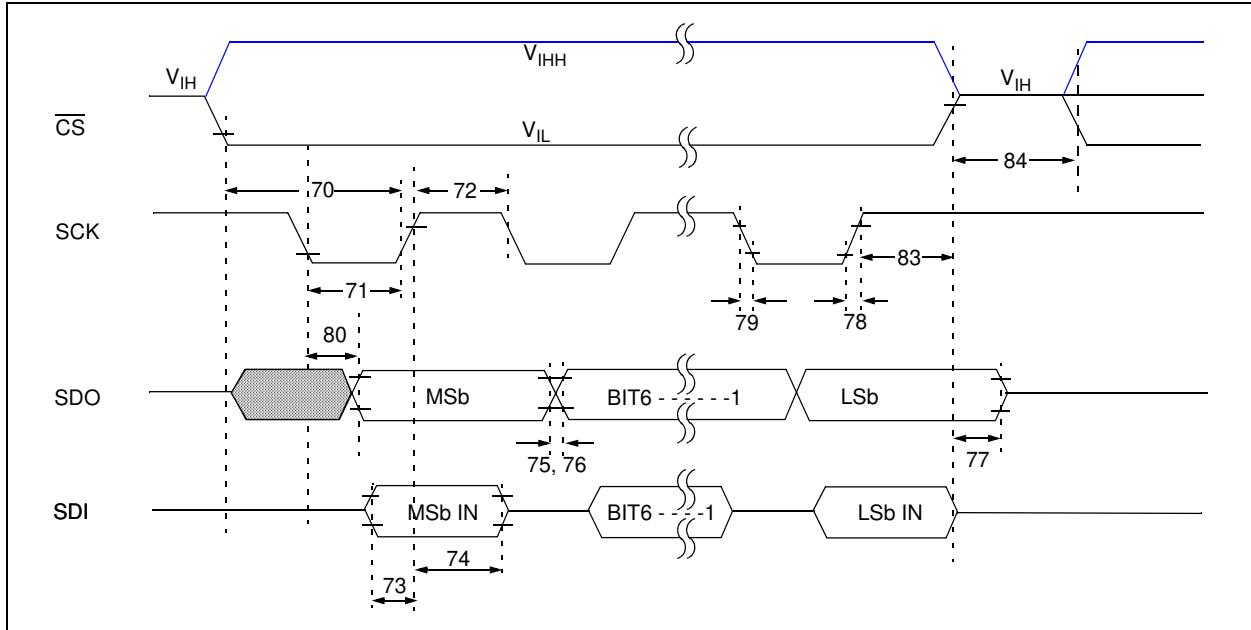
## 1.1 SPI Mode Timing Waveforms and Requirements



**FIGURE 1-1:** RESET Waveforms.

**TABLE 1-1: RESET TIMING**

Timing Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) All parameters apply across the specified operating ranges unless noted. $V_{DD} = +2.7\text{V}$ to $5.5\text{V}$ , $5\text{ k}\Omega$ , $10\text{ k}\Omega$ , $50\text{ k}\Omega$ , $100\text{ k}\Omega$ devices. Typical specifications represent values for $V_{DD} = 5.5\text{V}$ , $T_A = +25^{\circ}\text{C}$ .				
Parameters	Sym	Min	Typ	Max	Units	Conditions
RESET pulse width	$t_{RST}$	50	—	—	ns	
RESET rising edge normal mode (Wiper driving and SPI interface operational)	$t_{RSTD}$	—	—	20	ns	



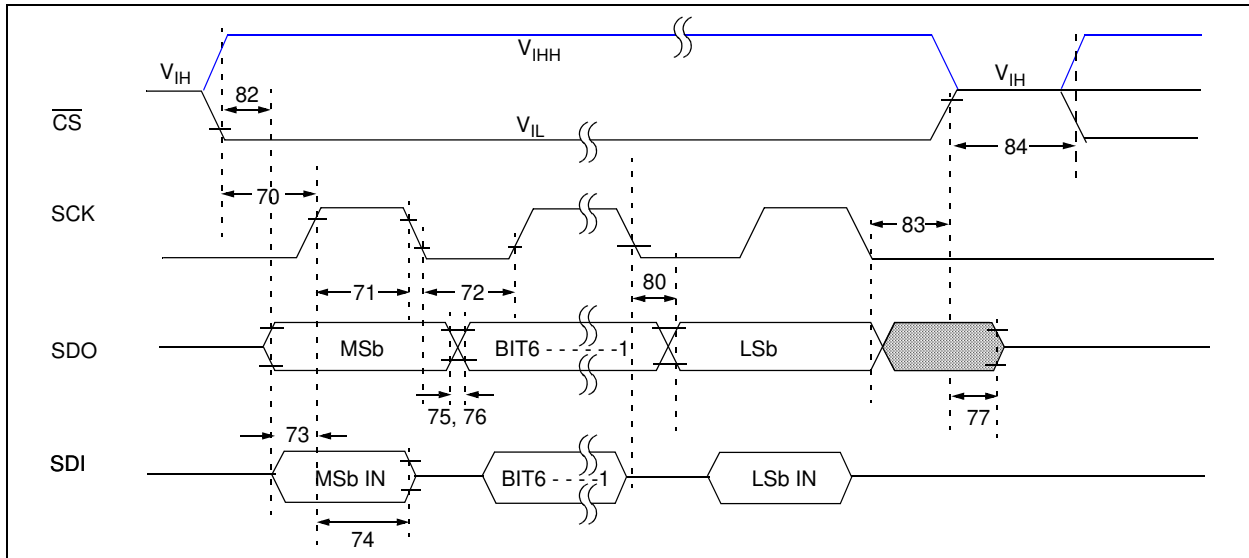
**FIGURE 1-2:** SPI Timing Waveform (Mode = 11).

**TABLE 1-2: SPI REQUIREMENTS (MODE = 11)**

#	Characteristic	Symbol	Min	Max	Units	Conditions
	SCK Input Frequency	$F_{SCK}$	—	10	MHz	$V_{DD} = 2.7V$ to $5.5V$
			—	1	MHz	$V_{DD} = 1.8V$ to $2.7V$
70	$\overline{CS}$ Active ( $V_{IL}$ or $V_{IHH}$ ) to SCK $\uparrow$ input	$T_{csA2scH}$	60	—	ns	
71	SCK input high time	$T_{scH}$	45	—	ns	$V_{DD} = 2.7V$ to $5.5V$
			500	—	ns	$V_{DD} = 1.8V$ to $2.7V$
72	SCK input low time	$T_{scL}$	45	—	ns	$V_{DD} = 2.7V$ to $5.5V$
			500	—	ns	$V_{DD} = 1.8V$ to $2.7V$
73	Setup time of SDI input to SCK $\uparrow$ edge	$T_{DIv2scH}$	10	—	ns	$V_{DD} = 2.7V$ to $5.5V$
			20	—	ns	$V_{DD} = 1.8V$ to $2.7V$
74	Hold time of SDI input from SCK $\uparrow$ edge	$T_{scH2DI}$	20	—	ns	
77	$\overline{CS}$ Inactive ( $V_{IH}$ ) to SDO output hi-impedance	$T_{csH2DOZ}$	—	50	ns	<b>Note 1</b>
80	SDO data output valid after SCK $\downarrow$ edge	$T_{scL2DOV}$	—	70	ns	$V_{DD} = 2.7V$ to $5.5V$
			—	170	ns	$V_{DD} = 1.8V$ to $2.7V$
83	$\overline{CS}$ Inactive ( $V_{IH}$ ) after SCK $\uparrow$ edge	$T_{scH2csl}$	100	—	ns	$V_{DD} = 2.7V$ to $5.5V$
			1	—	ms	$V_{DD} = 1.8V$ to $2.7V$
84	Hold time of $\overline{CS}$ Inactive ( $V_{IH}$ ) to $\overline{CS}$ Active ( $V_{IL}$ or $V_{IHH}$ )	$T_{csA2csl}$	50	—	ns	

**Note 1:** This specification by design.

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**FIGURE 1-3:** SPI Timing Waveform (Mode = 00).

**TABLE 1-3: SPI REQUIREMENTS (MODE = 00)**

#	Characteristic	Symbol	Min	Max	Units	Conditions
	SCK Input Frequency	$F_{SCK}$	—	10	MHz	$V_{DD} = 2.7V$ to 5.5V
			—	1	MHz	$V_{DD} = 1.8V$ to 2.7V
70	$\overline{CS}$ Active ( $V_{IL}$ or $V_{IHH}$ ) to SCK $\uparrow$ input	$T_{csA2sch}$	60	—	ns	
71	SCK input high time	$T_{sch}$	45	—	ns	$V_{DD} = 2.7V$ to 5.5V
			500	—	ns	$V_{DD} = 1.8V$ to 2.7V
72	SCK input low time	$T_{scL}$	45	—	ns	$V_{DD} = 2.7V$ to 5.5V
			500	—	ns	$V_{DD} = 1.8V$ to 2.7V
73	Setup time of SDI input to SCK $\uparrow$ edge	$T_{diV2sch}$	10	—	ns	
74	Hold time of SDI input from SCK $\uparrow$ edge	$T_{sch2diL}$	20	—	ns	
77	$\overline{CS}$ Inactive ( $V_{IH}$ ) to SDO output hi-impedance	$T_{csH2doZ}$	—	50	ns	<b>Note 1</b>
80	SDO data output valid after SCK $\downarrow$ edge	$T_{scL2doV}$	—	70	ns	$V_{DD} = 2.7V$ to 5.5V
			—	170	ns	$V_{DD} = 1.8V$ to 2.7V
82	SDO data output valid after $\overline{CS}$ Active ( $V_{IL}$ or $V_{IHH}$ )	$T_{ssL2doV}$	—	85	ns	
83	$\overline{CS}$ Inactive ( $V_{IH}$ ) after SCK $\downarrow$ edge	$T_{sch2csl}$	100	—	ns	$V_{DD} = 2.7V$ to 5.5V
			1	—	ms	$V_{DD} = 1.8V$ to 2.7V
84	Hold time of $\overline{CS}$ Inactive ( $V_{IH}$ ) to $\overline{CS}$ Active ( $V_{IL}$ or $V_{IHH}$ )	$T_{csA2csl}$	50	—	ns	

**Note 1:** This specification by design.

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_{SS} = GND$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+125	°C	
Operating Temperature Range	$T_A$	-40	—	+125	°C	
Storage Temperature Range	$T_A$	-65	—	+150	°C	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	°C/W	
Thermal Resistance, 20L-QFN	$\theta_{JA}$	—	43	—	°C/W	
Thermal Resistance, 20L-TSSOP	$\theta_{JA}$	—	90	—	°C/W	



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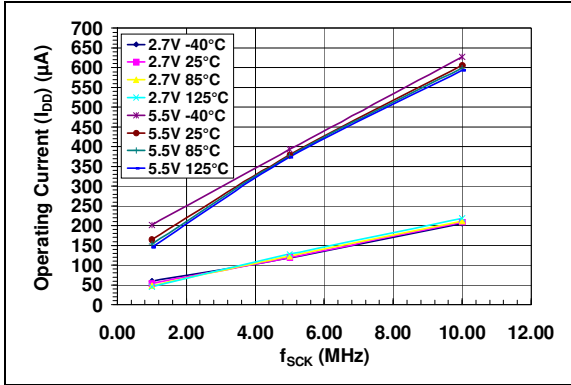
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NOTES:

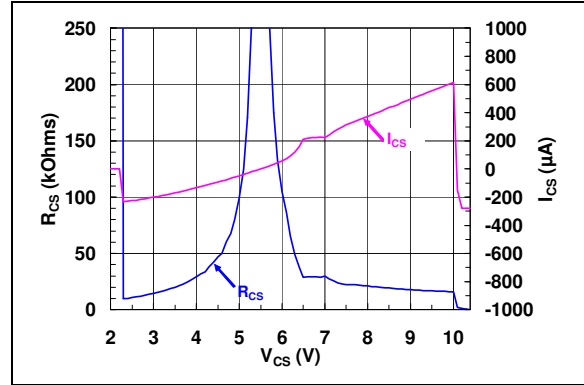
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

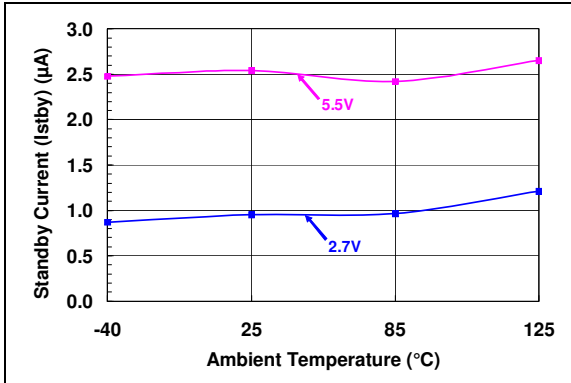
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



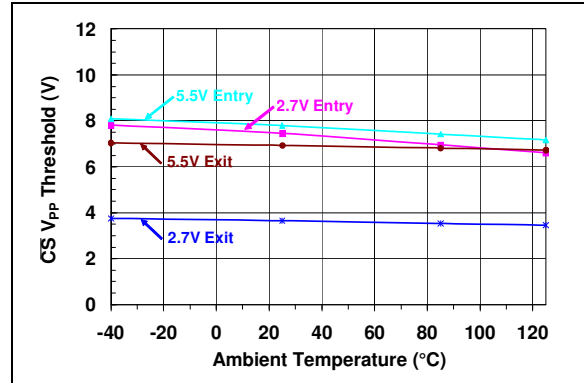
**FIGURE 2-1:** Device Current ( $I_{DD}$ ) vs. SPI Frequency ( $f_{SCK}$ ) and Ambient Temperature ( $V_{DD} = 2.7\text{V}$  and  $5.5\text{V}$ ).



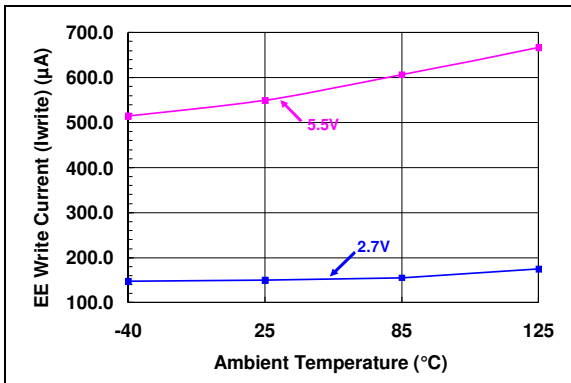
**FIGURE 2-4:**  $\overline{CS}$  Pull-up/Pull-down Resistance ( $R_{\overline{CS}}$ ) and Current ( $I_{\overline{CS}}$ ) vs.  $\overline{CS}$  Input Voltage ( $V_{\overline{CS}}$ ) ( $V_{DD} = 5.5\text{V}$ ).



**FIGURE 2-2:** Device Current ( $I_{SHDN}$ ) and  $V_{DD}$  ( $\overline{CS} = V_{DD}$ ) vs. Ambient Temperature.



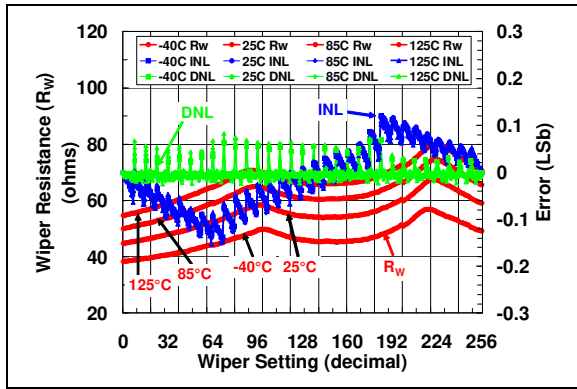
**FIGURE 2-5:**  $\overline{CS}$  High Input Entry/Exit Threshold vs. Ambient Temperature and  $V_{DD}$ .



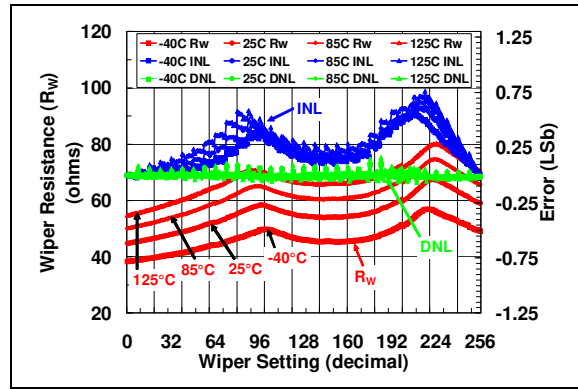
**FIGURE 2-3:** Write Current ( $I_{WRITE}$ ) vs. Ambient Temperature and  $V_{DD}$ .

# MCP434X/436X

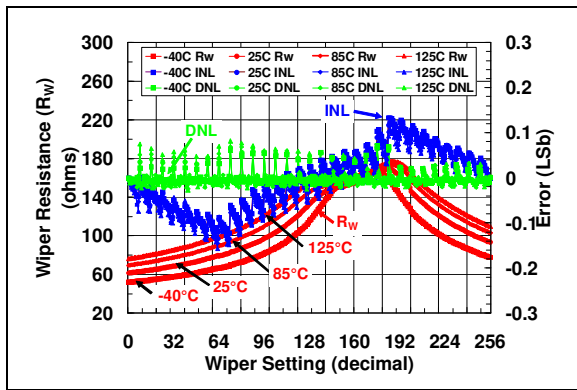
Note: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



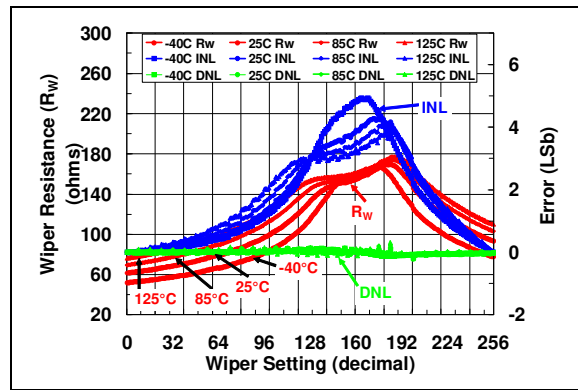
**FIGURE 2-6:** 5 kΩ Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



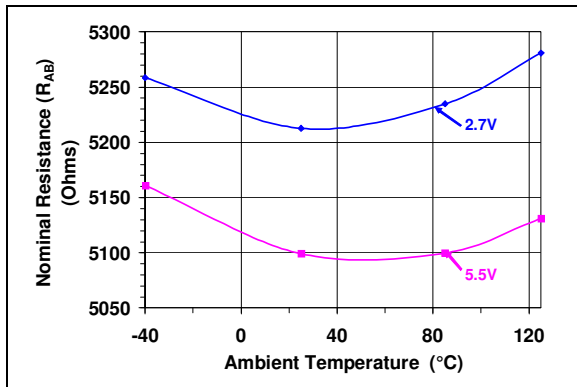
**FIGURE 2-9:** 5 kΩ Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



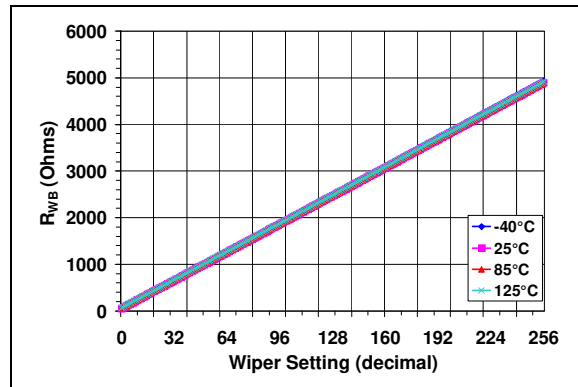
**FIGURE 2-7:** 5 kΩ Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).



**FIGURE 2-10:** 5 kΩ Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).

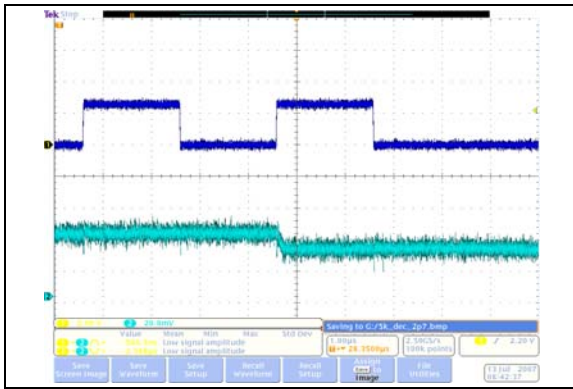


**FIGURE 2-8:** 5 kΩ – Nominal Resistance ( $\Omega$ ) vs. Ambient Temperature and  $V_{DD}$ .

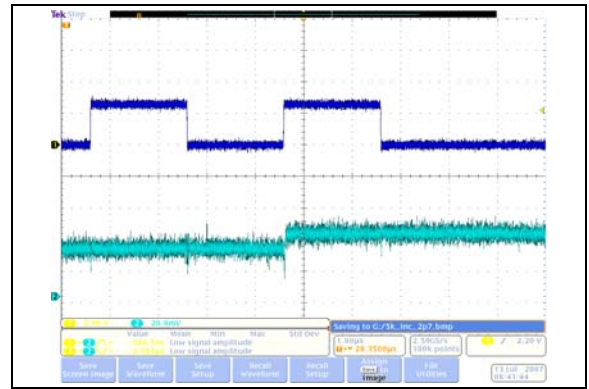


**FIGURE 2-11:** 5 kΩ –  $R_{WB}$  ( $\Omega$ ) vs. Wiper Setting and Ambient Temperature.

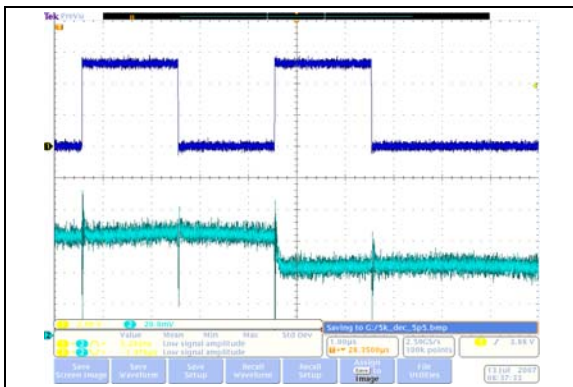
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



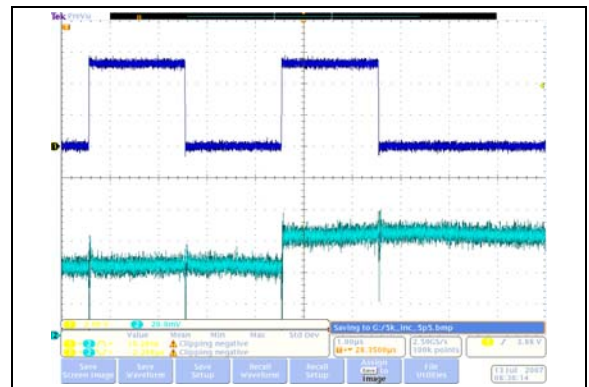
**FIGURE 2-12:** 5 k $\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



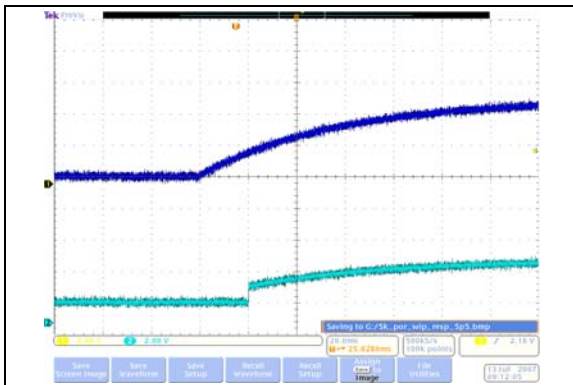
**FIGURE 2-15:** 5 k $\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



**FIGURE 2-13:** 5 k $\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



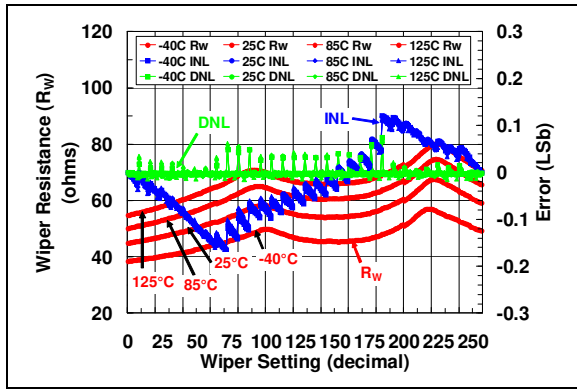
**FIGURE 2-16:** 5 k $\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



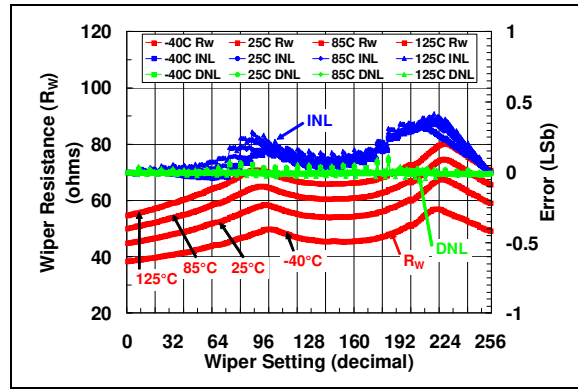
**FIGURE 2-14:** 5 k $\Omega$  – Power-Up Wiper Response Time (20 ms/Div).

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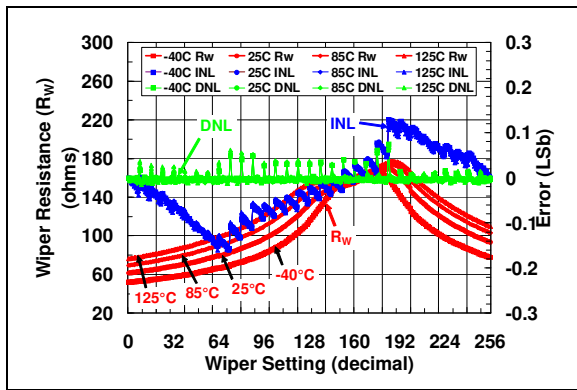
Note: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



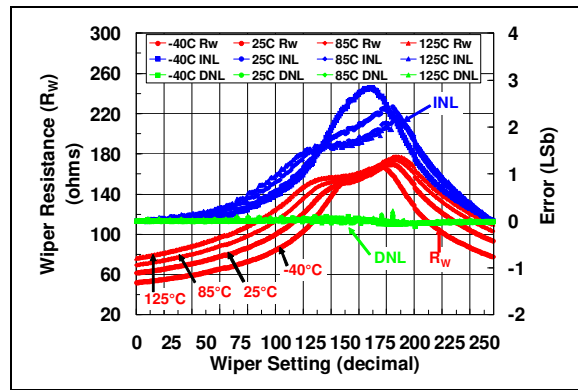
**FIGURE 2-17:** 10 kΩ Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



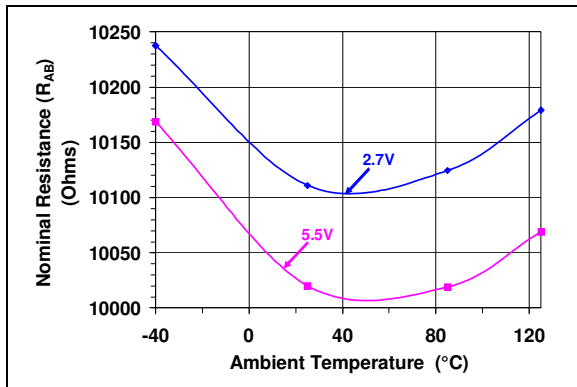
**FIGURE 2-20:** 10 kΩ Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



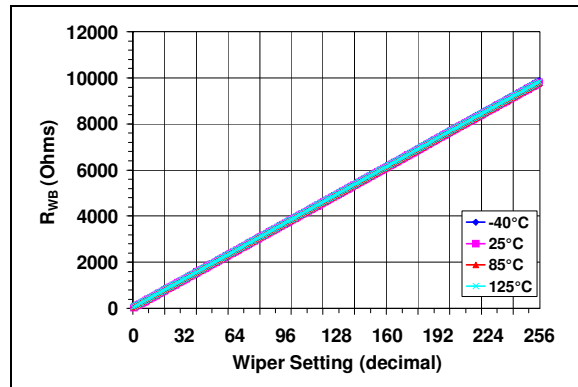
**FIGURE 2-18:** 10 kΩ Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).



**FIGURE 2-21:** 10 kΩ Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).

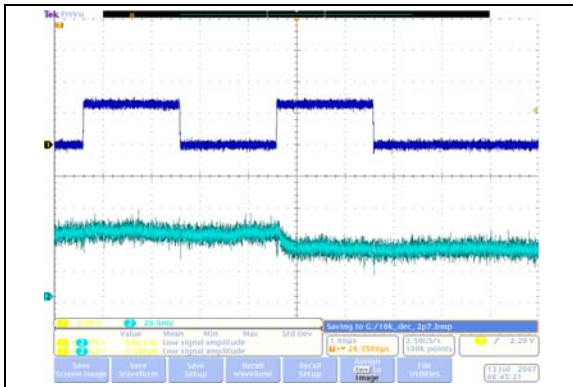


**FIGURE 2-19:** 10 kΩ – Nominal Resistance ( $\Omega$ ) vs. Ambient Temperature and  $V_{DD}$ .

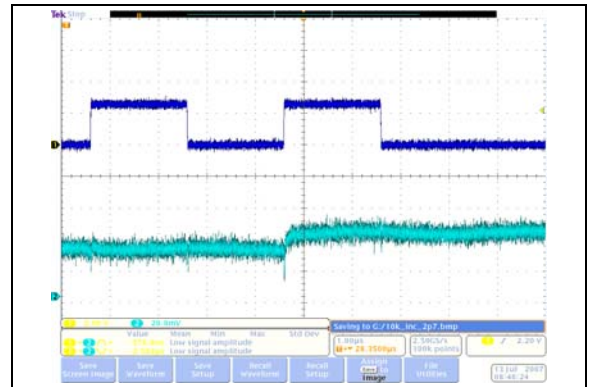


**FIGURE 2-22:** 10 kΩ –  $R_{WB}$  ( $\Omega$ ) vs. Wiper Setting and Ambient Temperature.

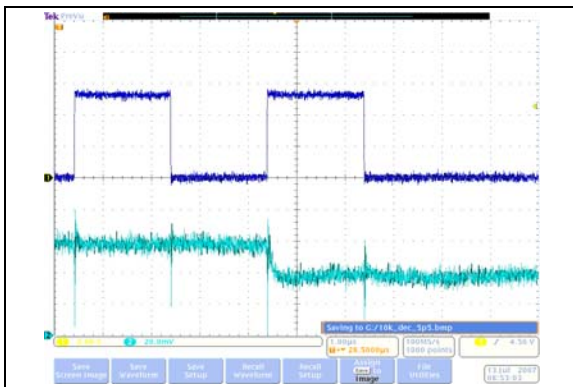
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



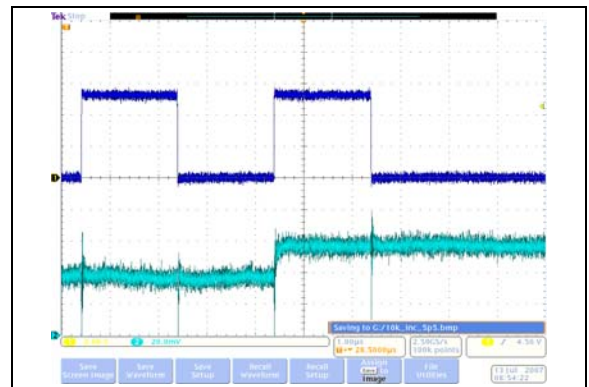
**FIGURE 2-23:** 10 k $\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



**FIGURE 2-25:** 10 k $\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



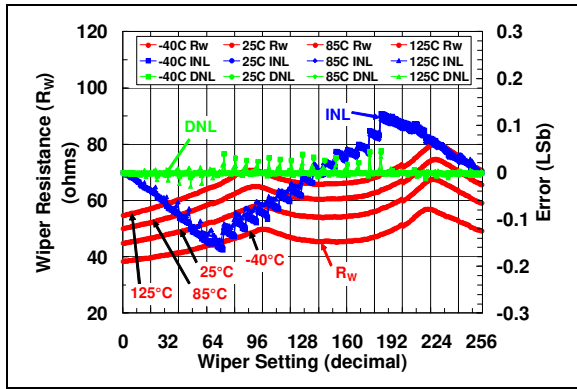
**FIGURE 2-24:** 10 k $\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).



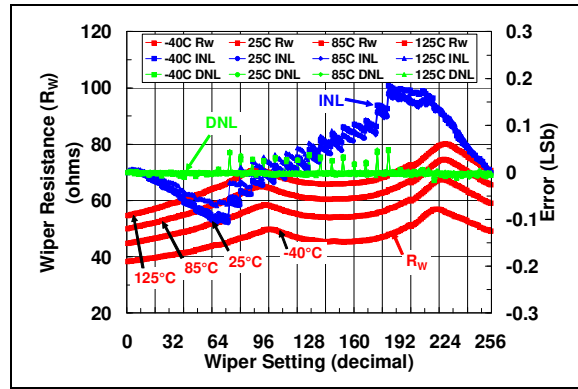
**FIGURE 2-26:** 10 k $\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) (1  $\mu\text{s}/\text{Div}$ ).

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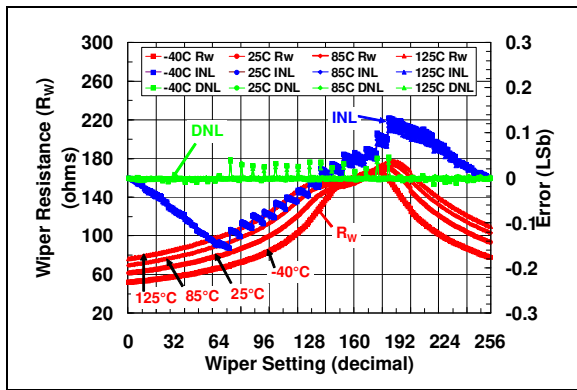
Note: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



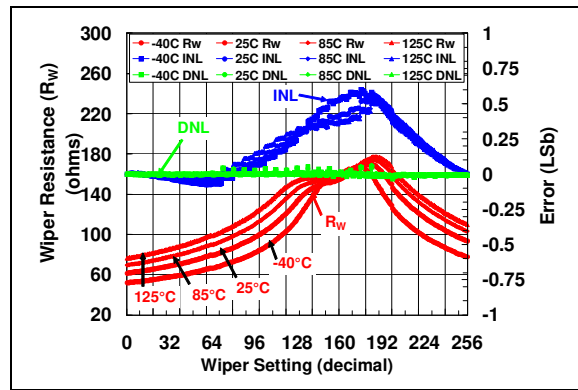
**FIGURE 2-27:** 50 k $\Omega$  Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



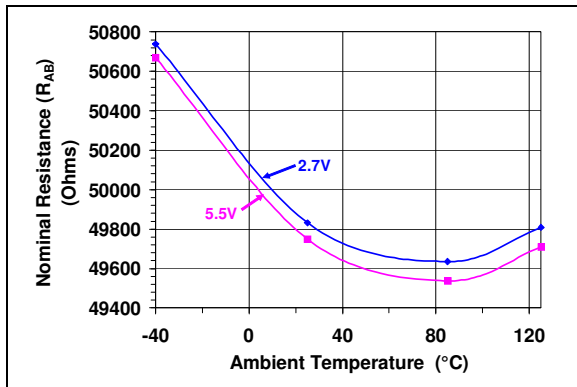
**FIGURE 2-30:** 50 k $\Omega$  Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



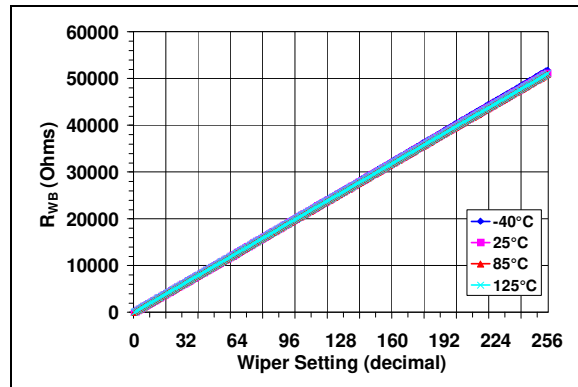
**FIGURE 2-28:** 50 k $\Omega$  Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).



**FIGURE 2-31:** 50 k $\Omega$  Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).

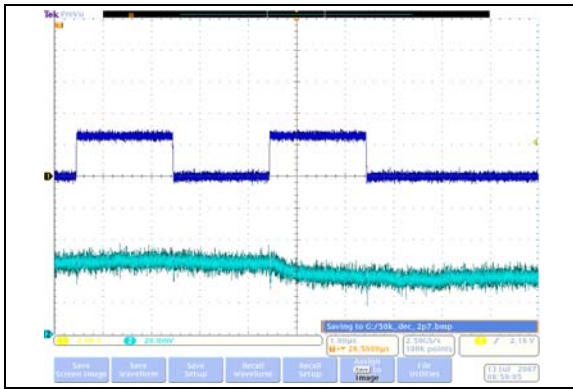


**FIGURE 2-29:** 50 k $\Omega$  – Nominal Resistance ( $\Omega$ ) vs. Ambient Temperature and  $V_{DD}$ .

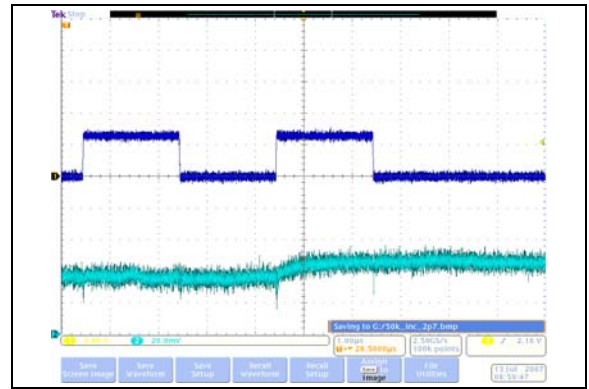


**FIGURE 2-32:** 50 k $\Omega$  –  $R_{WB}$  ( $\Omega$ ) vs. Wiper Setting and Ambient Temperature.

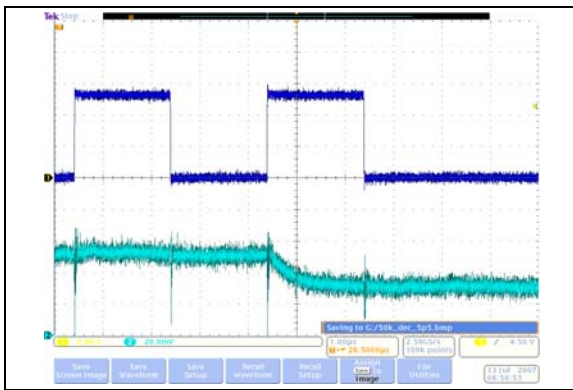
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



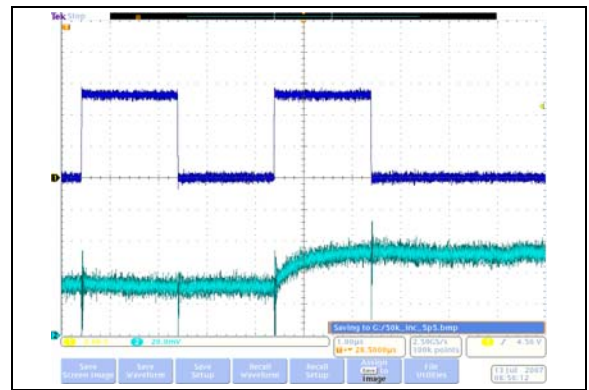
**FIGURE 2-33:**  $50\text{ k}\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) ( $1\ \mu\text{s}/\text{Div}$ ).



**FIGURE 2-35:**  $50\text{ k}\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) ( $1\ \mu\text{s}/\text{Div}$ ).



**FIGURE 2-34:**  $50\text{ k}\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) ( $1\ \mu\text{s}/\text{Div}$ ).

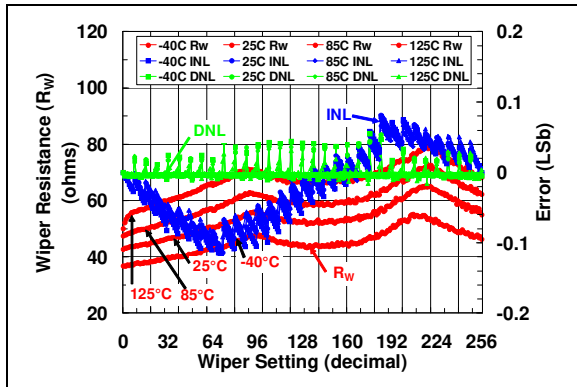


**FIGURE 2-36:**  $50\text{ k}\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) ( $1\ \mu\text{s}/\text{Div}$ ).

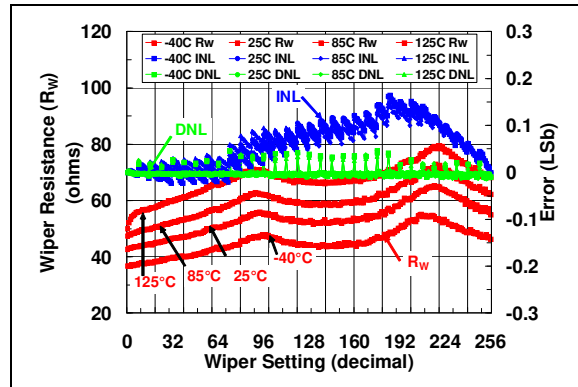


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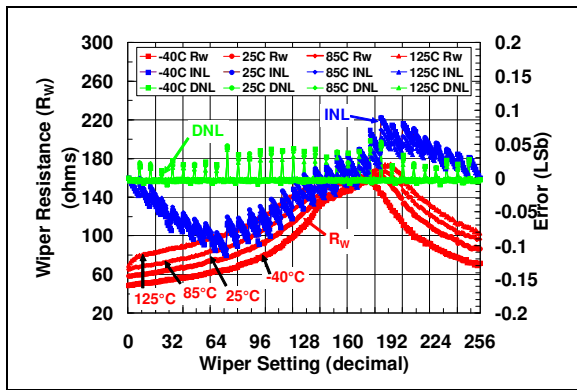
Note: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



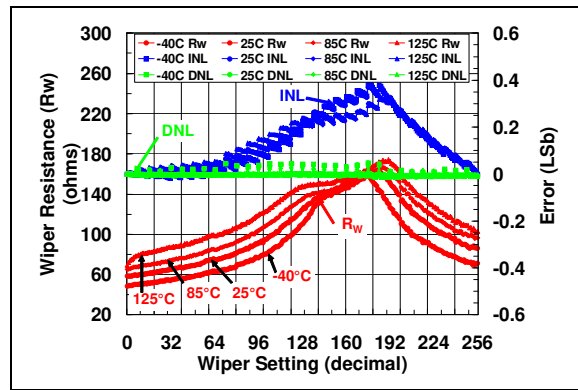
**FIGURE 2-37:** 100 k $\Omega$  Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



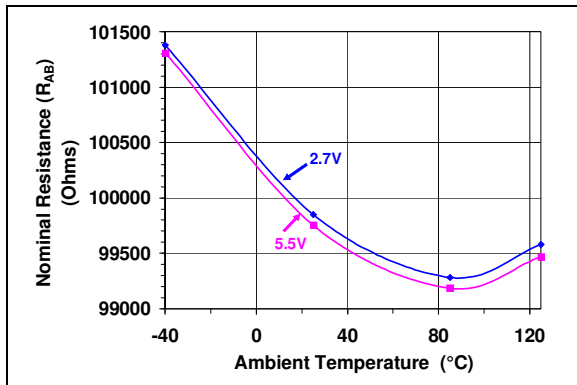
**FIGURE 2-40:** 100 k $\Omega$  Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 5.5\text{V}$ ).



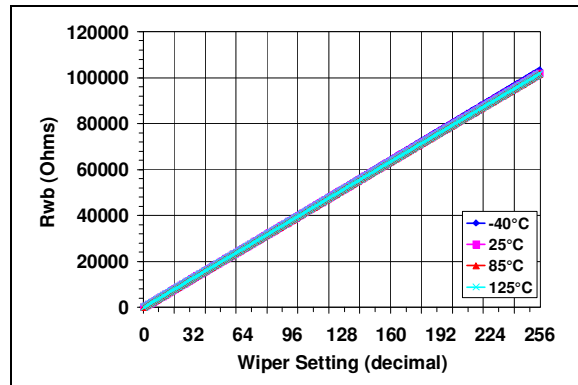
**FIGURE 2-38:** 100 k $\Omega$  Pot Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).



**FIGURE 2-41:** 100 k $\Omega$  Rheo Mode –  $R_W$  ( $\Omega$ ), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ( $V_{DD} = 3.0\text{V}$ ).

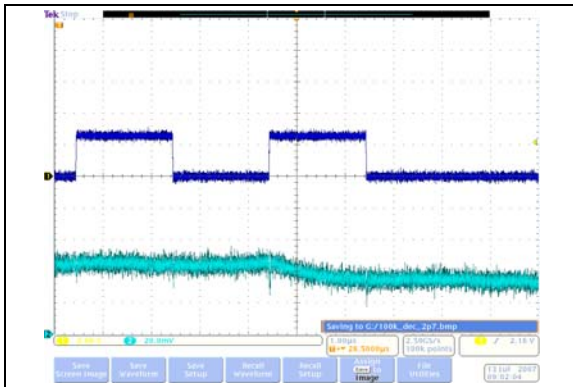


**FIGURE 2-39:** 100 k $\Omega$  – Nominal Resistance ( $\Omega$ ) vs. Ambient Temperature and  $V_{DD}$ .

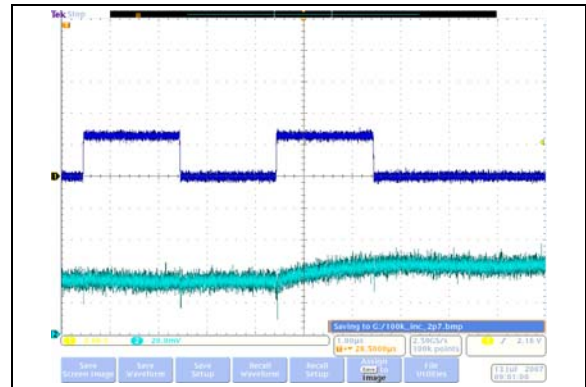


**FIGURE 2-42:** 100 k $\Omega$  –  $R_{WB}$  ( $\Omega$ ) vs. Wiper Setting and Ambient Temperature.

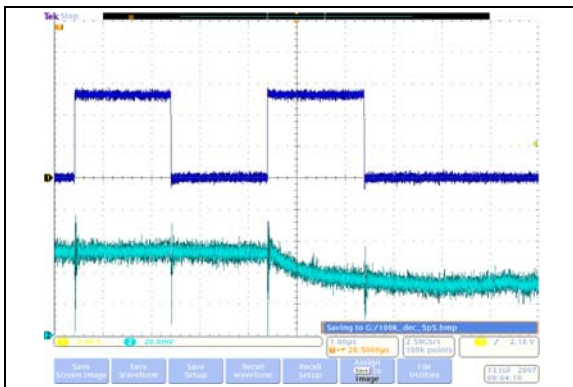
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ .



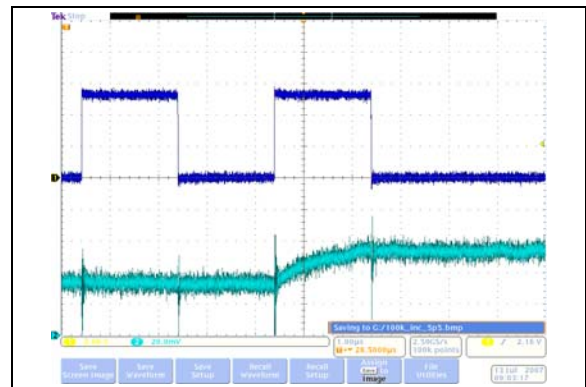
**FIGURE 2-43:** 100 k $\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) ( $1 \mu\text{s}/\text{Div}$ ).



**FIGURE 2-45:** 100 k $\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 2.7\text{V}$ ) ( $1 \mu\text{s}/\text{Div}$ ).



**FIGURE 2-44:** 100 k $\Omega$  – Low-Voltage Decrement Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) ( $1 \mu\text{s}/\text{Div}$ ).



**FIGURE 2-46:** 100 k $\Omega$  – Low-Voltage Increment Wiper Settling Time ( $V_{DD} = 5.5\text{V}$ ) ( $1 \mu\text{s}/\text{Div}$ ).