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MCP443X/5X

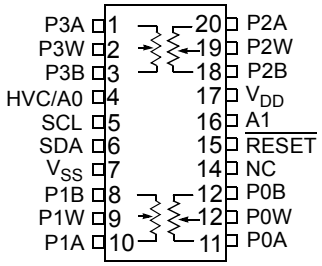
7/8-Bit Volatile Quad Digital POT with I²C Interface

Features

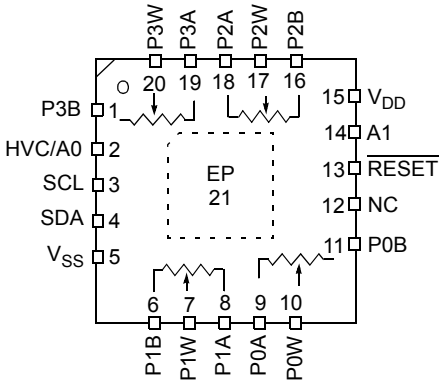
- Quad Resistor Network
- Potentiometer or Rheostat Configuration Options
- Resistor Network Resolution:
  - 7-bit – 128 Resistors (129 Taps)
  - 8-bit – 256 Resistors (257 Taps)
- Four R_{AB} Resistances options:
  - 5 kΩ
  - 10 kΩ
  - 50 kΩ
  - 100 kΩ
- Zero-scale to Full-scale Wiper Operation
- Low Wiper Resistance – 75 Ω typical
- Low Tempco:
  - Absolute (Rheostat) – 50 ppm typical (0°-70°C)
  - Ratiometric (Potentiometer) – 15 ppm typical
- I²C Serial Interface Support:
  - 100 kHz
  - 400 kHz
  - 3.4 MHz
- Serial Protocol Allows High-Speed Read/Write to Wiper
- Resistor Network Terminal Disconnect Feature via Terminal Control (TCON) Register
- Reset Input Pin
- Brown-out Reset Protection – 1.5V typical
- Serial Interface Inactive Current – 2.5 uA typical
- High-Voltage Tolerant Digital Inputs Up to 12.5V
- Supports Split Rail Applications
- Internal Weak Pull-up on All Digital Inputs, except SCL and SDA
- Wide Operating Voltage:
  - 2.7V to 5.5V - Device Characteristics Specified
  - 1.8V to 5.5V - Device Operation
- Wide Bandwidth (-3 dB) Operation – 2 MHz typical for 5.0 kΩ Device
- Extended Temperature Range (-40°C to +125°C)
- Three Package Types:
  - 4x4 QFN-20
  - TSSOP-20
  - TSSOP-14

Package Types (Top View)

MCP44X1 Quad Potentiometers

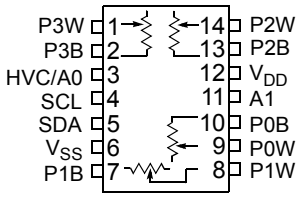


TSSOP



4x4 QFN

MCP44X2 Quad Rheostat



TSSOP

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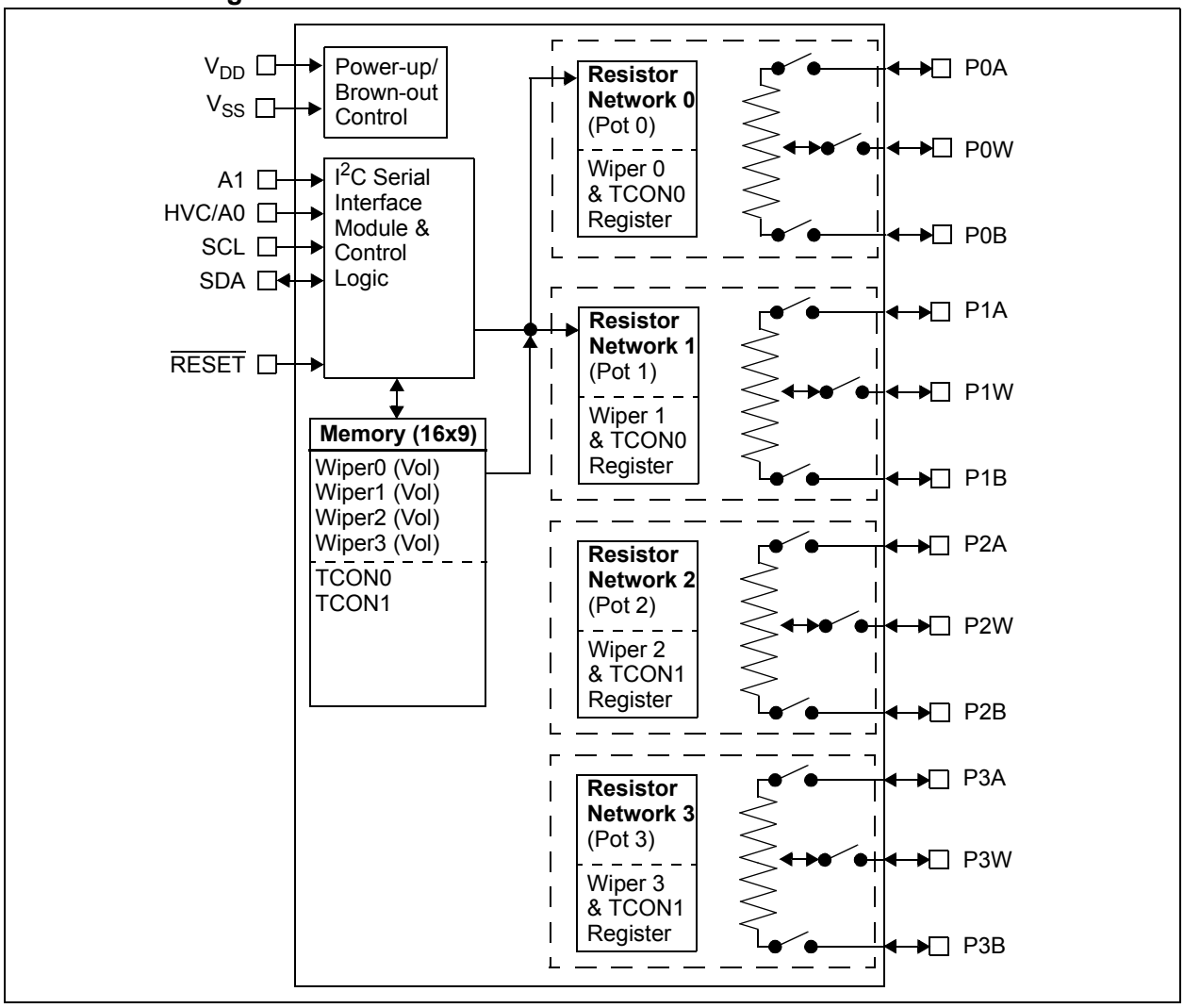
Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control	Memory Type	WiperLock Technology	POR Wiper Setting	Resistance (typical)		# of Taps	V_{DD} Operating Range(2)
							R_{AB} Options (kΩ)	Wiper - R_W (Ω)		
MCP4431	4	Potentiometer (1)	I2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4432	4	Rheostat	I2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4441	4	Potentiometer (1)	I2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4442	4	Rheostat	I2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4451	4	Potentiometer(1)	I2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4452	4	Rheostat	I2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4461	4	Potentiometer(1)	I2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4462	4	Rheostat	I2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

2: Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +7.0V
Voltage on HVC/A0, A1, SCL, SDA, and $\overline{RESET}$, with respect to V_{SS} ..... -0.6V to 12.5V
Voltage on all other pins (PxA, PxW, and PxB), with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK}
(V_I < 0, V_I > V_{DD}, V_I > V_{PP} ON HV pins) ..... ±20 mA
Output clamp current, I_{OK}
(V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any Output pin
..... 25 mA
Maximum output current sourced by any Output pin
..... 25 mA
Maximum current out of V_{SS} pin ..... 100 mA
Maximum current into V_{DD} pin ..... 100 mA
Maximum current into PxA, PxW & PxB pins . ±2.5 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied
..... -40°C to +125°C
Package power dissipation (T_A = +50°C, T_J = +150°C)
TSSOP-14 ..... 1000 mW
TSSOP-20 ..... 1110 mW
QFN-20 (4x4) ..... 2320 mW
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV (HBM),
..... ≥ 300V (MM)
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Supply Voltage	V_{DD}	2.7	—	5.5	V		
		1.8	—	2.7	V	Serial Interface only.	
HVC/A0, SDA, SCL, A1, RESET pin Voltage Range	V_{HV}	V_{SS}	—	12.5V	V	$V_{DD} \geq$ 4.5V	The HVC/A0 pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}). (**Note 6**)
		V_{SS}	—	V_{DD} + 8.0V	V	V_{DD} < 4.5V	
V_{DD} Start Voltage to ensure Wiper Reset	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}	
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 9**)			V/ms		
Delay after device exits the Reset state (V_{DD} > V_{BOR})	T_{BORD}	—	10	20	µs		
Supply Current (**Note 10**)	I_{DD}	—	—	600	µA	Serial Interface Active, HVC/A0 = V_{IH} (or V_{IL}) (**Note 11**) Write all 0's to volatile Wiper 0 V_{DD} = 5.5V, F_{SCL} @ 3.4 MHz	
		—	—	250	µA	Serial Interface Active, HVC/A0 = V_{IH} (or V_{IL}) (**Note 11**) Write all 0's to volatile Wiper 0 V_{DD} = 5.5V, F_{SCL} @ 100 kHz	
		—	2.5	5	µA	Serial Interface Inactive, (Stop condition, SCL = SDA = V_{IH}), Wiper = 0 V_{DD} = 5.5V, HVC/A0 = V_{IH}	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Resistance (± 20%)	R_{AB}	4.0	5	6.0	kΩ	-502 devices (**Note 1**)	
		8.0	10	12.0	kΩ	-103 devices (**Note 1**)	
		40.0	50	60.0	kΩ	-503 devices (**Note 1**)	
		80.0	100	120.0	kΩ	-104 devices (**Note 1**)	
Resolution	N		257		Taps	8-bit	No Missing Codes
			129		Taps	7-bit	No Missing Codes
Step Resistance	R_S	—	R_{AB} / (256)	—	Ω	8-bit	**Note 6**
		—	R_{AB} / (128)	—	Ω	7-bit	**Note 6**
Nominal Resistance Match	(| R_{ABWC} - R_{ABMEAN} |) / R_{ABMEAN}	—	0.2	1.50	%	5 kΩ	**MCP44X1** devices only
		—	0.2	1.25	%	10 kΩ	
		—	0.2	1.0	%	50 kΩ	
		—	0.2	1.0	%	100 kΩ	
	(| R_{BWWC} - R_{BWMEAN} |) / R_{BWMEAN}	—	0.25	1.75	%	5 kΩ	Code = Full Scale
		—	0.25	1.50	%	10 kΩ	
		—	0.25	1.25	%	50 kΩ	
		—	0.25	1.25	%	100 kΩ	
Wiper Resistance (**Note 3**, **Note 4**)	R_W	—	75	160	Ω	V_{DD} = 5.5 V, I_W = 2.0 mA, code = 00h	
		—	75	300	Ω	V_{DD} = 2.7 V, I_W = 2.0 mA, code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (80h or 40h)	
Resistance Tracking	ΔR_{TRACK}	**Section 2.0**			ppm/°C	See **Typical Performance Curves**	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	V_{SS}	—	V_{DD}	V	**Note 5, Note 6**	
Maximum current through A, W or B (**Note 6**)	I_W	—	—	2.5	mA	Terminal A	I_{AW}, W = Full Scale (FS)
		—	—	2.5	mA	Terminal B	I_{BW}, W = Zero Scale (ZS)
		—	—	2.5	mA	Terminal W	I_{AW} (W = FS) or I_{BW} (W = ZS)
Maximum R_{AB} current (I_{AB}) (**Note 6**)	I_{AB}	—	—	1.38	mA	V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 4000Ω	
		—	—	0.688	mA	V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 8000Ω	
		—	—	0.138	mA	V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 40000Ω	
		—	—	0.069	mA	V_B = 0V, V_A = 5.5V, $R_{AB(MIN)}$ = 80000Ω	
Leakage current into A, W or B	I_{WL}	—	100	—	nA	**MCP44X1** PxA = PxW = PxB = V_{SS}	
		—	100	—	nA	**MCP44X2** PxB = PxW = V_{SS}	
		—	100	—	nA	Terminals Disconnected (R0A = R0W = R0B = 0; R1A = R1W = R1B = 0; R2A = R2W = R2B = 0; R3A = R3W = R3B = 0)	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Full Scale Error (**MCP44X1** only) (8-bit code = 100h, 7-bit code = 80h)	V_{WFSE}	-6.0	-0.1	—	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-4.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-3.5	-0.1	—	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-2.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.8	-0.1	—	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Zero Scale Error (**MCP44X1** only) (8-bit code = 00h, 7-bit code = 00h)	V_{WZSE}	—	+0.1	+6.0	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.5	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+2.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.8	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Potentiometer Integral Non-linearity	INL	-1	±0.5	+1	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP44X1** devices only **(Note 2)**	
		-0.5	±0.25	+0.5	LSb	7-bit		
Potentiometer Differential Non-linearity	DNL	-0.5	±0.25	+0.5	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP44X1** devices only **(Note 2)**	
		-0.25	±0.125	+0.25	LSb	7-bit		
Bandwidth -3 dB (See Figure 2-90, load = 30 pF)	BW	—	2	—	MHz	5 kΩ	8-bit	Code = 80h
		—	2	—	MHz		7-bit	Code = 40h
		—	1	—	MHz	10 kΩ	8-bit	Code = 80h
		—	1	—	MHz		7-bit	Code = 40h
		—	200	—	kHz	50 kΩ	8-bit	Code = 80h
		—	200	—	kHz		7-bit	Code = 40h
		—	100	—	kHz	100 kΩ	8-bit	Code = 80h
		—	100	—	kHz		7-bit	Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Integral Non-linearity **MCP44X1** (**Note 4**, **Note 8**) **MCP44X2** devices only (**Note 4**)	R-INL	-1.5	±0.5	+1.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-8.25	+4.5	+8.25	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 900 µA
		-6.0	+4.5	+6.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-1.5	±0.5	+1.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-5.5	+2.5	+5.5	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 450 µA
		-4.0	+2.5	+4.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-1.5	±0.5	+1.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-2.0	+1	+2.0	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 90 µA
		-1.5	+1	+1.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-1.0	±0.5	+1.0	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-1.5	+0.25	+1.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA
		-0.8	±0.5	+0.8	LSb		7-bit	5.5V, I_W = 45 µA
		-1.125	+0.25	+1.125	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Differential Non-linearity **MCP44X1** (**Note 4**, **Note 8**) **MCP44X2** devices only (**Note 4**)	R-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-1.0	+0.5	+1.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 900 µA
		-0.75	+0.5	+0.75	LSb			3.0V, I_W = 480 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 190 µA
		-0.5	±0.25	+0.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-1.0	+0.25	+1.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 450 µA
		-0.75	+0.5	+0.75	LSb			3.0V, I_W = 240 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 150 µA
		-0.5	±0.25	+0.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-0.5	±0.25	+0.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 90 µA
		-0.375	±0.25	+0.375	LSb			3.0V, I_W = 48 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 30 µA
		-0.5	±0.25	+0.5	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-0.5	±0.25	+0.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 45 µA
		-0.375	±0.25	+0.375	LSb			3.0V, I_W = 24 µA (**Note 7**)
		Section 2.0						1.8V, I_W = 15 µA

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Digital Inputs/Outputs (HVC/A0, A1, SDA, SCL, $\overline{RESET}$)							
Schmitt Trigger High Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	All Inputs except SDA and SCL	2.7V ≤ V_{DD} ≤ 5.5V (Allows 2.7V Digital V_{DD} with 5V Analog V_{DD})
		0.5 V_{DD}	—	—	V		1.8V ≤ V_{DD} ≤ 2.7V
		0.7 V_{DD}	—	V_{MAX}	V	SDA and SCL	100 kHz
		0.7 V_{DD}	—	V_{MAX}	V		400 kHz
		0.7 V_{DD}	—	V_{MAX}	V		1.7 MHz
		0.7 V_{DD}	—	V_{MAX}	V		3.4 Mhz
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	0.2V_{DD}	V	All inputs except SDA and SCL	
		-0.5	—	0.3V_{DD}	V	SDA and SCL	100 kHz
		-0.5	—	0.3V_{DD}	V		400 kHz
		-0.5	—	0.3V_{DD}	V		1.7 MHz
		-0.5	—	0.3V_{DD}	V		3.4 Mhz
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1V_{DD}	—	V	All inputs except SDA and SCL	
		N.A.	—	—	V	SDA and SCL	100 kHz, V_{DD} < 2.0V
		N.A.	—	—	V		100 kHz, V_{DD} ≥ 2.0V
		0.1 V_{DD}	—	—	V		400 kHz, V_{DD} < 2.0V
		0.05 V_{DD}	—	—	V		400 kHz, V_{DD} ≥ 2.0V
		0.1 V_{DD}	—	—	V		1.7 MHz
		0.1 V_{DD}	—	—	V		3.4 Mhz
High Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	12.5 **(Note 6)**	V	Threshold for WiperLock Technology	
High Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V **(Note 6)**	V		
High Voltage Limit	V_{MAX}	—	—	12.5 **(Note 6)**	V	Pin can tolerate V_{MAX} or less.	
Output Low Voltage (SDA)	V_{OL}	V_{SS}	—	0.2V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA,	
		V_{SS}	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Weak Pull-up Current	I_{PU}	—	—	1.75	mA	Internal V_{DD} pull-up, V_{IHH} pull-down, V_{DD} = 5.5V, V_{HVC} = 12.5V	
		—	170	—	µA	HVC pin, V_{DD} = 5.5V, V_{HVC} = 3V	
HVC Pull-up / Pull-down Resistance	R_{HVC}	—	16	—	kΩ	V_{DD} = 5.5V, V_{HVC} = 3V	
$\overline{\text{RESET}}$ Pull-up Resistance	R_{RESET}	—	16	—	kΩ	V_{DD} = 5.5V, $V_{\overline{\text{RESET}}}$ = 0V	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} (all pins) and V_{IN} = V_{SS} (all pins except $\overline{\text{RESET}}$)	
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 20 MHz	
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, Code = Full Scale	
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, Code = Full Scale	
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, Code = Full Scale	
RAM (Wiper, TCON) Value							
Value Range	N	0h	—	1FFh	hex	8-bit device	
		0h	—	1FFh	hex	7-bit device	
TCON POR/BOR Setting		1FF			hex	All Terminals connected	
Power Requirements							
Power Supply Sensitivity (**MCP44X1**)	PSS	—	0.0015	0.0035	%/%	8-bit	V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 80h
		—	0.0015	0.0035	%/%	7-bit	V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP44X1** only.

4: **MCP44X2** only, includes V_{WZSE} and V_{WFSE}.

5: Polarity of resistor terminals A, W and B, with respect to each other, is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

8: The **MCP44X1** is externally connected to match the configurations of the **MCP44X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network.

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification.

1.1 I²C Mode Timing Waveforms and Requirements

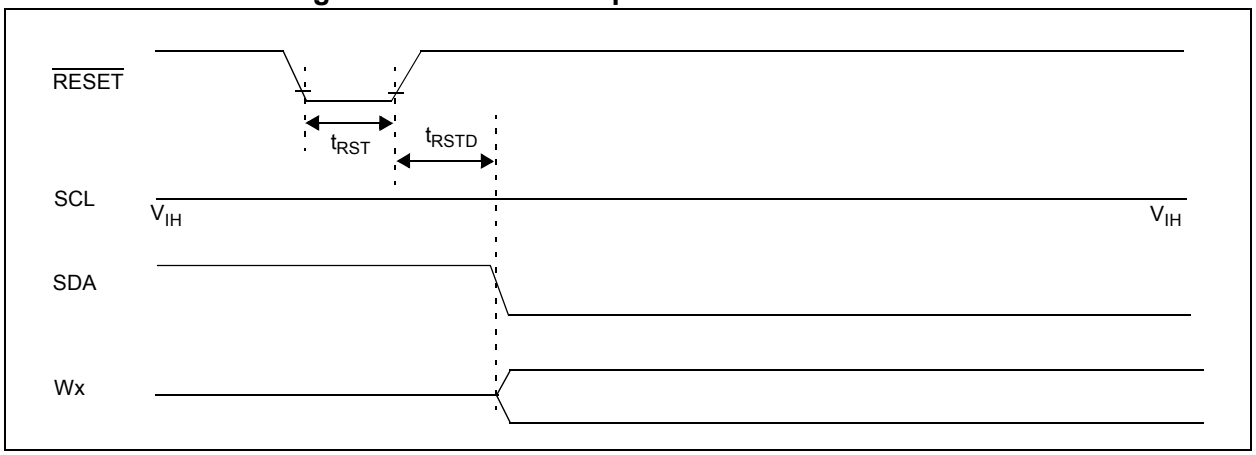

FIGURE 1-1: *RESET Waveforms.*

TABLE 1-1: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
$\overline{\text{RESET}}$ pulse width	t_{RST}	50	—	—	ns	
$\overline{\text{RESET}}$ rising edge normal mode (Wiper driving and I²C interface operational)	t_{RSTD}	—	—	20	ns	

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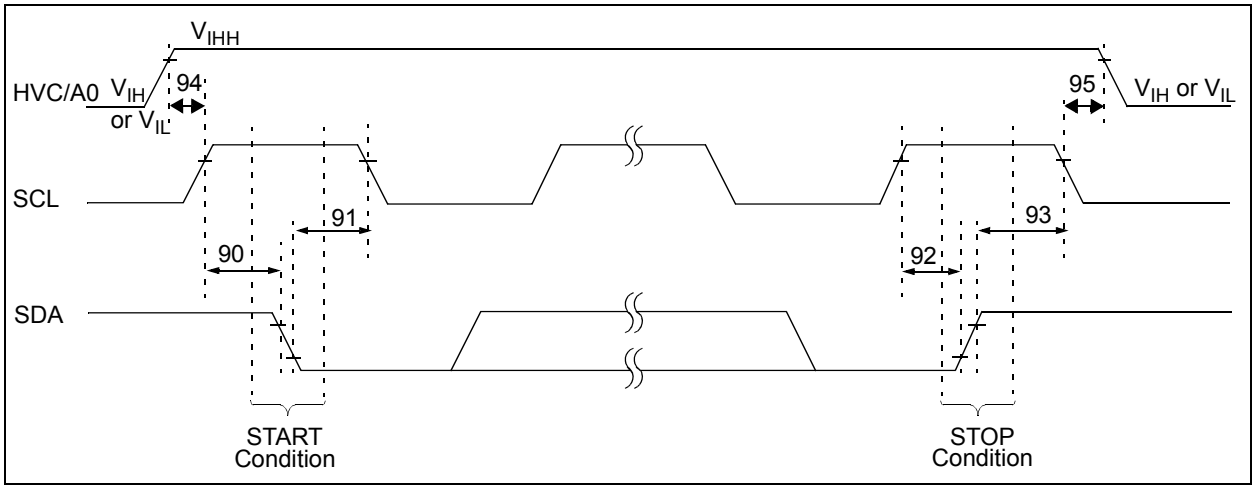

FIGURE 1-2: *I^2C Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-2: I^2C BUS START/STOP BITS REQUIREMENTS

I^2C AC Characteristics				**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage VDD range is described in **AC/DC characteristics**			
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	Cb	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	TSU:STO	STOP condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
94	T_{HVCSU}	HVC to SCL Setup time		25	—	uS	High Voltage Commands
95	T_{HVCHD}	SCL to HVC Hold time		25	—	uS	High Voltage Commands

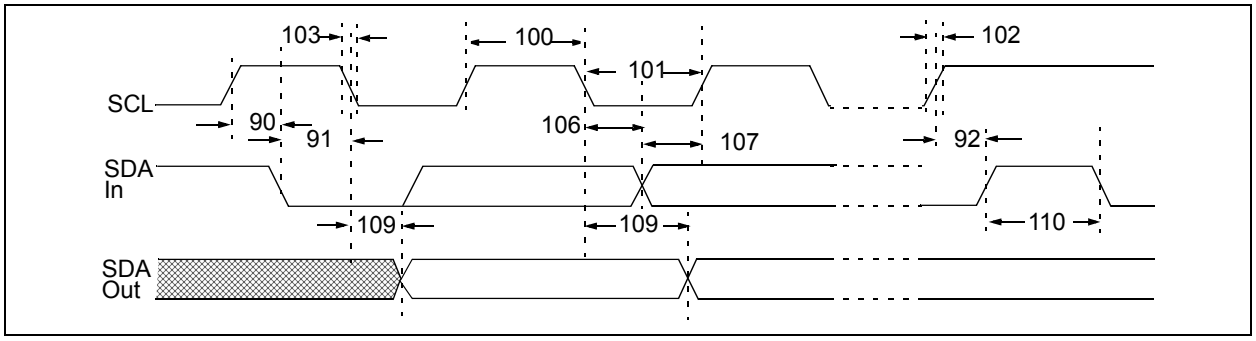

FIGURE 1-3: *I^2C Bus Data Timing.*

TABLE 1-3: I^2C BUS DATA REQUIREMENTS (SLAVE MODE)

I^2C AC Characteristics				**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **AC/DC characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	THIGH	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120		ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	TLOW	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320		ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

3: The MCP44X1/MCP44X2 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use Cb in pF for the calculations.

5: Not Tested.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

7: Ensured by the T_{AA} 3.4 MHz specification test.

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TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **AC/DC characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
102A (5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B (5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
103A (5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B (5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb (4)	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V, **Note 6**
			400 kHz mode	0	—	ns	2.7V-5.5V, **Note 6**
			1.7 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**
			3.4 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP44X1/MCP44X2 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use Cb in pF for the calculations.

5: Not Tested.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

7: Ensured by the T_{AA} 3.4 MHz specification test.

TABLE 1-3: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **AC/DC characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**Note 2**
			400 kHz mode	100	—	ns	
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	**Note 1**
			400 kHz mode	—	900	ns	
			1.7 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**, **Note 7**
				—	310	ns	Cb = 400 pF, **Note 1**, **Note 5**
			3.4 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP specification states N.A.
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line T_R max.+$t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP44X1/MCP44X2 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use Cb in pF for the calculations.

5: Not Tested.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

7: Ensured by the T_{AA} 3.4 MHz specification test.

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 20L-QFN	θ_{JA}	—	43	—	°C/W	
Thermal Resistance, 20L-TSSOP	θ_{JA}	—	90	—	°C/W	

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

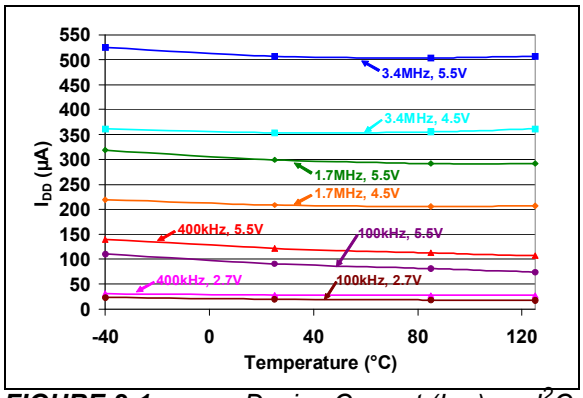


FIGURE 2-1: *Device Current (I_{DD}) vs. I^2C Frequency (f_{SCL}) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

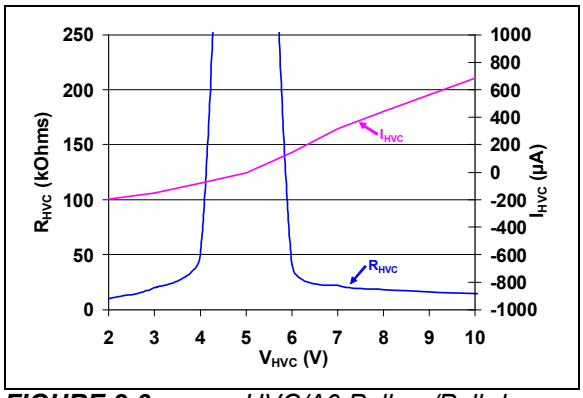


FIGURE 2-3: *HVC/A0 Pull-up/Pull-down Resistance (R_{HVC}) and Current (I_{HVC}) vs. HVC/A0 Input Voltage (V_{HVC}) (V_{DD} = 5.5V).*

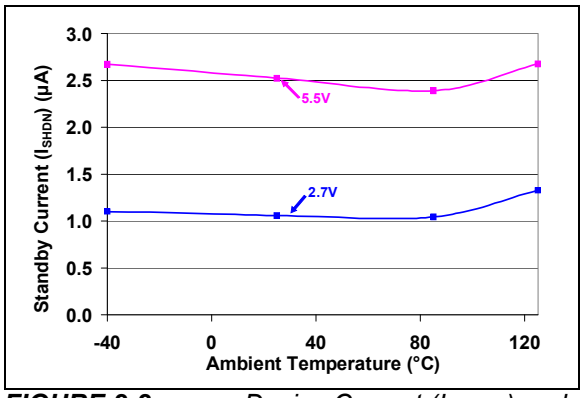


FIGURE 2-2: *Device Current (I_{SHDN}) and V_{DD}. (HVC/A0 = V_{DD}) vs. Ambient Temperature.*

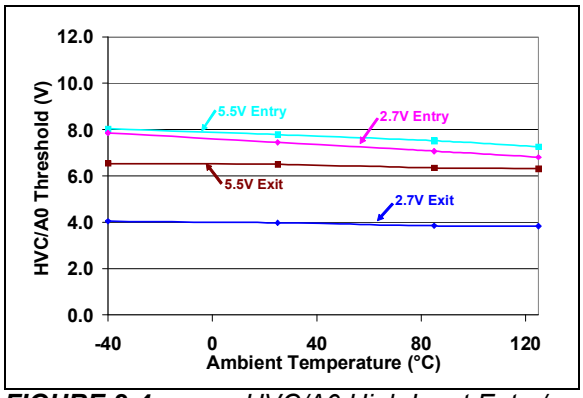


FIGURE 2-4: *HVC/A0 High Input Entry/Exit Threshold vs. Ambient Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

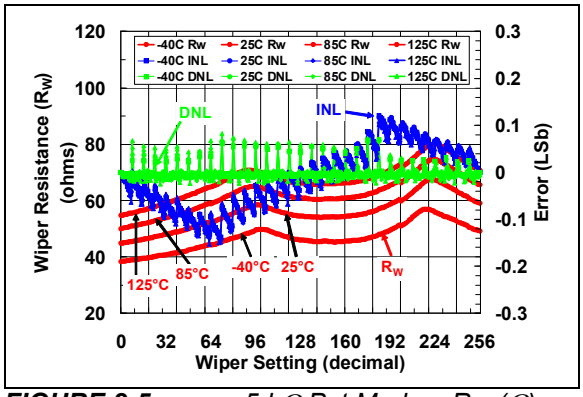


FIGURE 2-5: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

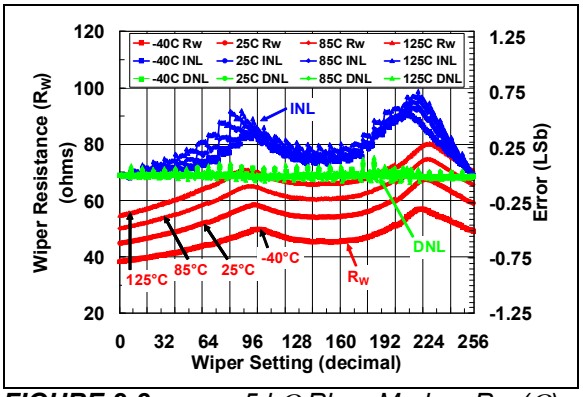


FIGURE 2-8: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

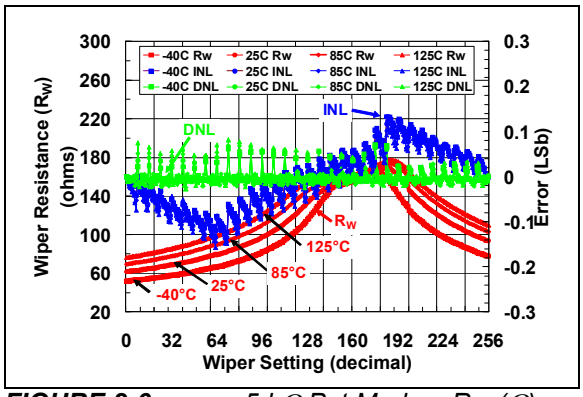


FIGURE 2-6: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*

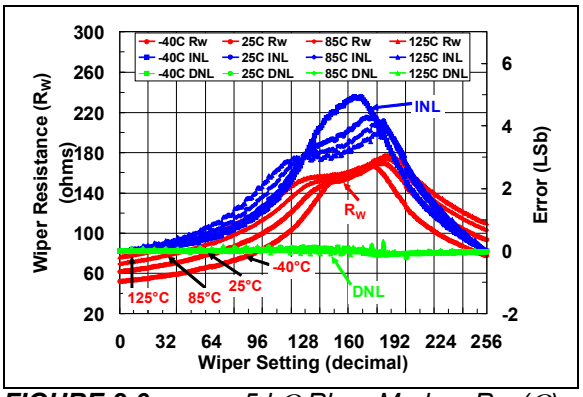
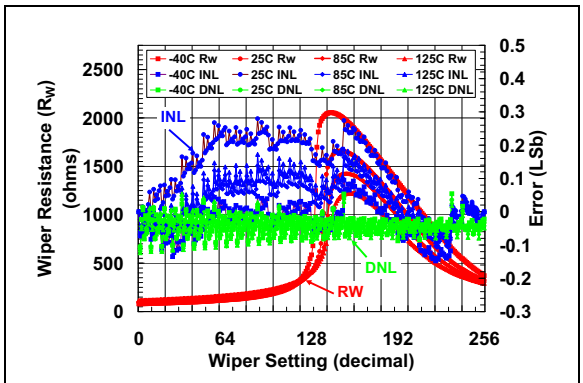
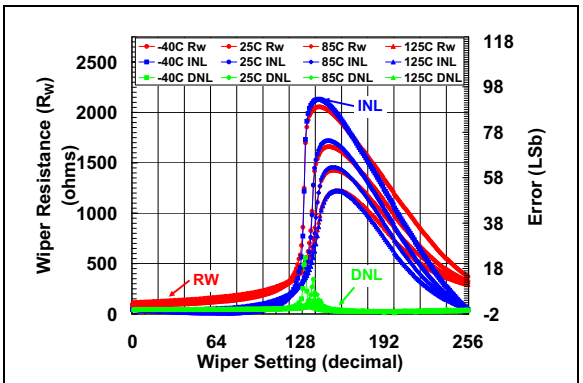


FIGURE 2-9: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-7: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-10: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 260 µA).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

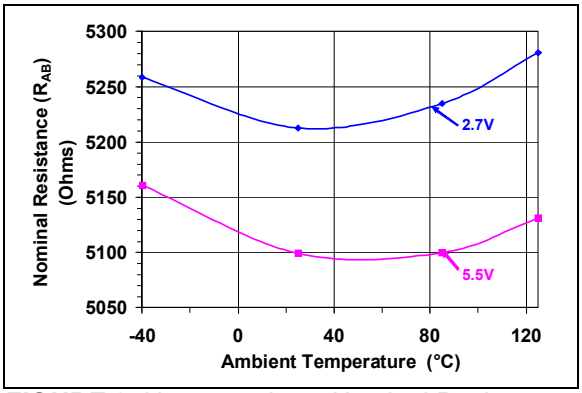


FIGURE 2-11: *5 kΩ – Nominal Resistance (R_{AB}) (Ω) vs. Ambient Temperature and V_{DD}.*

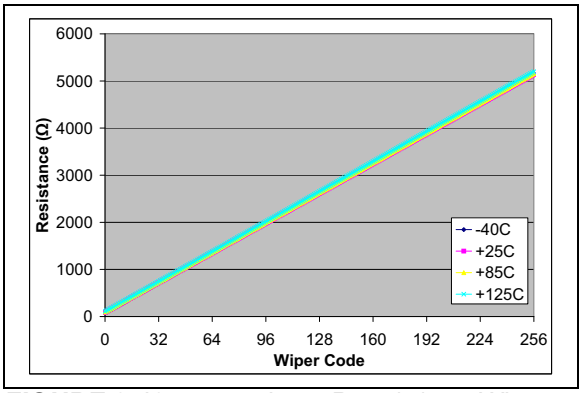


FIGURE 2-12: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 190 µA).*

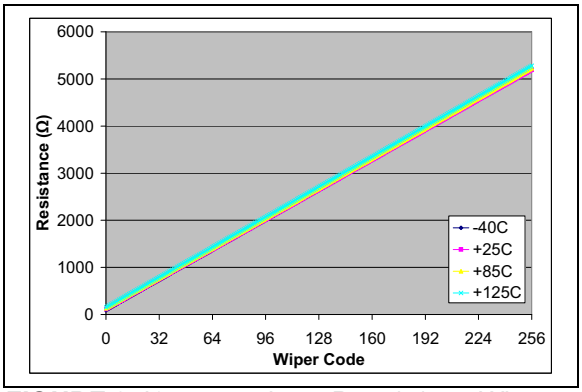
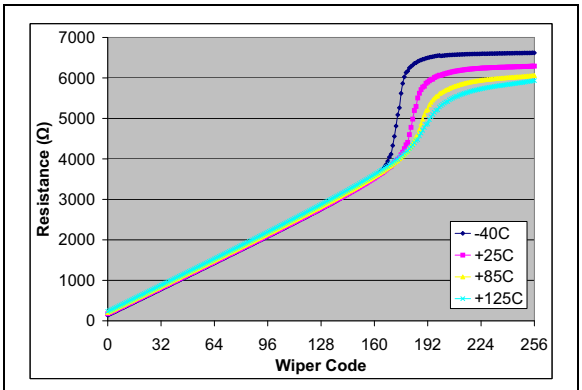


FIGURE 2-13: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 190 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-14: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 190 µA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

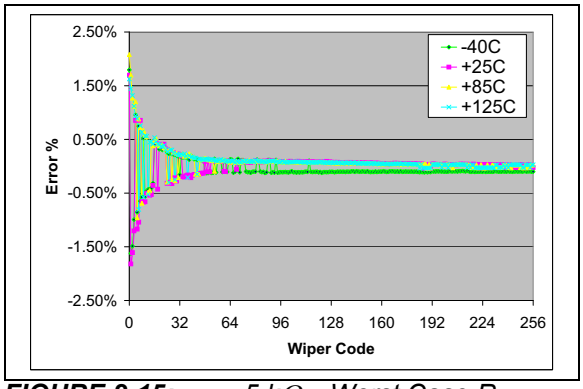


FIGURE 2-15: *5 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 5.5V, I_W = 190 µA).*

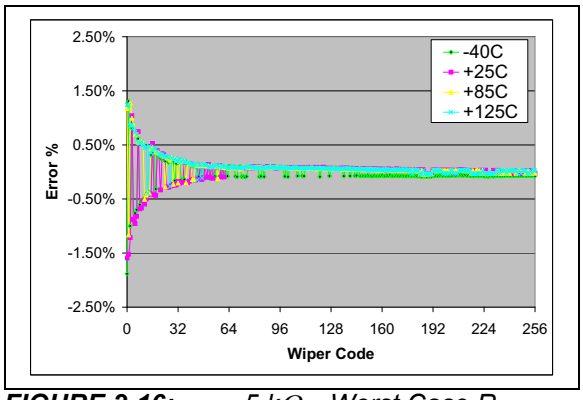
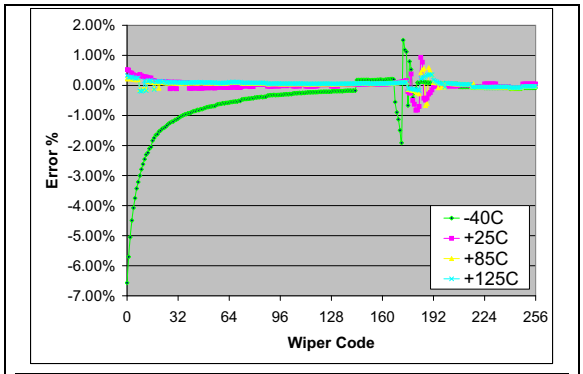


FIGURE 2-16: *5 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 3.0V, I_W = 190 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-17: *5 kΩ – Worst Case R_{BW} from Average R_{BW} (R_{BW0}-R_{BW3}) Error (%) vs. Wiper Setting and Temperature (V_{DD} = 1.8V, I_W = 190 µA).*

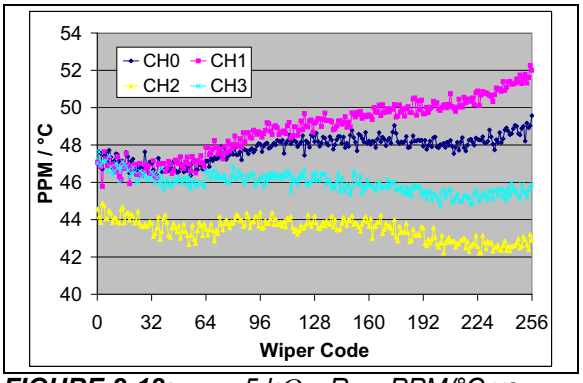


FIGURE 2-18: *5 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 5.5V, I_W = 190 µA).*

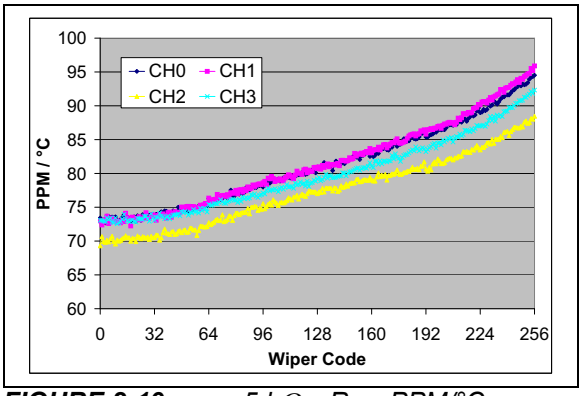
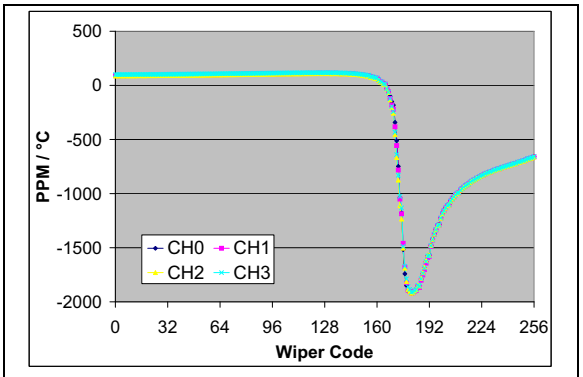


FIGURE 2-19: *5 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 3.0V, I_W = 190 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-20: *5 kΩ – R_{WB} PPM/°C vs. Wiper Setting. ($R_{BW(code=n,\ 125°C)}$-$R_{BW(code=n,\ -40°C)}$)/$R_{BW(code\ =\ 256,\ 25°C)}$/165°C * 1,000,000) ($V_{DD}$ = 1.8V, I_W = 190 µA).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

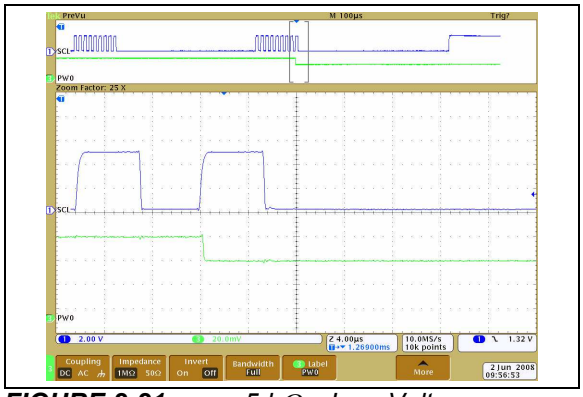


FIGURE 2-21: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

FIGURE 2-24: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

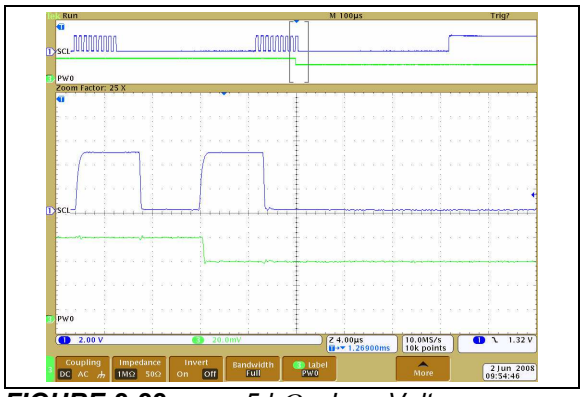


FIGURE 2-22: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

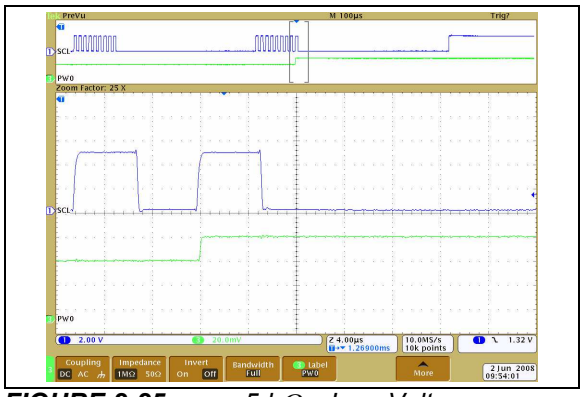


FIGURE 2-25: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

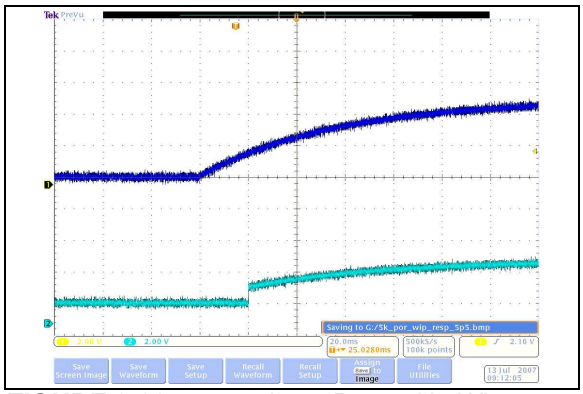


FIGURE 2-23: *5 kΩ – Power-Up Wiper Response Time (20 ms/Div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

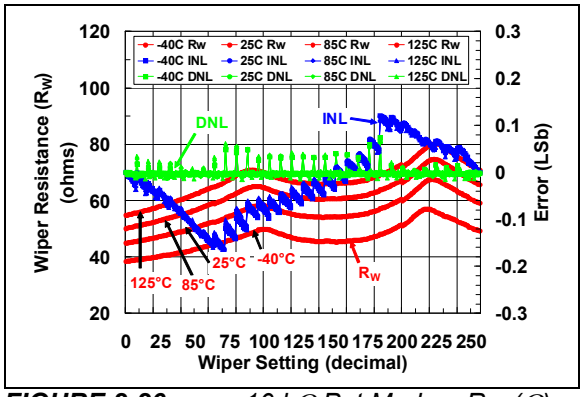


FIGURE 2-26: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

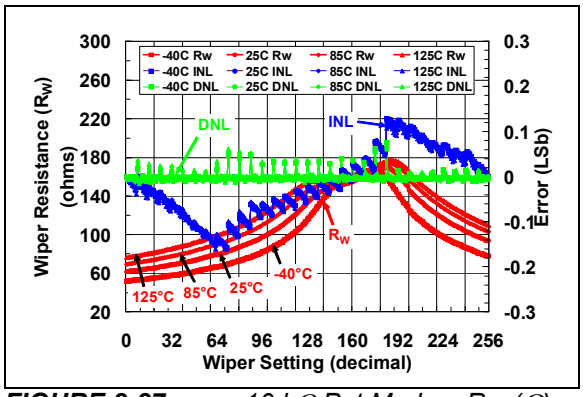
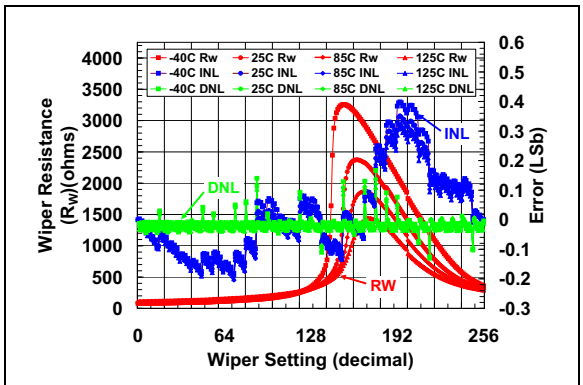


FIGURE 2-27: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-28: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

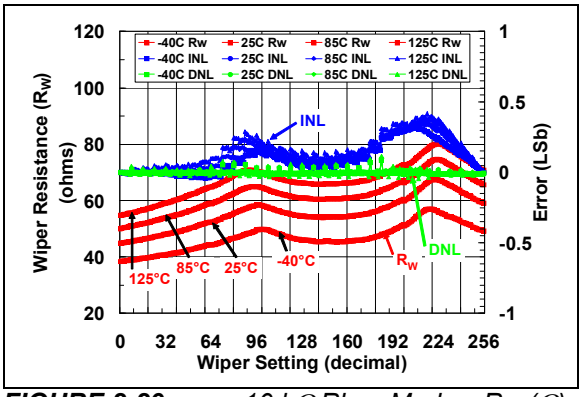


FIGURE 2-29: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

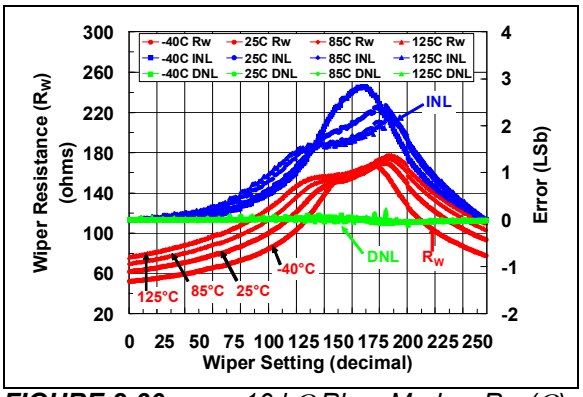
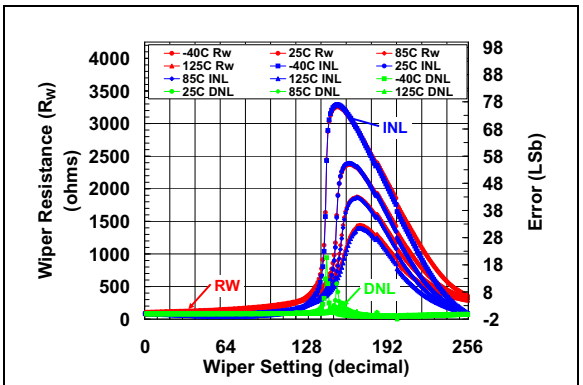


FIGURE 2-30: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*



Note:	See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-31: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 125 µA).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

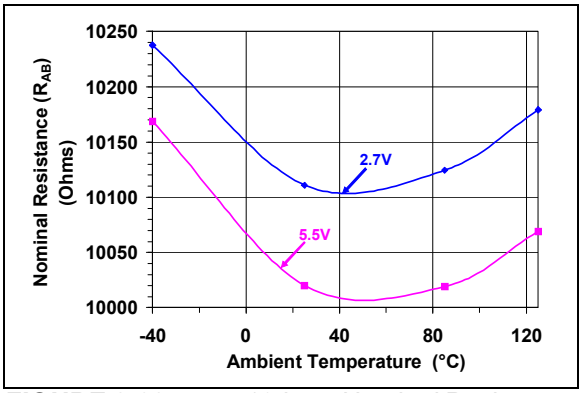


FIGURE 2-32: *10 kΩ – Nominal Resistance (R_{AB}) (Ω) vs. Ambient Temperature and V_{DD}.*

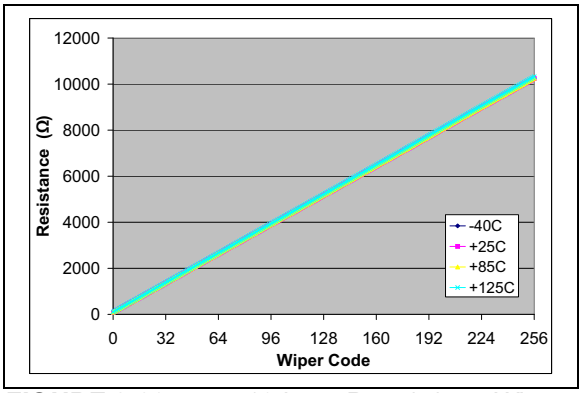


FIGURE 2-33: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V, I_W = 150 µA).*

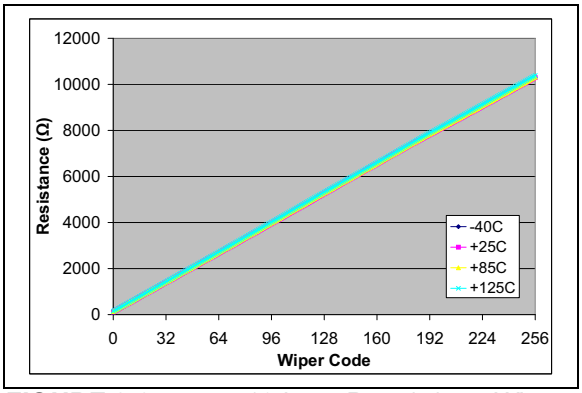
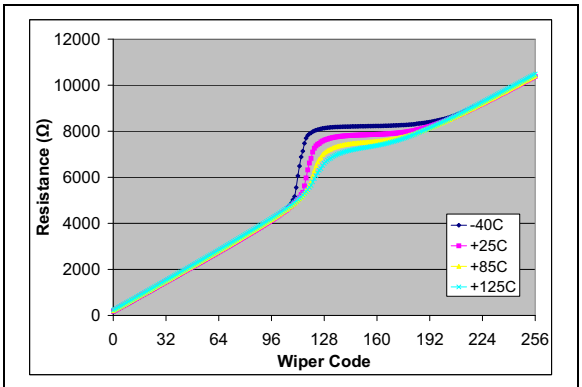


FIGURE 2-34: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V, I_W = 150 µA).*



Note: See **Appendix B:** for additional information of R_W resistance variation characteristics for V_{DD} > 2.7V.

FIGURE 2-35: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V, I_W = 150 µA).*