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MCP45HVX1

7/8-Bit Single, +36V (±18V) Digital POT with I²C™ Serial Interface and Volatile Memory

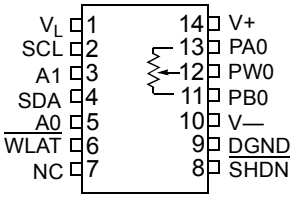
Features:

- High-Voltage Analog Support:
  - +36V Terminal Voltage Range (DGND = V-)
  - ±18V Terminal Voltage Range (DGND = V- + 18V)
- Wide Operating Voltage:
  - Analog: 10V to 36V (specified performance)
  - Digital: 2.7V to 5.5V
    1.8V to 5.5V ($V_L \geq$ V- + 2.7V)
- Single-Resistor Network
- Resistor Network Resolution
  - 7-bit: 127 Resistors (128 Taps)
  - 8-bit: 255 Resistors (256 Taps)
- R_{AB} Resistance Options:
  - 5 kΩ – 10 kΩ
  - 50 kΩ – 100 kΩ
- High Terminal/Wiper Current (I_W) Support:
  - 25 mA (for 5 kΩ)
  - 12.5 mA (for 10 kΩ)
  - 6.5 mA (for 50 kΩ and 100 kΩ)
- Zero-Scale to Full-Scale Wiper Operation
- Low Wiper Resistance: 75 Ω (typical)
- Low Tempco:
  - Absolute (Rheostat): 50 ppm typical (0°C to +70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- I²C Serial Interface:
  - 100 kHz, 400 kHz, 1.7 MHz, and 3.4 MHz support
- Resistor Network Terminal Disconnect Via:
  - Shutdown Pin ($\overline{SHDN}$)
  - Terminal Control (TCON) Register
- Write Latch ($\overline{WLAT}$) Pin to Control Update of Volatile Wiper Register (such as Zero Crossing)
- Power-On Reset/Brown-Out Reset for Both:
  - Digital supply (V_L/DGND); 1.5V typical
  - Analog supply (V+/V-); 3.5V typical
- Serial Interface Inactive Current (3 µA typical)
- 500 kHz Typical Bandwidth (-4 dB) Operation (5.0 kΩ Device)
- Extended Temperature Range (-40°C to +125°C)
- Package Types: TSSOP-14 and QFN-20 (5x5)

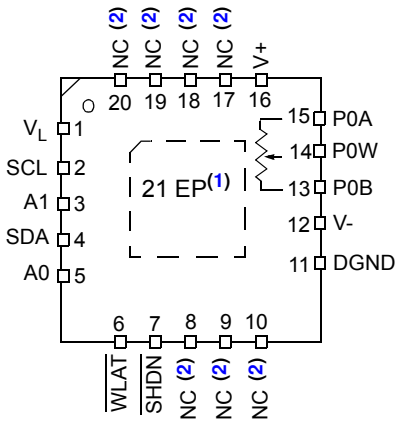
Package Types (Top View)

MCP45HVX1 Single Potentiometer

TSSOP (ST)



QFN 5x5 (MQ)



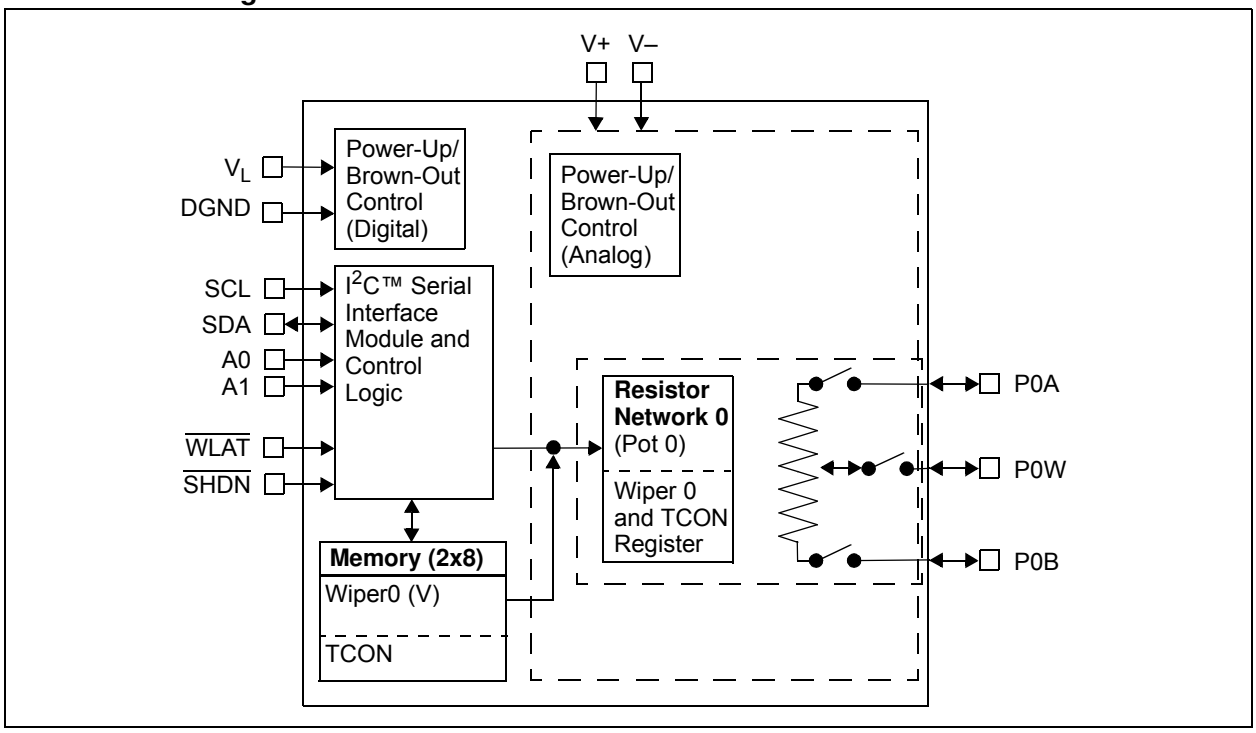
Note 1: Exposed Pad (EP)
2: NC = Not Internally Connected

Description:

The MCP45HVX1 family of devices have dual power rails (analog and digital). The analog power rail allows high voltage on the resistor network terminal pins. The analog voltage range is determined by the V+ and V– voltages. The maximum analog voltage is +36V, while the operating analog output minimum specifications are specified from either 10V or 20V. As the analog supply voltage becomes smaller, the analog switch resistances increase, which affect certain performance specifications. The system can be implemented as dual rail (±18V) relative to the digital logic ground (DGND).

The device also has a Write Latch ($\overline{WLAT}$) function, which will inhibit the volatile Wiper register from being updated (latched) with the received data, until the $\overline{WLAT}$ pin is Low. This allows the application to specify a condition where the volatile Wiper register is updated (such as zero crossing).

Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control Interface	POR Wiper Setting	Resistance (Typical)		Number of:		Specified Operating Range	
					R_{AB} Options (kΩ)	Wiper - R_W (Ω)	R_S	Taps	V_L (2)	V+ (3)
MCP45HV31	1	Potentiometer (1)	I²C™	3Fh	5.0, 10.0, 50.0, 100.0	75	127	128	1.8V to 5.5V	10V (4) to 36V
MCP45HV51	1	Potentiometer (1)	I²C	7Fh	5.0, 10.0, 50.0, 100.0	75	255	256	1.8V to 5.5V	10V (4) to 36V
MCP41HV31 (5)	1	Potentiometer	SPI	3Fh	5.0, 10.0, 50.0, 100.0	75	127	128	1.8V to 5.5V	10V (4) to 36V
MCP41HV51 (5)	1	Potentiometer (5)	SPI	7Fh	5.0, 10.0, 50.0, 100.0	75	255	256	1.8V to 5.5V	10V (4) to 36V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

2: This is relative to the DGND signal. There is a separate requirement for the V+/V- voltages. $V_L \geq$ V- + 2.7V.

3: Relative to V-, the V_L and DGND signals must be between (inclusive) V- and V+.

4: Analog operation will continue while the V+ voltage is above the device's analog Power-On Reset (POR)/ Brown-out Reset (BOR) voltage. Operational characteristics may exceed specified limits while the V+ voltage is below the specified minimum voltage.

5: For additional information on these devices, refer to DS20005207.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V- with respect to DGND ..... DGND + 0.6V to -40.0V
Voltage on V+ with respect to DGND ..... DGND - 0.3V to 40.0V
Voltage on V+ with respect to V- ..... DGND - 0.3V to 40.0V
Voltage on V_L with respect to V+ ..... -0.6V to -40.0V
Voltage on V_L with respect to V- ..... -0.6V to +40.0V
Voltage on V_L with respect to DGND ..... -0.6V to +7.0V
Voltage on SCL, SDA, A0, A1, $\overline{WLAT}$, and $\overline{SHDN}$ with respect to DGND ..... -0.6V to V_L + 0.6V
Voltage on all other pins (PxA, PxW, and PxB) with respect to V- .....-0.3V to V+ + 0.3V
Input clamp current, I_{IK} (V_I < 0, V_I > V_L, V_I > V_{PP} on HV pins) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_L) ..... ±20 mA
Maximum current out of DGND pin ..... 100 mA
Maximum current into V_L pin ..... 100 mA
Maximum current out of V- pin ..... 100 mA
Maximum current into V+ pin .....100 mA
Maximum current into PxA, PxW, and PxB pins (Continuous)
- R_{AB} = 5 kΩ ..... ±25 mA
- R_{AB} = 10 kΩ ..... ±12.5 mA
- R_{AB} = 50 kΩ ..... ±6.5 mA
- R_{AB} = 100 kΩ ..... ±6.5 mA

Maximum current into PxA, PxW, and PxB pins (Pulsed)
- F_{PULSE} > 10 kHz ..... (Max $I_{Continuous}$) / (Duty Cycle)
- F_{PULSE} ≤ 10 kHz ..... (Max $I_{Continuous}$) / √ (Duty Cycle)

Maximum output current sunk by any Output pin ..... 25 mA
Maximum output current sourced by any Output pin ..... 25 mA
Package Power Dissipation (T_A = + 50°C, T_J = +150°C)
- TSSOP-14 ..... 1000 mW
- QFN-20 (5 x 5) ..... 2800 mW

Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins
- Human Body Model (HBM) ..... ≥ ±5 kV
- Machine Model (MM) ..... ≥ ±400V

Maximum Junction Temperature (T_J) ..... 150°C
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Positive Supply Voltage (V_L)	V_L	2.7	—	5.5	V	With respect to DGND (**Note 4**)
		1.8	—	5.5	V	V_L ≥ V- + 2.7V (**Note 1**, **Note 4**)
		—	—	0	V	With respect to V+
Analog Positive Supply Voltage (V+)	V+	V_L (16)	—	36.0	V	With respect to V- (**Note 4**)
Digital Ground Voltage (DGND)	V_{DGND}	V-	—	V+ - V_L	V	With respect to V- (**Note 4**, **Note 5**)
Analog Negative Supply Voltage (V-)	V-	-36.0 + V_L	—	0	V	With respect to DGND and with V_L = 1.8V
Resistor Network Supply Voltage	V_{RN}	—	—	36.0	V	Delta voltage between V+ and V- (**Note 4**)
V_L Start Voltage to ensure Wiper Reset	V_{DPOR}	—	—	1.8	V	With respect to DGND, V+ > 6.0V RAM retention voltage (V_{RAM}) < V_{DBOR}
V+ Voltage to ensure Wiper Reset	V_{APOR}	—	—	6.0	V	With respect to V-, V_L = 0V RAM retention voltage (V_{RAM}) < V_{BOR}
Digital to Analog Level Shifter Operational Voltage	V_{LS}	—	—	2.3	V	V_L to V- voltage. DGND = V-
Power Rail Voltages during Power-Up (**Note 1**)	V_{LPOR}	—	—	5.5	V	Digital Powers (V_L/DGND) up 1st: V+ and V- floating or as V+/V- powers-up (V+ must be ≥ to DGND) (**Note 18**)
	$V+_{POR}$	—	—	36	V	Analog Powers (V+/V-) up 1st: V_L and DGND floating or as V_L/DGND powers-up (DGND must be between V- and V+) (**Note 18**)
V_L Rise Rate to ensure Power-On Reset	V_{LRR}	(**Note 6**)			V/ms	With respect to DGND

Note 1: This specification by design.

Note 4: V+ voltage is dependent on V- voltage. The maximum delta voltage between V+ and V- is 36V. The digital logic DGND potential can be anywhere between V+ and V-, the V_L potential must be >= DGND and <= V+.

Note 5: Minimum value determined by maximum V- to V+ potential equals 36V and minimum V_L = 1.8V for operation. So 36V - 1.8V = 34.2V.

Note 6: POR/BOR is not rate dependent.

Note 16: For specified analog performance, V+ must be 20V or greater (unless otherwise noted).

Note 18: During the power-up sequence, to ensure expected analog POR operation, the two power systems (analog and digital) should have a common reference to ensure that the driven DGND voltage is not at a higher potential than the driven V+ voltage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Delay after device exits the Reset state ($V_L > V_{BOR}$)	T_{BORD}	—	10	20	µs		
Supply Current (**Note 7**)	I_{DDD}	—	45	650	µA	Serial Interface Active, Write all 0's to Volatile Wiper 0 (address 0h) V_L = 5.5V, F_{SCL} = 3.4 MHz, V- = DGND	
		—	4	7	µA	Serial Interface Inactive, V_L = 5.5V, SCL = V_{IH}, Wiper = 0, V- = DGND	
	I_{DDA}	—	—	5	µA	Current V+ to V-, PxA = PxB = PxW, DGND = V- +(V+/2)	
Resistance (± 20%) (**Note 8**)	R_{AB}	4.0	5	6.0	kΩ	-502 devices, V+/V- = 10V to 36V	
		8.0	10	12.0	kΩ	-103 devices, V+/V- = 10V to 36V	
		40.0	50	60.0	kΩ	-503 devices, V+/V- = 10V to 36V	
		80.0	100	120.0	kΩ	-104 devices, V+/V- = 10V to 36V	
R_{AB} Current	I_{AB}	—	—	9.00	mA	-502 devices	36V / $R_{AB(MIN)}$, V- = -18V, V+ = +18V, (**Note 9**)
		—	—	4.50	mA	-103 devices	
		—	—	0.90	mA	-503 devices	
		—	—	0.45	mA	-104 devices	
Resolution	N	256			Taps	8-bit	No Missing Codes
		128			Taps	7-bit	No Missing Codes
Step Resistance (see **Appendix B.4**)	R_S	—	R_{AB}/(255)	—	Ω	8-bit	**Note 1**
		—	R_{AB}/(127)	—	Ω	7-bit	**Note 1**

Note 1: This specification by design.

Note 7: Supply current (IDDD and IDDA) is independent of current through the resistor network.

Note 8: Resistance (RAB) is defined as the resistance between Terminal A to Terminal B.

Note 9: Ensured by the R_{AB} specification and Ohm's Law.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Wiper Resistance (see **Appendix B.5**)	R_W	—	75	170	Ω	I_W = 1 mA	V+ = +18V, V- = -18V, code = 00h, PxA = floating, PxB = V-.
		—	145	200	Ω	I_W = 1 mA	V+ = +5.0V, V- = -5.0V, code = 00h, PxA = floating, PxB = V-. (**Note 2**)
Nominal Resistance Tempco (see **Appendix B.23**)	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -40°C to +85°C	
		—	100	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco (see **Appendix B.22**)	$\Delta V_{BW}/\Delta T$	—	15	—	ppm/°C	Code = Mid scale (7Fh or 3Fh)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	V-	—	V+	V	**Note 1**, **Note 11**	
Current through Terminals (A, B, and Wiper) (**Note 1**)	I_T, I_W	—	—	25	mA	-502 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	12.5	mA	-103 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	6.5	mA	-503 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	6.5	mA	-104 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	36	mA	$I_{BW(W = ZS)}$, or $I_{AW(W = FS)}$	
Leakage current into A, W or B	I_{TL}	—	5	—	nA	A = W = B = V-	

Note 1: This specification by design.

Note 2: This parameter is not tested, but specified by characterization.

Note 11: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Full Scale Error (Potentiometer) (8-bit code = FFh, 7-bit code = 7Fh) (**Note 10**, **Note 17**) (V_A = V+, V_B = V-) (see **Appendix B.10**)	V_{WFSE}	-10.5	—	—	LSb	5 kΩ	8-bit	V_{AB} = 20V to 36V
		-8.5	—	—	LSb			V_{AB} = 20V to 36V –40°C ≤ T_A ≤ +85°C (**Note 2**)
		-14.0	—	—	LSb			V_{AB} = 10V to 36V
		-5.5	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-4.5	—	—	LSb			V_{AB} = 20V to 36V –40°C ≤ T_A ≤ +85°C (**Note 2**)
		-7.5	—	—	LSb			V_{AB} = 10V to 36V
		-4.5	—	—	LSb	10 kΩ	8-bit	V_{AB} = 20V to 36V
		-6.0	—	—	LSb			V_{AB} = 10V to 36V
		-2.65	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-2.25	—	—	LSb			V_{AB} = 20V to 36V –40°C ≤ T_A ≤ +85°C (**Note 2**)
		-3.5	—	—	LSb			V_{AB} = 10V to 36V
		-1.0	—	—	LSb	50 kΩ	8-bit	V_{AB} = 20V to 36V
		-1.4	—	—	LSb			V_{AB} = 10V to 36V
		-1.0	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-1.2	—	—	LSb			V_{AB} = 10V to 36V
		-0.7	—	—	LSb	100 kΩ	8-bit	V_{AB} = 20V to 36V
		-0.95	—	—	LSb			V_{AB} = 10V to 36V
		-0.85	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-0.975	—	—	LSb			V_{AB} = 10V to 36V

Note 2: This parameter is not tested, but specified by characterization.

Note 10: Measured at V_W with V_A = V+ and V_B = V-.

Note 17: Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Zero Scale Error (Potentiometer) (8-bit code = 00h, 7-bit code = 00h) **(Note 10, Note 17)** **(**V_A = V+, V_B = V- **)** (see **Appendix B.11**)	V_{WZSE}	—	—	+9.5	LSb	5 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+8.5	LSb			V_{AB} = 20V to 36V –40°C ≤ T_A ≤ +85°C **(Note 2)**
		—	—	+14.5	LSb			V_{AB} = 10V to 36V
		—	—	+4.5	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+7.0	LSb			V_{AB} = 10V to 36V
		—	—	+4.25	LSb	10 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+6.5	LSb			V_{AB} = 10V to 36V
		—	—	+2.125	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+3.25	LSb			V_{AB} = 10V to 36V
		—	—	+0.9	LSb	50 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+1.3	LSb			V_{AB} = 10V to 36V
		—	—	+0.5	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+0.7	LSb			V_{AB} = 10V to 36V
		—	—	+0.6	LSb	100 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+0.95	LSb			V_{AB} = 10V to 36V
		—	—	+0.3	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+0.475	LSb			V_{AB} = 10V to 36V

Note 2: This parameter is not tested, but specified by characterization.

Note 10: Measured at V_W with V_A = V+ and V_B = V-.

Note 17: Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Potentiometer Integral Nonlinearity (**Note 10**, **Note 17**) (see **Appendix B.12**)	P-INL	-1	±0.5	+1	LSb	5 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb		7-bit	V_{AB} = 10V to 36V
		-1	±0.5	+1	LSb	10 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb		7-bit	V_{AB} = 10V to 36V
		-1.1	±0.5	+1.1	LSb	50 kΩ	8-bit	V_{AB} = 10V to 36V
		-1	±0.5	+1	LSb			V_{AB} = 20V to 36V, **(Note 2)**
		-1	±0.5	+1	LSb			V_{AB} = 10V to 36V, –40°C ≤ T_A ≤ +85°C **(Note 2)**
		-0.6	±0.25	+0.6	LSb		7-bit	V_{AB} = 10V to 36V
		-1.85	±0.5	+1.85	LSb	100 kΩ	8-bit	V_{AB} = 10V to 36V
		-1.2	±0.5	+1.2	LSb			V_{AB} = 20V to 36V, **(Note 2)**
		-1	±0.5	+1	LSb			V_{AB} = 10V to 36V, –40°C ≤ T_A ≤ +85°C **(Note 2)**
		-1	±0.5	+1	LSb		7-bit	V_{AB} = 10V to 36V
Potentiometer Differential Nonlinearity (**Note 10**, **Note 17**) (see **Appendix B.13**)	P-DNL	-0.7	±0.25	+0.7	LSb	5 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb			V_{AB} = 20V to 36V **(Note 2)**
		-0.25	±0.125	+0.25	LSb		7-bit	V_{AB} = 10V to 36V
		-0.375	±0.125	+0.375	LSb	10 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.25	±0.1	+0.25	LSb		7-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb	50 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	±0.1	+0.125	LSb		7-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb	100 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	±0.1	+0.125	LSb		7-bit	V_{AB} = 10V to 36V

Note 2: This parameter is not tested, but specified by characterization.

Note 10: Measured at V_W with V_A = V+ and V_B = V-.

Note 17: Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Bandwidth -3 dB (load = 30 pF)	BW	—	480	—	kHz	5 kΩ	8-bit	Code = 7Fh
		—	480	—	kHz		7-bit	Code = 3Fh
		—	240	—	kHz	10 kΩ	8-bit	Code = 7Fh
		—	240	—	kHz		7-bit	Code = 3Fh
		—	48	—	kHz	50 kΩ	8-bit	Code = 7Fh
		—	48	—	kHz		7-bit	Code = 3Fh
		—	24	—	kHz	100 kΩ	8-bit	Code = 7Fh
		—	24	—	kHz		7-bit	Code = 3Fh
V_W Settling Time (V_A = 10V, V_B = 0V, ±1LSb error band, C_L = 50 pF) (see **Appendix B.17**)	t_S	—	1	—	µs	5 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h	
		—	1	—	µs	10 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h	
		—	2.5	—	µs	50 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h	
		—	5	—	µs	100 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h	

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Rheostat Integral Nonlinearity (**Note 12**, **Note 13**, **Note 14**, **Note 17**) (see **Appendix B.5**)	R-INL	-2.0.	—	+2.0	LSb	5 kΩ	8-bit	I_W = 6.0 mA, (V+ - V-) = 36V (**Note 2**)
		-2.5	—	+2.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V (**Note 2**)
		-4.5	—	+4.5	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb		7-bit	I_W = 6.0 mA, (V+ - V-) = 36V (**Note 2**)
		-1.5	—	+1.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V (**Note 2**)
		-2.0	—	+2.0	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-1.2	—	+1.2	LSb	10 kΩ	8-bit	I_W = 3.0 mA, (V+ - V-) = 36V (**Note 2**)
		-1.75	—	+1.75	LSb			I_W = 1.7 mA, (V+ - V-) = 20V (**Note 2**)
		-2.0	—	+2.0	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.6	—	+0.6	LSb		7-bit	I_W = 3.0 mA, (V+ - V-) = 36V (**Note 2**)
		-0.8	—	+0.8	LSb			I_W = 1.7 mA, (V+ - V-) = 20V (**Note 2**)
		-1.1	—	+1.1	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	50 kΩ	8-bit	I_W = 600 µA, (V+ - V-) = 36V (**Note 2**)
		-1.0	—	+1.0	LSb			I_W = 330 µA, (V+ - V-) = 20V (**Note 2**)
		-1.2	—	+1.2	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb		7-bit	I_W = 600 µA, (V+ - V-) = 36V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 330 µA, (V+ - V-) = 20V (**Note 2**)
		-0.6	—	+0.6	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	100 kΩ	8-bit	I_W = 300 µA, (V+ - V-) = 36V (**Note 2**)
		-1.0	—	+1.0	LSb			I_W = 170 µA, (V+ - V-) = 20V(**Note 2**)
		-1.2	—	+1.2	LSb			I_W = 83 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb		7-bit	I_W = 300 µA, (V+ - V-) = 36V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 20V (**Note 2**)
		-0.6	—	+0.6	LSb			I_W = 83 µA, (V+ - V-) = 10V

Note 2: This parameter is not tested, but specified by characterization.

Note 12: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

Note 13: Externally connected to a Rheostat configuration (RBW), and then tested.

Note 14: Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).

Note 17: Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Rheostat Differential Nonlinearity (**Note 12**, **Note 13**, **Note 14**, **Note 17**) (see **Appendix B.5**)	R-DNL	-0.5	—	+0.5	LSb	5 kΩ	8-bit	I_W = 6.0 mA, (V+ - V-) = 36V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V (**Note 2**)
		-0.8	—	+0.8	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 6.0 mA, (V+ - V-) = 36V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 3.3 mA, (V+ - V-) = 20V (**Note 2**)
		-0.4	—	+0.4	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	10 kΩ	8-bit	I_W = 3.0 mA, (V+ - V-) = 36V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 1.7 mA, (V+ - V-) = 20V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 3.0 mA, (V+ - V-) = 36V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 1.7 mA, (V+ - V-) = 20V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	50 kΩ	8-bit	I_W = 600 µA, (V+ - V-) = 36V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 330 µA, (V+ - V-) = 20V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 600 µA, (V+ - V-) = 36V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 330 µA, (V+ - V-) = 20V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	100 kΩ	8-bit	I_W = 300 µA, (V+ - V-) = 36V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 20V (**Note 2**)
		-0.5	—	+0.5	LSb			I_W = 83 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 300 µA, (V+ - V-) = 36V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 170 µA, (V+ - V-) = 20V (**Note 2**)
		-0.25	—	+0.25	LSb			I_W = 83 µA, (V+ - V-) = 10V

Note 2: This parameter is not tested, but specified by characterization.

Note 12: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

Note 13: Externally connected to a Rheostat configuration (RBW), and then tested.

Note 14: Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).

Note 17: Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Capacitance (P_A)	C_A	—	75	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid Scale
Capacitance (P_w)	C_W	—	120	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid Scale
Capacitance (P_B)	C_B	—	75	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid Scale
Common-Mode Leakage	I_{CM}	—	5	—	nA	$V_A = V_B = V_W$
Digital Interface Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 400 kHz
Digital Inputs/Outputs (SDA, SCL, A0, A1, $\overline{\text{SHDN}}$, $\overline{\text{WLAT}}$)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.7 V_L	—	V_L + 0.3V	V	1.8V ≤ V_L ≤ 5.5V
Schmitt Trigger Low-Input Threshold	V_{IL}	DGND - 0.5V	—	0.3 V_L	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_L	—	V	
Output Low Voltage (SDA)	V_{OL}	DGND	—	0.2 V_L	V	V_L = 5.5V, I_{OL} = 5 mA
		DGND	—	0.2 V_L	V	V_L = 1.8V, I_{OL} = 800 µA
Input Leakage Current	I_{IL}	-1		1	uA	$V_{IN} = V_L$ and V_{IN} = DGND

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
RAM (Wiper, TCON) Value							
Wiper Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	7Fh	hex	7-bit	
Wiper POR/BOR Value	$N_{POR/BOR}$	7Fh			hex	8-bit	
		3Fh			hex	7-bit	
TCON Value Range	N	0h	—	FFh	hex		
TCON POR/BOR Value	N_{TCON}	FF			hex	All Terminals connected	
Power Requirements							
Power Supply Sensitivity (see **Appendix B.20**)	PSS	—	0.0015	0.0035	%/%	8-bit	V_L = 2.7V to 5.5V, V+ = 18V, V- = -18V, Code = 7Fh
		—	0.0015	0.0035	%/%	7-bit	V_L = 2.7V to 5.5V, V+ = 18V, V- = -18V, Code = 3Fh
Power Dissipation	P_{DISS}	—	260	—	mW	5 kΩ	V_L = 5.5V, V+ = 18V, V- = -18V **(Note 15)**
		—	130	—	mW	10 kΩ	
		—	26	—	mW	50 kΩ	
		—	13	—	mW	100 kΩ	

Note 15: $P_{DISS} = I * V$, or ((I_{DDD} * 5.5V) + (I_{DDA} * 36V) + (I_{AB} * 36V)).

DC Notes:

1. This specification by design.
2. This parameter is not tested, but specified by characterization.
3. See Absolute Maximum Ratings.
4. V+ voltage is dependent on V- voltage. The maximum delta voltage between V+ and V- is 36V. The digital logic DGND potential can be anywhere between V+ and V-, the V_L potential must be >= DGND and <= V+.
5. Minimum value determined by maximum V- to V+ potential equals 36V and minimum V_L = 1.8V for operation. So 36V - 1.8V = 34.2V.
6. POR/BOR is not rate dependent.
7. Supply current (I_{DDD} and I_{DDA}) is independent of current through the resistor network.
8. Resistance (R_{AB}) is defined as the resistance between Terminal A to Terminal B.
9. Ensured by the R_{AB} specification and Ohm's Law.
10. Measured at V_W with V_A = V+ and V_B = V-.
11. Resistor terminals A, W and B's polarity with respect to each other is not restricted.
12. Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
13. Externally connected to a Rheostat configuration (R_{BW}), and then tested.
14. Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).
15. P_{DISS} = I * V, or ((I_{DDD} * 5.5V) + (I_{DDA} * 36V) + (I_{AB} * 36V)).
16. For specified analog performance, V+ must be 20V or greater (unless otherwise noted).
17. Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.
18. During the power-up sequence, to ensure expected analog POR operation, the two power systems (analog and digital) should have a common reference to ensure that the driven DGND voltage is not at a higher potential than the driven V+ voltage.

1.1 Timing Waveforms and Requirements

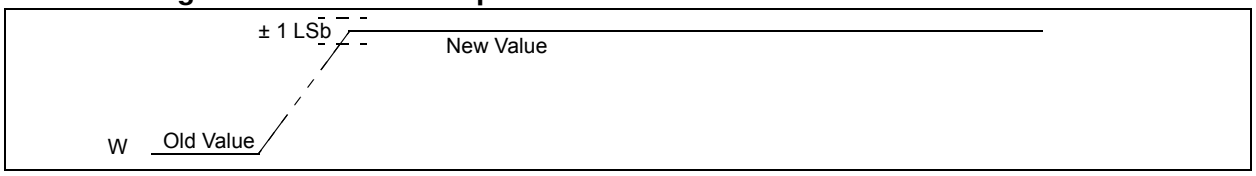


FIGURE 1-1: *Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V and V- = -5.0V to -18V (referenced to DGND -> ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_W Settling Time (V_A = 10V, V_B = 0V, ±1LSb error band, C_L = 50 pF)	t_S	—	1	—	µs	5 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h
		—	1	—	µs	10 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h
		—	2.5	—	µs	50 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h
		—	5	—	µs	100 kΩ	Code = 00h -> FFh (7Fh); FFh (7Fh) -> 00h

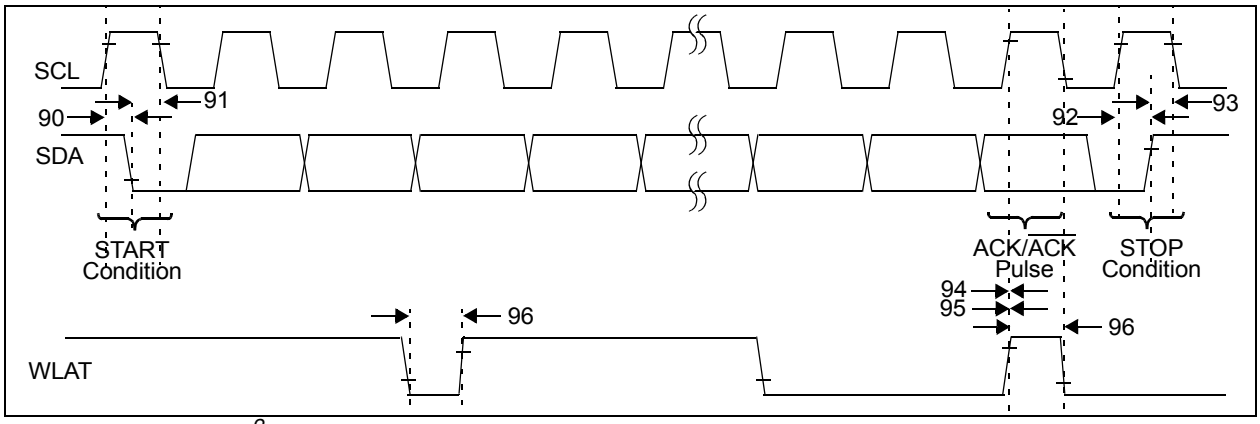


FIGURE 1-2: *I^2C Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-2: I^2C BUS START/STOP BITS AND $\overline{WLAT}$ REQUIREMENTS

I^2C™ AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) 2.7V ≤ V_L ≤ 5.5V; DGND = V- (Note 1)				
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
	F_{SCL}		Standard mode	0	100	kHz	C_b = 400 pF, 1.8V ≤ V_L ≤ 5.5V
			Fast mode	0	400	kHz	C_b = 400 pF, 2.7V ≤ V_L ≤ 5.5V
			High Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V ≤ V_L ≤ 5.5V
			High Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V ≤ V_L ≤ 5.5V
D102	Cb	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	$T_{SU:STA}$	Start condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated Start condition
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	$T_{HD:STA}$	Start condition Hold time	100 kHz mode	4000	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	$T_{SU:STO}$	Stop condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	$T_{HD:STO}$	Stop condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
94	T_{WLSU}	$\overline{WLAT}$ ↑ to SCL↑ (write data ACK bit) Setup time		10	—	ns	Write Data delayed, Note 9
95	T_{WLHD}	SCL ↑ to $\overline{WLAT}$↑ (write data ACK bit) Hold time		250	—	ns	Write Data delayed, Note 9
96	T_{WLATL}	$\overline{WLAT}$ High or Low Time		2	—	µs	

Note 1: Serial Interface has equal performance when DGND >= V- + 0.9V.

Note 9: The transition of the WLAT signal between 10 ns before the rising edge (Spec 94) and 200 ns after the rising edge (Spec 95) of the SCL signal is indeterminant if the Write Data is delayed or not.

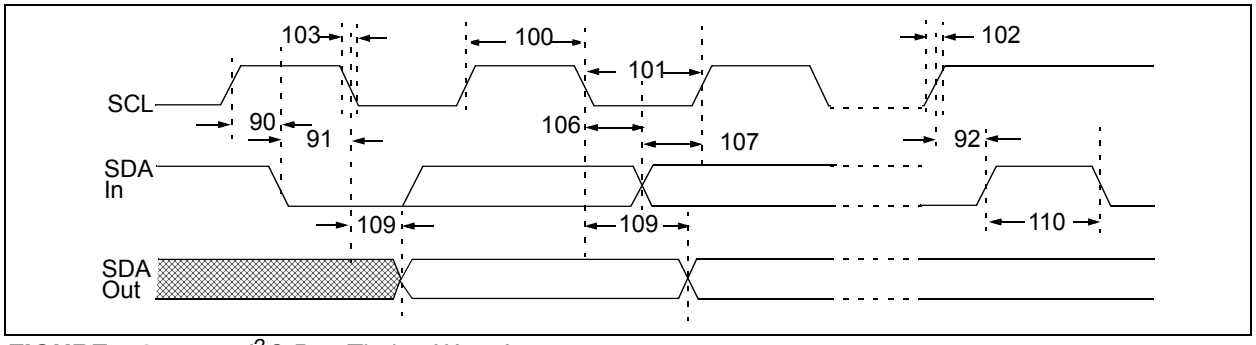


FIGURE 1-3: *I^2C Bus Timing Waveforms.*

TABLE 1-3: I^2C BUS REQUIREMENTS (SLAVE MODE)

I^2C™ AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) 2.7V ≤ V_L ≤ 5.5V; DGND = V- (Note 1)				
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
100	T_{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120	—	ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	T_{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320	—	ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V
102A (6)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B (6)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	

Note 1: Serial Interface has equal performance when DGND >= V- + 0.9V.

Note 6: Not tested.

TABLE 1-4: I²C BUS REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C™ AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) 2.7V ≤ V_L ≤ 5.5V; DGND = V- (Note 1)				
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
103A (5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B (5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb (4)	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V, **Note 7**
			400 kHz mode	0	—	ns	2.7V-5.5V, **Note 7**
			1.7 MHz mode	0	—	ns	4.5V-5.5V, **Note 7**
			3.4 MHz mode	0	—	ns	4.5V-5.5V, **Note 7**
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**Note 3**
			400 kHz mode	100	—	ns	
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	**Note 2**
			400 kHz mode	—	900	ns	
			1.7 MHz mode	—	150	ns	Cb = 100 pF, **Note 2**, **Note 8**
				—	310	ns	Cb = 400 pF, **Note 2**, **Note 6**
			3.4 MHz mode	—	150	ns	Cb = 100 pF, **Note 2**
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP Spec states N.A.
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression

Note 1: Serial Interface has equal performance when DGND >= V- + 0.9V.

Note 2: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

Note 3: A fast-mode (400 kHz) I²C bus device can be used in a standard mode (100 kHz) I²C bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

Note 6: Not tested.

Note 7: A master transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

Note 8: Ensured by the T_{AA} 3.4 MHz specification test.

Timing Table Notes:

1. Serial Interface has equal performance when DGND >= V- + 0.9V.
2. As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
3. A fast-mode (400 kHz) I^2C bus device can be used in a standard mode (100 kHz) I^2C bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line
   T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard mode I^2C bus specification) before the SCL line is released.
4. The MCP45HVX1 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.
5. Use Cb in pF for the calculations.
6. Not tested.
7. A master transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
8. Ensured by the T_{AA} 3.4 MHz specification test.
9. The transition of the $\overline{WLAT}$ signal between 10 ns before the rising edge (Spec 94) and 200 ns after the rising edge (Spec 95) of the SCL signal is indeterminant if the Write Data is delayed or not.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_L = +2.7V to +5.5V, V+ = +10V to +36V, V- = DGND = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-TSSOP (ST)	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 20L-QFN (MQ)	θ_{JA}	—	36.1	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The device Performance Curves are available in a separate document. This is done to keep the file size of this PDF document less than the 10MB file attachment limit of many mail servers.
The MCP45HVX1 Performance Curves document is literature number DS20005307, and can be found on the Microchip web site. Look at the MCP45HVX1 Product Page under Documentation and Software, in the Data Sheets category.

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.
Additional descriptions of the device pins follows.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP45HVX1

Pin		Symbol	Type	Buffer Type	Function
TSSOP 14L	QFN 20L				
1	1	V_L	P	—	Positive Digital Power Supply Input
2	2	SCL	I	ST	I^2C™ Serial Clock pin
3	3	A1	I	ST	I^2C Address 1
4	4	SDA	I/O	ST	I^2C Serial Data pin
5	5	A0	I	ST	I^2C Address 0
6	6	$\overline{WLAT}$	I	ST	Wiper Latch Enable 0 = Received I^2C Shift Register Buffer (SPBUF) value is transfered to Wiper register. 1 = Received I^2C data value is held in I^2C Shift Register Buffer (SPBUF).
7	8, 9, 10, 17, 18, 19, 20	NC	—	—	Pin not internally connected to die. To reduce noise coupling, connect pin either to DGND or V_L.
8	7	$\overline{SHDN}$	I	ST	Shutdown
9	11	DGND	P	—	Ground
10	12	V-	P	—	Analog Negative Potential Supply
11	13	P0B	I/O	A	Potentiometer 0 Terminal B
12	14	P0W	I/O	A	Potentiometer 0 Wiper Terminal
13	15	P0A	I/O	A	Potentiometer 0 Terminal A
14	16	V+	P	—	Analog Positive Potential Supply
—	21	EP	P	—	Exposed Pad, connect to V- signal or Not Connected (floating). **(Note 1)**

Legend: A = Analog ST = Schmitt Trigger
I = Input O = Output I/O = Input/Output P = Power

Note 1: The QFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device's V- pin.

3.1 Positive Power Supply Input (V_L)

The V_L pin is the device's positive power supply input. The input power supply is relative to DGND and can range from 1.8V to 5.5V. A decoupling capacitor on V_L (to DGND) is recommended to achieve maximum performance.

3.2 Digital Ground (DGND)

The DGND pin is the device's digital ground reference.

3.3 Analog Positive Voltage (V+)

Analog circuitry positive supply voltage. Must have a higher potential than the V- pin.

3.4 Analog Negative Voltage (V-)

Analog circuitry negative supply voltage. The V- potential must be lower than or equal to the DGND pin potential.

3.5 Serial Clock (SCL)

The SCL pin is the serial interface's Serial Clock pin. This pin is connected to the Host Controller's SCL pin. The MCP45HVX1 is an I^2C slave device, so its SCL pin is an input-only pin.

3.6 Serial Data (SDA)

The SDA pin is the serial interface's Serial Data In/Out pin. This pin is connected to the Host Controller's SDA pin. The SDA pin is an open-drain N-Channel driver.

This pin allows the host controller to read and write the digital potentiometer registers (Wiper and TCON).

3.7 Address 0 (A0)

The A0 pin is the Address 0 input for the I^2C interface. At the device's POR/BOR the value of the A0 address bit is latched. This input along with the A1 pin completes the device address. This allows up to four MCP45HVXX devices to be on a single I^2C bus.

3.8 Address 1 (A1)

The A1 pin is the I^2C interface's Address 1 pin. Along with the A0 pins, up to four MCP45HVXX devices can be on a single I^2C bus.

3.9 Wiper Latch ($\overline{WLAT}$)

The $\overline{WLAT}$ pin is used to hold off the transfer of the received wiper value (in the Shift register) to the Wiper register. This allows this transfer to be synchronized to an external event (such as zero crossing). See **Section 4.3.2**.

3.10 Shutdown ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is used to force the resistor network terminals into the hardware shutdown state. See **Section 4.3.1**.

3.11 Potentiometer Terminal B

The Terminal B pin is connected to the internal potentiometer's Terminal B.

The potentiometer's Terminal B is the fixed connection to the zero-scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The Terminal B pin does not have a polarity relative to the Terminal W or A pins. The Terminal B pin can support both positive and negative current. The voltage on Terminal B must be between V+ and V-.

3.12 Potentiometer Wiper (W) Terminal

The Terminal W pin is connected to the internal potentiometer's Terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The Terminal W pin does not have a polarity relative to Terminal's A or B pins. The Terminal W pin can support both positive and negative current. The voltage on Terminal W must be between V+ and V-.

If the V+ voltage powers-up before the V_L voltage, the wiper is forced to mid scale once the analog POR voltage is crossed.

If the V+ voltage powers-up after the V_L voltage is greater than the digital POR voltage, the wiper is forced to the value in the Wiper register once the analog POR voltage is crossed.

3.13 Potentiometer Terminal A

The Terminal A pin is connected to the internal potentiometer's Terminal A.

The potentiometer's Terminal A is the fixed connection to the full scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0xFF for 8-bit devices or 0x7F for 7-bit devices.

The Terminal A pin does not have a polarity relative to the Terminal W or B pins. The Terminal A pin can support both positive and negative current. The voltage on Terminal A must be between V+ and V-.

3.14 Exposed Pad (EP)

This pad is only on the bottom of the QFN packages. This pad is conductively connected to the device substrate. The EP pin must be connected to the V- signal or left floating. This pad could be connected to a PCB heat sink to assist as a heat sink for the device.

3.15 Not Connected (NC)

This pin is not internally connected to the die. To reduce noise coupling, these pins should be connected to either V_L or DGND.