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MCP4725

12-Bit Digital-to-Analog Converter with EEPROM Memory in SOT-23-6

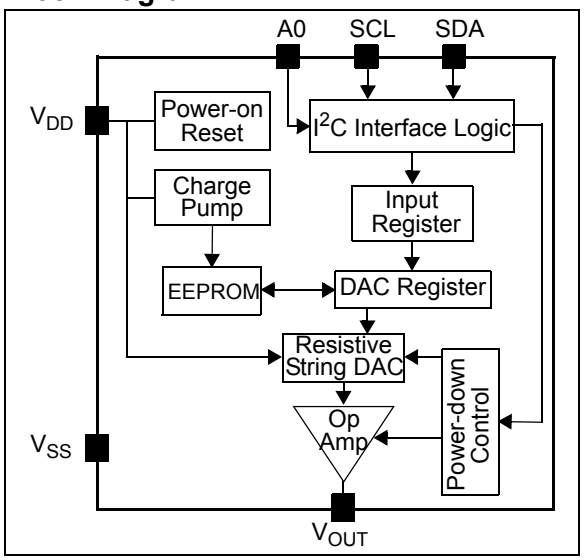
Features

- 12-Bit Resolution
- On-Board Non-Volatile Memory (EEPROM)
- ±0.2 LSB DNL (typical)
- External A0 Address Pin
- Normal or Power-Down Mode
- Fast Settling Time: 6 µs (typical)
- External Voltage Reference (V_{DD})
- Rail-to-Rail Output
- Low Power Consumption
- Single-Supply Operation: 2.7V to 5.5V
- I^2C^{TM} Interface:
  - Eight Available Addresses
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (3.4 Mbps) Modes
- Small 6-lead SOT-23 Package
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Closed-Loop Servo Control
- Low Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems

Block Diagram



DESCRIPTION

The MCP4725 is a low-power, high accuracy, single channel, 12-bit buffered voltage output Digital-to-Analog Convertor (DAC) with non-volatile memory (EEPROM). Its on-board precision output amplifier allows it to achieve rail-to-rail analog output swing.

The DAC input and configuration data can be programmed to the non-volatile memory (EEPROM) by the user using I^2C interface command. The non-volatile memory feature enables the DAC device to hold the DAC input code during power-off time, and the DAC output is available immediately after power-up. This feature is very useful when the DAC device is used as a supporting device for other devices in the network.

The device includes a Power-On-Reset (POR) circuit to ensure reliable power-up and an on-board charge pump for the EEPROM programming voltage. The DAC reference is driven from V_{DD} directly. In power-down mode, the output amplifier can be configured to present a known low, medium, or high resistance output load.

The MCP4725 has an external A0 address bit selection pin. This A0 pin can be tied to V_{DD} or V_{SS} of the user's application board.

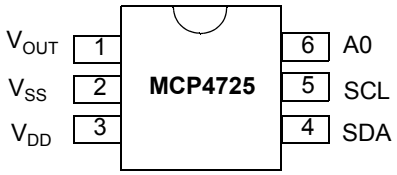
The MCP4725 has a two-wire I^2C™ compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

The MCP4725 is an ideal DAC device where design simplicity and small footprint is desired, and for applications requiring the DAC device settings to be saved during power-off time.

The device is available in a small 6-pin SOT-23 package.

Package Type

SOT-23-6



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....6.5V
All inputs and outputs w.r.t V_{SS} .....–0.3V to V_{DD}+0.3V
Current at Input Pins .....±2 mA
Current at Supply Pins .....±50 mA
Current at Output Pins .....±25 mA
Storage Temperature .....-65°C to +150°C
Ambient Temp. with Power Applied .....-55°C to +125°C
ESD protection on all pins ..... ≥ 6 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF, T_A = -40°C to +125°C. Typical values are at +25°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Supply Current	I_{DD}	—	210	400	µA	Digital input pins are grounded, Output pin (V_{OUT}) is not connected (unloaded), Code = 000h
Power-Down Current	I_{DDP}	—	0.06	2.0	µA	V_{DD} = 5.5V
Power-On-Reset Threshold Voltage	V_{POR}	—	2	—	V	
DC Accuracy						
Resolution	n	12	—	—	Bits	Code Range = 000h to FFFh
INL Error	INL	—	±2	±14.5	LSB	**Note 1**
DNL	DNL	-0.75	±0.2	±0.75	LSB	**Note 1**
Offset Error	V_{OS}		0.02	0.75	% of FSR	Code = 000h
Offset Error Drift	ΔV_{OS}/°C	—	±1	—	ppm/°C	-45°C to +25°C
		—	±2	—	ppm/°C	+25°C to +85°C
Gain Error	G_E	-2	-0.1	2	% of FSR	Code = FFFh, Offset error is not included.
Gain Error Drift	ΔG_E/°C	—	-3	—	ppm/°C	
Output Amplifier						
Phase Margin	p_M	—	66	—	Degree(°)	C_L = 400 pF, R_L = ∞
Capacitive Load Stability	C_L	—	—	1000	pF	R_L = 5 kΩ, **Note 2**
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	15	24	mA	V_{DD} = 5V, V_{OUT} = Grounded
Output Voltage Settling Time	T_S	—	6	—	µs	**Note 3**

Note 1: Test Code Range: 100 to 4000.
2: This parameter is ensure by design and not 100% tested.
3: Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.
4: Logic state of external address selection pin (A0 pin).

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = + 2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF, T_A = -40°C to +125°C. Typical values are at +25°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Power Up Time	T_{PU}	—	2.5	—	µs	V_{DD} = 5V
		—	5	—	µs	V_{DD} = 3V Exit Power-down Mode, (Started from falling edge of ACK pulse)
DC Output Impedance	R_{OUT}	—	1	—	Ω	Normal mode (V_{OUT} to V_{SS})
		—	1	—	kΩ	Power-Down Mode 1 (V_{OUT} to V_{SS})
		—	100	—	kΩ	Power-Down Mode 2 (V_{OUT} to V_{SS})
		—	500	—	kΩ	Power-Down Mode 3 (V_{OUT} to V_{SS})
Supply Voltage Power-up Ramp Rate for EEPROM loading	V_{DD_RAMP}	1	—	—	V/ms	Validation only.
Dynamic Performance						
Major Code Transition Glitch		—	45	—	nV-s	1 LSB change around major carry (from 800h to 7FFh) (**Note 2)**
Digital Feedthrough		—	<10	—	nV-s	**Note 2**
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	$0.7V_{DD}$	—	—	V	
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	$0.3V_{DD}$	V	
Input High Voltage (A0 Pin)	$V_{A0\text{-}Hi}$	$0.8V_{DD}$	—	—		**Note 4**
Input Low Voltage (A0 Pin)	$V_{A0\text{-}IL}$	—	—	$0.2V_{DD}$		**Note 4**
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = A0 = V_{SS} or SCL = SDA = A0 = V_{DD}
Pin Capacitance	C_{PIN}	—	—	3	pF	**Note 2**
EEPROM						
EEPROM Write Time	TWRITE	—	25	50	ms	
Data Retention		—	200	—	Years	At +25°C, **(Note 2)**
Endurance		1	—	—	Million Cycles	At +25°C, **(Note 2)**

Note 1: Test Code Range: 100 to 4000.

2: This parameter is ensure by design and not 100% tested.

3: Within 1/2 LSB of the final value when code changes from 1/4 to 3/4 (400h to C00h) of full scale range.

4: Logic state of external address selection pin (A0 pin).

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	190.5	—	°C/W	

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

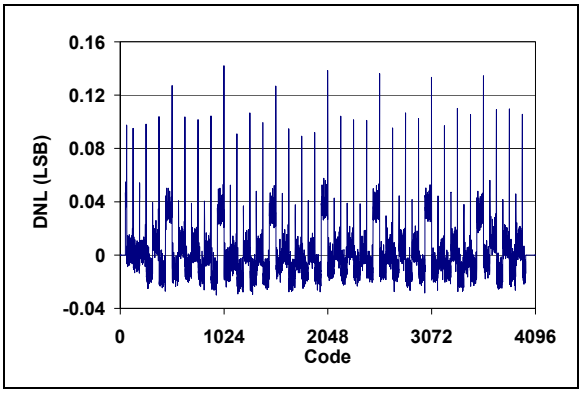


FIGURE 2-1: *DNL vs. Code (V_{DD} = 5.5V).*

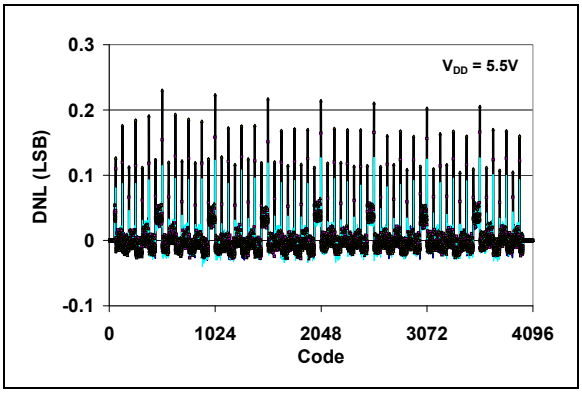


FIGURE 2-2: *DNL vs. Code and Temperature (T_A = -40°C to +125°C).*

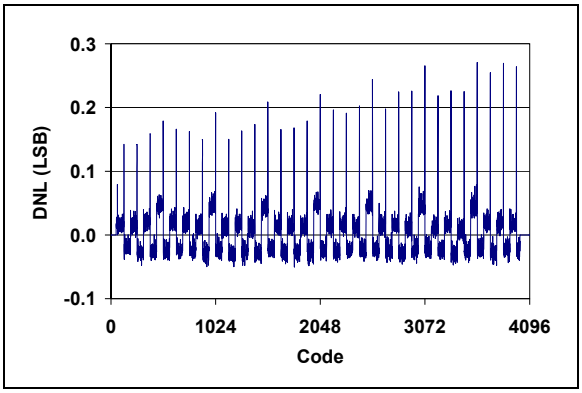


FIGURE 2-3: *DNL vs. Code (V_{DD} = 2.7V).*

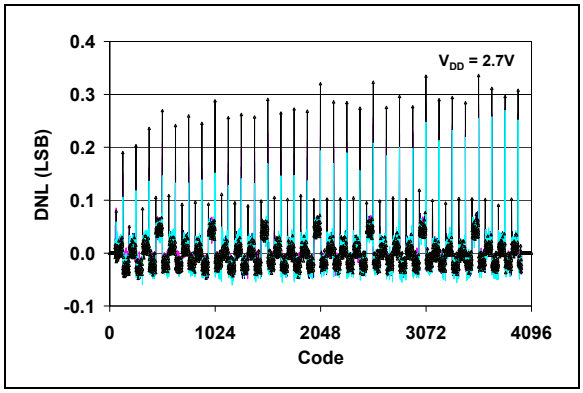


FIGURE 2-4: *DNL vs. Code and Temperature (T_A = -40°C to +125°C).*

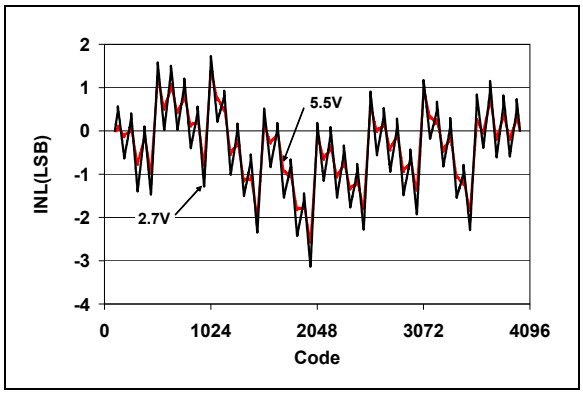


FIGURE 2-5: *INL vs. Code.*

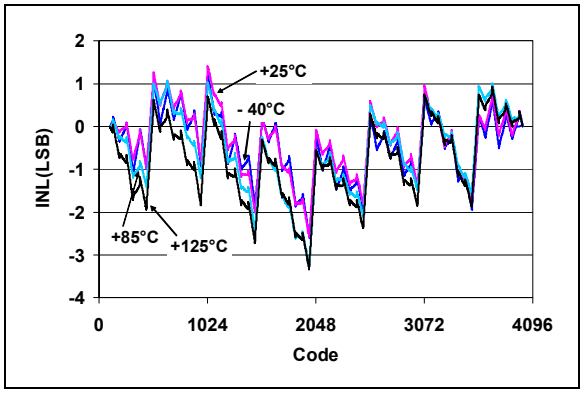


FIGURE 2-6: *INL vs. Code and Temperature (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

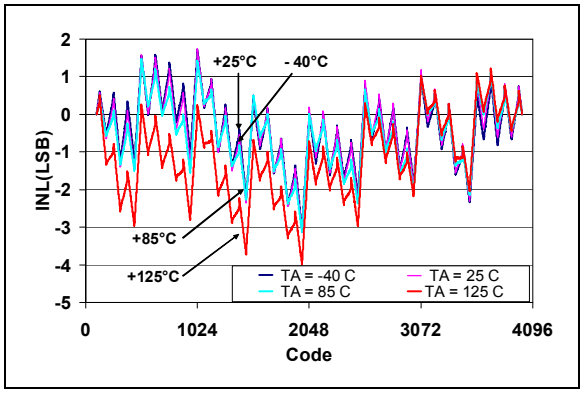


FIGURE 2-7: *INL vs. Code and Temperature (V_{DD} = 2.7V).*

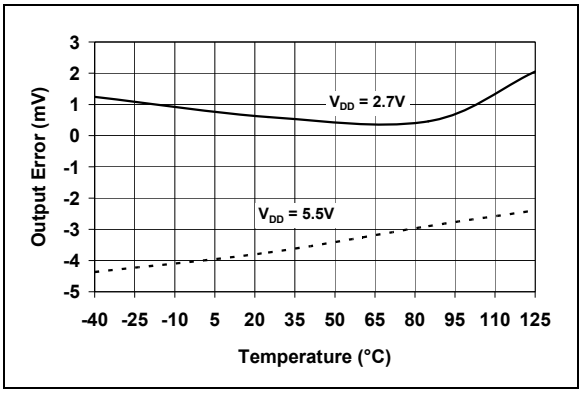


FIGURE 2-10: *Output Error vs. Temperature (Code = 4000d).*

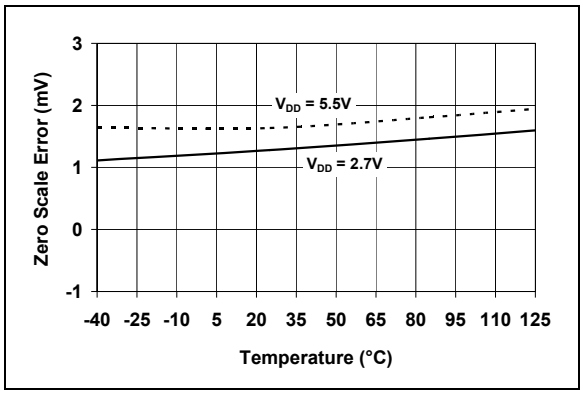


FIGURE 2-8: *Zero Scale Error vs. Temperature (Code = 000d).*

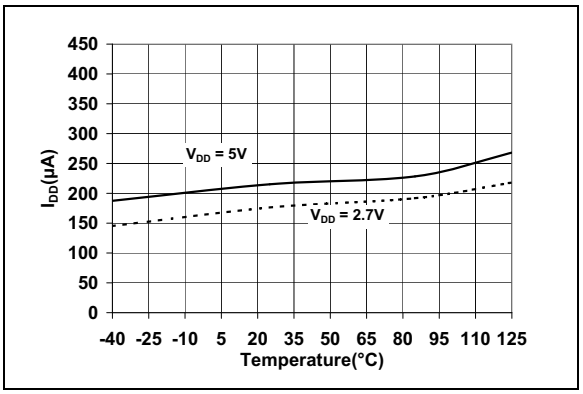


FIGURE 2-11: *I_{DD} vs. Temperature.*

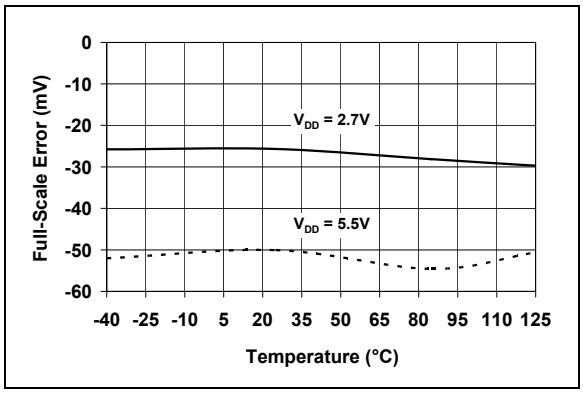


FIGURE 2-9: *Full Scale Error vs. Temperature (Code = 4095d).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

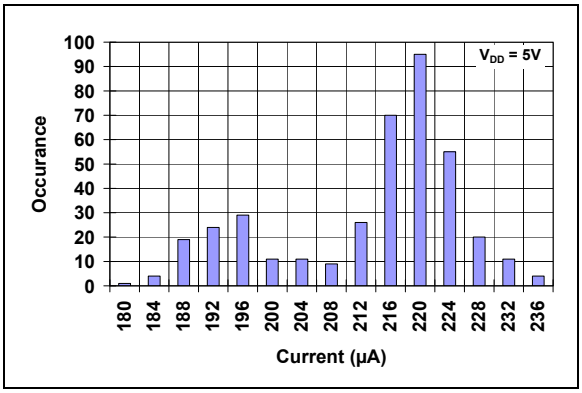


FIGURE 2-12: *I_{DD} Histogram .*

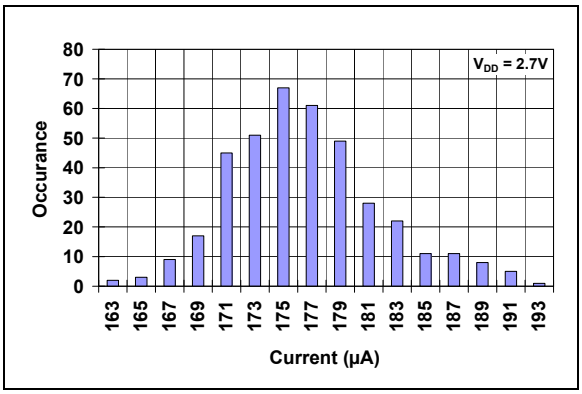


FIGURE 2-13: *I_{DD} Histogram.*

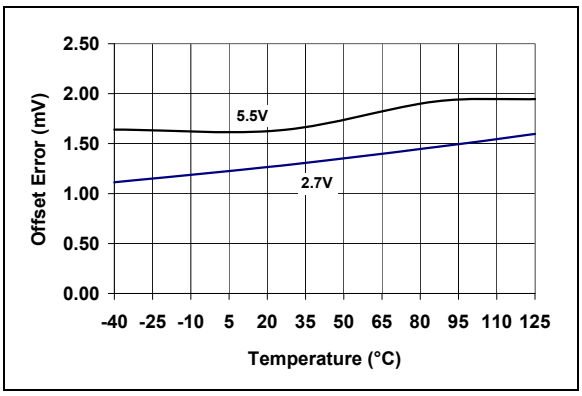


FIGURE 2-14: *Offset Error vs. Temperature and V_{DD}.*

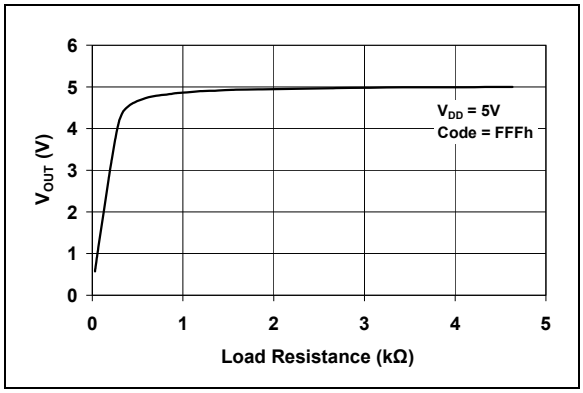


FIGURE 2-15: *V_{OUT} vs. Resistive Load.*

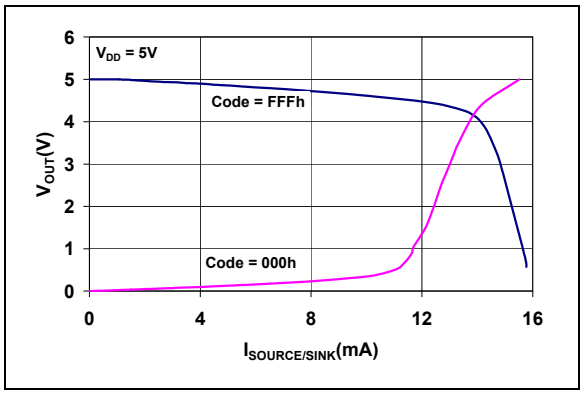


FIGURE 2-16: *Source and Sink Current Capability.*

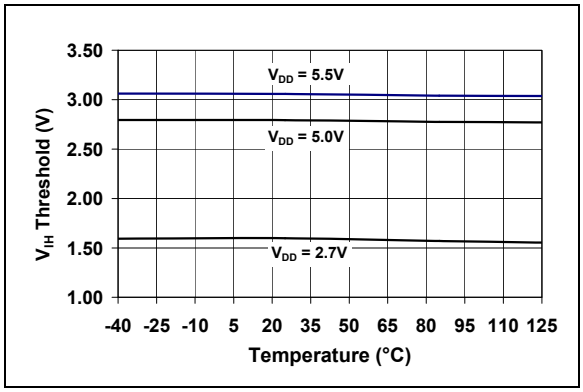


FIGURE 2-17: *V_{IN} High Threshold vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

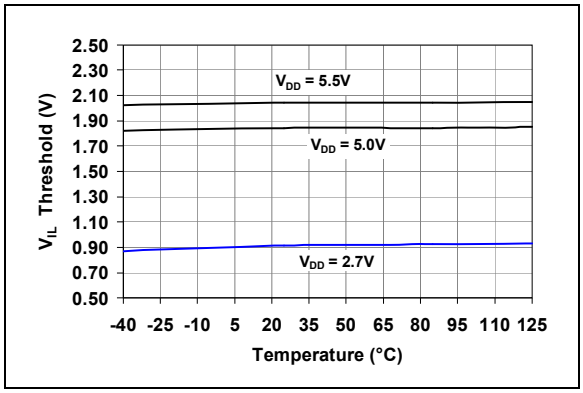


FIGURE 2-18: *V_{IN} Low Threshold vs. Temperature and V_{DD}.*

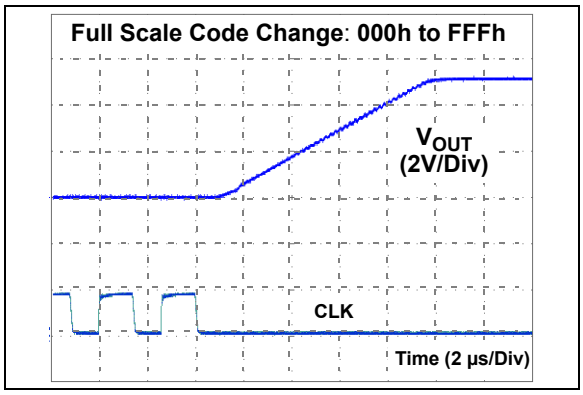


FIGURE 2-19: *Full Scale Settling Time.*

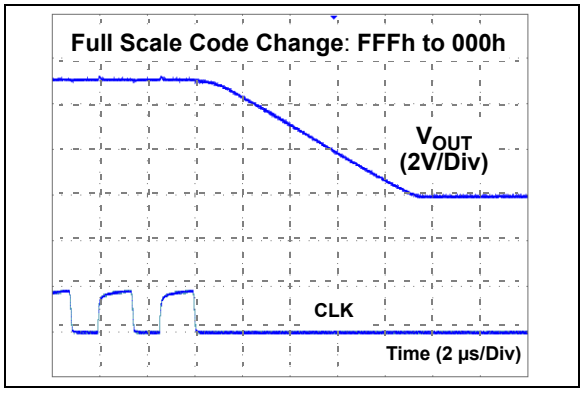


FIGURE 2-20: *Full Scale Settling Time.*

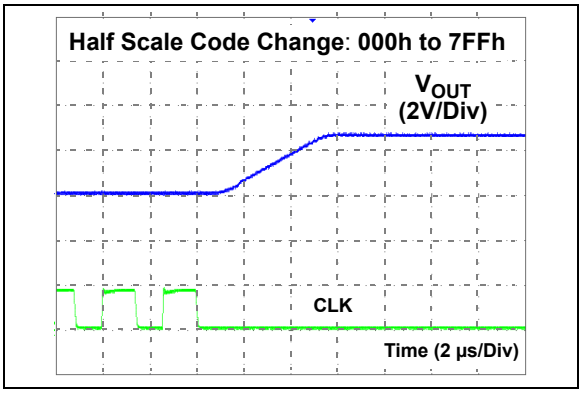


FIGURE 2-21: *Half Scale Settling Time.*

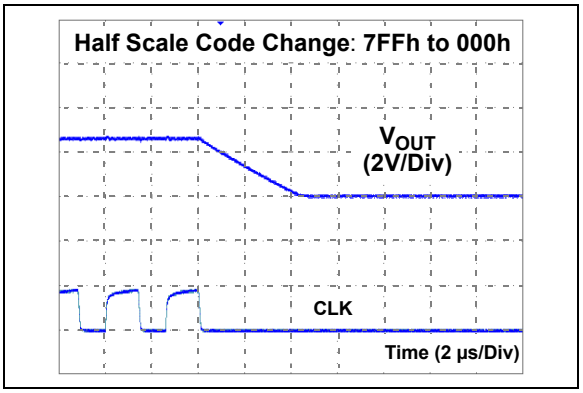


FIGURE 2-22: *Half Scale Settling Time.*

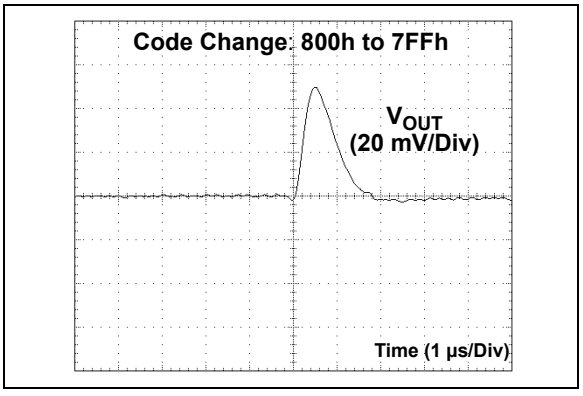


FIGURE 2-23: *Code Change Glitch.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ to V_{SS}, C_L = 100 pF.

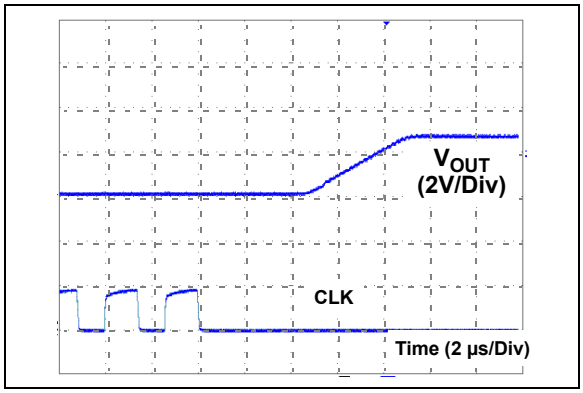


FIGURE 2-24: *Exiting Power Down Mode.*

NOTES:.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP4725 SOT-23	Name	Description
1	V_{OUT}	Analog Output Voltage
2	V_{SS}	Ground Reference
3	V_{DD}	Supply Voltage
4	SDA	I^2C Serial Data
5	SCL	I^2C Serial Clock Input
6	A0	I^2C Address Bit Selection pin (A0 bit). This pin can be tied to V_{SS} or V_{DD}, or can be actively driven by the digital logic levels. The logic state of this pin determines what the A0 bit of the I^2C address bits should be.

3.1 Analog Output Voltage (V_{OUT})

V_{OUT} is an analog output voltage from the DAC device. DAC output amplifier drives this pin with a range of V_{SS} to V_{DD}.

3.2 Supply Voltage (V_{DD} or V_{SS})

V_{DD} is the power supply pin for the device. The voltage at the V_{DD} pin is used as the supply input as well as the DAC reference input. The power supply at the V_{DD} pin should be clean as possible for a good DAC performance.

This pin requires an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in application boards. The supply voltage (V_{DD}) must be maintained in the 2.7V to 5.5V range for specified operation.

V_{SS} is the ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC register and EEPROM data. The SDA pin is an open-drain N-chan nel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin. Except for START and STOP conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 7.0 "I^2C Serial Interface Communication"** for more details of I^2C Serial Interface communication.

3.4 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP4725 acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP4725 occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 7.0 "I^2C Serial Interface Communication"** for more details of I^2C Serial Interface communication.

3.5 Device Address Selection Pin (A0)

This pin is used to select the A0 address bit by the user. The user can tie this pin to V_{SS} (logic '0'), or V_{DD} (logic '1'), or can be actively driven by the digital logic levels, such as the I^2C Master Output. See **Section 7.2 "Device Addressing"** for more details of the address bits.

NOTES:

4.0 TERMINOLOGY

4.1 Resolution

The resolution is the number of DAC output states that divide the full scale range. For the 12-bit DAC, the resolution is 2^{12} or the DAC code ranges from 0 to 4095.

4.2 LSB

The least significant bit or the ideal voltage difference between two successive codes.

EQUATION 4-1:

$$LSB_{Ideal} = \frac{V_{REF}}{2^n} = \frac{(V_{Full\ Scale} - V_{Zero\ Scale})}{2^n - 1}$$

Where:

V_{REF} = The reference voltage = V_{DD} in the MCP4725. This V_{REF} is the ideal full scale voltage range

n = The number of digital input bits. (n = 12 for MCP4725)

4.3 Integral Nonlinearity (INL) or Relative Accuracy

INL error is the maximum deviation between an actual code transition point and its corresponding ideal transition point (straight line). Figure 2-5 shows the INL curve of the MCP4725. The end-point method is used for the calculation. The INL error at a given input DAC code is calculated as:

EQUATION 4-2:

$$INL = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

V_{Ideal} = Code*LSB

V_{OUT} = The output voltage measured at the given input code

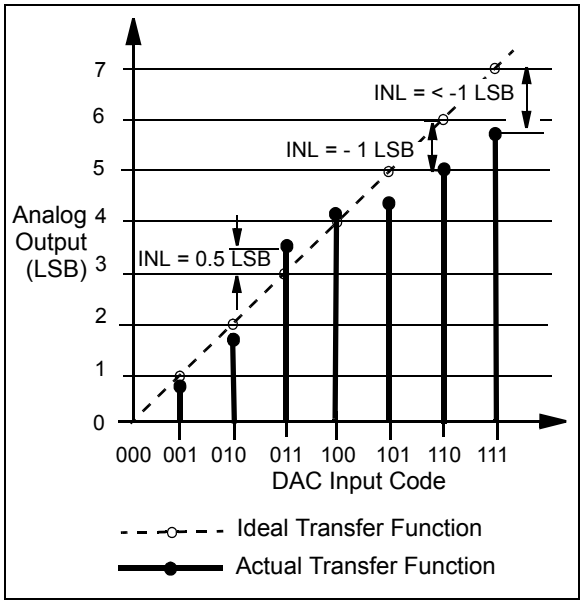


FIGURE 4-1: *INL Accuracy.*

4.4 Differential Nonlinearity (DNL)

Differential nonlinearity error (Figure 4-2) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSB. A DNL error of zero would imply that every code is exactly 1 LSB wide. If the DNL error is less than 1 LSB, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

EQUATION 4-3:

$$DNL = \frac{\Delta V_{OUT} - LSB}{LSB}$$

Where:

ΔV_{OUT} = The measured DAC output voltage difference between two adjacent input codes.

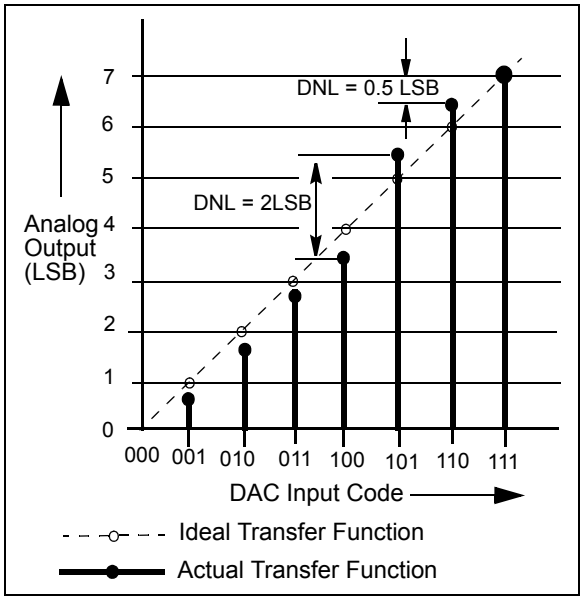


FIGURE 4-2: *DNL Accuracy.*

4.5 Offset Error

Offset error (Figure 4-3) is the deviation from zero voltage output when the digital input code is zero. This error affects all codes by the same amount. In the MCP4725, the offset error is not trimmed at the factory. However, it can be calibrated by software in application circuits.

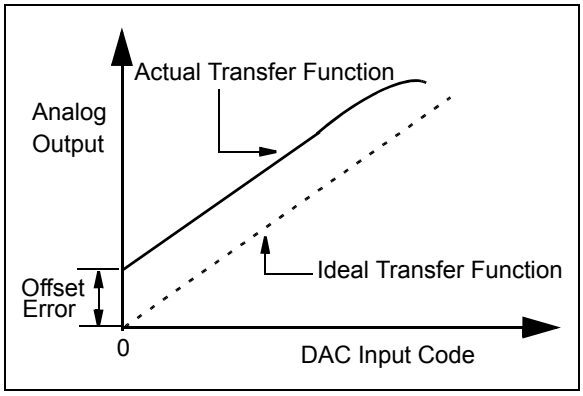


FIGURE 4-3: *Offset Error.*

4.6 Gain Error

Gain error (see Figure 4-4) is the difference between the actual full scale output voltage from the ideal output voltage on the transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full scale range (% of FSR) or in LSB.

In the MCP4725, the gain error is not calibrated at the factory and most of the gain error is contributed by the output op amp saturation near the code range beyond 4000. For the applications which need the gain error specification less than 1% maximum, the user may consider using the DAC code range between 100 and 4000 instead of using full code range (code 0 to 4095). The DAC output of the code range between 100 and 4000 is much linear than full scale range (0 to 4095). The gain error can be calibrated by software in applications.

4.7 Full Scale Error (FSE)

Full scale error (Figure 4-4) is the sum of offset error plus gain error. It is the difference between the ideal and measured DAC output voltage with all bits set to one (DAC input code = FFFh).

EQUATION 4-4:

$$FSE = \frac{(V_{OUT} - V_{Ideal})}{LSB}$$

Where:

V_{Ideal} = $(V_{REF})\ (1 - 2^{-n}) - V_{OFFSET}$

V_{REF} = The reference voltage.
$V_{REF} = V_{DD}$ in the MCP4725

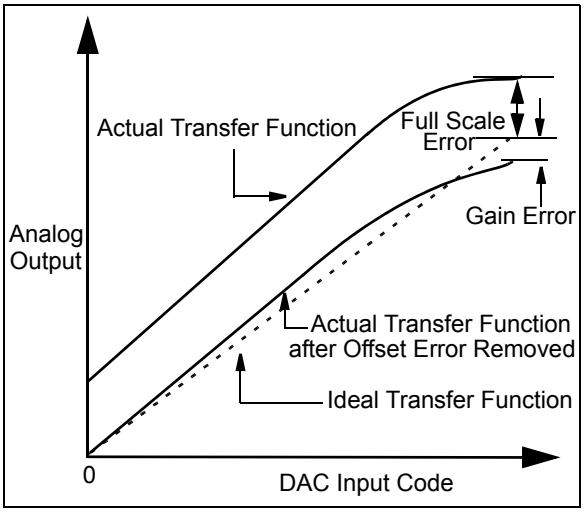


FIGURE 4-4: *Gain Error and Full Scale Error.*

4.8 Gain Error Drift

Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C.

4.9 Offset Error Drift

Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/^{o}C.

4.10 Settling Time

The Settling time is the time delay required for the DAC output to settle to its new output value from the start of code transition, within specified accuracy. In the MCP4725, the settling time is a measure of the time delay until the DAC output reaches its final value (within 0.5 LSB) when the DAC code changes from 400h to C00h.

4.11 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec. and is measured when the digital code is changed by 1 LSB at the major carry transition (Example: 011...111 to 100... 000, or 100... 000 to 011 ... 111).

4.12 Digital Feedthrough

Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. It is specified in nV-Sec. and is measured with a full scale change on the digital input pins (Example: 000... 000 to 111... 111, or 111... 111 to 000... 000). The digital feedthrough is measured when the DAC is not being written to the register.

NOTES:

5.0 GENERAL DESCRIPTION

The MCP4725 is a single channel buffered voltage output 12-bit DAC with non-volatile memory (EEPROM). The user can store configuration register bits (2 bits) and DAC input data (12 bits) in non-volatile EEPROM (14 bits) memory.

When the device is powered on first, it loads the DAC code from the EEPROM and outputs the analog output accordingly with the programmed settings. The user can reprogram the EEPROM or DAC register any time.

The device uses a resistor string architecture. DAC's output is buffered with a low power precision amplifier. This output amplifier provides low offset voltage and low noise, as well as rail-to-rail output. The amplifier can also provide high source currents (V_{OUT} pin to V_{SS}).

The DAC can be configured to normal or power saving power-down mode by setting the configuration register bits.

The device uses a two-wire I^2C compatible serial interface and operates from a single power supply ranging from 2.7V to 5.5V.

5.1 Output Voltage

The input coding to the MCP4725 device is unsigned binary. The output voltage range is from 0V to V_{DD}. The output voltage is given in Equation 5-1:

EQUATION 5-1:

$$V_{OUT} = \frac{(V_{REF} \times D_n)}{4096}$$

Where:

V_{REF} = V_{DD}

D_n = Input code

5.1.1 OUTPUT AMPLIFIER

The DAC output is buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to **Section 1.0 "Electrical Characteristics"** for range and load conditions.

The output amplifier can drive the resistive and high capacitive loads without oscillation. The amplifier can provide maximum load current as high as 25 mA which is enough for most of a programmable voltage reference applications.

5.1.2 DRIVING RESISTIVE AND CAPACITIVE LOADS

The MCP4725 output stage is capable of driving loads up to 1000 pF in parallel with 5 kΩ load resistance. Figure 2-15 shows the V_{OUT} vs. Resistive Load. V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ.

5.2 LSB SIZE

One LSB is defined as the ideal voltage difference between two successive codes. (see Equation 4-1). Table 5-1 shows an example of the LSB size over full scale range (V_{DD}).

TABLE 5-1: LSB SIZES FOR MCP4725 (EXAMPLE)

Full Scale Range (V_{DD})	LSB Size	Condition
3.0V	0.73 mV	3V / 4096
5.0V	1.22 mV	5V / 4096

5.3 Voltage Reference

The MCP4725 device uses the V_{DD} as its voltage reference. Any variation or noises on the V_{DD} line can affect directly on the DAC output. The V_{DD} needs to be as clean as possible for accurate DAC performance.

5.4 Reset Conditions

In the Reset conditions, the device uploads the EEPROM data into the DAC register. The device can be reset by two independent events: (a) by POR or (b) by I^2C General Call Reset Command.

The factory default settings for the EEPROM prior to shipment are shown in Table 5-3 (set for a middle scale output). The user can rewrite or read the DAC register or EEPROM anytime after the Power-On-Reset event.

5.4.1 POWER-ON-RESET

The device's internal Power-On-Reset (POR) circuit ensures that the device powers up in a defined state.

If the power supply voltage is less than the POR threshold (V_{POR} = 2V, typical), all circuits are disabled and there will be no DAC output. When the V_{DD} increases above the V_{POR}, the device takes a reset state. During the reset period, the device uploads all configuration and DAC input codes from EEPROM. The DAC output will be the same as for the value last stored in the EEPROM. This enables the device returns to the same state that it was at the last write to the EEPROM before it was powered off.

5.4.2 V_{DD} RAMP RATE AND EEPROM

The MCP4725 uploads the EEPROM data to the DAC register during power-up sequence. However, if the V_{DD} ramp rate is too slow (<1 V/ms), the device may not be able to load the EEPROM data to the DAC register. Therefore, the DAC output that is corresponding to the current EEPROM data may not available to the output pin. It is highly recommended to send a General Call Reset Command (see **Section 7.3.1 "General call reset"**) after power-up. This command will reset the device at a stable V_{DD} and make the DAC output available immediately using the EEPROM data.

5.5 Normal and Power-Down Modes

The device has two modes of operation: Normal mode and power-down mode. The mode is selected by programming the power-down bits (PD1 and PD0) in the Configuration register. The user can also program the two power-down bits in non-volatile EEPROM memory.

When the normal mode is selected, the device operates a normal digital-to-analog conversion. If the power-down mode is selected, the device enters a power saving condition by shutting down most of the internal circuits. During the power-down mode, all internal circuits except the I^2C interface are disabled and there is no data conversion event, and no V_{OUT} is available. The device also switches the output stage from the output of the amplifier to a known resistive load. The value of the resistive load is determined by the state of the power-down bits (PD1 and PD0). Table 5-2 shows the outcome of the power-down bit and the resistive load.

During the power-down mode, the device draws about 60 nA (typical). Although most of internal circuits are shutdown, the serial interface remains active in order to receive the I^2C command.

The device exits the power-down mode immediately when (a) it receives a new write command for normal mode or (b) it receives an I^2C General Call Wake-Up Command.

When the DAC operation mode is changed from power-down to normal mode, the output settling time takes less than 10 µs, but greater than the standard Active mode settling time (6 µs, typical).

TABLE 5-2: POWER-DOWN BITS

PD1	PD0	Function
0	0	Normal Mode
0	1	1 kΩ resistor to ground (1)
1	0	100 kΩ resistor to ground (1)
1	1	500 kΩ resistor to ground (1)

Note 1: In the power-down mode: V_{OUT} is off and most of internal circuits are disabled.

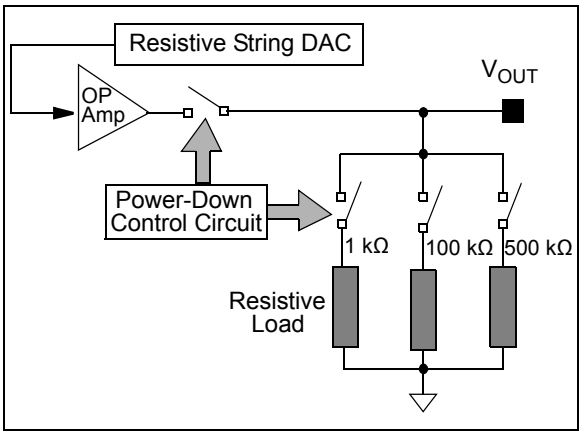


FIGURE 5-1: *Output Stage for Power-Down Mode.*

5.6 Non-Volatile EEPROM Memory

The MCP4725 device has a 14-bit wide EEPROM memory to store configuration bit (2 bits) and DAC input data (12 bits). These bits are readable and re-writable with I^2C interface commands. The device has an on-chip charge pump circuit to write the EEPROM memory bits without using an external program voltage.

The EEPROM writing operation is initiated when the device receives an EEPROM write command (C2 = 0, C1 = 1, C0 = 1). The configuration and writing data bits are transferred to the EEPROM memory block. A status bit, RDY/$\overline{BSY}$, stays low during the EEPROM writing and goes high as the write operation is completed. While the RDY/$\overline{BSY}$ bit is low (during the EEPROM writing), any new write command is ignored (for EEPROM or DAC register). Table 5-3 shows the EEPROM bits and factory default settings. Table 5-4 shows the DAC input register bits of the MCP4725.

TABLE 5-3: EEPROM MEMORY AND FACTORY DEFAULT SETTINGS (TOTAL NUMBER OF BITS: 14 BITS)

Bit Name	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Power-Down Select (2 bits)		DAC Input Data (12 bits)											
Factory Default Value	0	0 (1)	1 (2)	0	0	0	0	0	0	0	0	0	0	0

Note 1: See Table 5-2 for details.

2: Bit D11 = '1' (while all other bits are "0") enables the device to output 0.5 * V_{DD} (= middle scale output).

TABLE 5-4: DAC REGISTER

Bit Name	C2	C1	C0	RDY/$\overline{BSY}$	POR	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	Command Type			(1)		Power-Down Select		Data (12 bits)											

Note 1: Write EEPROM status indication bit (0:EEPROM write is not completed. 1:EEPROM write is complete.)

NOTES:

6.0 THEORY OF OPERATION

When the device is connected to the I^2C bus line, the device is working as a slave device. The Master (MCU) can write/read the DAC input register or EEPROM using the I^2C interface command. The MCP4725 device address contains four fixed bits (1100 = device code) and three address bits (A2, A1, A0). The A2 and A1 bits are hard-wired during manufacturing, and A0 bit is determined by the logic state of A0 pin. The A0 pin can be connected to V_{DD} or V_{SS}, or actively driven by digital logic levels.

The following sections describe the communication protocol to send or read the data code and write/read the EEPROM using the I^2C interface. See **Section 7.0 "I^2C Serial Interface Communication"**.

6.1 Write Commands

The write commands are used to load the configuration bits and DAC input code to the DAC register, or to write to the EEPROM of the device. The write command types are defined by using three write command type bits (C2, C1, C0). Table 6-2 shows the write command types and their functions. There are three command types for the MCP4725. The four "reserved" commands in Table 6-2 are for future use. The MCP4725 ignores the "reserved" commands. Write command protocol examples are shown in Figure 6-1 and Figure 6-2.

The input data code is coded as shown in Table 6-1. The MSB of the data is always transmitted first and the format is unipolar binary.

TABLE 6-1: INPUT DATA CODING

Input Code	Nominal Output Voltage (V)
111111111111 (FFFh)	V_{DD} - 1 LSB
111111111110 (FFEh)	V_{DD} - 2 LSB
000000000010 (002h)	2 LSB
000000000001 (001h)	1 LSB
000000000000 (000h)	0

6.1.1 WRITE COMMAND FOR FAST MODE (C2 = 0, C1 = 0, C0 = X, X = DON'T CARE)

The fast write command is used to update the DAC register. The data in the EEPROM of the device is not affected by this command. This command updates Power-Down mode selection bits (PD1 and PD0) and 12 bits of the DAC input code in the DAC register. Figure 6-1 shows an example of the fast write command for the MCP4725 device.

6.1.2 WRITE COMMAND FOR DAC INPUT REGISTER (C2 = 0, C1 = 1, C0 = 0)

In MCP4725, this command performs the same function as the Fast Mode command in **Section 6.1.1 "Write Command for Fast mode (C2 = 0, C1 = 0, C0 = X, X = Don't Care)"**. Figure 6-2 shows the write command protocol for the MCP4725.

As shown in Figure 6-2, the D11 - D0 bits in the third and fourth bytes are DAC input data. The last 4 bits (X, X, X, X) in the fourth byte are don't care bits.

The device executes the Master's write command after receiving the last byte (4th byte). The Master can send a STOP bit to terminate the current sequence, or send a Repeated START bit followed by an address byte. If the device receives three data bytes continuously after the 4th byte, it updates from the 2nd to the 4th data bytes with the last three input data bytes.

The contents of the register are updated at the end of the 4th byte. The device ignores any partially received data bytes if the I^2C communication with the Master ends before completing the 4th byte.

6.1.3 WRITE COMMAND FOR DAC INPUT REGISTER AND EEPROM (C2 = 0, C1 = 1, C0 = 1)

When the device receives this command, it (a) loads the configuration and data bits to the DAC register, and (b) also writes the EEPROM. When the device is writing the EEPROM, the RDY/$\overline{BSY}$ bit goes low and stays low until the EEPROM write operation is completed. The state of the RDY/$\overline{BSY}$ bit can be monitored by a read command. Figure 6-2 shows the details of the this write command protocol and Figure 6-3 shows the details of the read command.

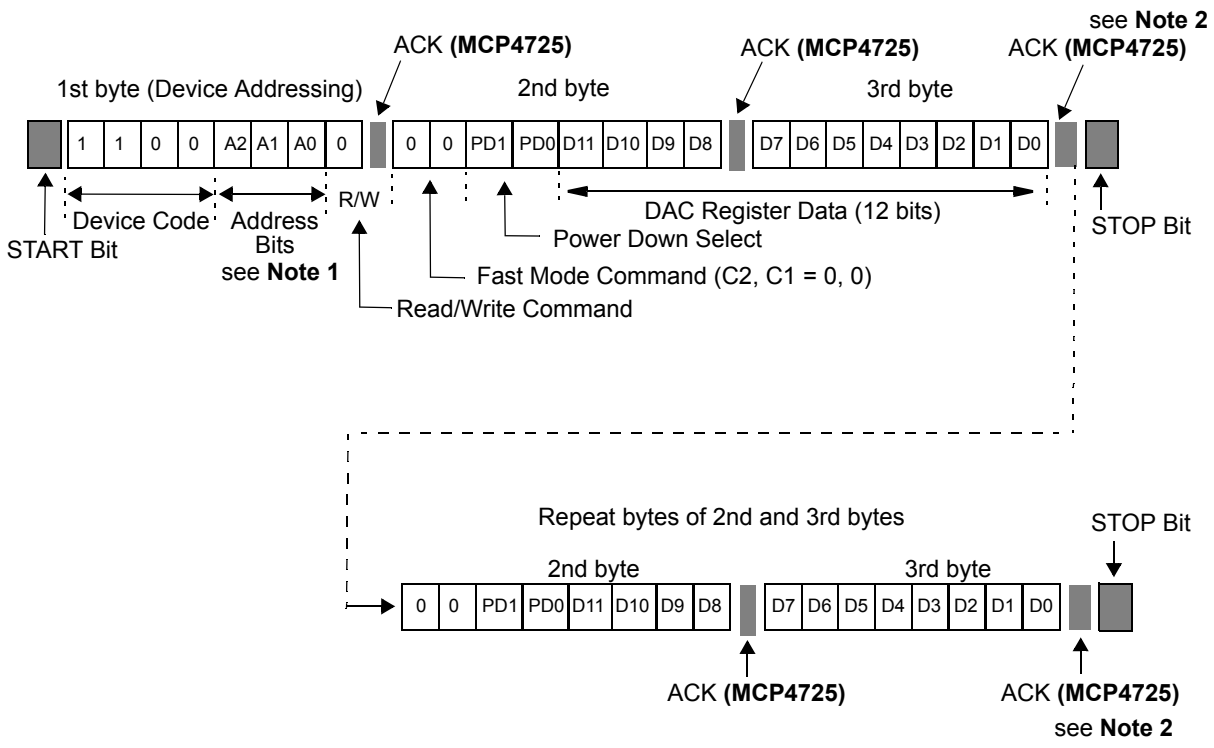
TABLE 6-2: WRITE COMMAND TYPE

C2	C1	C0	Command Name	Function
0	0	X	Fast Mode	This command is used to change the DAC register. EEPROM is not affected
0	0	X	“	“
0	1	0	Write DAC Register	Load configuration bits and data code to the DAC Register
0	1	1	Write DAC Register and EEPROM	(a) Load configuration bits and data code to the DAC Register and (b) also write the EEPROM
1	0	0	Reserved	Reserved for future use
1	0	1	Reserved	Reserved for future use
1	1	0	Reserved	Reserved for future use
1	1	1	Reserved	Reserved for future use

Note 1: X = Dont’ Care. Fast Mode does not use C0 bit.

2: The MCP4725 ignores the “Reserved” commands.

Write DAC Register using Fast Mode Write Command: (C2, C1) = (0, 0)



Note 1: A2 and A1 bits are programmed at the factory by hard-wired, and A0 bit is determined by the logic state of A0 pin.

2: The device updates V_{OUT} at the falling edge of the ACK pulse of the 3rd byte.

FIGURE 6-1: *Fast Mode Write Command.*

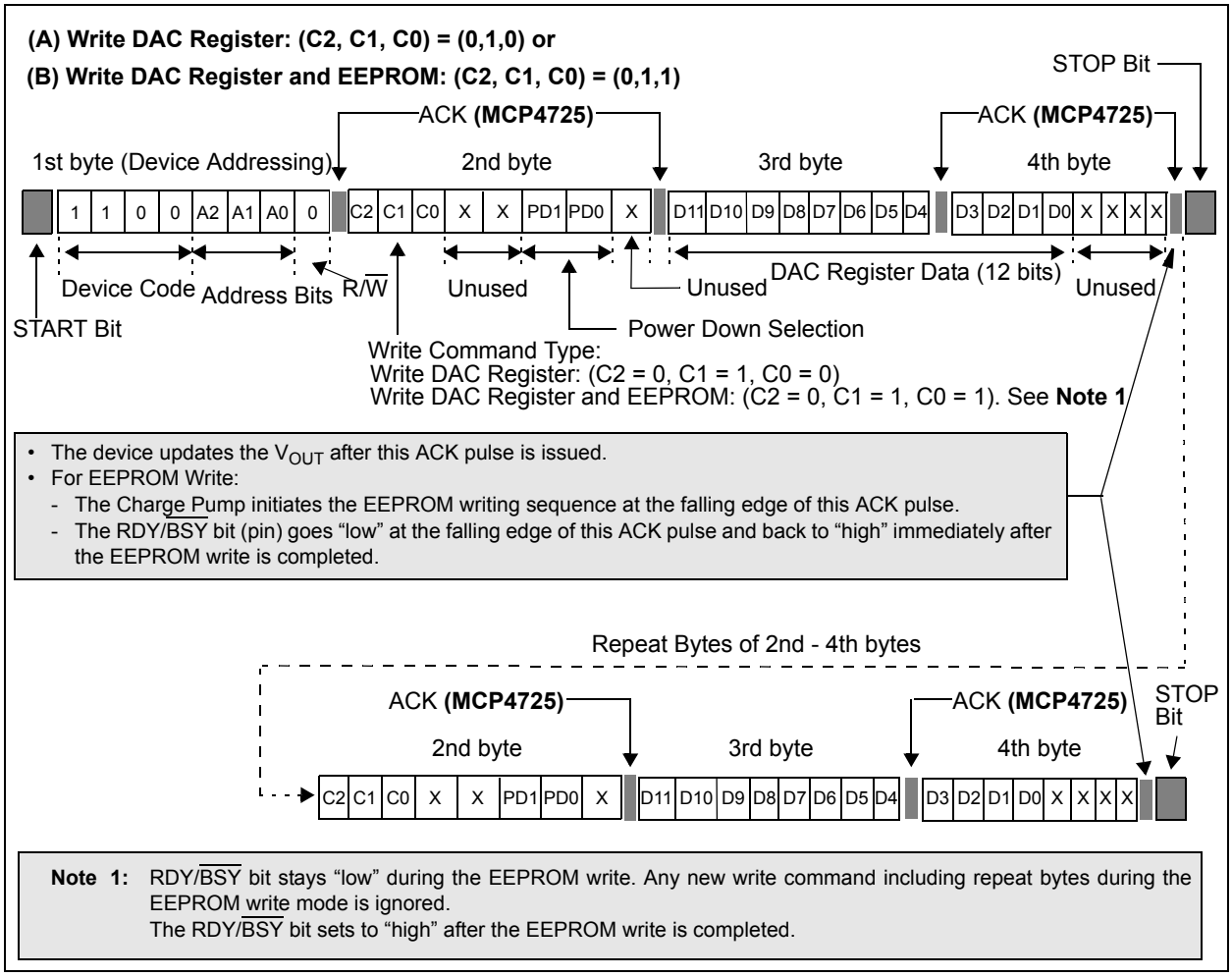


FIGURE 6-2: *Write Commands for DAC Input Register and EEPROM.*