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MCP4728

12-Bit, Quad Digital-to-Analog Converter with EEPROM Memory

Features

- 12-Bit Voltage Output DAC with Four Buffered Outputs
- On-Board Nonvolatile Memory (EEPROM) for DAC Codes and I²C™ Address Bits
- Internal or External Voltage Reference Selection
- Output Voltage Range:
  - Using Internal V_{REF} (2.048V):
    0.000V to 2.048V with Gain Setting = 1
    0.000V to 4.096V with Gain Setting = 2
  - Using External V_{REF} (V_{DD}):
    0.000V to V_{DD}
- ±0.2 Least Significant Bit (LSB) Differential Nonlinearity (DNL) (typical)
- Fast Settling Time: 6 µs (typical)
- Normal or Power-Down Mode
- Low Power Consumption
- Single-Supply Operation: 2.7V to 5.5V
- I²C Interface:
  - Address bits: User Programmable to EEPROM
  - Standard (100 kbps), Fast (400 kbps) and High Speed (HS) Mode (3.4 Mbps)
- 10-Lead MSOP Package
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Adjustment
- Sensor Calibration
- Closed-Loop Servo Control
- Low Power Portable Instrumentation
- PC Peripherals
- Programmable Voltage and Current Source
- Industrial Process Control
- Instrumentation
- Bias Voltage Adjustment for Power Amplifiers

Description

The MCP4728 device is a quad, 12-bit voltage output Digital-to-Analog Convertor (DAC) with nonvolatile memory (EEPROM). Its on-board precision output amplifier allows it to achieve rail-to-rail analog output swing.

The DAC input codes, device configuration bits, and I²C address bits are programmable to the nonvolatile memory (EEPROM) by using I²C serial interface commands. The nonvolatile memory feature enables the DAC device to hold the DAC input codes during power-off time, allowing the DAC outputs to be available immediately after power-up with the saved settings. This feature is very useful when the DAC device is used as a supporting device for other devices in the application's network.

The MCP4728 device has a high precision internal voltage reference (V_{REF} = 2.048V). The user can select the internal reference or external reference (V_{DD}) for each channel individually.

Each channel can be operated in Normal mode or Power-Down mode individually by setting the configuration register bits. In Power-Down mode, most of the internal circuits in the powered down channel are turned off for power savings, and the output amplifier can be configured to present a known low, medium, or high resistance output load.

The MCP4728 device includes a Power-on Reset (POR) circuit to ensure reliable power-up and an on-board charge pump for the EEPROM programming voltage.

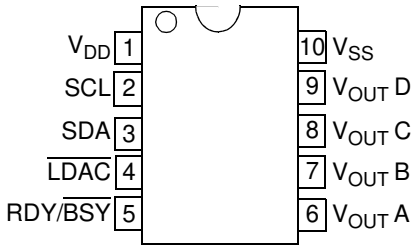
The MCP4728 has a two-wire I²C compatible serial interface for standard (100 kHz), fast (400 kHz), or high speed (3.4 MHz) mode.

The MCP4728 DAC is an ideal device for applications requiring design simplicity with high precision, and for applications requiring the DAC device settings to be saved during power-off time.

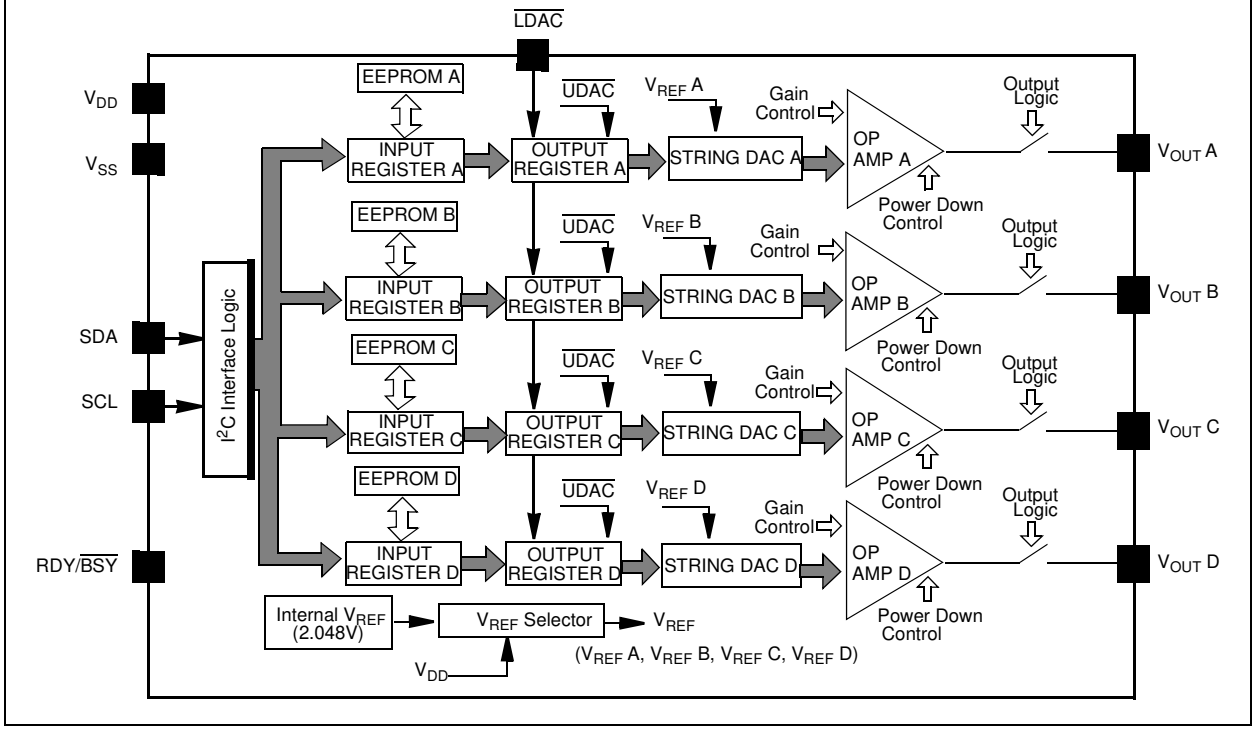
The MCP4728 device is available in a 10-lead MSOP package and operates from a single 2.7V to 5.5V supply voltage.

Package Type

MCP4728
MSOP



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....6.5V
All inputs and outputs w.r.t V_{SS} ..... -0.3V to V_{DD}+0.3V
Current at Input Pins .....±2 mA
Current at Supply Pins .....±110 mA
Current at Output Pins .....±25 mA
Storage Temperature .....-65°C to +150°C
Ambient Temp. with Power Applied .....-55°C to +125°C
ESD protection on all pins ..... ≥ 4 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T_J) .....+150°C

† Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, V_{IH} = V_{DD}, V_{IL} = V_{SS}.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Supply Current with External Reference (V_{REF} = V_{DD}) **(Note 1)**	I_{DD_EXT}	—	800	1400	µA	V_{REF} = V_{DD}, V_{DD} = 5.5V All 4 channels are in Normal mode.
		—	600	—	µA	3 channels are in Normal mode, 1 channel is powered down.
		—	400	—	µA	2 channels are in Normal mode, 2 channel are powered down.
		—	200	—	µA	1 channel is in Normal mode, 3 channels are powered down.
Power-Down Current with External Reference	I_{PD_EXT}	—	40	—	nA	All 4 channels are powered down. (V_{REF} = V_{DD})
Supply Current with Internal Reference (V_{REF} = Internal) **(Note 1)**	I_{DD_INT}	—	800	1400	µA	V_{REF} = Internal Reference V_{DD} = 5.5V All 4 channels are in normal mode.
		—	600	—	µA	3 channels are in Normal mode, 1 channel is powered down.
		—	400	—	µA	2 channels are in Normal mode, 2 channels are powered down.
		—	200	—	µA	1 channel is in Normal mode, 3 channels are powered down.
Power-Down Current with Internal Reference	I_{PD_INT}	—	45	60	µA	All 4 channels are powered down. V_{REF} = Internal Reference

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to "High", Output pins are unloaded, code = 0 x 000.
2: The power-up ramp rate measures the rise of V_{DD} over time.
3: This parameter is ensured by design and not 100% tested.
4: This parameter is ensured by characterization and not 100% tested.
5: Test code range: 100 - 4000 codes, V_{REF} = V_{DD}, V_{DD} = 5.5V.
6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.
7: This parameter is indirectly tested by Offset and Gain error testing.
8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.
9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Power-on Reset Threshold Voltage	V_{POR}	—	2.2	—	V	All circuits, including EEPROM, are ready to operate.
Power-Up Ramp Rate	V_{RAMP}	1	—	—	V/s	**Note 2**, **Note 4**
DC Accuracy						
Resolution	n	12	—	—	Bits	Code Change: 000h to FFFh
Integral Nonlinearity (INL) Error	INL	—	±2	±13	LSB	**Note 5**
DNL Error	DNL	-0.75	±0.2	±0.75	LSB	**Note 5**
Offset Error	V_{OS}	—	5	20	mV	Code = 000h See Figure 2-24
Offset Error Drift	ΔV_{OS}/°C	—	±0.16	—	ppm/°C	-45°C to +25°C
		—	±0.44	—	ppm/°C	+25°C to +125°C
Gain Error	G_E	-1.25	0.4	+1.25	% of FSR	Code = FFFh, Offset error is not included. Typical value is at room temperature See Figure 2-25
Gain Error Drift	ΔG_E/°C	—	-3	—	ppm/°C	
Internal Voltage Reference (V_{REF}), (Note 3)						
Internal Voltage Reference	V_{REF}	2.007	2.048	2.089	V	
Temperature Coefficient	ΔV_{REF}/°C	—	125	—	ppm/°C	-40 to 0°C
		—	0.25	—	LSB/°C	
		—	45	—	ppm/°C	0 to +125°C
		—	0.09	—	LSB/°C	
Reference Output Noise	E_{NREF}	—	290	—	μV_{p-p}	Code = FFFh, 0.1 – 10 Hz, G_x = 1
Output Noise Density	e_{NREF}	—	1.2	—	$\mu V/\sqrt{Hz}$	Code = FFFh, 1 kHz, G_x = 1
		—	1.0	—		Code = FFFh, 10 kHz, G_x = 1
1/f Corner Frequency	f_{CORNER}	—	400	—	Hz	

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to “High”, Output pins are unloaded, code = 0 x 000.

2: The power-up ramp rate measures the rise of V_{DD} over time.

3: This parameter is ensured by design and not 100% tested.

4: This parameter is ensured by characterization and not 100% tested.

5: Test code range: 100 - 4000 codes, $V_{REF} = V_{DD}$, V_{DD} = 5.5V.

6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.

7: This parameter is indirectly tested by Offset and Gain error testing.

8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.

9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, V_{IH} = V_{DD}, V_{IL} = V_{SS}.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Analog Output (Output Amplifier)						
Output Voltage Swing	V_{OUT}	—	FSR	—	V	**Note 7**
Full Scale Range **(Note 7)**	FSR	—	V_{DD}	—	V	V_{REF} = V_{DD} FSR = from 0.0V to V_{DD}
		—	V_{REF}	—	V	V_{REF} = Internal, G_x = 1, FSR = from 0.0 V to V_{REF}
		—	2 * V_{REF}	—	V	V_{REF} = Internal, G_x = 2, FSR = from 0.0V to 2 * V_{REF}
Output Voltage Settling Time	$T_{SETTLING}$	—	6	—	µs	**Note 8**
Analog Output Time Delay from Power-Down Mode	Td_{EXPD}	—	4.5	—	µs	V_{DD} = 5V, **Note 4**, **Note 9**
Time delay to settle to new reference **(Note 4, Note 6)**	Td_{REF}	—	26	—	µs	From External to Internal Reference
		—	44	—	µs	From Internal to External Reference
Power Supply Rejection	PSRR	—	-57	—	dB	V_{DD} = 5V ±10%, V_{REF} = Internal
Capacitive Load Stability	C_L	—	—	1000	pF	R_L = 5 kΩ No oscillation, **Note 4**
Slew Rate	SR	—	0.55	—	V/µs	
Phase Margin	p_M	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Short Circuit Current	I_{SC}	—	15	24	mA	V_{DD} = 5V, All V_{OUT} Pins = Grounded. Tested at room temperature.
Short Circuit Current Duration	T_{SC_DUR}	—	Infinite	—	hours	**Note 4**
DC Output Impedance **(Note 4)**	R_{OUT}	—	1	—	Ω	Normal mode
		—	1	—	kΩ	Power-Down mode 1 (PD1:PD0 = 0:1), V_{OUT} to V_{SS}
		—	100	—	kΩ	Power-Down mode 2 (PD1:PD0 = 1:0), V_{OUT} to V_{SS}
		—	500	—	kΩ	Power-Down mode 3 (PD1:PD0 = 1:1), V_{OUT} to V_{SS}

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to "High", Output pins are unloaded, code = 0 x 000.

2: The power-up ramp rate measures the rise of V_{DD} over time.

3: This parameter is ensured by design and not 100% tested.

4: This parameter is ensured by characterization and not 100% tested.

5: Test code range: 100 - 4000 codes, V_{REF} = V_{DD}, V_{DD} = 5.5V.

6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.

7: This parameter is indirectly tested by Offset and Gain error testing.

8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.

9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF, G_X = 1, T_A = -40°C to +125°C. Typical values are at +25°C, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$.

Parameter	Symbol	Min	Typical	Max	Units	Conditions
Dynamic Performance (Note 4)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSB code change around major carry (from 7FFh to 800h)
Digital Feedthrough		—	<10	—	nV-s	
Analog Crosstalk		—	<10	—	nV-s	
DAC-to-DAC Crosstalk		—	<10	—	nV-s	
Digital Interface						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA SDA and RDY/$\overline{BSY}$ pins
Schmitt Trigger Low Input Threshold Voltage	V_{IL}	—	—	$0.3V_{DD}$	V	V_{DD} > 2.7V. SDA, SCL, $\overline{LDAC}$ pins
		—	—	$0.2V_{DD}$	V	$V_{DD} \leq$ 2.7V. SDA, SCL, $\overline{LDAC}$ pins
Schmitt Trigger High Input Threshold Voltage	V_{IH}	$0.7V_{DD}$	—	—	V	SDA, SCL, $\overline{LDAC}$ pins
Input Leakage	I_{LI}	—	—	±1	µA	SCL = SDA = $\overline{LDAC}$ = V_{DD}, SCL = SDA = $\overline{LDAC}$ = V_{SS}
Pin Capacitance	C_{PIN}	—	—	3	pF	**Note 4**
EEPROM						
EEPROM Write Time	TWRITE	—	25	50	ms	EEPROM write time
Data Retention		—	200	—	Years	At +25°C, **Note 3**
$\overline{LDAC}$ Input						
$\overline{LDAC}$ Low Time	$T_{\overline{LDAC}}$	210	—	—	ns	Updates analog outputs **(Note 3)**

Note 1: All digital input pins (SDA, SCL, $\overline{LDAC}$) are tied to "High", Output pins are unloaded, code = 0 x 000.

2: The power-up ramp rate measures the rise of V_{DD} over time.

3: This parameter is ensured by design and not 100% tested.

4: This parameter is ensured by characterization and not 100% tested.

5: Test code range: 100 - 4000 codes, $V_{REF} = V_{DD}$, V_{DD} = 5.5V.

6: Time delay to settle to a new reference when switching from external to internal reference or vice versa.

7: This parameter is indirectly tested by Offset and Gain error testing.

8: Within 1/2 LSB of the final value when code changes from 1/4 of to 3/4 of full scale.

9: This time delay is measured from the falling edge of ACK pulse in I^2C command to the beginning of V_{OUT}. This time delay is not included in the output settling time specification.

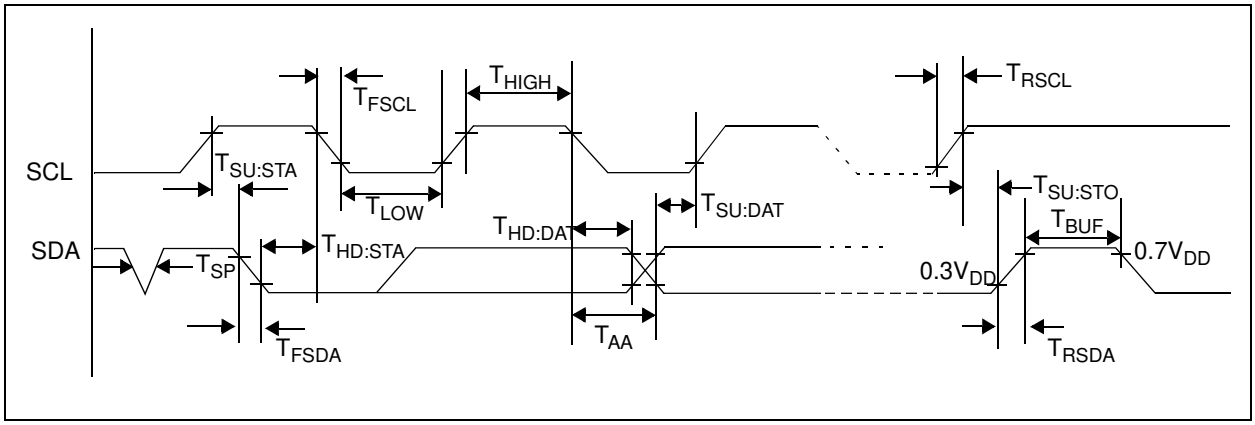


FIGURE 1-1: *I^2C Bus Timing Data.*

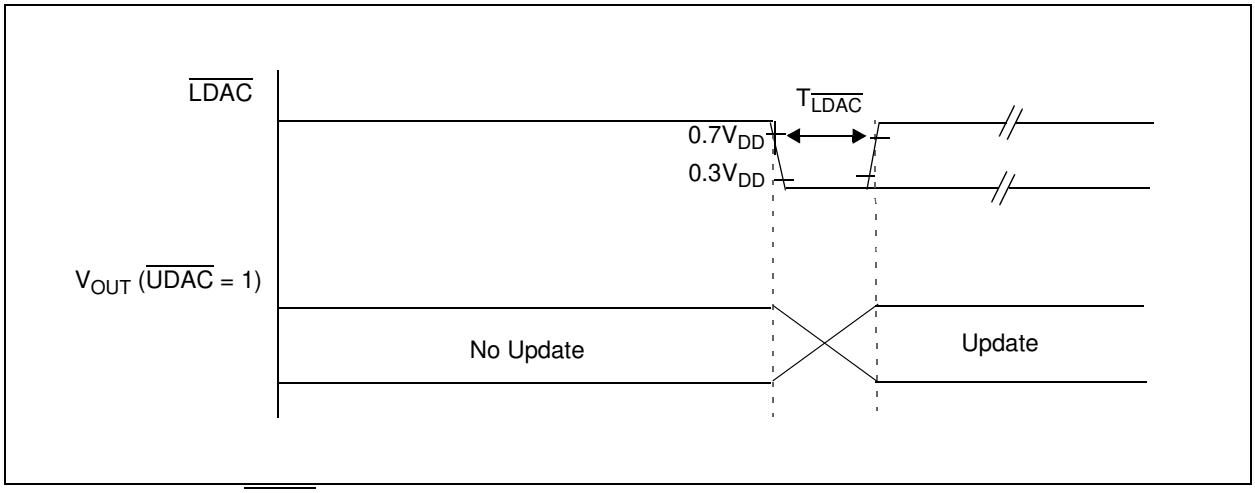


FIGURE 1-2: *$\overline{LDAC}$ Pin Timing vs. V_{OUT} Update.*

I²C SERIAL TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +125°C, V_{SS} = 0V,
Standard and Fast Mode: V_{DD} = +2.7V to +5.5V
High Speed Mode: V_{DD} = +4.5V to +5.5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	f_{SCL}	0	—	100	kHz	Standard Mode C_b = 400 pF, 2.7V – 5.5V
		0	—	400	kHz	Fast Mode C_b = 400 pF, 2.7V – 5.5V
		0	—	1.7	MHz	High Speed Mode 1.7 C_b = 400 pF, 4.5V – 5.5V
		0	—	3.4	MHz	High Speed Mode 3.4 C_b = 100 pF, 4.5V – 5.5V
Bus Capacitive Loading	Cb	—	—	400	pF	Standard Mode 2.7V – 5.5V
		—	—	400	pF	Fast Mode 2.7V – 5.5V
		—	—	400	pF	High Speed Mode 1.7 4.5V – 5.5V
		—	—	100	pF	High Speed Mode 3.4 4.5V – 5.5V
Start Condition Setup Time (Start, Repeated Start)	$T_{SU:STA}$	4700		—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		160	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4
Start Condition Hold Time	$T_{HD:STA}$	4000		—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		160	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4
Stop Condition Setup Time	$T_{SU:STO}$	4000		—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		160	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4
Clock High Time	T_{HIGH}	4000	—	—	ns	Standard Mode
		600	—	—	ns	Fast Mode
		120	—	—	ns	High Speed Mode 1.7
		60	—	—	ns	High Speed Mode 3.4
Clock Low Time	T_{LOW}	4700	—	—	ns	Standard Mode
		1300	—	—	ns	Fast Mode
		320	—	—	ns	High Speed Mode 1.7
		160	—	—	ns	High Speed Mode 3.4

Note 1: This parameter is ensured by characterization and is not 100% tested.

2: After a Repeated Start condition or an Acknowledge bit.

3: If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

4: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (OR T_{RSDA}).

5: Time between Start and Stop conditions.

I²C SERIAL TIMING SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +125°C, V_{SS} = 0V,
Standard and Fast Mode: V_{DD} = +2.7V to +5.5V
High Speed Mode: V_{DD} = +4.5V to +5.5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
SCL Rise Time (Note 1)	T_{RSCL}	—	—	1000	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	80	ns	High Speed Mode 1.7
		20	—	160	ns	High Speed Mode 1.7 (Note 2)
		10	—	40	ns	High Speed Mode 3.4
		10	—	80	ns	High Speed Mode 3.4 (Note 2)
SDA Rise Time (Note 1)	T_{RSDA}	—	—	1000	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	80	ns	High Speed Mode 1.7
		10	—	40	ns	High Speed Mode 3.4
SCL Fall Time (Note 1)	T_{FSCL}	—	—	300	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	80	ns	High Speed Mode 1.7
		10	—	40	ns	High Speed Mode 3.4
SDA Fall Time (Note 1)	T_{FSDA}	—	—	300	ns	Standard Mode
		20 + 0.1Cb	—	300	ns	Fast Mode
		20	—	160	ns	High Speed Mode 1.7
		10	—	80	ns	High Speed Mode 3.4
Data Input Setup Time	$T_{SU:DAT}$	250	—	—	ns	Standard Mode
		100	—	—	ns	Fast Mode
		10	—	—	ns	High Speed Mode 1.7
		10	—	—	ns	High Speed Mode 3.4
Data Hold Time (Input, Output) (Note 3)	$T_{HD:DAT}$	0	—	3450	ns	Standard Mode
		0	—	900	ns	Fast Mode
		0	—	150	ns	High Speed Mode 1.7
		0	—	70	ns	High Speed Mode 3.4
Output Valid from Clock (Note 4)	T_{AA}	0	—	3750	ns	Standard Mode
		0	—	1200	ns	Fast Mode
		0	—	310	ns	High Speed Mode 1.7
		0	—	150	ns	High Speed Mode 3.4

Note 1: This parameter is ensured by characterization and is not 100% tested.

2: After a Repeated Start condition or an Acknowledge bit.

3: If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

4: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (OR T_{RSDA}).

5: Time between Start and Stop conditions.

I²C SERIAL TIMING SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +125°C, V_{SS} = 0V,
Standard and Fast Mode: V_{DD} = +2.7V to +5.5V
High Speed Mode: V_{DD} = +4.5V to +5.5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Bus Free Time (Note 5)	T_{BUF}	4700	—	—	ns	Standard Mode
		1300	—	—	ns	Fast Mode
		—	—	—	ns	High Speed Mode 1.7
		—	—	—	ns	High Speed Mode 3.4
Input Filter Spike Suppression (SDA and SCL) **(Not Tested)**	T_{SP}	—	—	—	ns	Standard Mode (Not Applicable)
		—	50	—	ns	Fast Mode
		—	10	—	ns	High Speed Mode 1.7
		—	10	—	ns	High Speed Mode 3.4

Note 1: This parameter is ensured by characterization and is not 100% tested.

2: After a Repeated Start condition or an Acknowledge bit.

3: If this parameter is too short, it can create an unintentional Start or Stop condition to other devices on the I²C bus line. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
Data Input: This parameter must be longer than t_{SP}.
Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

4: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_{FSDA}$ (OR T_{RSDA}).

5: Time between Start and Stop conditions.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

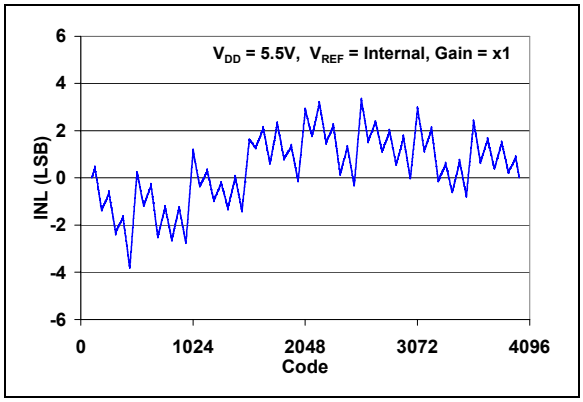


FIGURE 2-1: *INL vs. Code (T_A = +25°C).*

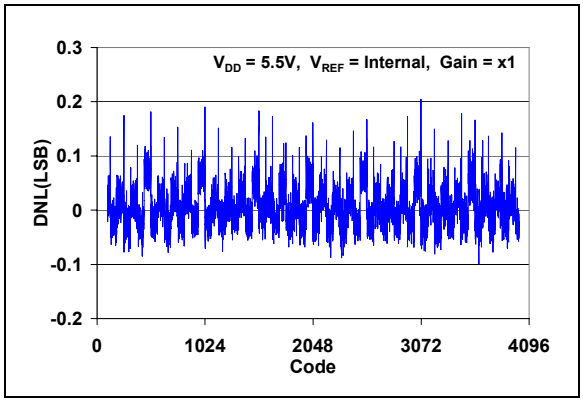


FIGURE 2-4: *DNL vs. Code (T_A = +25°C).*

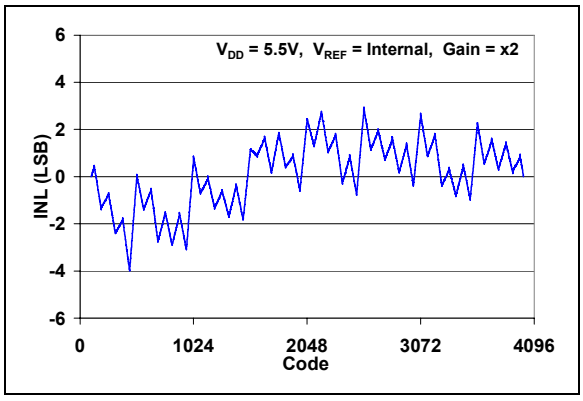


FIGURE 2-2: *INL vs. Code (T_A = +25°C).*

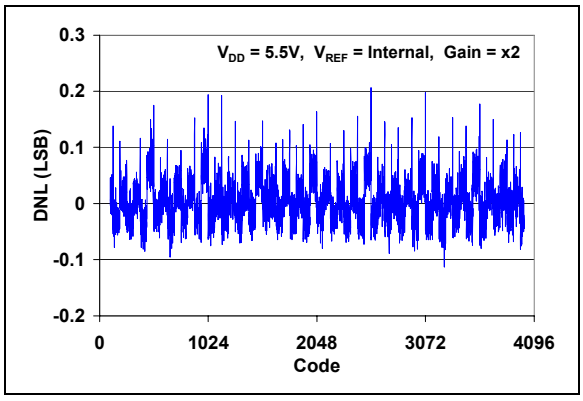


FIGURE 2-5: *DNL vs. Code (T_A = +25°C).*

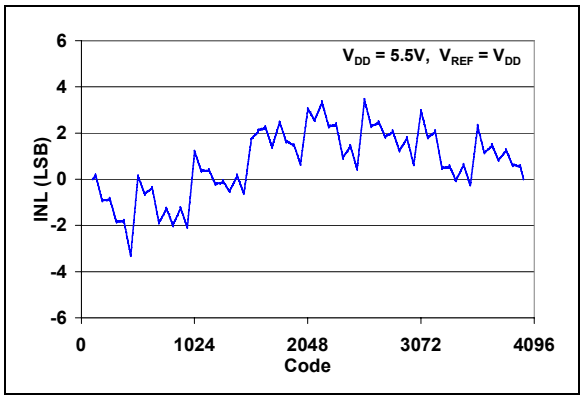


FIGURE 2-3: *INL vs. Code (T_A = +25°C).*

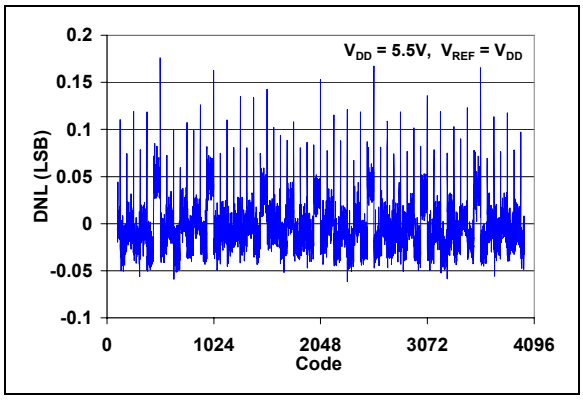


FIGURE 2-6: *DNL vs. Code (T_A = +25°C).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

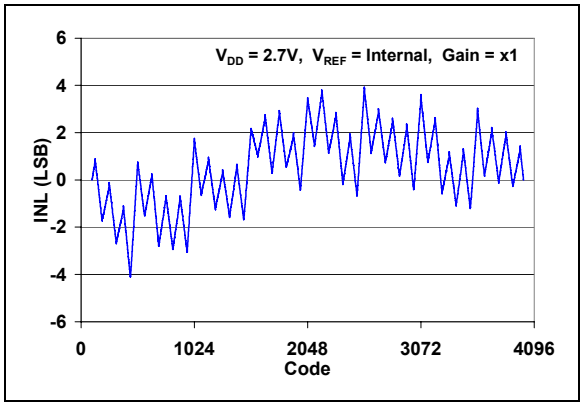


FIGURE 2-7: *INL vs. Code (T_A = +25°C).*

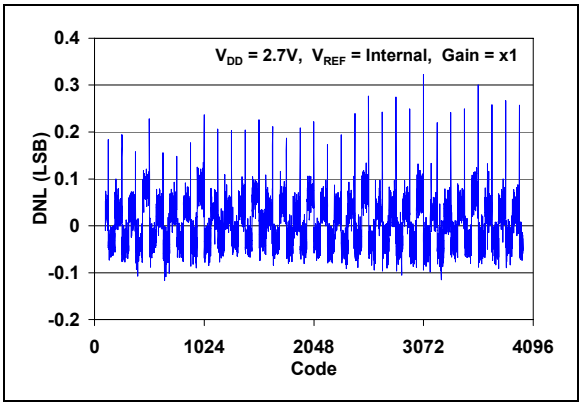


FIGURE 2-10: *DNL vs. Code (T_A = +25°C).*

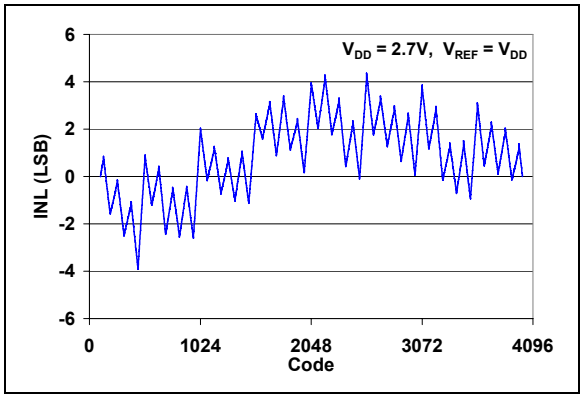


FIGURE 2-8: *INL vs. Code (T_A = +25°C).*

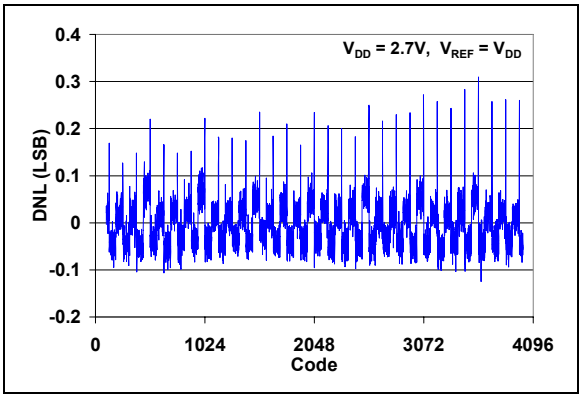


FIGURE 2-11: *DNL vs. Code (T_A = +25°C).*

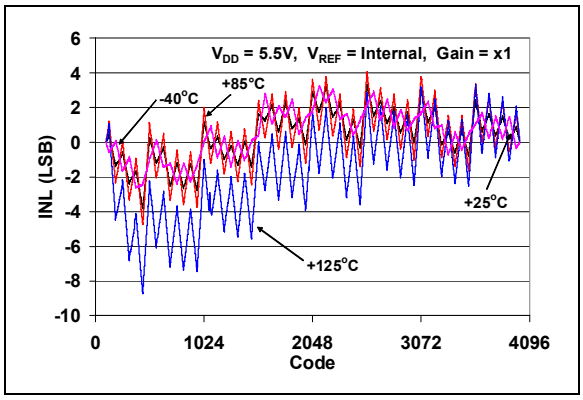


FIGURE 2-9: *INL vs. Code and Temperature.*

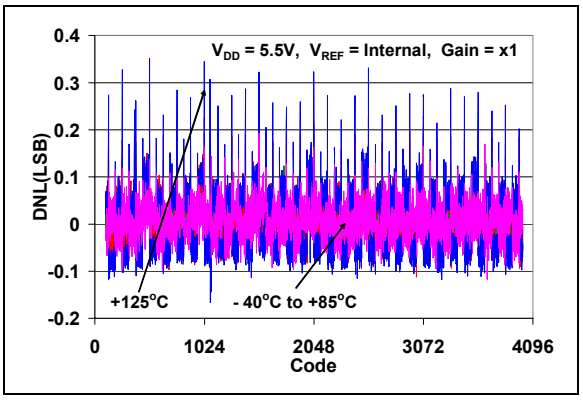


FIGURE 2-12: *DNL vs. Code and Temperature.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

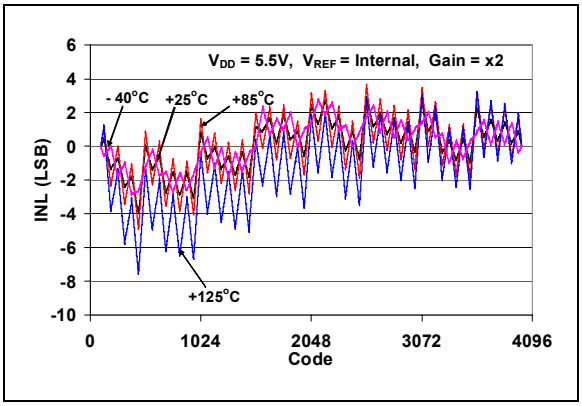


FIGURE 2-13: *INL vs. Code and Temperature.*

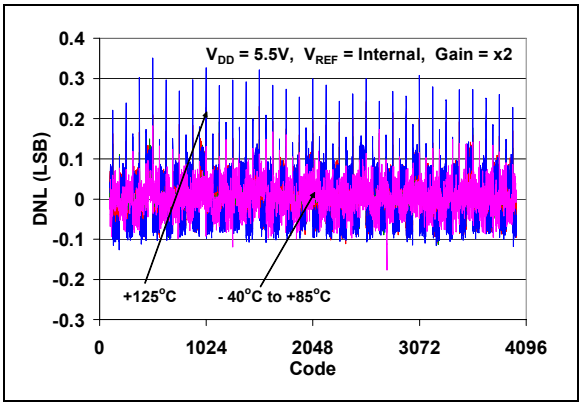


FIGURE 2-16: *DNL vs. Code and Temperature.*

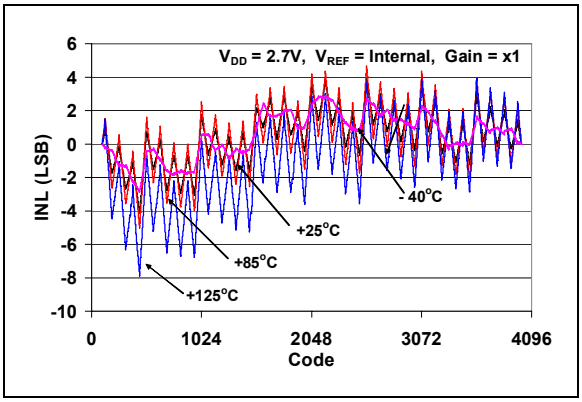


FIGURE 2-14: *INL vs. Code and Temperature.*

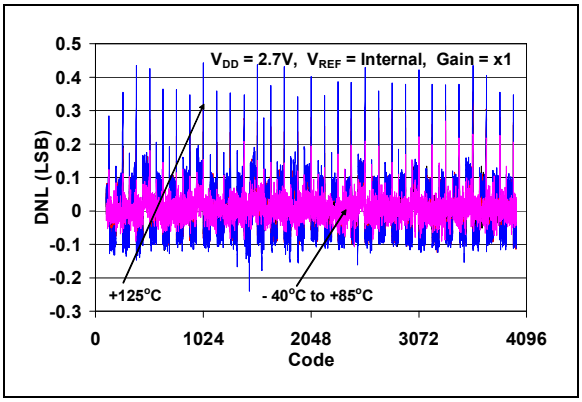


FIGURE 2-17: *DNL vs. Code and Temperature.*

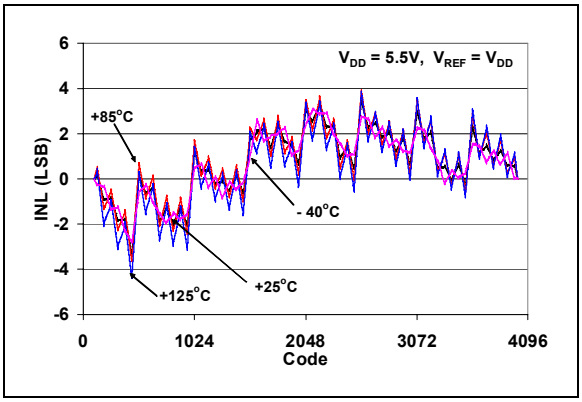


FIGURE 2-15: *INL vs. Code and Temperature.*

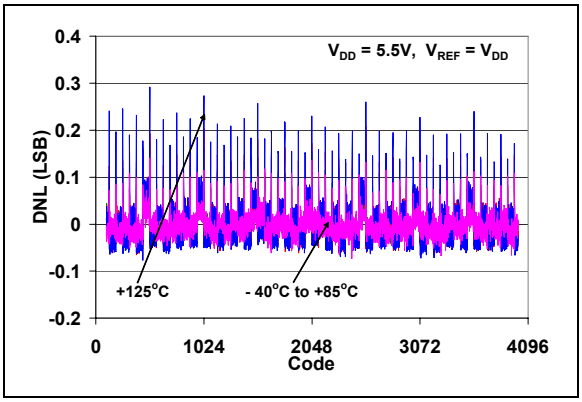


FIGURE 2-18: *DNL vs. Code and Temperature.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

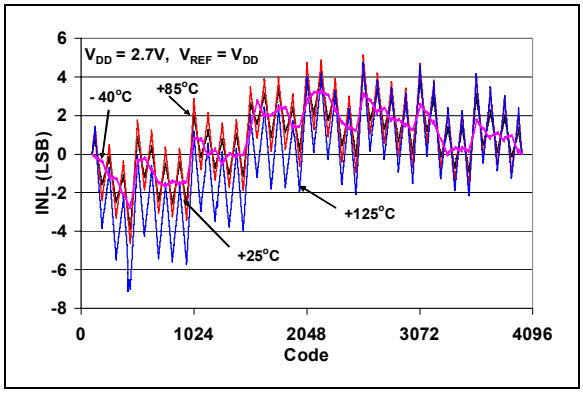


FIGURE 2-19: *INL vs. Code and Temperature.*

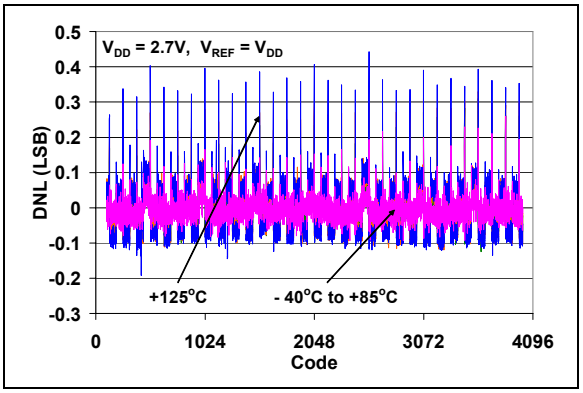


FIGURE 2-22: *DNL vs. Code and Temperature.*

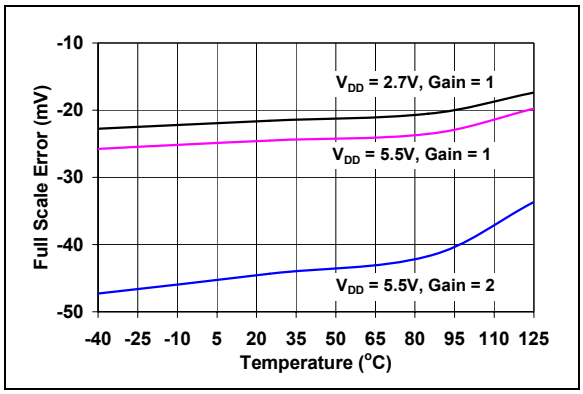


FIGURE 2-20: *Full Scale Error vs. Temperature (Code = FFFh, V_{REF} = Internal).*

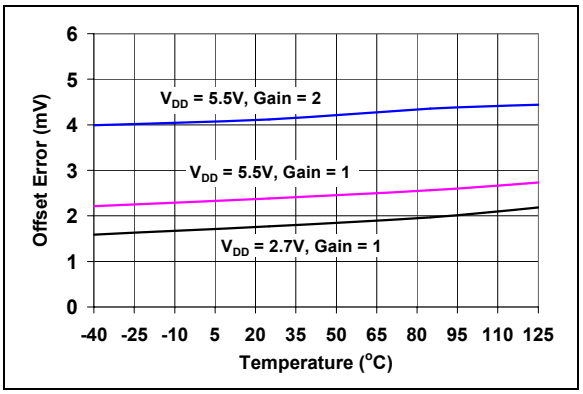


FIGURE 2-23: *Zero Scale Error vs. Temperature (Code = 000h, V_{REF} = Internal).*

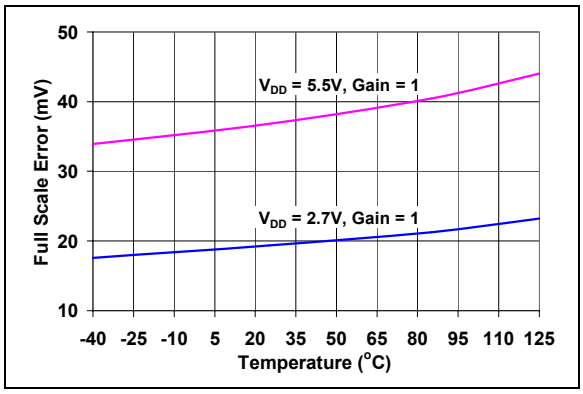


FIGURE 2-21: *Full Scale Error vs. Temperature (Code = FFFh, V_{REF} = V_{DD}).*

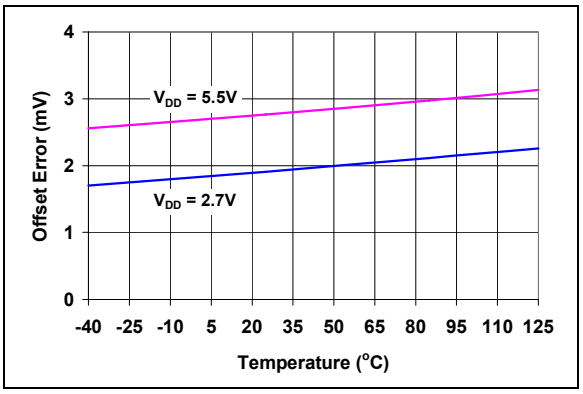


FIGURE 2-24: *Offset Error (Zero Scale Error).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

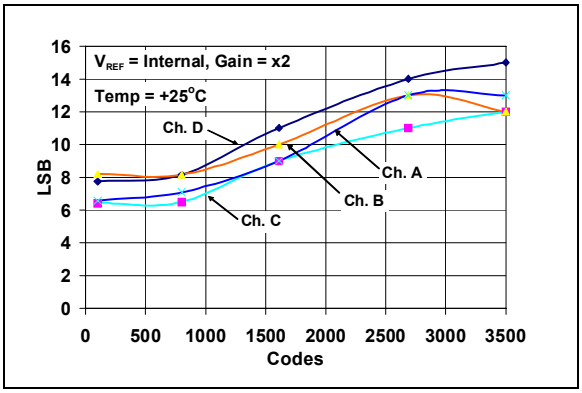


FIGURE 2-25: *Absolute DAC Output Error (V_{DD} = 5.5V).*

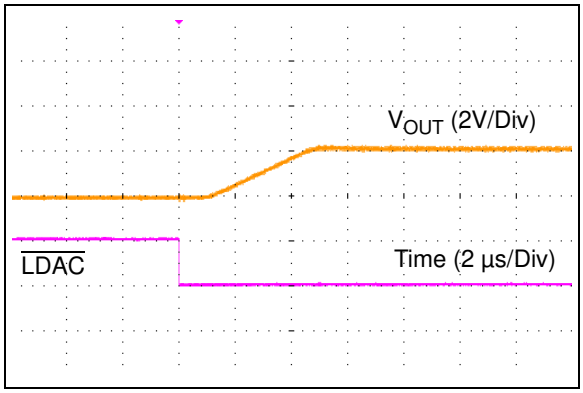


FIGURE 2-28: *Full Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Gain = x1, Code Change: 000h to FFFh).*

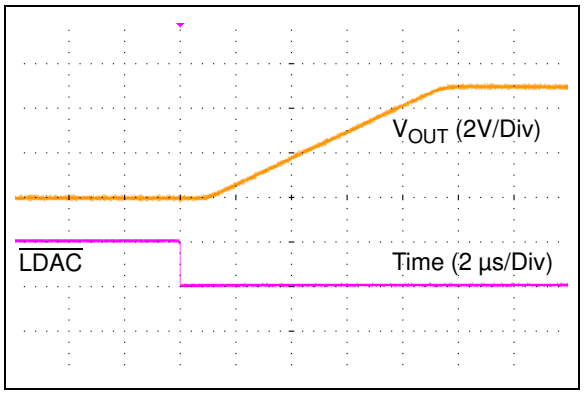


FIGURE 2-26: *Full Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 000h to FFFh).*

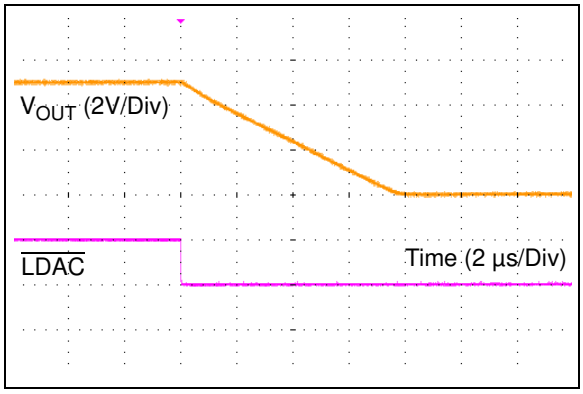


FIGURE 2-29: *Full Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: FFFh to 000h).*

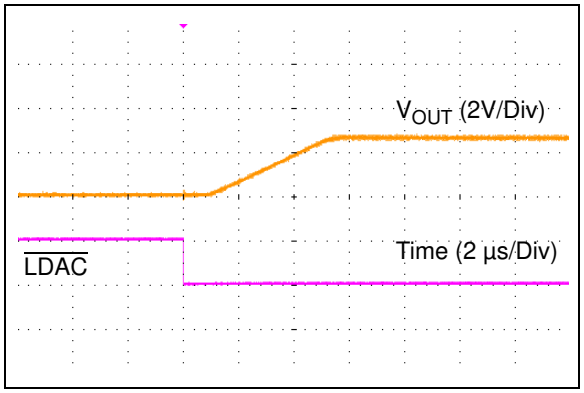


FIGURE 2-27: *Half Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 000h to 7FFh).*

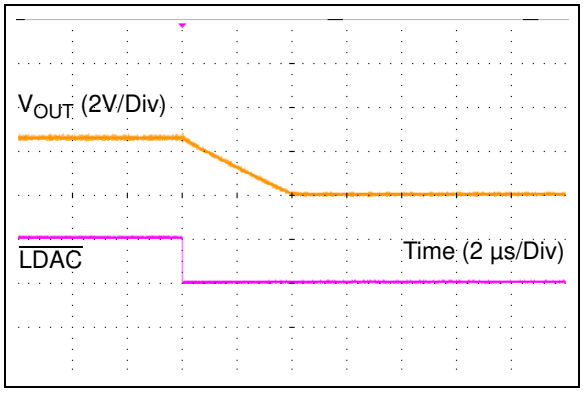


FIGURE 2-30: *Half Scale Settling Time (V_{REF} = V_{DD}, V_{DD} = 5V, $\overline{UDAC}$ = 1, Code Change: 7FFh to 000h).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

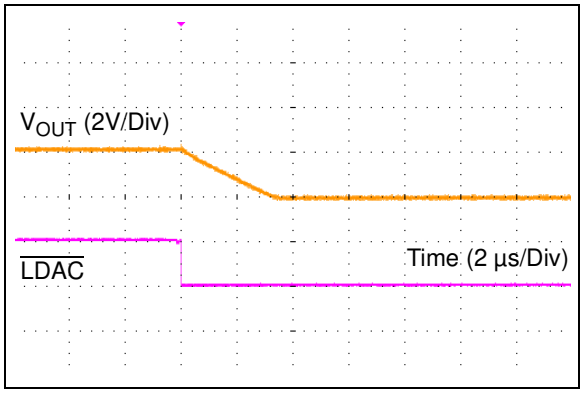


FIGURE 2-31: *Full Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Gain = x1, Code Change: FFFh to 000h).*

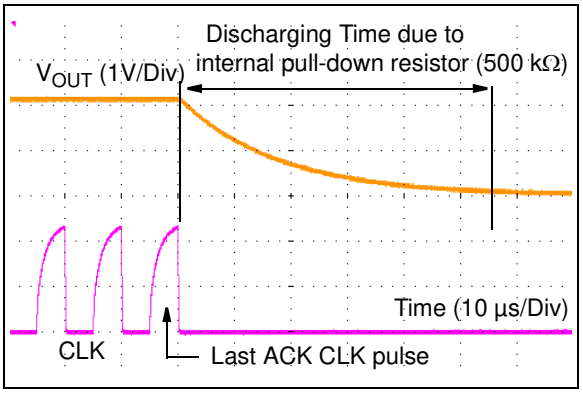


FIGURE 2-34: *Entering Power Down Mode (Code: FFFh, V_{REF} = Internal, V_{DD} = 5V, Gain = x1, PD1= PD0 = 1, No External Load).*

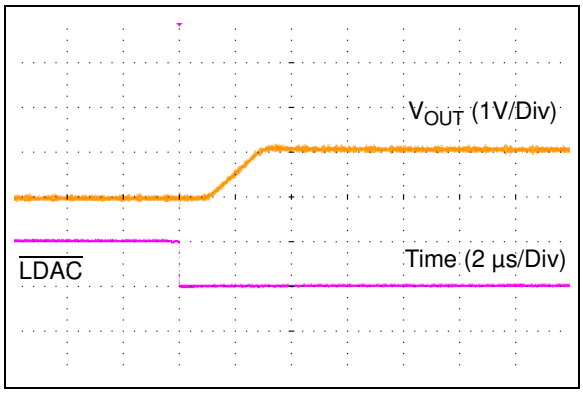


FIGURE 2-32: *Half Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Gain = x1, Code Change: 000h to 7FFh).*

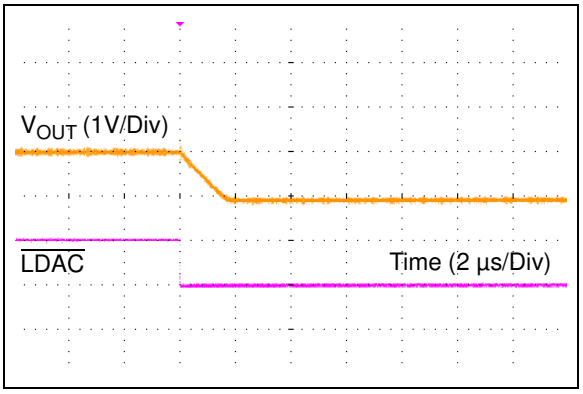


FIGURE 2-35: *Half Scale Settling Time (V_{REF} = Internal, V_{DD} = 5V, $\overline{UDAC}$ = 1, Gain = x1, Code Change: 7FFh to 000h).*

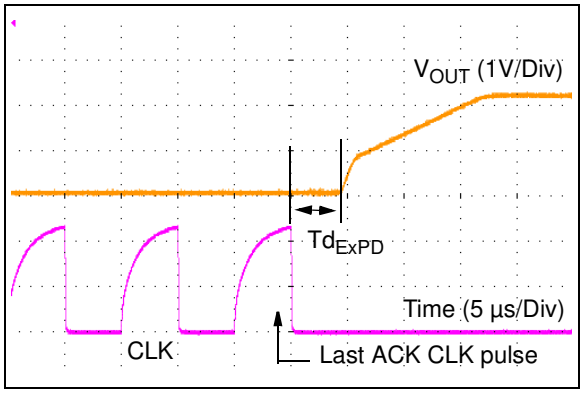


FIGURE 2-33: *Exiting Power Down Mode (Code: FFFh, V_{REF} = Internal, V_{DD} = 5V, Gain = x1, for all Channels.).*

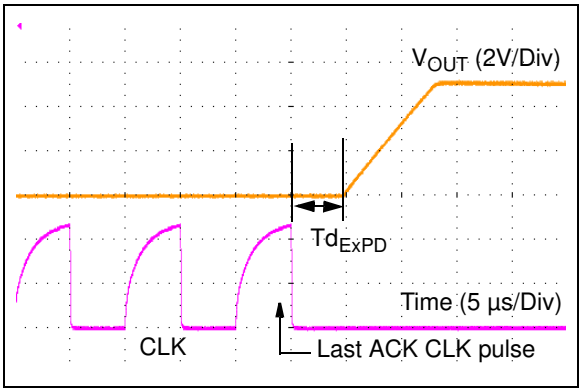


FIGURE 2-36: *Exiting Power Down Mode (Code: FFFh, V_{REF} = V_{DD}, V_{DD} = 5V, for all Channels).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

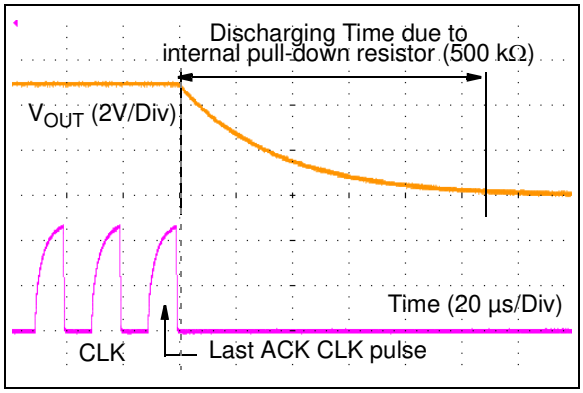


FIGURE 2-37: *Entering Power Down Mode (Code: FFFh, V_{REF} = V_{DD}, V_{DD} = 5V, PD1= PD0 = 1, No External Load).*

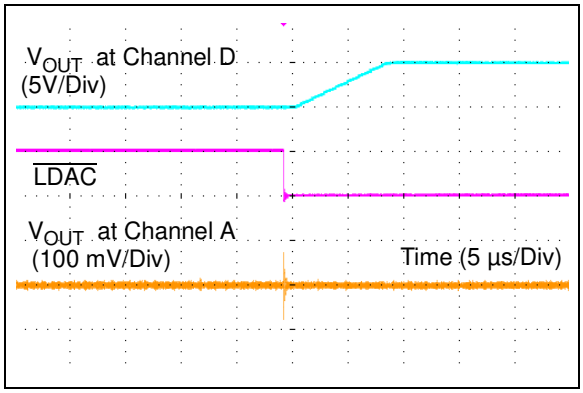


FIGURE 2-40: *Channel Cross Talk (V_{REF} = V_{DD}, V_{DD} = 5V).*

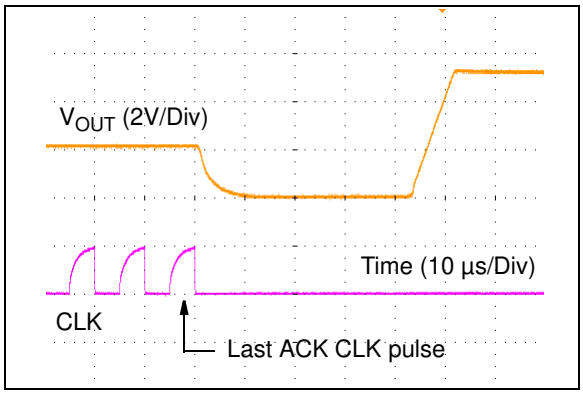


FIGURE 2-38: *V_{OUT} Time Delay when V_{REF} changes from Internal Reference to V_{DD}.*

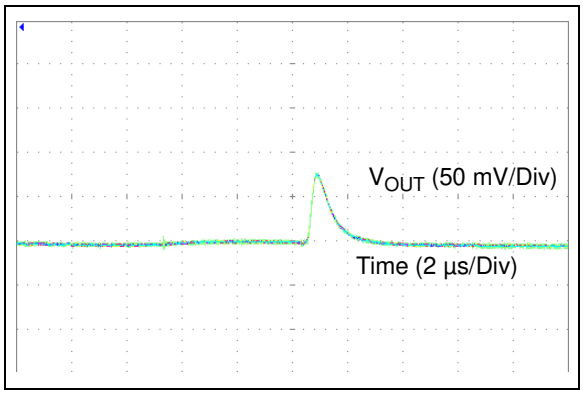


FIGURE 2-41: *Code Change Glitch (V_{REF} = External, V_{DD} = 5V, No External Load), Code Change: 800h to 7FFh.*

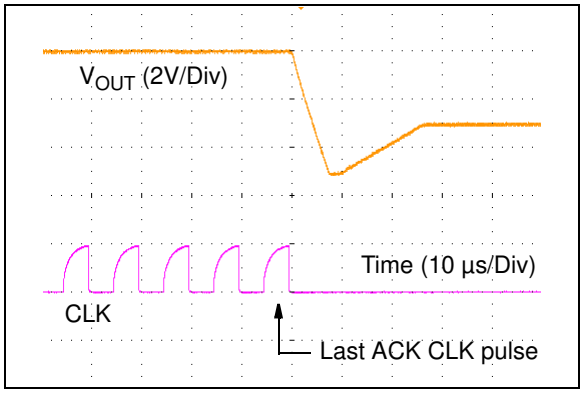


FIGURE 2-39: *V_{OUT} Time Delay when V_{REF} changes from V_{DD} to Internal Reference.*

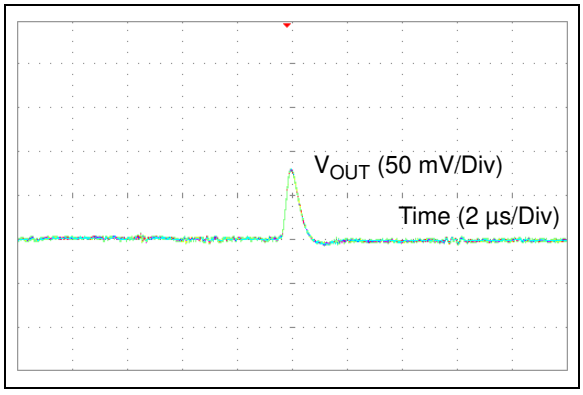


FIGURE 2-42: *Code Change Glitch (V_{REF} = Internal, V_{DD} = 5V, Gain = 1, No External Load), Code Change: 800h to 7FFh.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

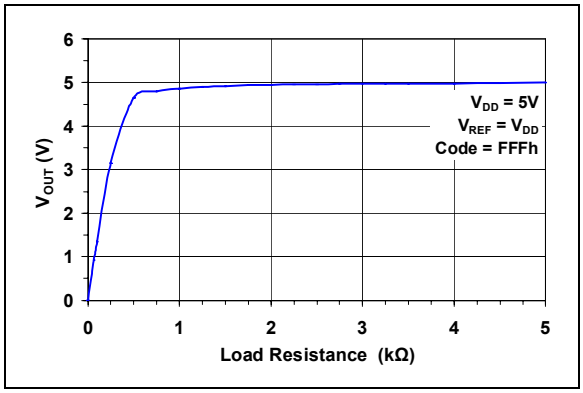


FIGURE 2-43: *V_{OUT} vs. Resistive Load.*

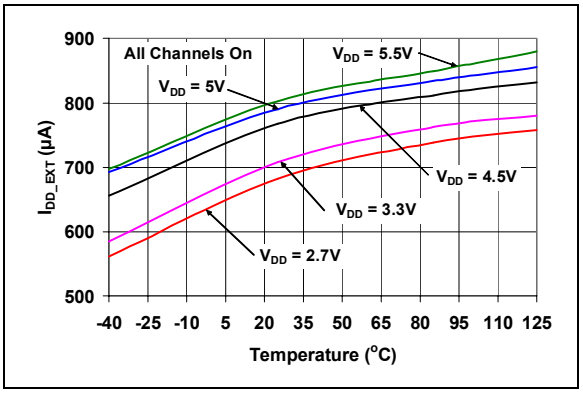


FIGURE 2-46: *I_{DD} vs. Temperature (V_{REF} = V_{DD}, All channels are in Normal Mode, Code = FFFh).*

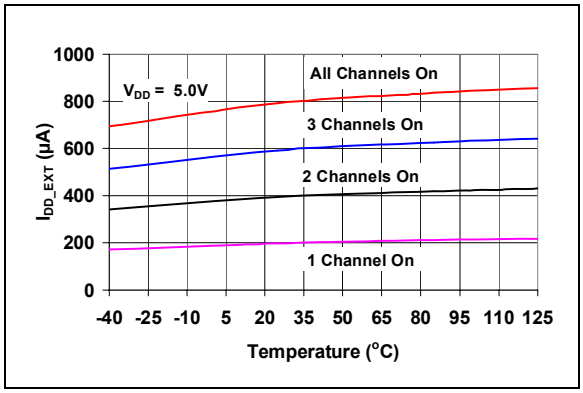


FIGURE 2-44: *I_{DD} vs. Temperature (V_{REF} = V_{DD}, V_{DD} = 5V, Code = FFFh).*

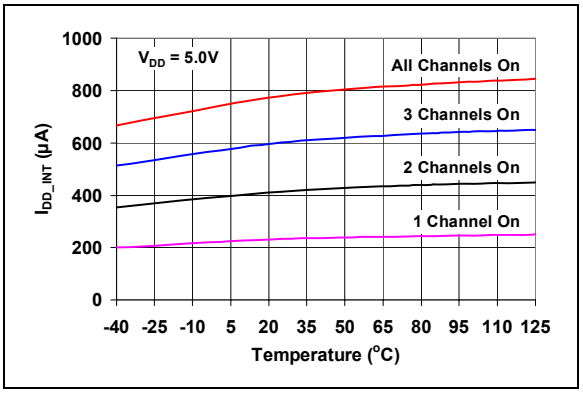


FIGURE 2-47: *I_{DD} vs. Temperature (V_{REF} = Internal, V_{REF} = 5V, Code = FFFh).*

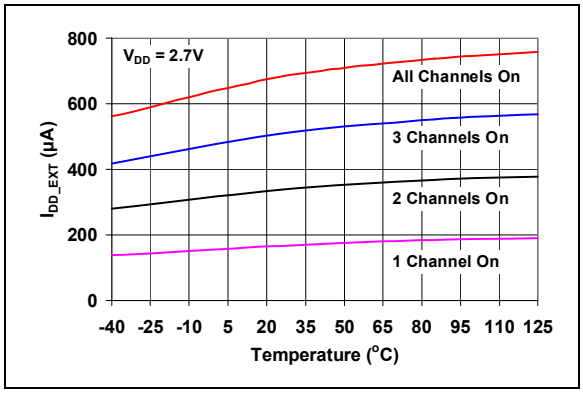


FIGURE 2-45: *I_{DD} vs. Temperature (V_{REF} = V_{DD}, V_{DD} = 2.7V, Code = FFFh).*

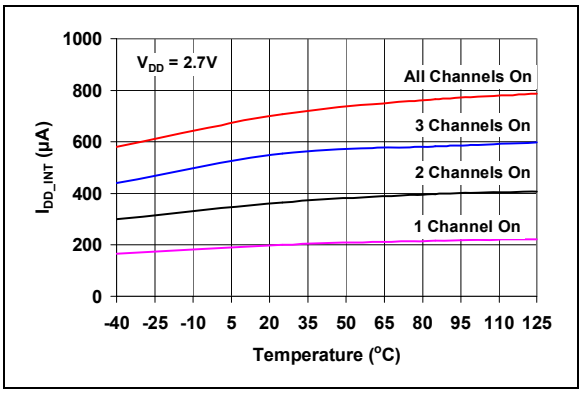


FIGURE 2-48: *I_{DD} vs. Temperature (V_{REF} = Internal, V_{DD} = 2.7V, Code = FFFh).*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = +5.0V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 100 pF.

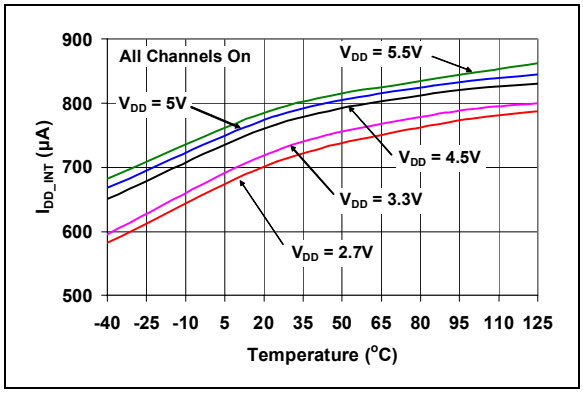


FIGURE 2-49: *I_{DD} vs. Temperature (V_{REF} = Internal, All Channels are in Normal Mode, Code = FFFh).*

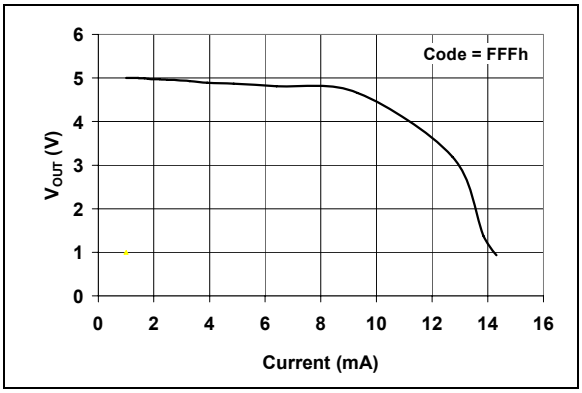


FIGURE 2-51: *Source Current Capability (V_{REF} = V_{DD}, Code = FFFh).*

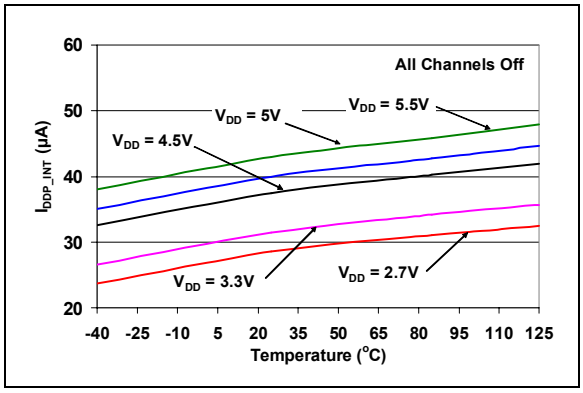


FIGURE 2-50: *I_{DD} vs. Temperature (V_{REF} = Internal, All Channels are in Powered Down).*

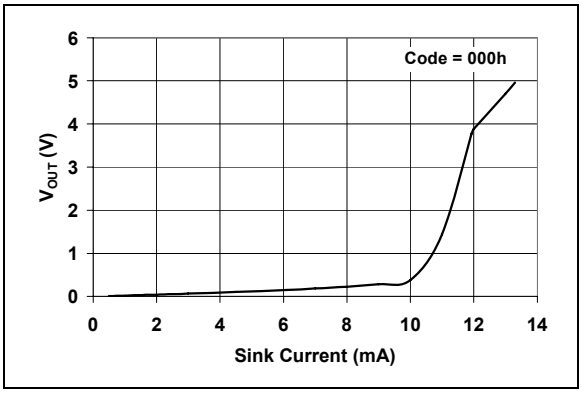


FIGURE 2-52: *Sink Current Capability (V_{REF} = V_{DD}, Code = 000h).*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Name	Pin Type	Function
1	V_{DD}	P	Supply Voltage
2	SCL	OI	I^2C Serial Clock Input **(Note 1)**
3	SDA	OI/OO	I^2C Serial Data Input and Output **(Note 1)**
4	$\overline{LDAC}$	ST	This pin is used for two purposes: (a) Synchronization Input. It is used to transfer the contents of the DAC input registers to the output registers (V_{OUT}). (b) Select the device for reading and writing I^2C address bits. **(Note 2)**
5	RDY/$\overline{BSY}$	OO	This pin is a status indicator of EEPROM programming activity. An external pull-up resistor (about 100 kΩ) is needed from RDY/$\overline{BSY}$ pin to V_{DD} line. **(Note 1)**
6	V_{OUT} A	AO	Buffered analog voltage output of channel A. The output amplifier has rail-to-rail operation.
7	V_{OUT} B	AO	Buffered analog voltage output of channel B. The output amplifier has rail-to-rail operation.
8	V_{OUT} C	AO	Buffered analog voltage output of channel C. The output amplifier has rail-to-rail operation.
9	V_{OUT} D	AO	Buffered analog voltage output of channel D. The output amplifier has rail-to-rail operation.
10	V_{SS}	P	Ground reference.

Legend: P = Power, OI = Open-Drain Input, OO = Open-Drain Output, ST = Schmitt Trigger Input Buffer, AO = Analog Output

Note 1: This pin needs an external pull-up resistor from V_{DD} line. Leave this pin float if it is not used.

2: This pin can be driven by MCU.

3.1 Supply Voltage Pins (V_{DD}, V_{SS})

V_{DD} is the power supply pin for the device. The voltage at the V_{DD} pin is used as a power supply input as well as a DAC external reference. The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance.

It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high-frequency noise present in application boards. The supply voltage (V_{DD}) must be maintained in the 2.7V to 5.5V range for specified operation.

V_{SS} is the ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application printed circuit board (PCB), it is highly recommended that the V_{SS} pin be tied to the analog ground path, or isolated within an analog ground plane of the circuit board.

3.2 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP4728 device acts only as a slave and the SCL pin accepts only external input serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock, and output from the MCP4728 occurs at the falling edges of the SCL clock.

The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin.

Refer to **Section 5.0 "I^2C Serial Interface Communications"** for more details on I^2C Serial Interface communication.

Typical range of the pull-up resistor value for SCL and SDA is from 5 kΩ to 10 kΩ for Standard (100 kHz) and Fast (400 kHz) modes, and less than 1 kΩ for High Speed mode (3.4 MHz).

3.3 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC register and EEPROM data. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high duration of the clock pulse. The High or Low state of the SDA pin can only change when the clock signal on the SCL pin is Low.

The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin.

Refer to **Section 5.0 "I^2C Serial Interface Communications"** for more details on the I^2C Serial Interface communication.

3.4 $\overline{\text{LDAC}}$ Pin

This pin can be driven by an external control device such as an MCU I/O pin. This pin is used to:

a) transfer the contents of the input registers to their corresponding DAC output registers and

b) select a device of interest when reading or writing I^2C address bits.

For more details on reading and writing the I^2C address bits, see **Section 5.4.4 "General Call Read Address Bits"** and **Section 5.6.8 "Write Command: Write I2C Address bits (C2=0, C1=1, C0=1)"**.

When the logic status of the $\overline{\text{LDAC}}$ pin changes from "High" to "Low", the contents of all input registers (Channels A – D) are transferred to their corresponding output registers, and all analog voltage outputs are updated simultaneously.

If this pin is permanently tied to "Low", the content of the input register is transferred to its output register (V_{OUT}) immediately at the last input data byte's acknowledge pulse.

The user can also use the $\overline{\text{UDAC}}$ bit instead. However, the $\overline{\text{UDAC}}$ bit updates a selected channel only. See **Section 4.8 "Output Voltage Update"** for more information on the $\overline{\text{LDAC}}$ pin and $\overline{\text{UDAC}}$ bit functions.

3.5 RDY/$\overline{\text{BSY}}$ Status Indicator Pin

This pin is a status indicator of EEPROM programming activity. This pin is "High" when the EEPROM has no programming activity, and "Low" when the EEPROM is in programming mode. It goes "High" when the EEPROM program is completed.

The RDY/$\overline{\text{BSY}}$ pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor (about 100 kΩ) from the V_{DD} line to the RDY/$\overline{\text{BSY}}$ pin. Let this pin float if it is not used.

3.6 Analog Output Voltage Pins (V_{OUT} A, V_{OUT} B, V_{OUT} C, V_{OUT} D)

The device has four analog voltage output (V_{OUT}) pins. Each output is driven by its own output buffer with a gain of 1 or 2, depending on the gain and V_{REF} selection bit settings. In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to 1 kΩ, 100 kΩ, or 500 kΩ, depending on the Power-Down selection bit settings.

The V_{OUT} pin can drive up to 1000 pF of capacitive load. It is recommended to use a load with R_L greater than 5 kΩ.

4.0 THEORY OF DEVICE OPERATION

The MCP4728 device is a 12-bit 4-channel buffered voltage output DAC with nonvolatile memory (EEPROM). The user can program the EEPROM with I^2C address bits, configuration and DAC input data of each channel. The device has an internal charge pump circuit to provide the programming voltage of the EEPROM.

When the device is first powered-up, it automatically loads the stored data in its EEPROM to the DAC input and output registers, and provides analog outputs with the saved settings immediately. This event does not require an $\overline{LDAC}$ or $\overline{UDAC}$ bit condition. After the device is powered-up, the user can update the input registers using I^2C write commands. The analog outputs can be updated with new register values if the $\overline{LDAC}$ pin or $\overline{UDAC}$ bit is low. The DAC output of each channel is buffered with a low power and precision output amplifier. This amplifier provides a rail-to-rail output with low offset voltage and low noise.

The device uses a resistor string architecture. The resistor ladder DAC can be driven from V_{DD} or internal V_{REF}, depending on the reference selection. The user can select internal (2.048V) or external reference (V_{DD}) for each DAC channel individually by software control. The V_{DD} is used as the external reference. Each channel is controlled and operated independently.

The device has a Power-Down mode feature. Most of the circuit in each powered down channel are turned off. Therefore, operating power can be saved significantly by putting any unused channel to the Power-Down mode.

4.1 Power-on Reset (POR)

The device contains an internal Power-on Reset (POR) circuit that monitors power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

If the power supply voltage is less than the POR threshold (V_{POR} = 2V, typical), all circuits are disabled and there will be no analog output. When the V_{DD} increases above the V_{POR}, the device takes a reset state. During the reset period, each channel uploads all configuration and DAC input codes from EEPROM, and analog output (V_{OUT}) will be available accordingly. This enables the device to return to the same state that it was at the last write to the EEPROM, before it was powered off. The POR status is monitored by the POR status bit by using the I^2C read command. See Figure 5-15 for the details of the POR status bit.

4.2 Reset Conditions

The device can be reset by two independent events:

a) by Power-on Reset
b) by I^2C General Call Reset Command

Under the reset conditions, the device uploads the EEPROM data into both of the DAC input and output registers simultaneously. The analog output voltage of each channel is available immediately, regardless of the $\overline{LDAC}$ and $\overline{UDAC}$ bit conditions.

The factory default settings for the EEPROM prior to the device shipment are shown in Table 4-2.

4.3 Output Amplifier

The DAC output is buffered with a low power precision amplifier. This amplifier provides low offset voltage and low noise, as well as rail-to-rail output.

The output amplifier can drive the resistive and high capacitive loads without oscillation. The amplifier can provide a maximum load current of 24 mA, which is enough for most of programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

4.3.1 PROGRAMMABLE GAIN BLOCK

The rail-to-rail output amplifier of each channel has configurable gain option. When the internal voltage reference is selected, the output amplifier gain has two selection options: Gain of 1 or Gain of 2.

When the external reference is selected ($V_{REF} = V_{DD}$), the Gain of 2 option is disabled, and only the Gain of 1 is used by default.

4.3.1.1 Resistive and Capacitive Loads

The analog output (V_{OUT}) pin is capable of driving capacitive loads up to 1000 pF in parallel with 5 kΩ load resistance. Figure 2-43 shows the V_{OUT} vs. Resistive Load.

4.4 DAC Input Registers and Non-Volatile EEPROM Memory

Each channel has its own volatile DAC input register and EEPROM. The details of the input registers and EEPROM are shown in Table 4-1 and Table 4-2, respectively.

TABLE 4-1: INPUT REGISTER MAP (VOLATILE)

	Configuration Bits										DAC Input Data (12 bits)											
Bit Name	RDY /BSY	A2	A1	A0	VREF	DAC1	DAC0	PD1	PD0	Gx	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	(Note 1)	I²C Address Bits (Note 2)			Ref. Select (Note 2)	DAC Channel (Note 2)		Power-Down Select (Note 2)		Gain Select (Note 2)	(Note 2)											
CH. A																						
CH. B																						
CH. C																						
CH. D																						

Note 1: EEPROM write status indication bit (flag).

2: Loaded from EEPROM during power-up, or can be updated by the user.

TABLE 4-2: EEPROM MEMORY MAP AND FACTORY DEFAULT SETTINGS

	Configuration Bits							DAC Input Data (12 bits)										
Bit Name	A2	A1	A0	VREF	PD1	PD0	Gx	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Function	I²C Address Bits (Note 1)			Ref. Select (Note 2)	Power-Down Select		Gain Select (Note 3)												
CH. A	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH. B				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH. C				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH. D				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note 1: Device I²C address bits. The user can also specify these bits during the device ordering process. The factory default setting is “000”. These bits can be reprogrammed by the user using the I²C Address Write command.

2: Voltage Reference Select: **0 =** External V_{REF} (V_{DD}), **1 =** Internal V_{REF} (2.048V).

3: Gain Select: **0 =** Gain of 1, **1 =** Gain of 2.

TABLE 4-3: CONFIGURATION BITS

Bit Name	Functions
RDY/$\overline{BSY}$	This is a status indicator (flag) of EEPROM programming activity: **1 =** EEPROM is not in programming mode **0 =** EEPROM is in programming mode **Note:** RDY/$\overline{BSY}$ status can also be monitored at the RDY/$\overline{BSY}$ pin.
(A2, A1, A0)	Device I^2C address bits. See **Section 5.3 "MCP4728 Device Addressing"** for more details.
V_{REF}	Voltage Reference Selection bit: **0 =** V_{DD} **1 =** Internal voltage reference (2.048V) **Note:** Internal voltage reference circuit is turned off if all channels select external reference ($V_{REF} = V_{DD}$).
DAC1, DAC0	DAC Channel Selection bits: **00 =** Channel A **01 =** Channel B **10 =** Channel C **11 =** Channel D
PD1, PD0	Power-Down selection bits: **00 =** Normal Mode **01 =** V_{OUT} is loaded with 1 kΩ resistor to ground. Most of the channel circuits are powered off. **10 =** V_{OUT} is loaded with 100 kΩ resistor to ground. Most of the channel circuits are powered off. **11 =** V_{OUT} is loaded with 500 kΩ resistor to ground. Most of the channel circuits are powered off. **Note:** See Table 4-7 and Figure 4-1 for more details.
G_X	Gain selection bit: **0 =** x1 (gain of 1) **1 =** x2 (gain of 2) **Note:** Applicable only when internal V_{REF} is selected. If $V_{REF} = V_{DD}$, the device uses a gain of 1 regardless of the gain selection bit setting.
$\overline{UDAC}$	DAC latch bit. Upload the selected DAC input register to its output register (V_{OUT}): **0 =** Upload. Output (V_{OUT}) is updated. **1 =** Do not upload. **Note:** $\overline{UDAC}$ bit affects the selected channel only.