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MCP47A1

6-Bit Volatile DAC with Command Code

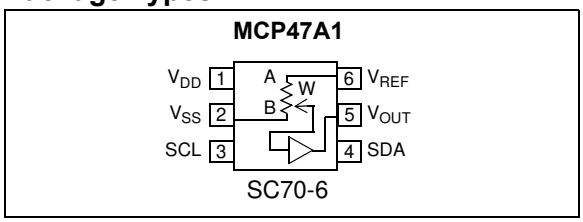
Features:

- 6-Bit DAC
  - 65 Taps: 64 Resistors with Taps to Full-Scale and Zero-Scale (Wiper Code 00h to 40h)
- V_{REF} Pull-down Resistance: 20 kΩ (typical)
- V_{OUT} Voltage Range
  - V_{SS} to V_{REF}
- $I^2C^{™}$ Protocol
  - Supports SMBus 2.0 Write Byte/Word Protocol Formats
  - Supports SMBus 2.0 Read Byte/Word Protocol Formats
  - Slave Addresses: 5Ch and 7Ch
- Brown-out Reset Protection (1.5V typical)
- Power-on Default Wiper Setting (Mid-scale)
- Low-Power Operation: 90 µA Static Current (typical)
- Wide Operating Voltage Range:
  - 1.8V to 5.5V
- Low Tempco: 15 ppm (typical)
- 100 kHz (typical) Bandwidth (-3 dB) Operation
- Extended Temperature Range (-40°C to +125°C)
- Small Packages, SC70-6
- Lead Free (Pb-free) Package

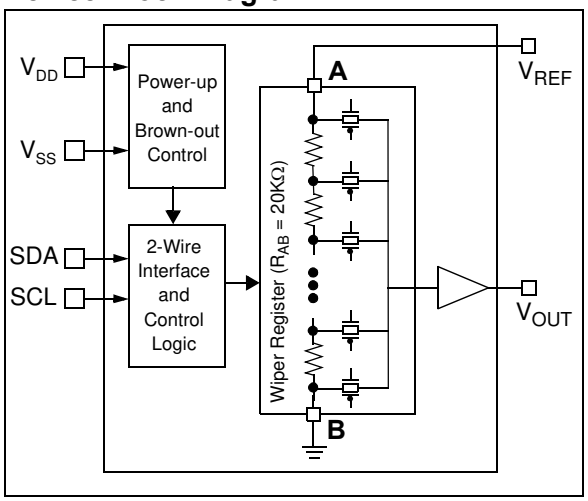
Applications

- Set point or offset trimming
- Cost-sensitive mechanical trim pot replacement

Package Types



Device Block Diagram



Description

The MCP47A1 devices are volatile, 6-Bit digital potentiometers with a buffered output. The wiper setting is controlled through an I^2C serial interface. The I^2C slave addresses of "010 1110" and "011 1110" are supported.

Device Features

Device	Interface	# of Taps	# of Resistors	V_{REF} Resistance (kΩ)	Data Value Range	POR/BOR Value	I^2C Slave Address	V_{DD} Operating Range	V_{OUT} Range	Package(s)
MCP47A1	I^2C	65	64	20	00h - 40h	20h	5Ch, 7Ch	1.8V (1) to 5.5V	V_{SS} to V_{REF}	SC70-6
MCP47DA1(2)	I^2C	65	64	30	00h - 7Fh	40h	5Ch, 7Ch	1.8V (1) to 5.5V	1/3 V_{REF} to 2/3 V_{REF}	SC70-6, SOT-23-6
MCP4706	I^2C	256	256	210	00h - FFh	7Fh	Cxh (3)	2.7V to 5.5V	V_{SS} to V_{DD} or V_{SS} to V_{REF} (5)	SOT-23-6, DFN-6 (2x2)
MCP4716	I^2C	1024	1024	210	000h - 3FFh	1FFh	Cxh (3)	2.7V to 5.5V	V_{SS} to V_{DD} or V_{SS} to V_{REF} (5)	SOT-23-6, DFN-6 (2x2)
MCP4726	I^2C	4096	4096	210	000h - FFFh	3FFh	Cxh (3)	2.7V to 5.5V	V_{SS} to V_{DD} or V_{SS} to V_{REF} (5)	SOT-23-6, DFN-6 (2x2)
MCP4725	I^2C	4096	4096	N.A.	000h - FFFh	3FFh	Cxh (4)	2.7V to 5.5V	V_{SS} to V_{DD}	SOT-23-6

Note 1: Analog characteristics only tested from 2.7V to 5.5V.

2: Refer to MCP47DA1 Data Sheet (DS25118).

3: The A2:A0 bits are determined by device ordered.

4: The A2 and A1 bits are determined by device ordered and A0 is determined by the state of the A0 pin.

5: User programmable.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... 0.6V to +7.0V
Voltage on SCL, and SDA with respect to V_{SS} ..... -0.6V to V_{DD} + 0.3V
Voltage on all other pins (V_{OUT} and V_{REF}) with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Maximum output current sunk by any Output pin ..... 25 mA
Maximum output current sourced by any Output pin ..... 25 mA
Maximum current out of V_{SS} pin ..... 100 mA
Maximum current into V_{DD} pin ..... 100 mA
Maximum current into V_{REF} pin ..... 250 uA
Maximum current sourced by V_{OUT} pin ..... 40 mA
Maximum current sunk by V_{REF} pin ..... 40 mA
Package power dissipation (T_A = +50°C, T_J = +150°C)
SC70-6 ..... 480 mW
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
ESD protection on all pins ..... ≥ 6 kV (HBM)
..... ≥ 400V (MM)
..... ≥ 1.5 kV (CDM)
Latchup (JEDEC JESD78A) at +125°C ..... ±100 mA
Soldering temperature of leads (10 seconds) ..... +300°C
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	Analog Characteristics specified
		1.8	—	5.5	V	Digital Characteristics specified
V_{DD} Start Voltage to ensure Wiper to default reset state	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	**Note 5**			V/ms	
Delay after device exits the reset state (V_{DD} > V_{BOR}) to Digital Interface Active	T_{BORD}	—	—	1	µS	
Delay after device exits the reset state (V_{DD} > V_{BOR}) to V_{OUT} valid	T_{OUTV}			20	µS	Within ± 0.5 LSb of V_{REF} / 2 (for default POR/BOR wiper value).
Supply Current **(Note 6)**	I_{DD}	—	130	220	µA	Serial Interface Active, Write all 0's to Volatile Wiper, No Load on V_{OUT} V_{DD} = 5.5V, V_{REF} = V_{DD}, F_{SCL} = 400 kHz
		—	90	130	µA	Serial Interface Inactive (Static), (Stop condition, SCL = SDA = V_{IH}), No Load on V_{OUT} Wiper = 0, V_{DD} = 5.5V, V_{REF} = V_{DD}
V_{REF} Input Range	V_{REF}	1	—	V_{DD}	V	**Note 7**

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	V_{SS}	—	V	Device Output minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{REF}	—	V	Device Output maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	5	15	24	mA	
Settling Time	$t_{SETTLING}$	—	15	—	µs	
External Reference (V_{REF}) (Note 3)						
Input Capacitance	C_{VREF}	—	7	—	pF	
Total Harmonic Distortion	THD	—	-73	—	dB	V_{REF} = 1.65V ± 0.1V, Frequency = 1 kHz
Dynamic Performance (Note 3)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (20h to 1Fh)
Digital Feedthrough		—	<10	—	nV-s	

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Resistance (± 20%)	R_{VREF}	16.0	20	24.0	kΩ	**Note 1,**
Resolution	N		65		Taps	No Missing Codes
Step Resistance	R_S	—	R_{VREF} / 64	—	Ω	**Note 3**
Nominal Resistance Tempco	$\Delta R_{VREF}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C
		—	100	—	ppm/°C	T_A = -40°C to +85°C
		—	150	—	ppm/°C	T_A = -40°C to +125°C
Ratiometeric Tempco	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (20h)
V_{OUT} Accuracy		0.72	0.75	0.78	V	V_{REF} = 1.5V, code = 20h
V_{OUT} Load	L_{VOUTR}	5	—	—	kΩ	Resistive Load
	L_{VOUTC}	—	—	1	nF	Capacitive Load
Maximum current through Terminal (V_{REF}) **Note 3**	I_{VREF}	—	—	345	µA	V_{REF} = 5.5V
Leakage current into V_{REF}	I_L	—	100	—	nA	V_{REF} = V_{SS}
Full-Scale Error (code = 40h)	V_{FSE}	-1	±0.35	+1	LSb	V_{REF} = V_{DD}
Zero-Scale Error (code = 00h)	V_{ZSE}	-0.75	±0.35	+0.75	LSb	V_{REF} = V_{DD}
V_{OUT} Integral Nonlinearity	INL	-1	±0.25	+1	LSb	**Note 2,** V_{REF} = V_{DD}
V_{OUT} Differential Nonlinearity	DNL	-0.5	±0.25	+0.5	LSb	**Note 2,** V_{REF} = V_{DD}
Bandwidth -3 dB	BW	—	100	—	kHz	V_{DD} = 5.0V, V_{REF} = 3.0V ± 2.0V, Code = 20h
Capacitance (V_{REF})	C_{REF}	—	75	—	pF	f =1 MHz, Code = Full-Scale

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Digital Inputs/Outputs (SDA, SCK)								
Schmitt Trigger High Input Threshold	V_{IH}	0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V		
Schmitt Trigger Low Input Threshold	V_{IL}	-0.5	—	0.3V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V		
Hysteresis of Schmitt Trigger Inputs **(Note 3)**	V_{HYS}	N.A.	—	—	V	SDA and SCL	100 kHz	V_{DD} < 2.0V
		N.A.	—	—	V			V_{DD} ≥ 2.0V
		0.1 V_{DD}	—	—	V		400 kHz	V_{DD} < 2.0V
		0.05 V_{DD}	—	—	V			V_{DD} ≥ 2.0V
Output Low Voltage (SDA)	V_{OL}	V_{SS}	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA		
		V_{SS}	—	0.2V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA		
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{REF} = V_{DD} and V_{REF} = V_{SS}		
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 400 kHz		
RAM (Wiper) Value								
Value Range	N	0h	—	40h	hex			
Wiper POR/BOR Value	$N_{POR/BOR}$	20h			hex			
Power Requirements								
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%		V_{REF} = V_{DD}, Code = 20h	

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

1.1 I²C Mode Timing Waveforms and Requirements

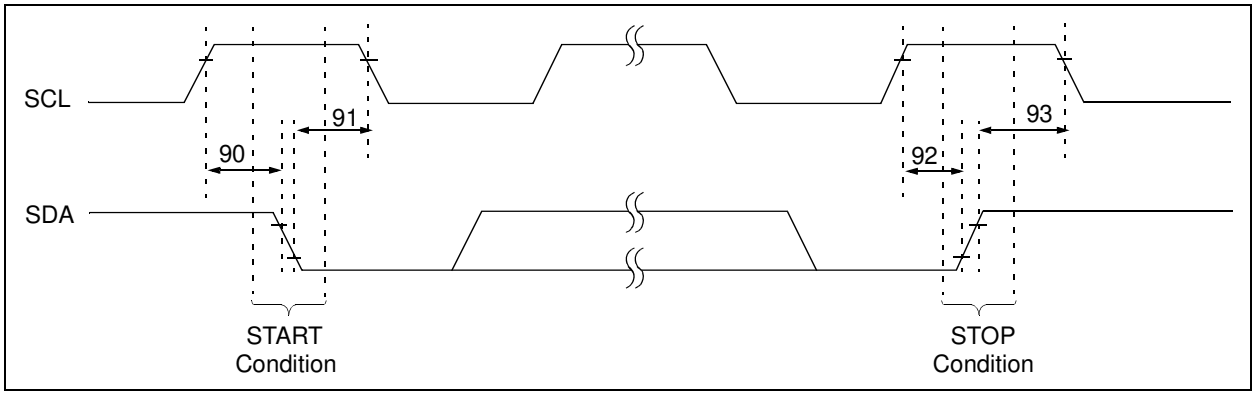
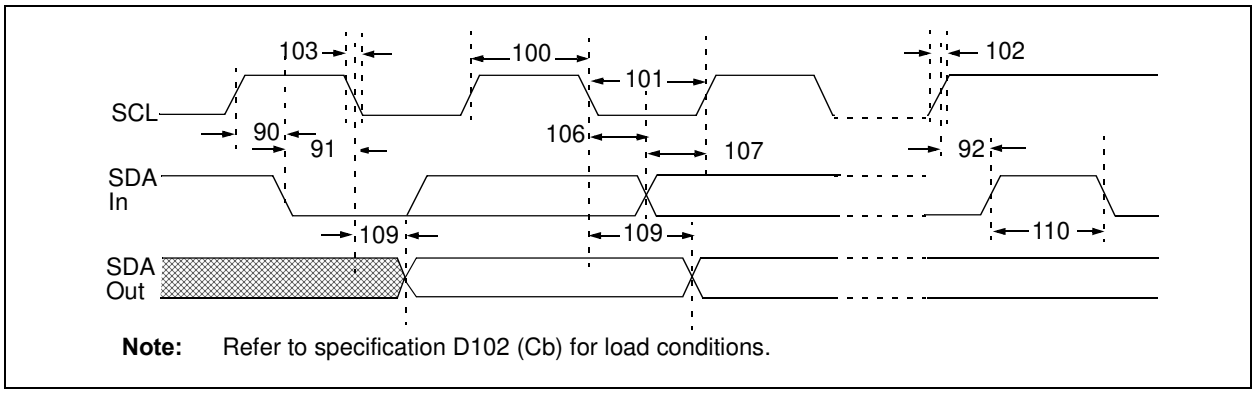


FIGURE 1-1: *I²C Bus Start/Stop Bits Timing Waveforms.*



Note: Refer to specification D102 (Cb) for load conditions.

FIGURE 1-2: *I²C Bus Data Timing.*

TABLE 1-1: I²C BUS START/STOP BITS REQUIREMENTS

I²C AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Section 2.0 "Typical Performance Curves"**				
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
D102	Cb	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	ns	
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
92	TSU:STO	STOP condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	

TABLE 1-2: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage VDD range is described in **AC/DC characteristics**			
Parameter No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	T_{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
101	T_{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
102A(5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
102B(5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
103A (5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	40	ns	
103B (5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb(5)	300	ns	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V **(Note 6)**
			400 kHz mode	0	—	ns	2.7V-5.5V **(Note 6)**
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**Note 5**
			400 kHz mode	100	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	**Note 5**
			400 kHz mode	—	900	ns	
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	Philips Spec states N.A.
			400 kHz mode	—	50	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu; DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP47A1 device must provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to guarantee that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not tested.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 6L-SC70	θ_{JA}	—	207	—	°C/W	**Note 1**

Note 1: Package Power Dissipation (P_{DIS}) is calculated as follows:
$P_{DIS} = (T_J - T_A) / \theta_{JA}$,
where: T_J = Junction Temperature, T_A = Ambient Temperature.

2.0 TYPICAL PERFORMANCE CURVES

Note 1: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

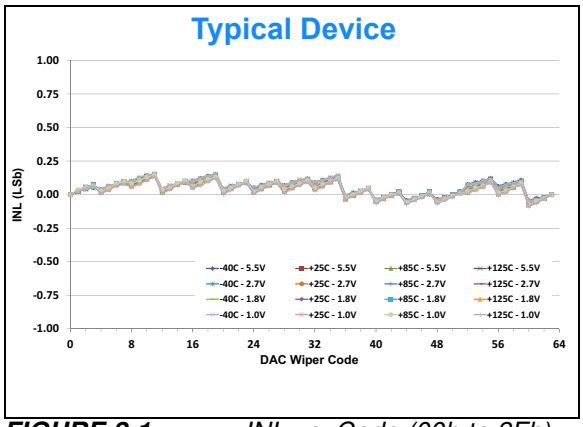


FIGURE 2-1: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

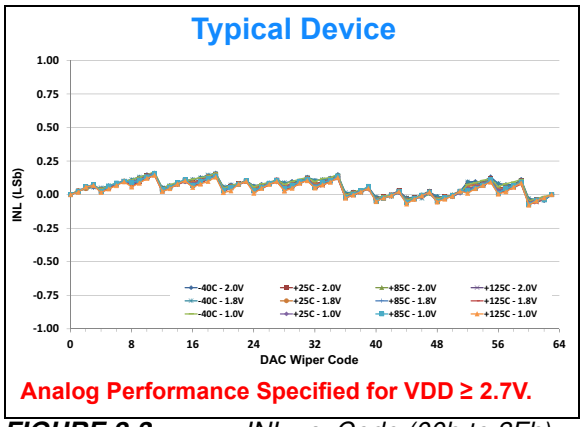


FIGURE 2-3: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

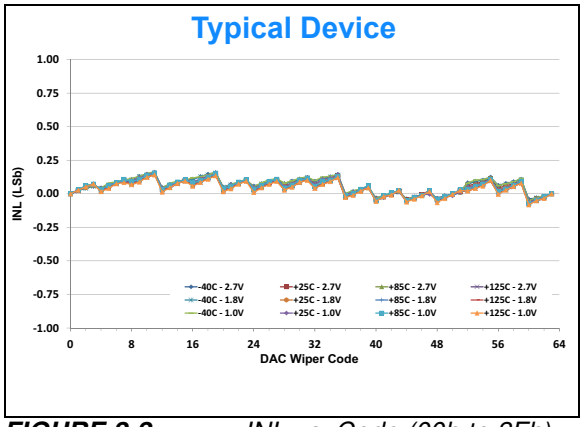


FIGURE 2-2: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

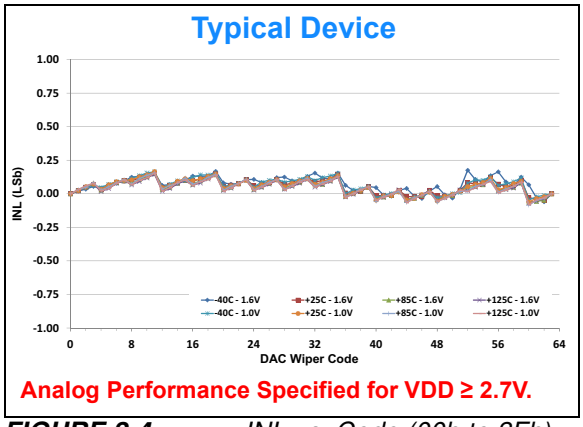


FIGURE 2-4: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

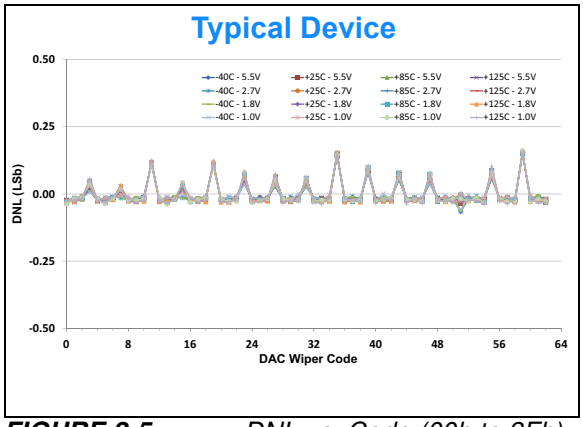


FIGURE 2-5: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

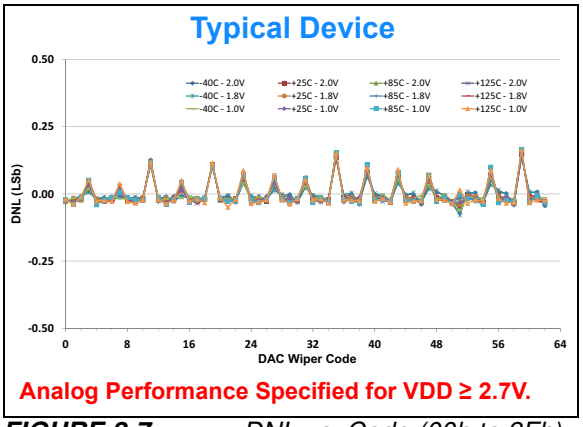


FIGURE 2-7: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

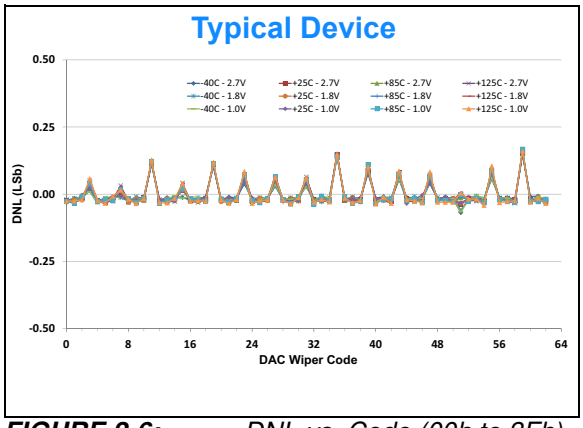


FIGURE 2-6: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

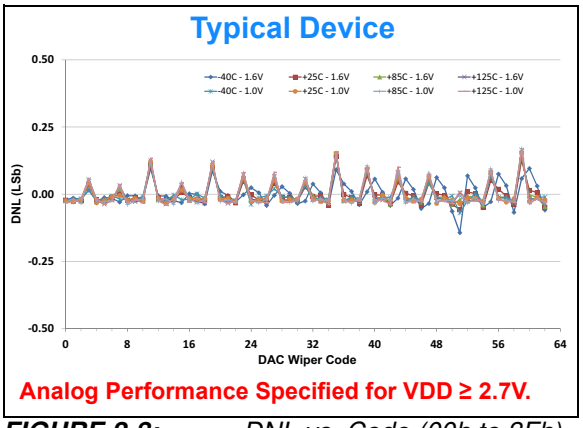


FIGURE 2-8: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

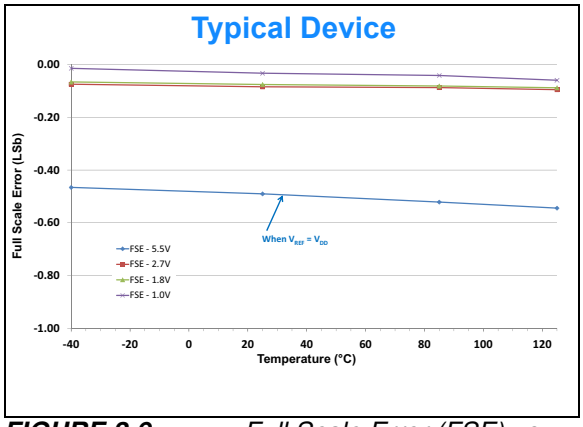


FIGURE 2-9: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

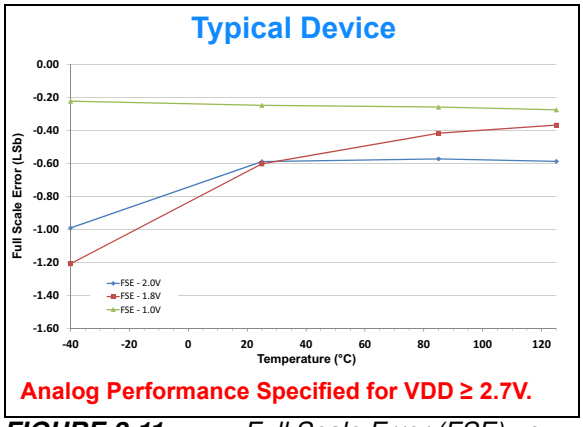


FIGURE 2-11: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

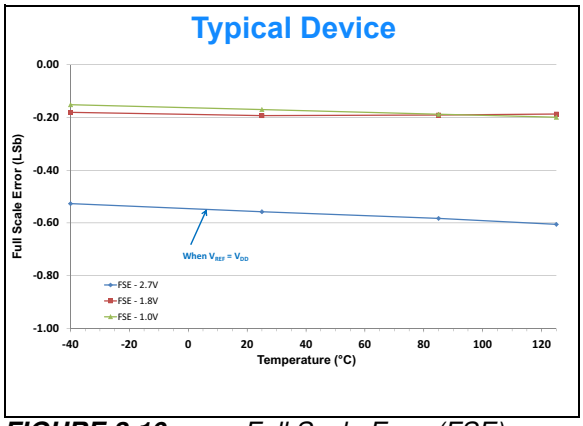


FIGURE 2-10: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

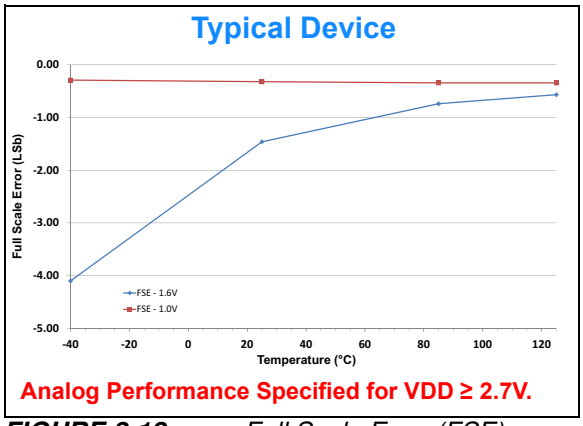


FIGURE 2-12: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

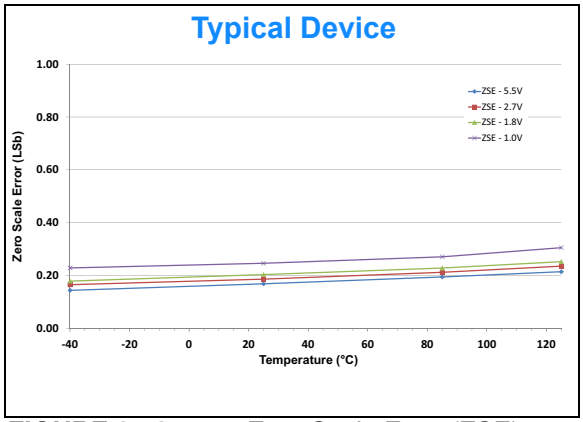


FIGURE 2-13: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

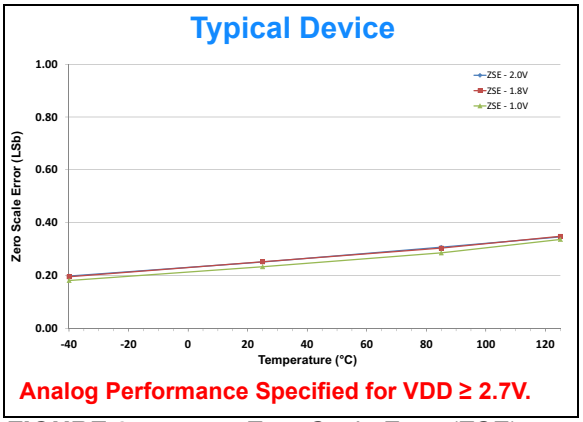


FIGURE 2-15: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

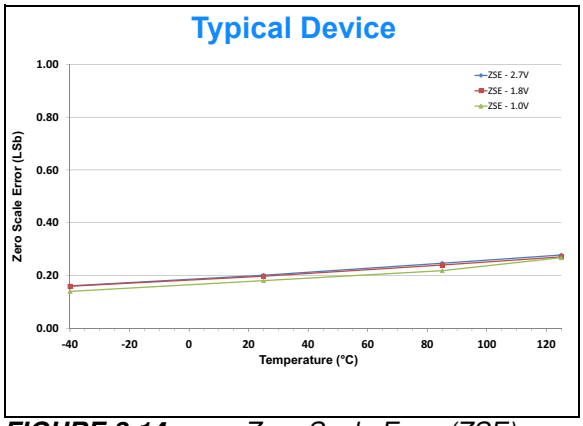


FIGURE 2-14: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

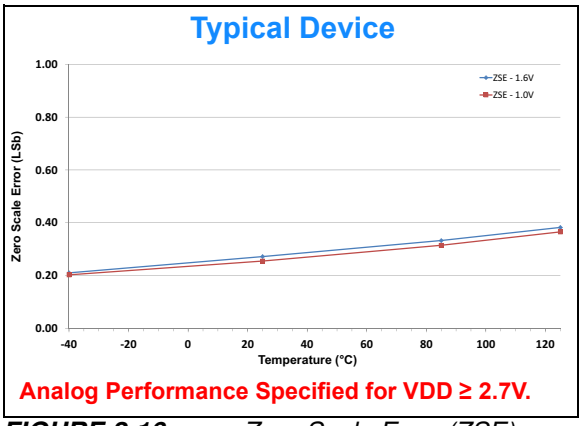


FIGURE 2-16: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

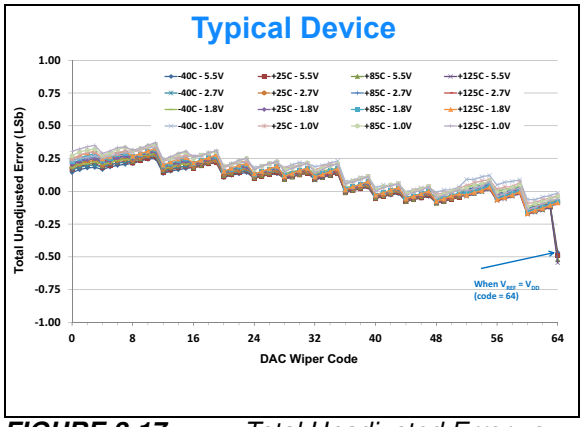


FIGURE 2-17: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.*

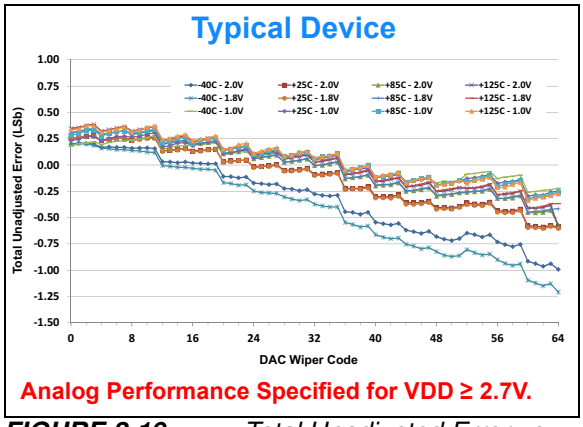


FIGURE 2-19: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.*

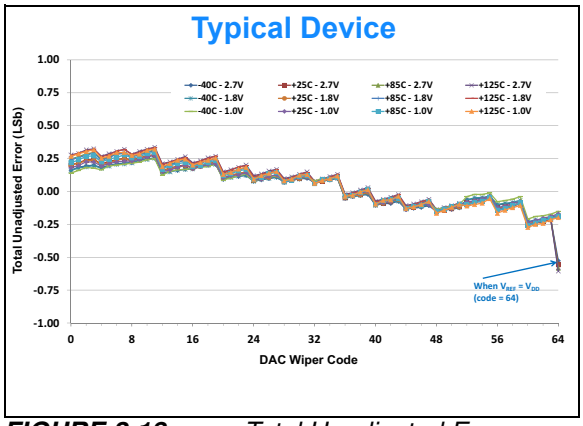


FIGURE 2-18: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.*

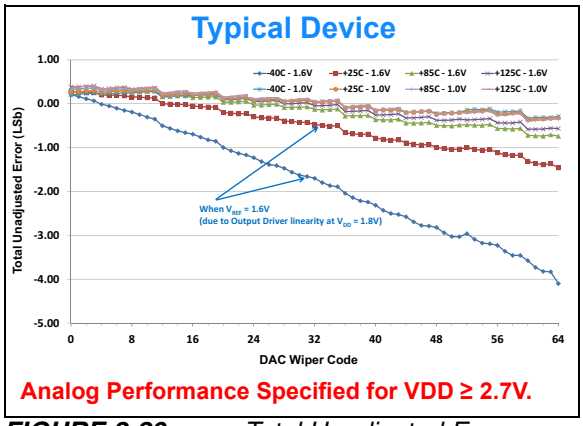


FIGURE 2-20: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

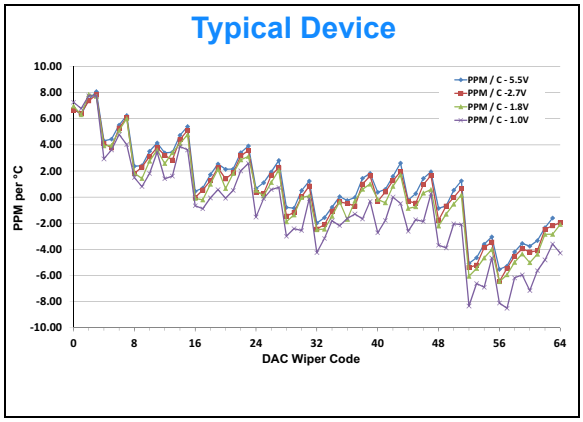


FIGURE 2-21: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000),*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

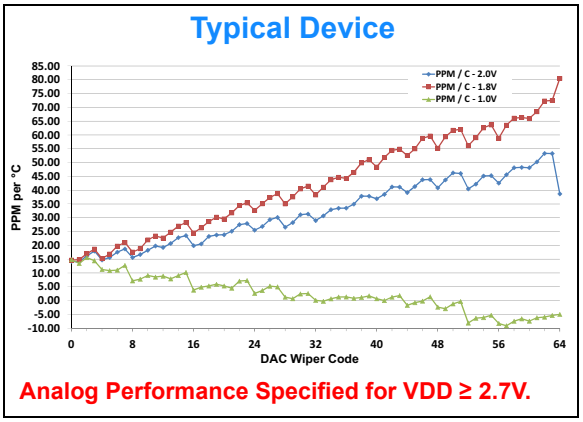


FIGURE 2-23: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000),*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

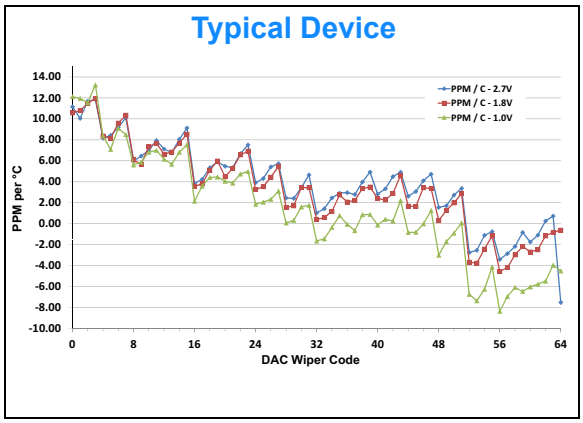


FIGURE 2-22: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000),*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

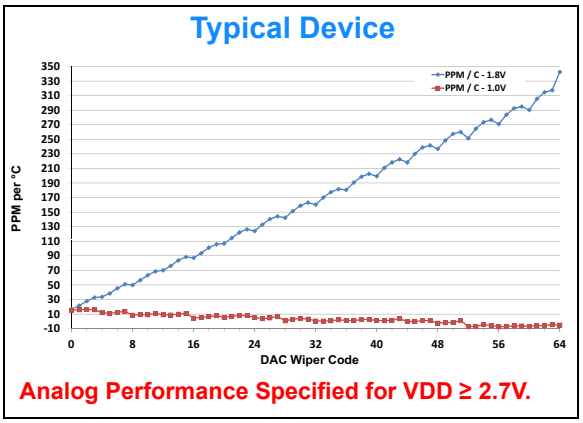


FIGURE 2-24: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000),*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

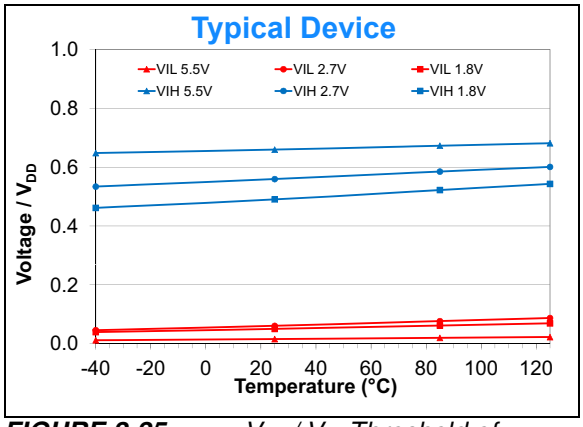


FIGURE 2-25: *V_{IH} / V_{IL} Threshold of SDA/SCL Inputs vs. Temperature and V_{DD}.*

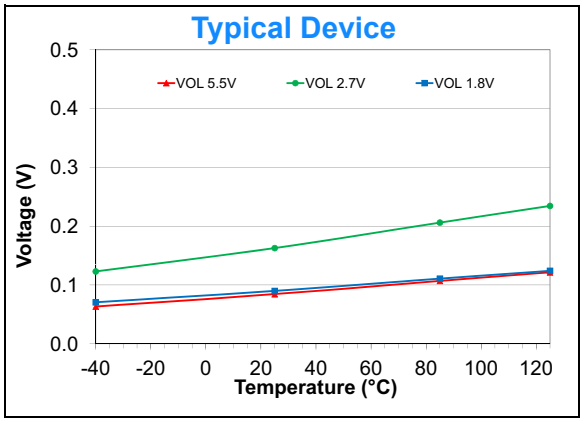


FIGURE 2-26: *V_{OL} (SDA) vs. V_{DD} and Temperature.*

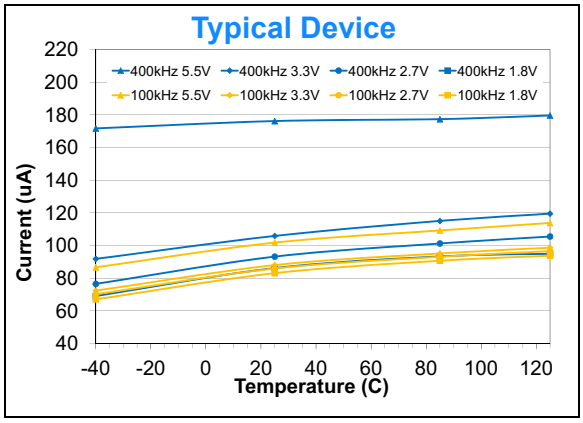


FIGURE 2-27: *Interface Active Current (I_{DD}) vs. SCL Frequency (f_{SCL}) and Temperature V_{DD} = 1.8V, 2.7V and 5.5V, V_{REF} = 1.0V and V_{DD}. (no load on V_{OUT}).*

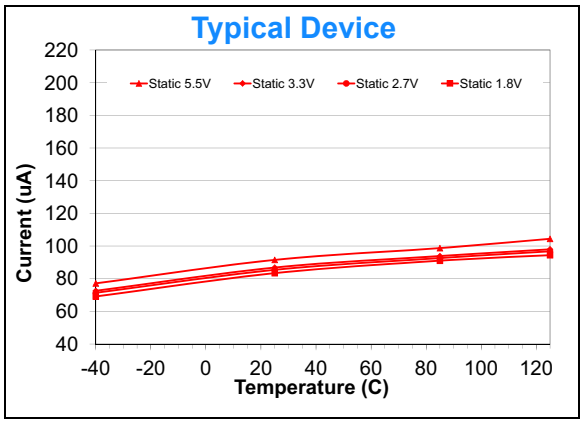


FIGURE 2-28: *Interface Inactive Current (STATIC) vs. Temperature and V_{DD}. V_{DD} = 1.8V, 2.7V and 5.5V, V_{REF} = 1.0V and V_{DD}. (no load on V_{OUT}, SCL = SDA = V_{DD}).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

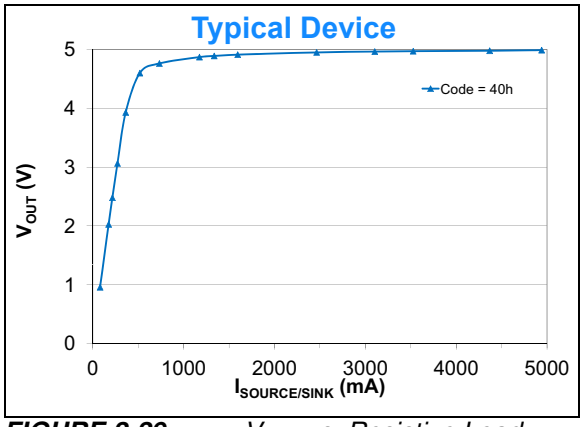


FIGURE 2-29: *V_{OUT} vs. Resistive Load. V_{DD} = 5.0V.*

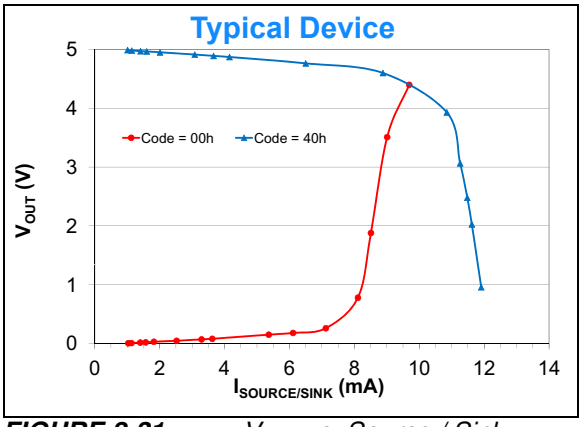


FIGURE 2-31: *V_{OUT} vs. Source / Sink Current. V_{DD} = 5.0V.*

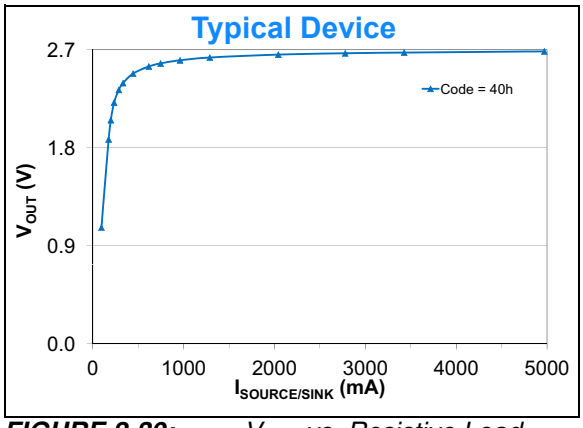


FIGURE 2-30: *V_{OUT} vs. Resistive Load. V_{DD} = 2.7V.*

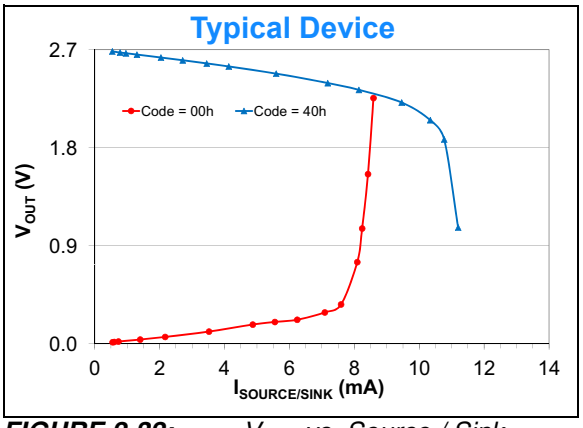


FIGURE 2-32: *V_{OUT} vs. Source / Sink Current. V_{DD} = 2.7V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

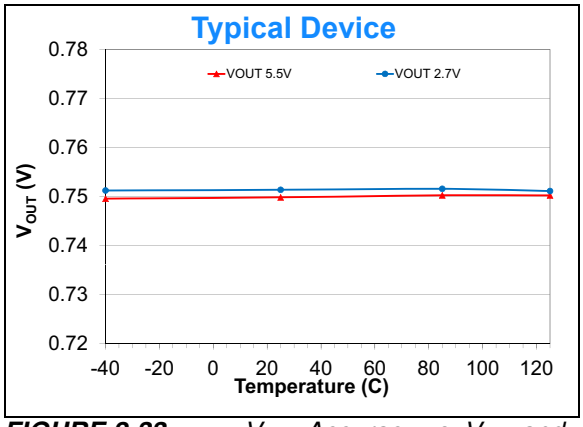


FIGURE 2-33: *V_{OUT} Accuracy vs. V_{DD} and Temperature.*

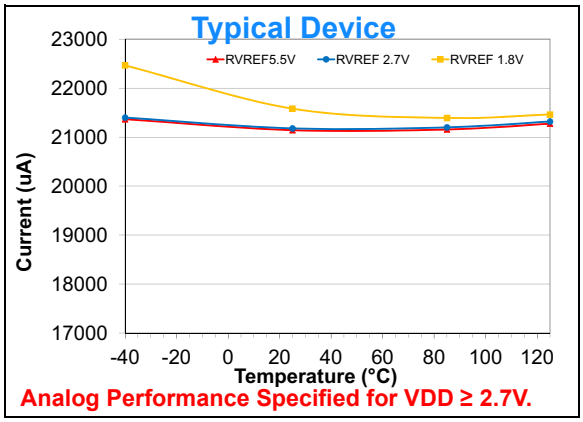


FIGURE 2-34: *R_{VREF} Resistances vs. V_{DD} and Temperature.*

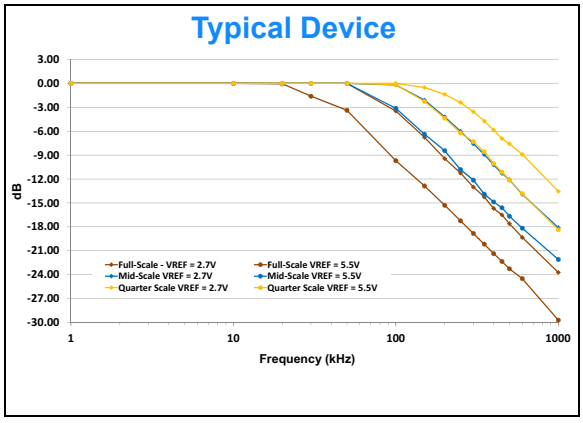


FIGURE 2-35: *-3dB Bandwidth vs Frequency, V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

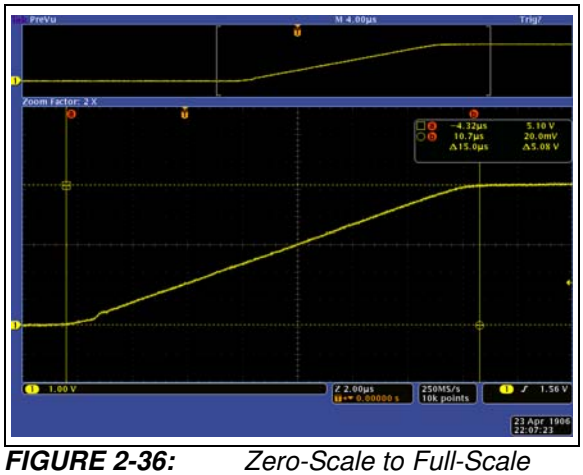


FIGURE 2-36: *Zero-Scale to Full-Scale Settling Time (00h to 40h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF (Time scale = 2 µs / div).*

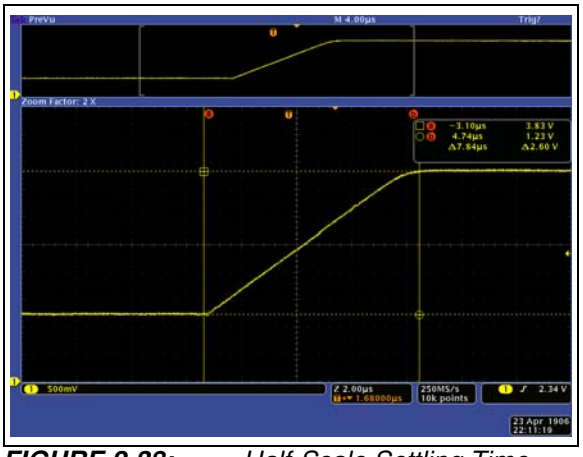


FIGURE 2-38: *Half-Scale Settling Time (10h to 30h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF. (Time scale = 2 µs / div)*

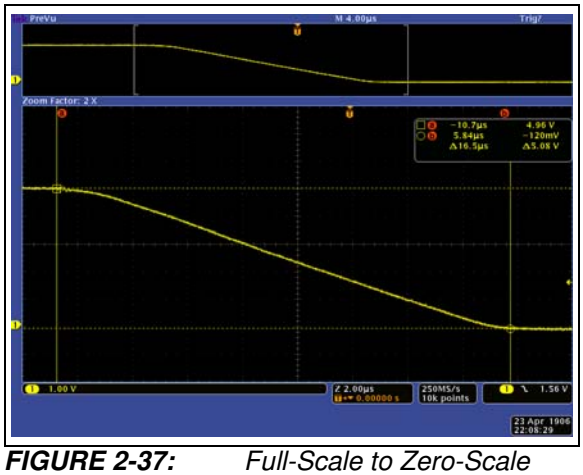


FIGURE 2-37: *Full-Scale to Zero-Scale Settling Time (40h to 00h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF (Time scale = 2 µs / div).*

FIGURE 2-39: *Half-Scale Settling Time (30h to 10h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF (Time scale = 2 µs / div).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

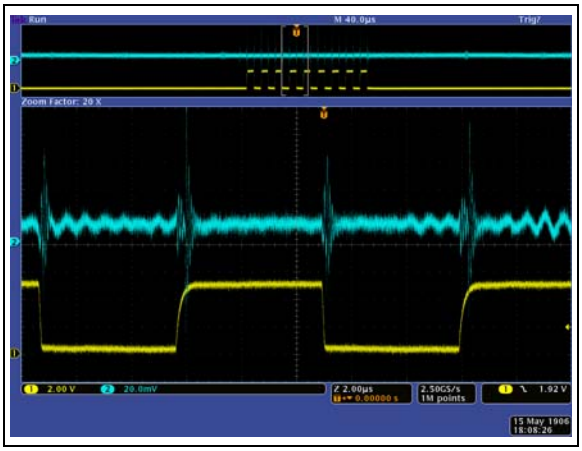


FIGURE 2-40: *Digital Feedthrough (SCL signal coupling to V_{OUT} pin); V_{DD} = 5.0V, V_{REF} = 5.0V, F_{SCL} = 100 kHz, V_{OUT} = 20h (V_{OUT} Voltage Scale = 20 mV/div, Time scale = 2 µs / div).*

2.1 Test Circuit

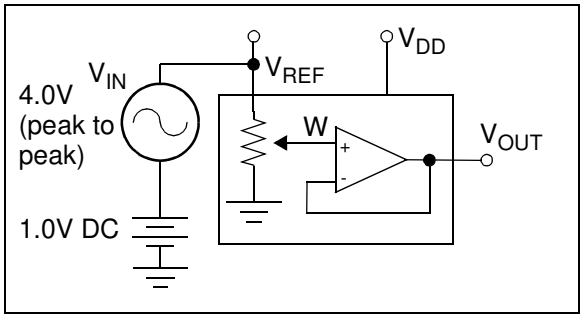


FIGURE 2-41: *-3 db Gain vs. Frequency Test.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1. Additional descriptions of the device pins follow.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP47A1

Pin Name	Package	Pin Type	Buffer Type	Function
	SC70-6			
V_{DD}	1	P	—	Positive Power Supply Input
V_{SS}	2	P	—	Ground
SCL	3	I/O	ST (OD)	I^2C Serial Clock pin
SDA	4	I/O	ST (OD)	I^2C Serial Data pin
V_{OUT}	5	I/O	A	Output voltage
V_{REF}	6	I/O	A	Reference Voltage for V_{OUT} output

Legend: A = Analog input, I = Input, ST (OD) = Schmitt Trigger with Open Drain, O = Output, I/O = Input/Output, P = Power

3.1 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device's positive power supply input. The input power supply is relative to V_{SS} and can range from 1.8V to 5.5V. A decoupling capacitor on V_{DD} (to V_{SS}) is recommended to achieve maximum performance. Analog specifications are tested from 2.7V.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.3 I^2C Serial Clock (SCL)

The SCL pin is the serial clock pin of the I^2C interface. The MCP47A1 acts only as a slave and the SCL pin accepts only external serial clocks. The SCL pin is an open-drain output. Refer to **Section 5.0 "Serial Interface - I^2C Module"** for more details of I^2C Serial Interface communication.

3.4 I^2C Serial Data (SDA)

The SDA pin is the serial data pin of the I^2C interface. The SDA pin has a Schmitt trigger input and an open-drain output. Refer to **Section 5.0 "Serial Interface - I^2C Module"** for more details of I^2C Serial Interface communication.

3.5 Analog Output Voltage Pin (V_{OUT})

V_{OUT} is the DAC analog output pin. The DAC output has an output amplifier.

V_{OUT} can swing from approximately V_{ZS} (= V_{SS}) to V_{FS} (= V_{REF}). In normal mode, the DC impedance of the output pin is about 1Ω . See **Section 7.0 "Output Buffer"** for more information.

3.6 Voltage Reference Pin (V_{REF})

This pin is the external voltage reference input. The V_{REF} pin signal is unbuffered so the reference voltage must have the current capability not to drop its voltage when connected to the internal resistor ladder circuit (20 kΩ typical). See **Section 6.0 "Resistor Network"** for more information.

NOTES:

4.0 GENERAL OVERVIEW

The MCP47A1 device is a general purpose DAC intended to be used in applications where a programmable voltage output with moderate bandwidth is desired.

Applications generally suited for the MCP47A1 devices include:

- Set point or offset trimming
- Sensor calibration
- Cost-sensitive mechanical trim pot replacement

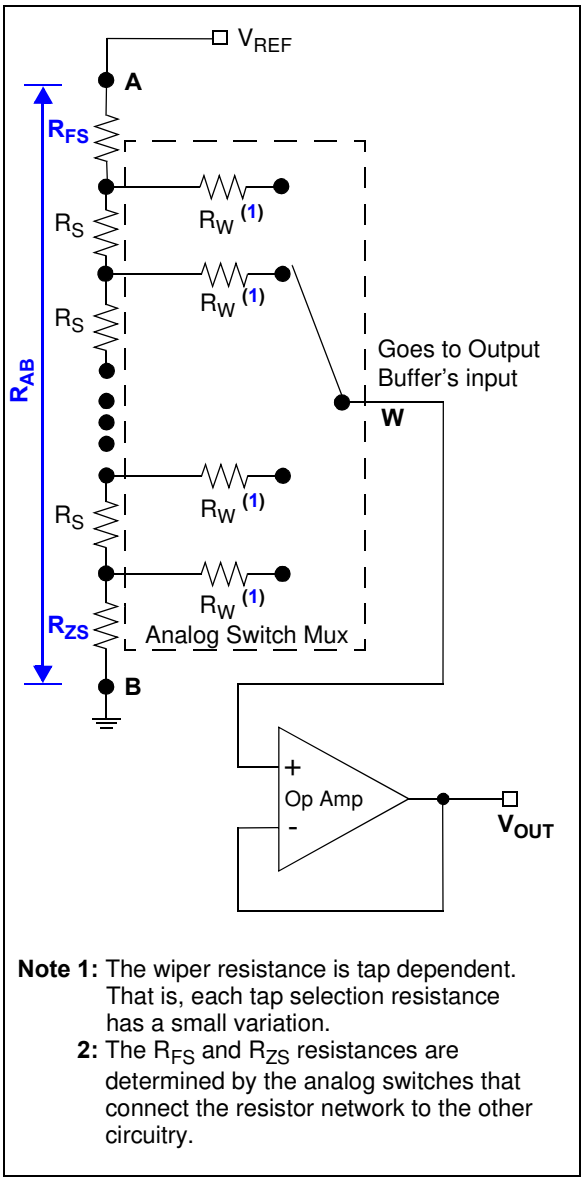
The MCP47A1 has four main functional blocks. These are:

- **POR/BOR Operation**
- **Serial Interface - I²C Module**
- **Resistor Network**
- **Output Buffer**

The POR/BOR operation is discussed in this section and the I²C and Resistor Network operation are described in their own sections. The commands are discussed in **Section 5.3, Serial Commands**.

Figure 4-1 shows a block diagram for the resistive network of the device. An external pin, called V_{REF}, is the DAC's reference voltage. The resistance from the V_{REF} pin to ground is typically 20 kΩ. The reference voltage connected to the V_{REF} pin needs to support this resistive load.

This resistor network functions as a windowed voltage divider. This means that the V_{OUT} pin's voltage range is from approximately V_{SS} to approximately V_{REF}.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation.
2: The R_{FS} and R_{ZS} resistances are determined by the analog switches that connect the resistor network to the other circuitry.

FIGURE 4-1: *Resistor Network and Output Buffer Block Diagram.*