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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP47FEBXX

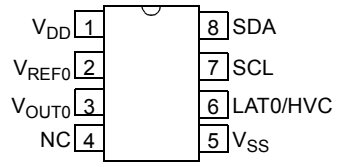
8-/10-/12-Bit Single/Dual Voltage Output Nonvolatile Digital-to-Analog Converters with I²C™ Interface

Features

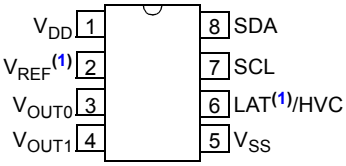
- Operating Voltage Range:
  - 2.7V to 5.5V - Full Specifications
  - 1.8V to 2.7V - Reduced Device Specifications
- Output Voltage Resolutions:
  - 8-bit: **MCP47FEB0X** (256 Steps)
  - 10-bit: **MCP47FEB1X** (1024 Steps)
  - 12-bit: **MCP47FEB2X** (4096 Steps)
- Rail-to-Rail Output
- Fast Settling Time of 6 µs (typical)
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal Band Gap (1.22V typical)
- Output Gain Options:
  - Unity (1x)
  - 2x (when not using internal V_{DD} as voltage source)
- Nonvolatile Memory (EEPROM):
  - User-programmed Power-on Reset (POR)/Brown-out Reset (BOR) output setting recall and device configuration bits
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power-Down)
- Power-on/Brown-out Reset Protection
- Nonvolatile Memory Write Protect ($\overline{WP}$) Bit
- Power-Down Modes:
  - Disconnects output buffer (High Impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- Low Power Consumption:
  - Normal operation: <180 µA (Single), 380 µA (Dual)
  - Power-down operation: 650 nA typical
  - EEPROM write cycle (1.9 mA maximum)
- I²C™ Interface:
  - Slave address options: four predefined addresses or user programmable (all 7 bits)
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (up to 3.4 Mbps) modes
- Package Types: 8-lead TSSOP
- Extended Temperature Range: -40°C to +125°C

Package Types

MCP47FEBX1
TSSOP
Single



MCP47FEBX2
TSSOP
Dual



Note 1: This pin's signal can be connected to DAC0 and/or DAC1.

General Description

The MCP47FEBXX are Single- and Dual-channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an I²C serial interface.

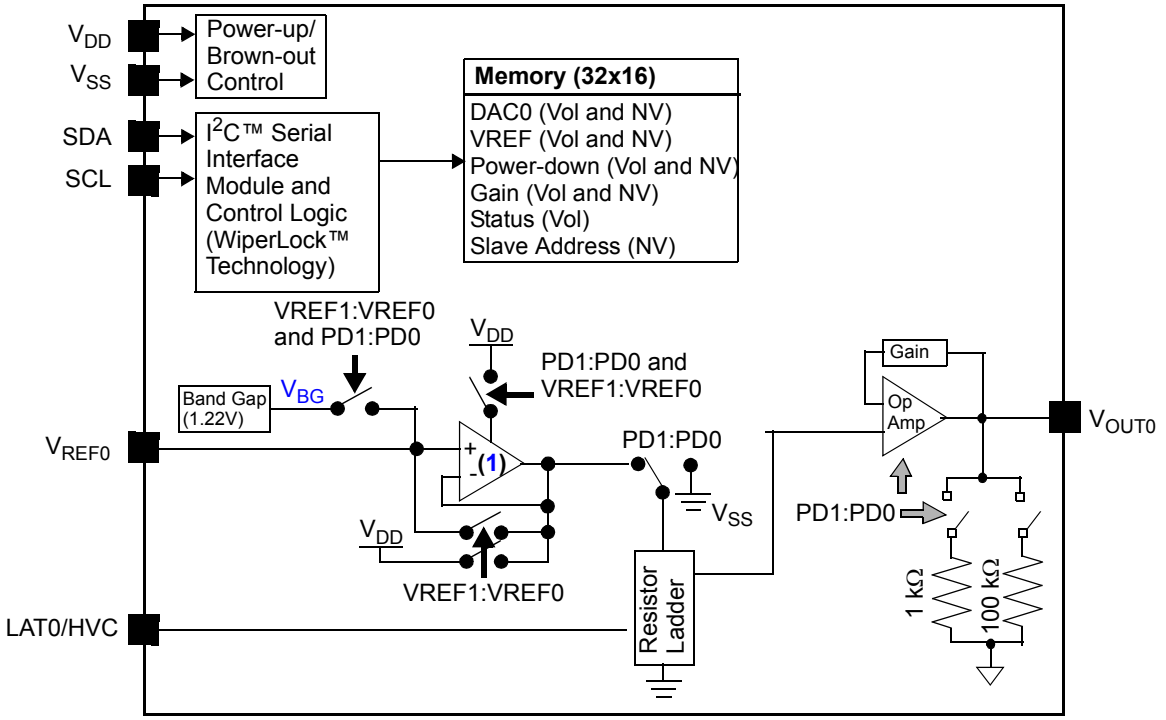
The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is connected internally to the DAC reference circuit. When the V_{REF} pin is used, the user can select the output buffer's gain to be 1 or 2. When the gain is 2, the V_{REF} pin voltage should be limited to a maximum of $V_{DD}/2$.

These devices have a two-wire I²C-compatible serial interface for Standard (100 kHz), Fast (400 kHz) or High-Speed (1.7 MHz and 3.4 MHz) modes.

Applications

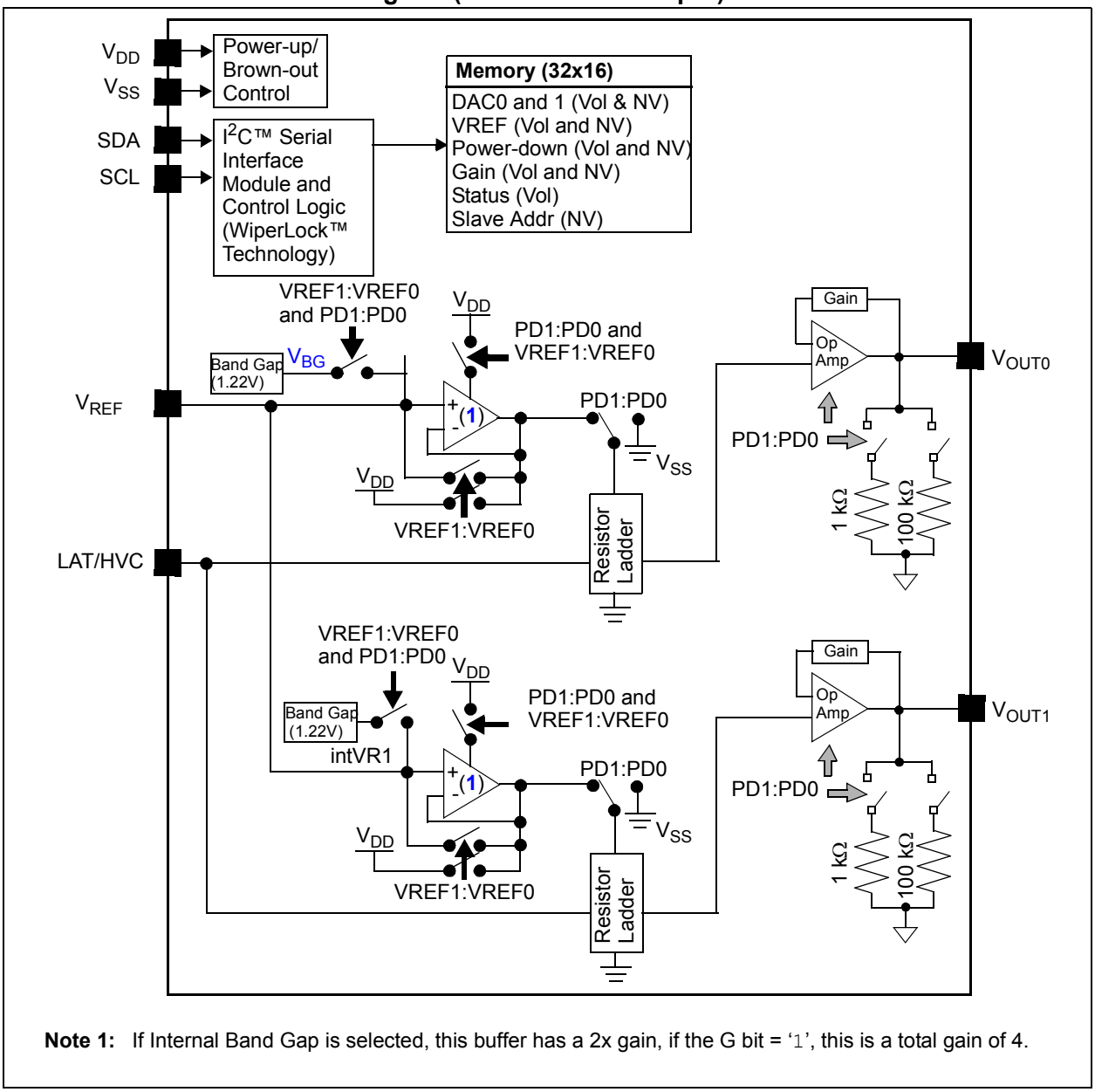
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

MCP47FEBX1 Device Block Diagram (Single-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain. If the G bit = '1', this is a total gain of 4.

MCP47FEBX2 Device Block Diagram (Dual-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain, if the G bit = '1', this is a total gain of 4.

Device Features

Device	# of Channels	Resolution (bits)	Control Interface	DAC Output POR/BOR Setting (1)	# of VREF Inputs	Internal band gap ?	# of LAT Inputs	Memory	Specified Operating Range (V_{DD})
MCP47FEB01	1	8	I²C™	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB11	1	10	I²C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB21	1	12	I²C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB02	2	8	I²C	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB12	2	10	I²C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB22	2	12	I²C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V

Note 1: The Factory Default value. The DAC output POR/BOR value can be modified via the nonvolatile DAC output register(s).

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +6.5V

Voltage on all pins with respect to V_{SS} ..... -0.6V to V_{DD}+0.3V

Input clamp current, I_{IK} (V_I < 0, V_I > V_{DD}, V_I > V_{PP} on HV pins) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum current out of V_{SS} pin (Single) ..... 50 mA
(Dual) ..... 100 mA

Maximum current into V_{DD} pin (Single) ..... 50 mA
(Dual) ..... 100 mA

Maximum current sourced by the V_{OUT} pin ..... 20 mA

Maximum current sunk by the V_{OUT} pin ..... 20 mA

Maximum current sunk by the V_{REF} pin ..... 125 µA

Maximum input current source/sunk by SDA, SCL pins ..... 2 mA

Maximum output current sunk by SDA Output pin ..... 25 mA

Total power dissipation (1) ..... 400 mW

Package power dissipation (T_A = +50°C, T_J = +150°C)
TSSOP-8 ..... 700 mW

ESD protection on all pins ..... ≥ ±4 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±2 kV (CDM)

Latch-Up (per JEDEC JESD78A) @ +125°C ..... ±100 mA

Storage temperature ..... -65°C to +150°C

Ambient temperature with power applied ..... -55°C to +125°C

Soldering temperature of leads (10 seconds) ..... +300°C

Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and Serial Interface
V_{DD} Voltage (rising) to ensure device Power-on Reset	$V_{POR/BOR}$	—	—	1.7	V	RAM retention voltage (V_{RAM}) < V_{POR} V_{DD} voltages greater than $V_{POR/BOR}$ limit ensure that device is out of reset.
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 3**)			V/ms	
High-Voltage Commands Voltage Range (HVC pin)	V_{HV}	V_{SS}	—	12.5	V	The HVC pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}) (1)
High-Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	—	V	Threshold for Entry into WiperLock™ Technology
High-Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V	V	**(Note 1)**
Power-on Reset to Output-Driven Delay	T_{PORD}	—	25	50	µs	V_{DD} rising, V_{DD} > V_{POR}

Note 1 This parameter is ensured by design.

Note 3 POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Supply Current	I_{DD}	—	—	500	µA	Single	Serial Interface Active (Not High-Voltage Command), VRxB:VRxA = '01' (6), V_{OUT} is unloaded, V_{DD} = 5.5V volatile DAC Register = 000h I^2C™: F_{SCL} = 3.4 MHz
		—	—	700	µA	Dual	
		—	—	400	µA	Single	Serial Interface Active (2) (Not High-Voltage Command), VRxB:VRxA = '10' (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V volatile DAC Register = 000h I^2C: F_{SCL} = 3.4 MHz
		—	—	550	µA	Dual	
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command), VRxB:VRxA = '00', SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 000h
		—	—	380	µA	Dual	
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command), VRxB:VRxA = '11', V_{REF} = V_{DD}, SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 000h
		—	—	380	µA	Dual	
		—	—	1.9	mA	EE Write Current V_{REF} = V_{DD} = 5.5V (after write, Serial Interface is Inactive), write all 0's to nonvolatile DAC 0 (address 10h), V_{OUT} pins are unloaded.	
		—	145	180	µA	Single	HVC = 12.5V (High-Voltage Command), Serial Interface Inactive V_{REF} = V_{DD} = 5.5V, LAT/HVC = V_{IHH}, DAC registers = 000h, V_{OUT} pins are unloaded.
		—	260	400	µA	Dual	
Power-Down Current	I_{DDP}	—	0.65	3.8	µA	PDxB:PDxA = '01' (5), V_{OUT} not connected	

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = '10'.

Note 5 The PDxB:PDxA = '01', '10', and '11' configurations should have the same current.

Note 6 By design, this is worst-case current mode.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Resistor Ladder Resistance	R_L	100	140	180	kΩ	1.8V ≤ V_{DD} ≤ 5.5V, V_{REF} ≥ 1.0V(7)	
Resolution (# of Resistors and # of Taps) (see C.1 "Resolution")	N	256			Taps	8-bit	No Missing Codes
		1024			Taps	10-bit	No Missing Codes
		4096			Taps	12-bit	No Missing Codes
Nominal V_{OUT} Match (12)	$\lvert V_{OUT} - V_{OUTMEAN} \rvert / V_{OUTMEAN}$	—	0.5	1.0	%	2.7V ≤ V_{DD} ≤ 5.5V(2)	
		—	—	1.2	%	1.8V(2)	
V_{OUT} Tempco (see C.19 "V_{OUT} Temperature Coefficient")	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (7Fh, 1FFh or 7FFh)	
V_{REF} pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V(1)	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 7 Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP47FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.

Note 12 Variation of one output voltage to mean output voltage.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Zero-Scale Error (see **C.5 "Zero-Scale Error (EZS)"**) (Code = 000h)	E_{ZS}	—	—	0.75	LSb	8-bit	VRxB:VRxA = '11', Gx = '0', V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0', V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0', No Load
		—	—	3	LSb	10-bit	VRxB:VRxA = '11', Gx = '0', V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0', V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0', No Load
		—	—	12	LSb	12-bit	VRxB:VRxA = '11', Gx = '0', V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0', V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0', No Load
Offset Error (see **C.7 "Offset Error (EOS)"**)	E_{OS}	-15	±1.5	+15	mV	VRxB:VRxA = '00', Gx = '0', No Load	
Offset Voltage Temperature Coefficient	V_{OSTC}	—	±10	—	µV/°C		

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Full-Scale Error (see **C.4 "Full-Scale Error (EFS)"**)	E_{FS}	—	—	4.5	LSb	8-bit	Code = FFh, VRxB:VRxA = '11', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = FFh, VRxB:VRxA = '10', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = FFh, VRxB:VRxA = '01', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = FFh, VRxB:VRxA = '00', No Load
		—	—	18	LSb	10-bit	Code = 3FFh, VRxB:VRxA = '11', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = 3FFh, VRxB:VRxA = '10', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = 3FFh, VRxB:VRxA = '01', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = 3FFh, VRxB:VRxA = '00', No Load
		—	—	70	LSb	12-bit	Code = FFFh, VRxB:VRxA = '11', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = FFFh, VRxB:VRxA = '10', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = FFFh, VRxB:VRxA = '01', Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Code = FFFh, VRxB:VRxA = '00', No Load

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Gain Error (see **C.9 "Gain Error (EG)"**)[9]	E_G	-1.0	±0.1	+1.0	% of FSR	8-bit	Code = 250, No Load VRxB:VRxA = '00', Gx = '0'
		-1.0	±0.1	+1.0	% of FSR	10-bit	Code = 1000, No Load VRxB:VRxA = '00', Gx = '0'
		-1.0	±0.1	+1.0	% of FSR	12-bit	Code = 4000, No Load VRxB:VRxA = '00', Gx = '0'
Gain-Error Drift (see **C.10 "Gain-Error Drift (EGD)"**)	ΔG/°C	—	-3	—	ppm/°C		
Total Unadjusted Error (see **C.6 "Total Unadjusted Error (ET)"**)[2]	E_T	-2.5	—	+0.5	LSb	8-bit	VRxB:VRxA = '00'. No Load.
		See **Section 2.0 "Typical Performance Curves"**			LSb		V_{DD} = 1.8V, VRxB:VRxA = '11', Gx = '0', V_{REF} = 1.0V, No Load.
		-10.0	—	+2.0	LSb	10-bit	VRxB:VRxA = '00'. No Load.
		See **Section 2.0 "Typical Performance Curves"**			LSb		V_{DD} = 1.8V, VRxB:VRxA = '11', Gx = '0', V_{REF} = 1.0V, No Load.
		-40.0	—	+8.0	LSb	12-bit	VRxB:VRxA = '00'. No Load.
		See **Section 2.0 "Typical Performance Curves"**			LSb		V_{DD} = 1.8V, VRxB:VRxA = '11', Gx = '0', V_{REF} = 1.0V, No Load.

Note 2 This parameter is ensured by characterization.

Note 9 This gain error does not include offset error.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Integral Nonlinearity (see **C.11 "Integral Nonlinearity (INL)"**)[8, 11]	INL	-0.5	±0.1	+0.5	LSb	8-bit	VRxB:VRxA = '10' (codes: 6 to 250), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '00', '01', '11'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '01', V_{DD} = 5.5V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '10', '11', V_{REF} = 1.0V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V
		-1.5	±0.4	+1.5	LSb	10-bit	VRxB:VRxA = '10' (codes: 25 to 1000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '00', '01', '11'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '01', V_{DD} = 5.5V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '10', '11', V_{REF} = 1.0V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V.
		-6	±1.5	+6	LSb	12-bit	VRxB:VRxA = '10' (codes: 100 to 4000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '00', '01', '11'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '01', V_{DD} = 5.5V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRxB:VRxA = '10', '11', V_{REF} = 1.0V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V.

Note 2 This parameter is ensured by characterization.

Note 8 INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRxB:VRxA = '00').

Note 11 Code Range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Differential Nonlinearity (see **C.12 "Differential Nonlinearity (DNL)"**)(8, 11)	DNL	-0.25	±0.0125	+0.25	LSb	8-bit	VRxB:VRxA = '10' (codes: 6 to 250), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '00', '01', '11'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '01', V_{DD} = 5.5V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '10', '11', V_{REF} = 1.0V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V
		-0.5	±0.05	+0.5	LSb	10-bit	VRxB:VRxA = '10' (codes: 25 to 1000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '00', '01', '11'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '01', V_{DD} = 5.5V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '10', '11', V_{REF} = 1.0V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V
		-1.0	±0.2	+1.0	LSb	12-bit	VRxB:VRxA = '10' (codes: 100 to 4000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '00', '01', '11'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '01', V_{DD} = 5.5V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		Char: VRxB:VRxA = '10', '11', V_{REF} = 1.0V, Gx = '1'.
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V

Note 2 This parameter is ensured by characterization.

Note 8 INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRxB:VRxA = '00').

Note 11 Code Range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
-3 dB Bandwidth (see **C.16 "-3 dB Bandwidth"**)	BW	—	86.5	—	kHz	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = '10', Gx = '0'
		—	67.7	—	kHz	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = '10', Gx = '1'
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	1.8V ≤ V_{DD} < 5.5V, Output Amplifier's minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.04	—	V	1.8V ≤ V_{DD} < 5.5V, Output Amplifier's maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate (10)	SR	—	0.44	—	V/µs	R_L = 5 kΩ
Short-Circuit Current	I_{SC}	3	9	14	mA	DAC code = Full Scale
Internal Band Gap						
Band Gap Voltage	V_{BG}	1.18	1.22	1.26	V	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	15	—	ppm/°C	
Operating Range (V_{DD})		2.0	—	5.5	V	V_{REF} pin voltage stable
		2.2	—	5.5	V	V_{OUT} output linear
External Reference (V_{REF})						
Input Range (1)	V_{REF}	V_{SS}	—	V_{DD} – 0.04	V	VRxB:VRxA = '11' (buffered mode)
		V_{SS}	—	V_{DD}	V	VRxB:VRxA = '10' (unbuffered mode)
Input Capacitance	C_{REF}	—	1	—	pF	VRxB:VRxA = '10' (unbuffered mode)
Total Harmonic Distortion (1)	THD	—	-64	—	dB	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = '10', Gx = '0', Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **C.14 "Major-Code Transition Glitch"**)		—	45	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **C.15 "Digital Feed-through"**)		—	<10	—	nV-s	

Note 1 This parameter is ensured by design.

Note 10 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Inputs/Outputs (LAT0/HVC)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V (Allows 2.7V Digital V_{DD} with 5V Analog V_{DD})
		0.5 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low-Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 3.4 MHz
Digital Interface (SDA, SCL)						
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA
		—	—	0.2 V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	0.3 V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V
Input Leakage	I_{LI}	-1	—	1	µA	SCL = SDA = V_{SS} or SCL = SDA = V_{DD}
Pin Capacitance	C_{PIN}	—	10	—	pF	f_C = 3.4 MHz

Note 1 This parameter is ensured by design.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
RAM Value							
Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	3FFh	hex	10-bit	
		0h	—	FFFh	hex	12-bit	
DAC Register POR/BOR Value	N	See **Table 4-2**			hex	8-bit	
		See **Table 4-2**			hex	10-bit	
		See **Table 4-2**			hex	12-bit	
PDCON Initial Factory Setting		See **Table 4-2**			hex		
EEPROM							
Endurance	EN_{EE}	—	1M	—	Cycles	**Note 1**, **Note 2**	
Data Retention	DR_{EE}	—	200	—	Years	At +25°C(**1**, **2**)	
EEPROM Range	N	0h	—	FFh	hex	8-bit	DACx Register(s)
		0h	—	3FFh	hex	10-bit	DACx Register(s)
		0h	—	FFFh	hex	12-bit	DACx Register(s)
Initial Factory Setting	N	See **Table 4-2**					
EEPROM Programming Write Cycle Time	t_{WC}	—	11	16	ms	V_{DD} = +1.8V to 5.5V	
Power Requirements							
Power Supply Sensitivity (**C.17 "Power-Supply Sensitivity (PSS)"**)	PSS	—	0.002	0.005	%/%	8-bit	Code = 7Fh
		—	0.002	0.005	%/%	10-bit	Code = 1FFh
		—	0.002	0.005	%/%	12-bit	Code = 7FFh

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = '10'.
5. The PDxB:PDxA = '01', '10', and '11' configurations should have the same current.
6. By design, this is worst-case current mode.
7. Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP47FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.
8. INL and DNL are measured at V_{OUT} with $V_{RL} = V_{DD}$ (VRxB:VRxA = '00').
9. This gain error does not include offset error.
10. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
11. Code Range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.
12. Variation of one output voltage to mean output voltage.

1.1 Timing Waveforms and Requirements

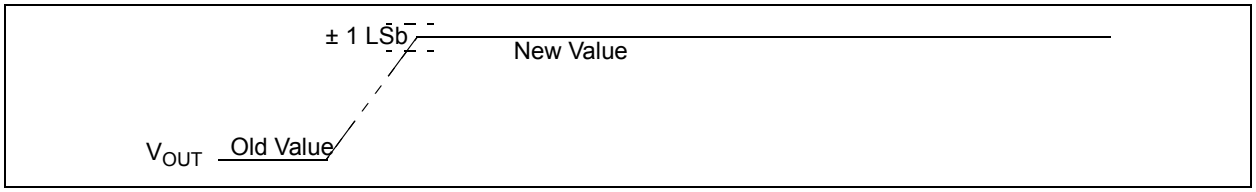


FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +1.8V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (±1LSb error band, C_L = 100 pF) (see **C.13 "Settling Time"**)	t_S	—	6	—	µs	8-bit	Code = 3Fh → BFh; BFh → 3Fh(1)
		—	6	—	µs	10-bit	Code = 0FFh → 2FFh; 2FFh → 0FFh(1)
		—	6	—	µs	12-bit	Code = 3FFh → BFFh; BFFh → 3FFh(1)

Note 1 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).

1.2 I²C Mode Timing Waveforms and Requirements

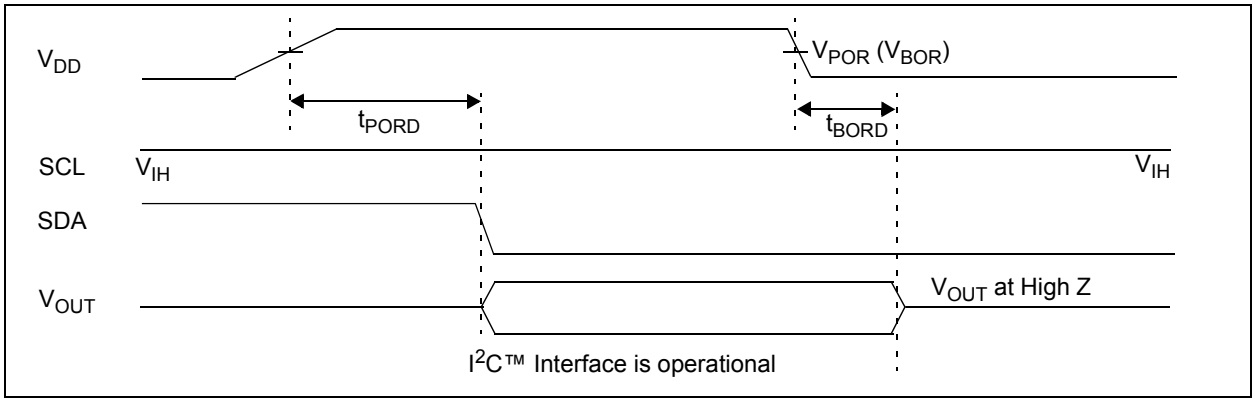


FIGURE 1-2: *Power-on and Brown-out Reset Waveforms.*

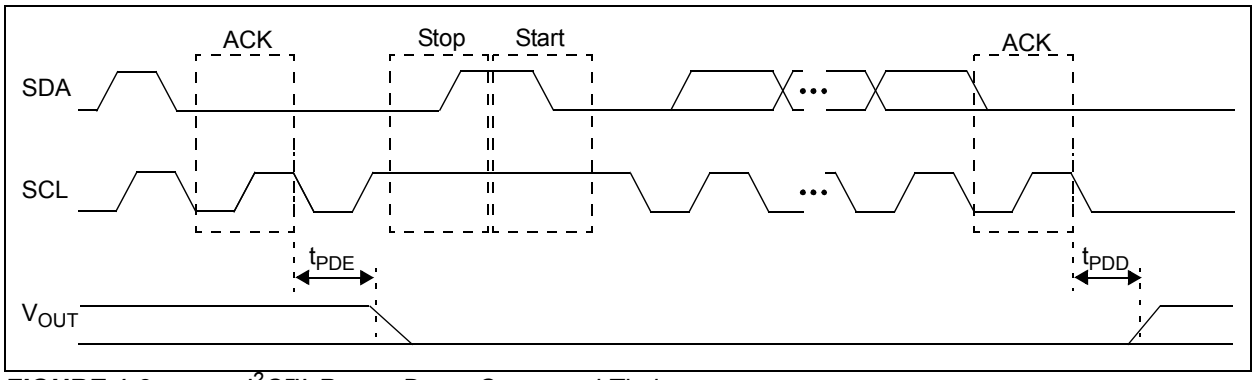


FIGURE 1-3: *I²C™ Power-Down Command Timing.*

TABLE 1-2: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +1.8V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power-on Reset Delay	t_{PORD}	—	60	—	µs	Monitor ACK bit response to ensure device responds to command.
Brown-out Reset Delay	t_{BORD}	—	45	—	µs	V_{DD} transitions from $V_{DD(MIN)} \rightarrow > V_{POR}$ V_{OUT} driven to V_{OUT} disabled
Power-Down Output Disable Time Delay	T_{PDD}	—	10.5	—	µs	PDxB:PDxA = '11', '10', or '01' -> "00" started from falling edge of the SCL at the end of the 8th clock cycle. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.
Power-Down Output Enable Time Delay	T_{PDE}	—	1	—	µs	PDxB:PDxA = "00" → '11', '10', or '01' started from falling edge of the SCL at the end of the 8th clock cycle. V_{OUT} = V_{OUT} - 10 mV. V_{OUT} not connected.

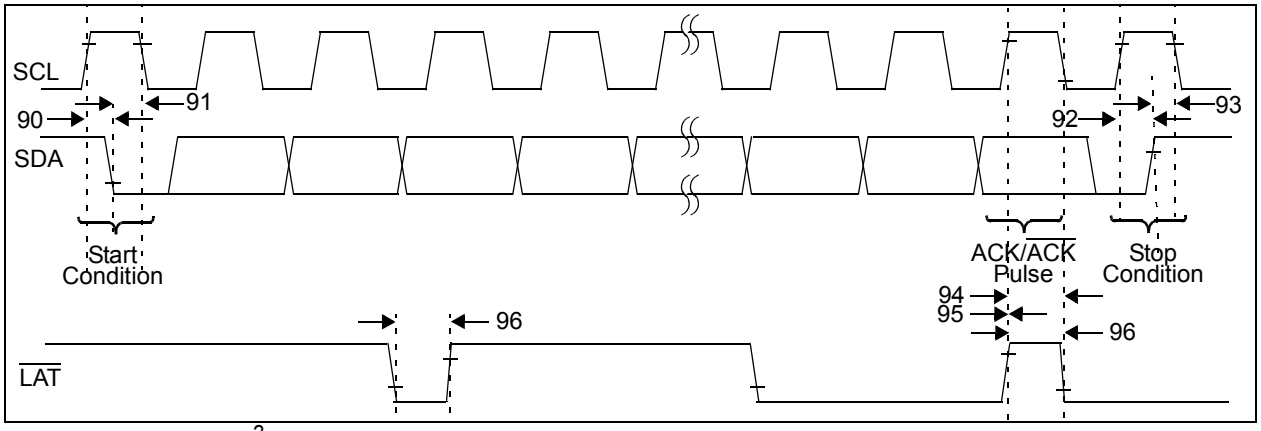


FIGURE 1-4: *I^2C™ Bus Start/Stop Bits Timing Waveforms.*

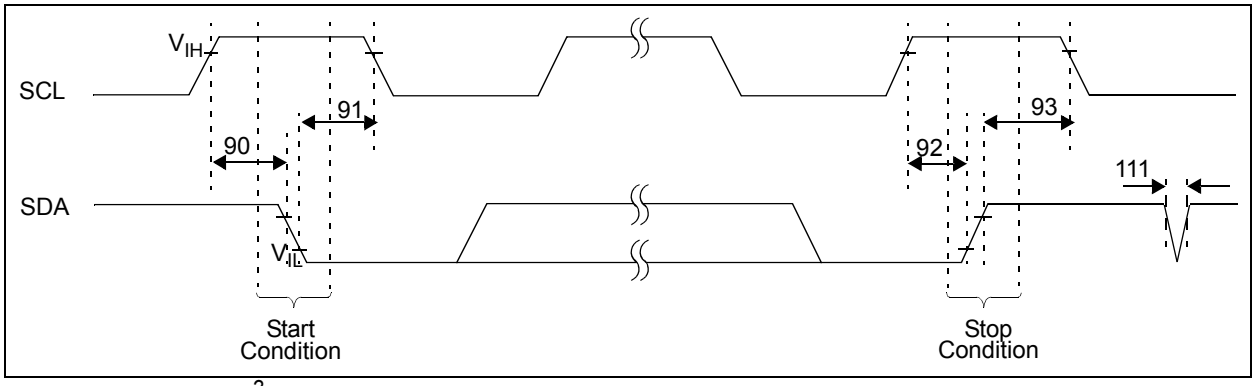


FIGURE 1-5: *I^2C™ Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-3: I²C BUS START/STOP BITS AND $\overline{LAT}$ REQUIREMENTS

I²C™ AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage range is described in DC Characteristics			
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V(2)
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	C_b	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	$T_{SU:STA}$	Start Condition Setup Time (Only relevant for repeated Start condition)	100 kHz mode	4700	—	ns	Note 2
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	$T_{HD:STA}$	Start Condition Hold time (After this period the first clock pulse is generated)	100 kHz mode	4000	—	ns	Note 2
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4000	—	ns	Note 2
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	4000	—	ns	Note 2
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
94	T_{LATSU}	$\overline{LAT}$ ↑ to SCL↑ (write data ACK bit) Setup Time		10	—	ns	Write Data delayed(3)
95	T_{LATHD}	SCL ↑ to $\overline{LAT}$↑ (write data ACK bit) Hold Time		250	—	ns	Write Data delayed(3)
96	T_{LAT}	$\overline{LAT}$ High or Low Time		50	—	ns	
97	T_{HVCSU}	HVC High to SCL High (of Start condition) - Setup Time		25	—	µs	High-Voltage Commands
98	T_{HVCHD}	SCL Low (of Stop condition) to HVC Low - Hold Time		25	—	µs	High-Voltage Commands

Note 2 Not Tested. This parameter ensured by characterization.

Note 3 The transition of the LAT signal between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal is indeterminate whether the change in V_{OUT} is delayed or not.

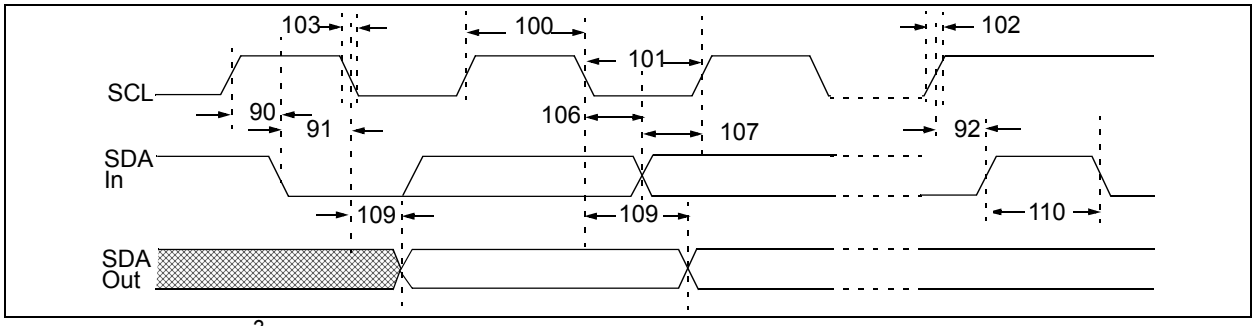


FIGURE 1-6: *I^2C™ Bus Timing Waveforms.*

TABLE 1-4: I^2C BUS REQUIREMENTS (SLAVE MODE)

I^2C™ AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**				
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
100	T_{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V(2)
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120	—	ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	T_{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V(2)
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320	—	ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V
102A(2)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B(2)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	

Note 2 Not Tested. This parameter ensured by characterization.

TABLE 1-5: I²C BUS REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C™ AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage range is described in DC Characteristics			
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
103A(2)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B (2)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V(2, 5)
			400 kHz mode	0	—	ns	2.7V-5.5V(5)
			1.7 MHz mode	0	—	ns	4.5V-5.5V(5)
			3.4 MHz mode	0	—	ns	4.5V-5.5V(5)
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	Note 2, Note 6
			400 kHz mode	100	—	ns	Note 6
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	Note 2, Note 7
			400 kHz mode	—	900	ns	Note 7
			1.7 MHz mode	—	150	ns	C_b = 100 pF(7, 8)
				—	310	ns	C_b = 400 pF(2, 7)
			3.4 MHz mode	—	150	ns	C_b = 100 pF(7)
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start(2)
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
111	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP Spec states N.A.(2)
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression

Note 2 Not Tested. This parameter ensured by characterization.

Note 4 Use Cb in pF for the calculations.

Note 5 A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

Note 6 A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

Note 7 As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

Note 8 Ensured by the T_{AA} 3.4 MHz specification test.

Timing Table Notes:

1. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).
2. Not Tested. This parameter ensured by characterization.
3. The transition of the LAT signal between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal is indeterminate whether the change in V_{OUT} is delayed or not.
4. Use Cb in pF for the calculations.
5. A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
6. A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line
   T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.
7. As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
8. Ensured by the T_{AA} 3.4 MHz specification test.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	139	—	°C/W	

Note 1: The MCP47FEBXX devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.