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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MICROCHIP MCP4801/4811/4821

8/10/12-Bit Voltage Output Digital-to-Analog Converter with Internal V_{REF} and SPI Interface

Features

- MCP4801: 8-Bit Voltage Output DAC
- MCP4811: 10-Bit Voltage Output DAC
- MCP4821: 12-Bit Voltage Output DAC
- Rail-to-Rail Output
- SPI Interface with 20 MHz Clock Support
- Simultaneous Latching of the DAC Output with $\overline{LDAC}$ Pin
- Fast Settling Time of 4.5 µs
- Selectable Unity or 2x Gain Output
- 2.048V Internal Voltage Reference
- 50 ppm/°C V_{REF} Temperature Coefficient
- 2.7V to 5.5V Single-Supply Operation
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Precision Selectable Voltage Reference
- Portable Instrumentation (Battery-Powered)
- Calibration of Optical Communication Devices

Related Products(1)

P/N	DAC Resolution	No. of Channel	Voltage Reference (V_{REF})
MCP4801	**8**	**1**	Internal (2.048V)
MCP4811	**10**	**1**	
MCP4821	**12**	**1**	
MCP4802	8	2	
MCP4812	10	2	
MCP4822	12	2	
MCP4901	8	1	External
MCP4911	10	1	
MCP4921	12	1	
MCP4902	8	2	
MCP4912	10	2	
MCP4922	12	2	

Note 1: The products listed here have similar AC/DC performances.

Description

The MCP4801/4811/4821 devices are single channel 8-bit, 10-bit and 12-bit buffered voltage output Digital-to-Analog Converters (DACs), respectively. The devices operate from a single 2.7V to 5.5V supply with an SPI compatible Serial Peripheral Interface.

The devices have a high precision internal voltage reference (V_{REF} = 2.048V). The user can configure the full-scale range of the device to be 2.048V or 4.096V by setting the Gain Selection Option bit (gain of 1 of 2).

The devices can be operated in Active or Shutdown mode by setting a Configuration register bit or using the $\overline{SHDN}$ pin. In Shutdown mode, most of the internal circuits, including the output amplifier, are turned off for power savings, while the amplifier output (V_{OUT}) stage is configured to present a known high resistance output load (500 kΩ, typical).

The devices include double-buffered registers, allowing a synchronous update of the DAC output using the $\overline{LDAC}$ pin. These devices also incorporate a Power-on Reset (POR) circuit to ensure reliable power-up.

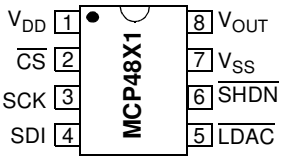
The devices utilize a resistive string architecture, with its inherent advantages of low DNL error, low ratio metric temperature coefficient and fast settling time. These devices are specified over the extended temperature range (+125°C).

The devices provide high accuracy and low noise performance for consumer and industrial applications where calibration or compensation of signals (such as temperature, pressure and humidity) are required.

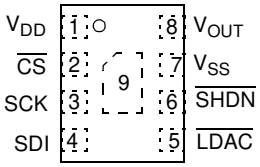
The MCP4801/4811/4821 devices are available in the PDIP, SOIC, MSOP and DFN packages.

Package Types

PDIP, SOIC, MSOP



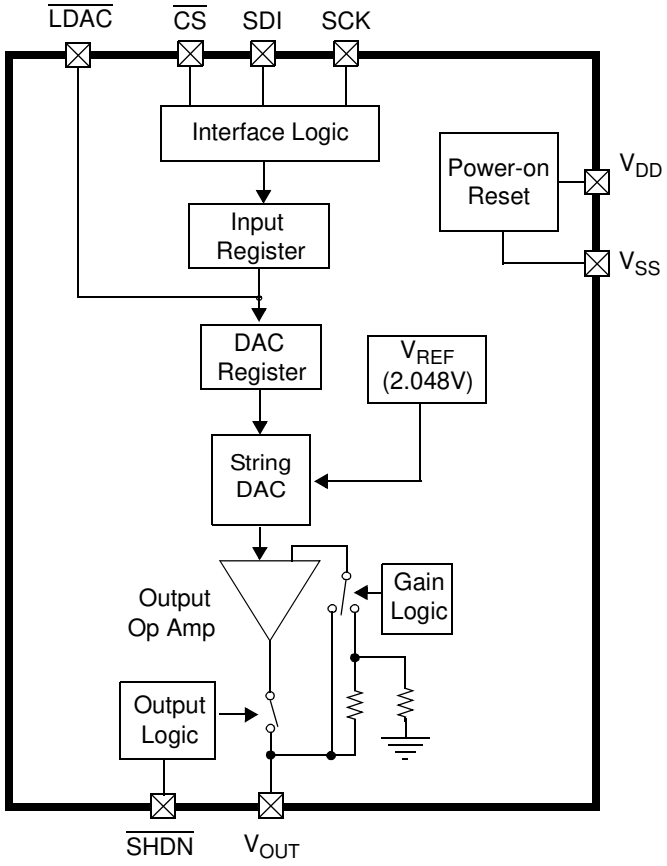
DFN (2x3)*



MCP4801: 8-bit single DAC
MCP4811: 10-bit single DAC
MCP4821: 12-bit single DAC

* Includes Exposed Thermal Pad (EP); see Table 3-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V
All inputs and outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Current at Input Pins ..... ±2 mA
Current at Supply Pins ..... ±50 mA
Current at Output Pins ..... ±25 mA
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -55°C to +125°C
ESD protection on all pins ..... ≥ 4 kV (HBM), ≥ 400V (MM)
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, RL = 5 kΩ to GND, C_L = 100 pF, T_A = -40 to +85°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5		
Operating Current	I_{DD}	—	330	400	µA	All digital inputs are grounded, analog output (V_{OUT}) is unloaded. Code = 000h
Hardware Shutdown Current	I_{SHDN}	—	0.3	2	µA	POR circuit is turned off
Software Shutdown Current	I_{SHDN_SW}	—	3.3	6	µA	POR circuit remains turned on
Power-on Reset Threshold	V_{POR}	—	2.0	—	V	
DC Accuracy						
MCP4801						
Resolution	n	8	—	—	Bits	
INL Error	INL	-1	±0.125	1	LSb	
DNL	DNL	-0.5	±0.1	+0.5	LSb	**Note 1**
MCP4811						
Resolution	n	10	—	—	Bits	
INL Error	INL	-3.5	±0.5	3.5	LSb	
DNL	DNL	-0.5	±0.1	+0.5	LSb	**Note 1**
MCP4821						
Resolution	n	12	—	—	Bits	
INL Error	INL	-12	±2	12	LSb	
DNL	DNL	-0.75	±0.2	+0.75	LSb	**Note 1**
Offset Error	V_{OS}	-1	±0.02	1	% of FSR	Code = 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	0.16	—	ppm/°C	-45°C to +25°C
		—	-0.44	—	ppm/°C	+25°C to +85°C
Gain Error	g_E	-2	-0.10	2	% of FSR	Code = 0xFFFh, not including offset error
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	

Note 1: Guaranteed monotonic by design over all codes.
2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, RL = 5 kΩ to GND, C_L = 100 pF, T_A = -40 to +85°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Internal Voltage Reference (V_{REF})						
Internal Reference Voltage	V_{REF}	2.008	2.048	2.088	V	V_{OUT} when G = 1x and Code = 0xFFFh
Temperature Coefficient **(Note 2)**	$\Delta V_{REF}/°C$	—	125	325	ppm/°C	-40°C to 0°C
		—	0.25	0.65	LSb/°C	-40°C to 0°C
		—	45	160	ppm/°C	0°C to +85°C
		—	0.09	0.32	LSb/°C	0°C to +85°C
Output Noise (V_{REF} Noise)	E_{NREF} (0.1-10 Hz)	—	290	—	μV_{p-p}	Code = 0xFFFh, G = 1x
Output Noise Density	e_{NREF} (1 kHz)	—	1.2	—	µV/√Hz	Code = 0xFFFh, G = 1x
	e_{NREF} (10 kHz)	—	1.0	—	µV/√Hz	Code = 0xFFFh, G = 1x
1/f Corner Frequency	f_{CORNER}	—	400	—	Hz	
Output Amplifier						
Output Swing	V_{OUT}	—	0.01 to V_{DD} – 0.04	—	V	Accuracy is better than 1 LSb for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	15	24	mA	
Settling Time	$t_{SETTLING}$	—	4.5	—	µs	Within ½ LSb of final value from ¼ to ¾ full-scale range
Dynamic Performance (Note 2)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (0111...1111 to 1000...0000)
Digital Feedthrough		—	<10	—	nV-s	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTIC WITH EXTENDED TEMPERATURE

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values are at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5		
Operating Current	I_{DD}	—	350	—	µA	All digital inputs are grounded, analog output (V_{OUT}) is unloaded. Code = 000h
Hardware Shutdown Current	I_{SHDN}	—	1.5	—	µA	POR circuit is turned off
Software Shutdown Current	I_{SHDN_SW}	—	5	—	µA	POR circuit remains turned on
Power-on Reset threshold	V_{POR}	—	1.85	—	V	
DC Accuracy						
MCP4801						
Resolution	n	8	—	—	Bits	
INL Error	INL	—	±0.25	—	LSb	
DNL	DNL	—	±0.2	—	LSb	**Note 1**
MCP4811						
Resolution	n	10	—	—	Bits	
INL Error	INL	—	±1	—	LSb	
DNL	DNL	—	±0.2	—	LSb	**Note 1**
MCP4821						
Resolution	n	12	—	—	Bits	
INL Error	INL	—	±4	—	LSb	
DNL	DNL	—	±0.25	—	LSb	**Note 1**
Offset Error	V_{OS}	—	±0.02	—	% of FSR	Code = 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	-5	—	ppm/°C	+25°C to +125°C
Gain Error	g_E	—	-0.10	—	% of FSR	Code = 0xFFFh, not including offset error
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	
Internal Voltage Reference (V_{REF})						
Internal Reference Voltage	V_{REF}	—	2.048	—	V	V_{OUT} when G = 1x and Code = 0xFFFh
Temperature Coefficient **(Note 2)**	ΔV_{REF}/°C	—	125	—	ppm/°C	-40°C to 0°C
		—	0.25	—	LSb/°C	-40°C to 0°C
		—	45	—	ppm/°C	0°C to +85°C
		—	0.09	—	LSb/°C	0°C to +85°C
Output Noise (V_{REF} Noise)	E_{NREF} (0.1 – 10 Hz)	—	290	—	μV_{p-p}	Code = 0xFFFh, G = 1x
Output Noise Density	e_{NREF} (1 kHz)	—	1.2	—	µV/√Hz	Code = 0xFFFh, G = 1x
	e_{NREF} (10 kHz)	—	1.0	—	µV/√Hz	Code = 0xFFFh, G = 1x
1/f Corner Frequency	f_{CORNER}	—	400	—	Hz	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTIC WITH EXTENDED TEMPERATURE (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values are at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output Amplifier						
Output Swing	V_{OUT}	—	0.01 to V_{DD} – 0.04	—	V	Accuracy is better than 1 LSb for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	17	—	mA	
Settling Time	$t_{SETTLING}$	—	4.5	—	µs	Within ½ LSb of final value from ¼ to ¾ full-scale range
Dynamic Performance (Note 2)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (0111...1111 to 1000...0000)
Digital Feedthrough		—	<10	—	nV-s	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

AC CHARACTERISTICS (SPI TIMING SPECIFICATIONS)

Electrical Specifications: Unless otherwise indicated, V_{DD}= 2.7V – 5.5V, T_A= -40 to +125°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Schmitt Trigger High-Level Input Voltage (All digital input pins)	V_{IH}	0.7 V_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage (All digital input pins)	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.05 V_{DD}	—		
Input Leakage Current	$I_{LEAKAGE}$	-1	—	1	µA	$\overline{SHDN}$ = $\overline{LDAC}$ = $\overline{CS}$ = SDI = SCK = V_{DD} or V_{SS}
Digital Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_{CLK} = 1 MHz **(Note 1)**
Clock Frequency	F_{CLK}	—	—	20	MHz	T_A = +25°C **(Note 1)**
Clock High Time	t_{HI}	15	—	—	ns	**Note 1**
Clock Low Time	t_{LO}	15	—	—	ns	**Note 1**
$\overline{CS}$ Fall to First Rising CLK Edge	t_{CSSR}	40	—	—	ns	Applies only when $\overline{CS}$ falls with CLK high. **(Note 1)**
Data Input Setup Time	t_{SU}	15	—	—	ns	**Note 1**
Data Input Hold Time	t_{HD}	10	—	—	ns	**Note 1**
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	15	—	—	ns	**Note 1**
$\overline{CS}$ High Time	t_{CSH}	15	—	—	ns	**Note 1**
$\overline{LDAC}$ Pulse Width	t_{LD}	100	—	—	ns	**Note 1**
$\overline{LDAC}$ Setup Time	t_{LS}	40	—	—	ns	**Note 1**
SCK Idle Time before $\overline{CS}$ Fall	t_{IDLE}	40	—	—	ns	**Note 1**

Note 1: This parameter is ensured by design and not 100% tested.

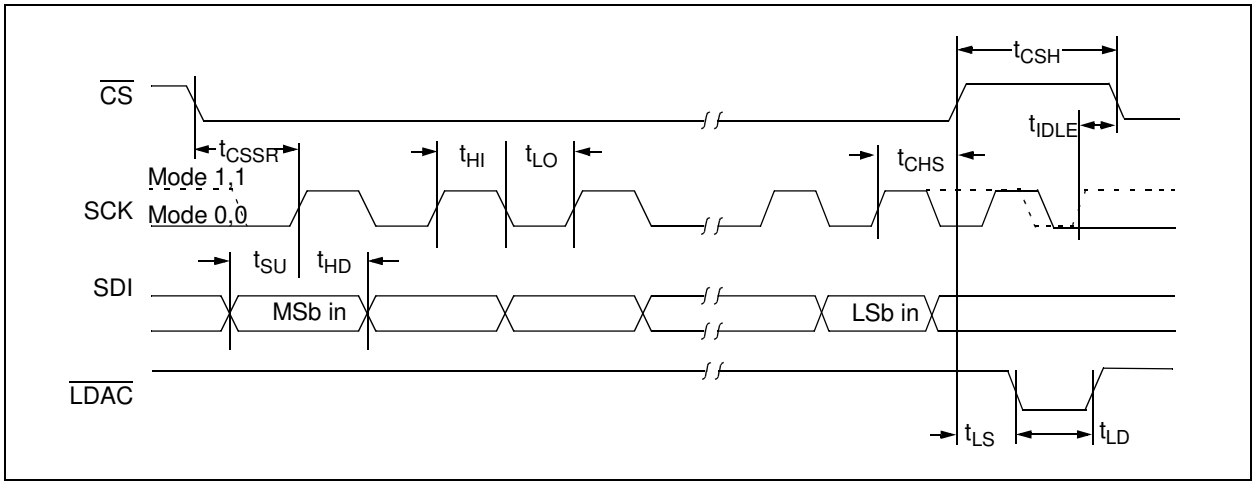


FIGURE 1-1: *SPI Input Timing Data.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-DFN (2x3)	θ_{JA}	—	68	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	90	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	

Note 1: The MCP4801/4811/4821 devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the maximum junction temperature of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

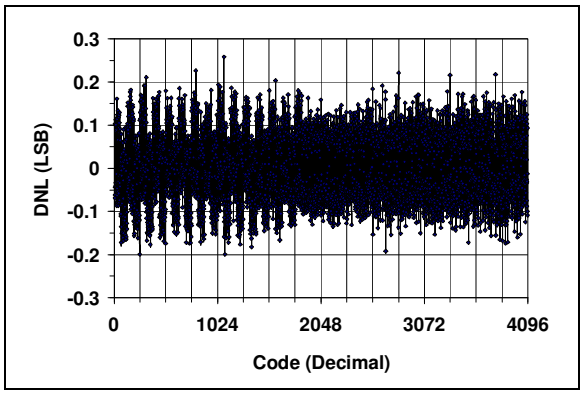


FIGURE 2-1: *DNL vs. Code (MCP4821).*

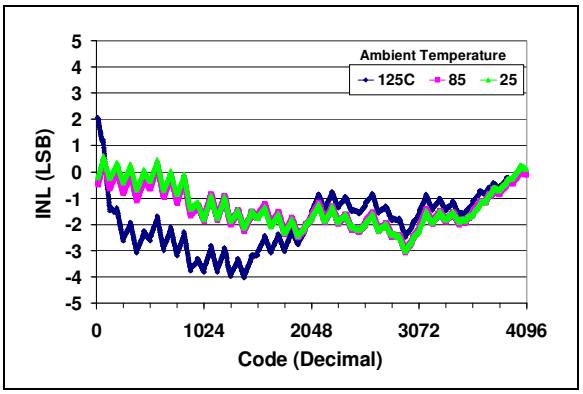


FIGURE 2-4: *INL vs. Code and Temperature (MCP4821).*

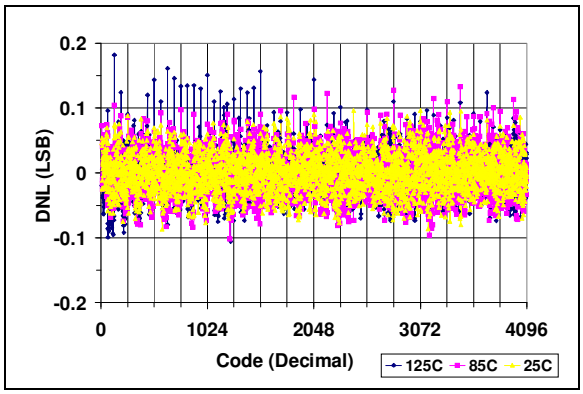


FIGURE 2-2: *DNL vs. Code and Temperature (MCP4821).*

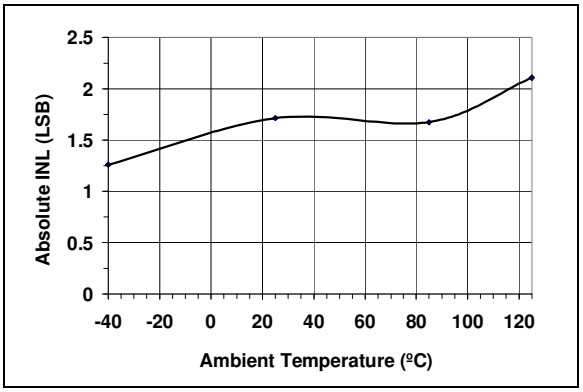


FIGURE 2-5: *Absolute INL vs. Temperature (MCP4821).*

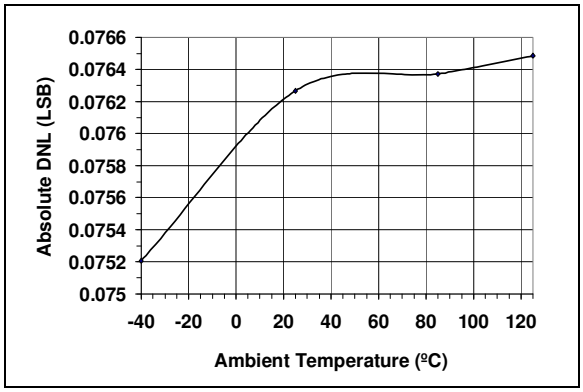


FIGURE 2-3: *Absolute DNL vs. Temperature (MCP4821).*

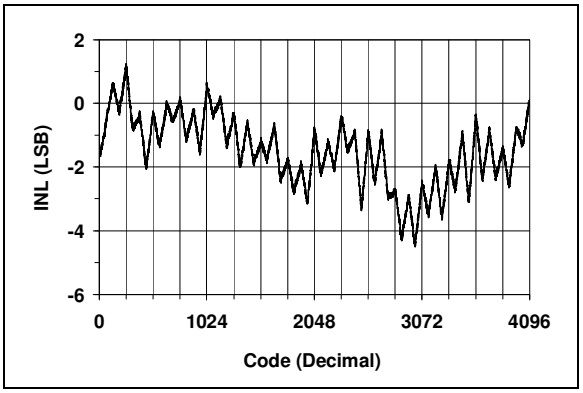


FIGURE 2-6: *INL vs. Code (MCP4821).*

Note:	Single device graph for illustration of 64 code effect.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

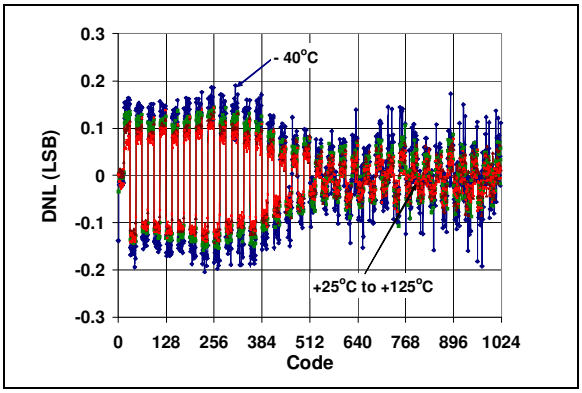


FIGURE 2-7: *DNL vs. Code and Temperature (MCP4811).*

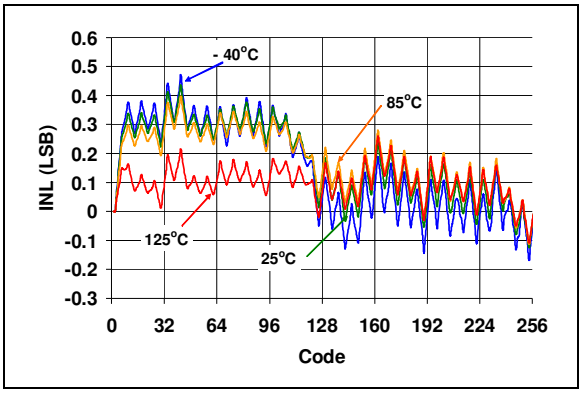


FIGURE 2-10: *INL vs. Code and Temperature (MCP4801).*

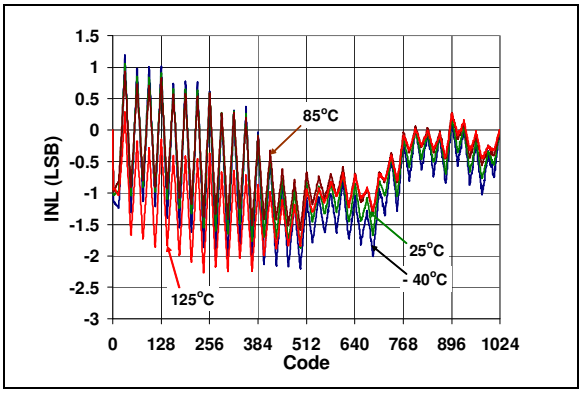


FIGURE 2-8: *INL vs. Code and Temperature (MCP4811).*

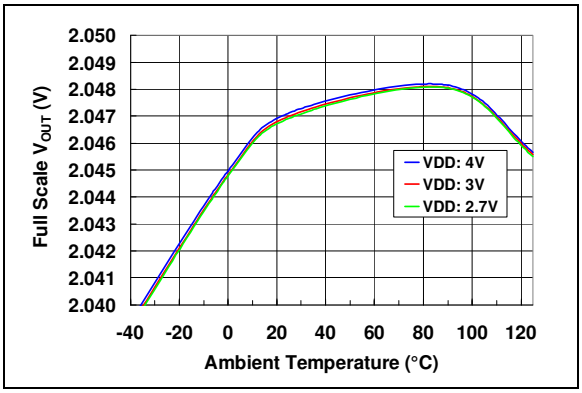


FIGURE 2-11: *Full-Scale V_{OUT} vs. Ambient Temperature and V_{DD}. Gain = 1x.*

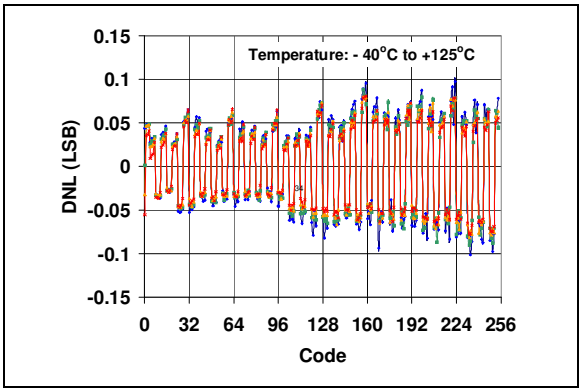


FIGURE 2-9: *DNL vs. Code and Temperature (MCP4801).*

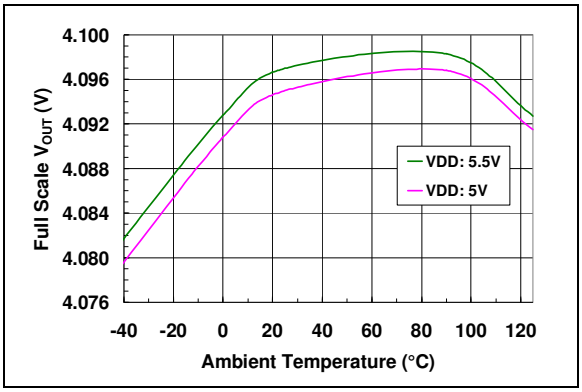


FIGURE 2-12: *Full-Scale V_{OUT} vs. Ambient Temperature and V_{DD}. Gain = 2x.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

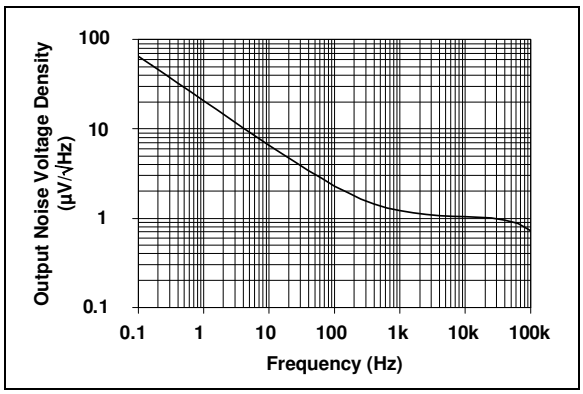


FIGURE 2-13: *Output Noise Voltage Density (V_{REF} Noise Density) vs. Frequency. Gain = 1x.*

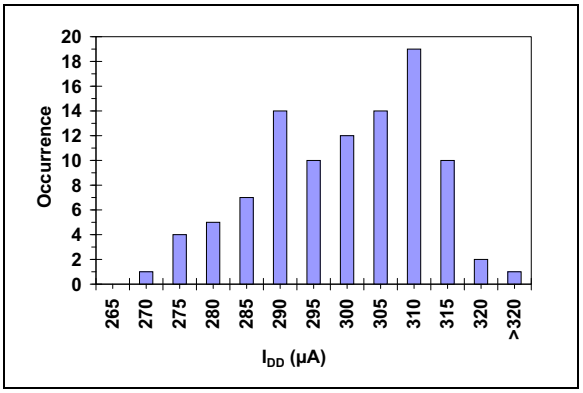


FIGURE 2-16: *I_{DD} Histogram (V_{DD} = 2.7V).*

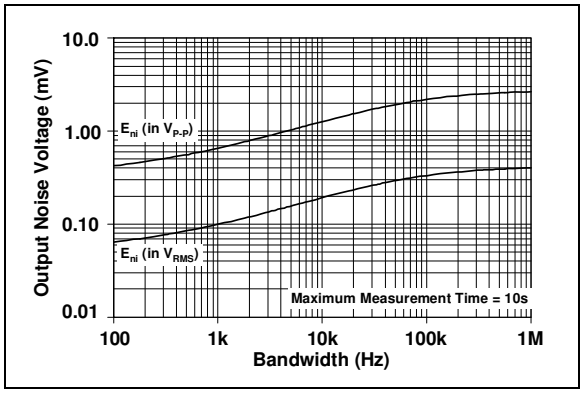


FIGURE 2-14: *Output Noise Voltage (V_{REF} Noise Voltage) vs. Bandwidth. Gain = 2x.*

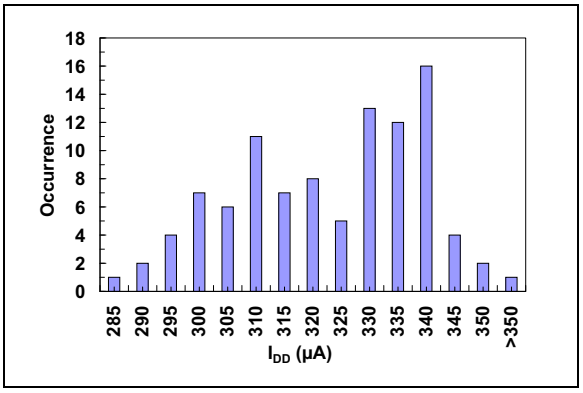


FIGURE 2-17: *I_{DD} Histogram (V_{DD} = 5.0V).*

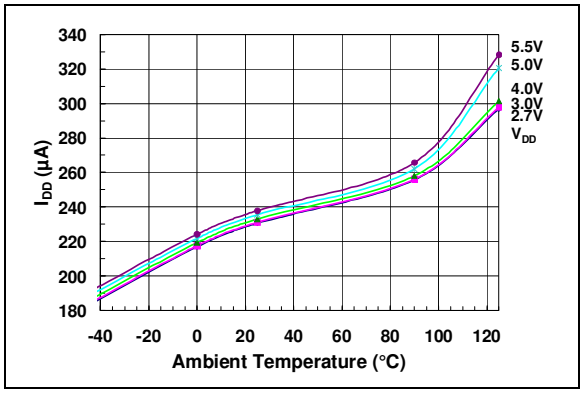


FIGURE 2-15: *I_{DD} vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

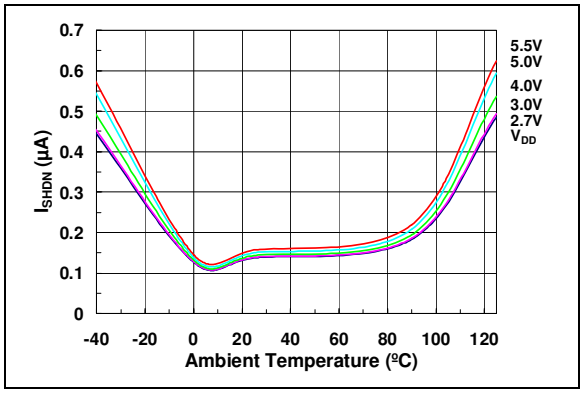


FIGURE 2-18: *Hardware Shutdown Current vs. Temperature and V_{DD}.*

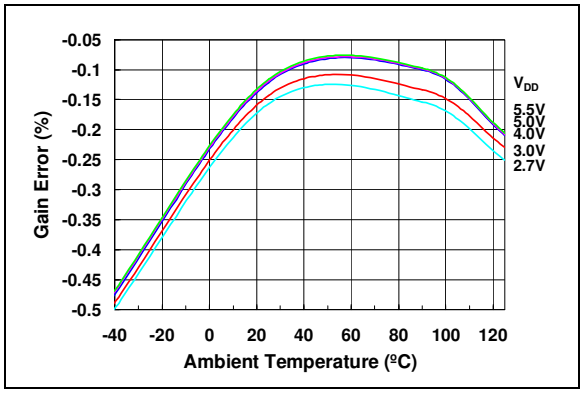


FIGURE 2-21: *Gain Error vs. Temperature and V_{DD}.*

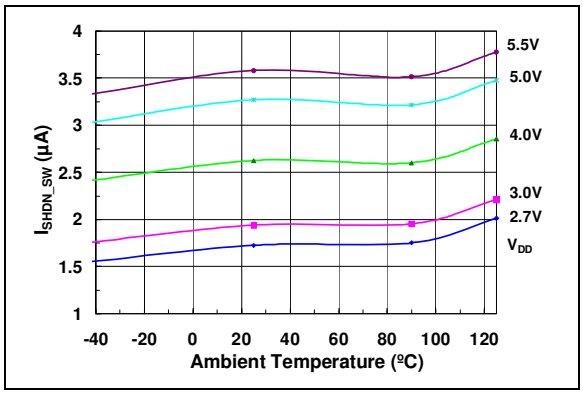


FIGURE 2-19: *Software Shutdown Current vs. Temperature and V_{DD}.*

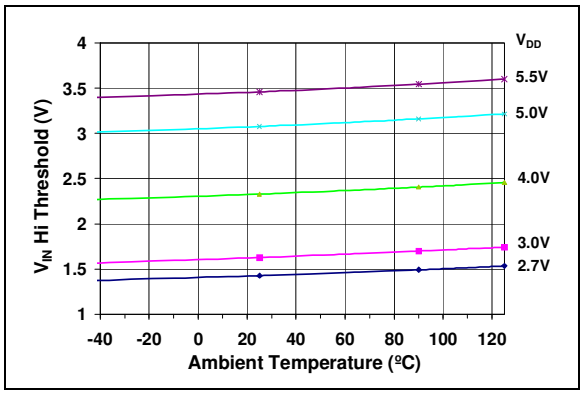


FIGURE 2-22: *V_{IN} High Threshold vs. Temperature and V_{DD}.*

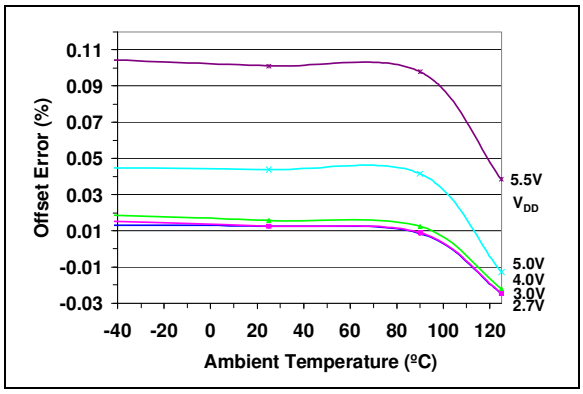


FIGURE 2-20: *Offset Error vs. Temperature and V_{DD}.*

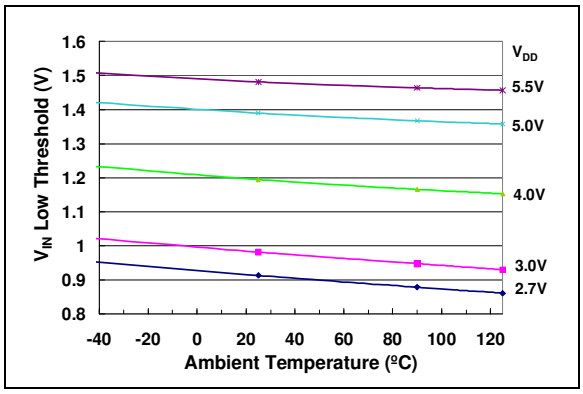


FIGURE 2-23: *V_{IN} Low Threshold vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

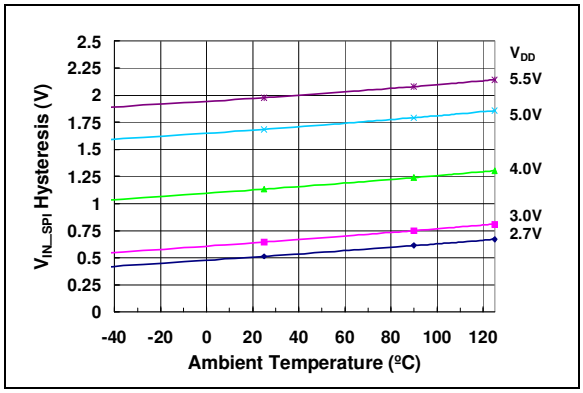


FIGURE 2-24: *Input Hysteresis vs. Temperature and V_{DD}.*

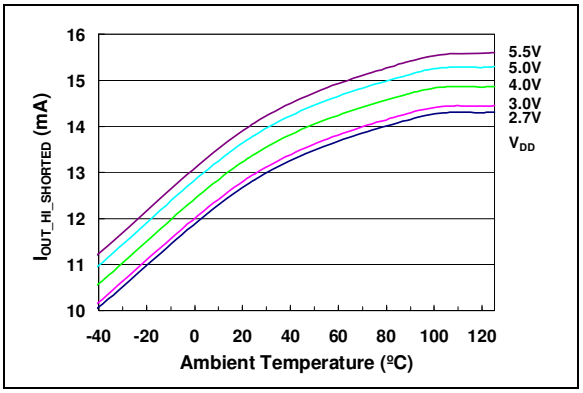


FIGURE 2-27: *I_{OUT} High Short vs. Temperature and V_{DD}.*

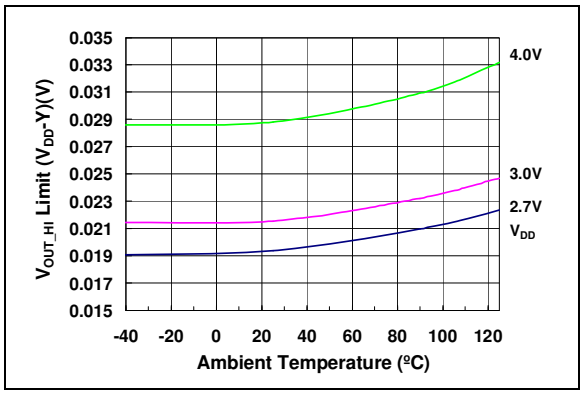


FIGURE 2-25: *V_{OUT} High Limit vs.Temperature and V_{DD}.*

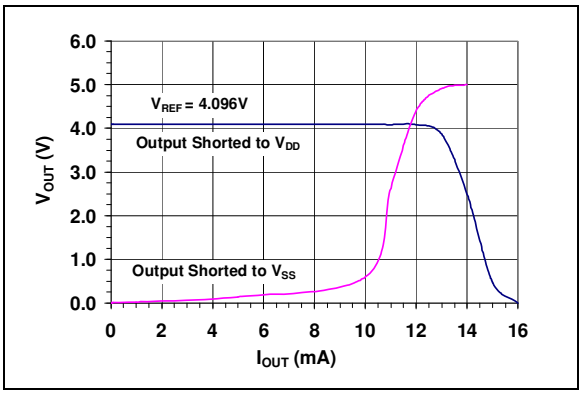


FIGURE 2-28: *I_{OUT} vs. V_{OUT}. Gain = 2x.*

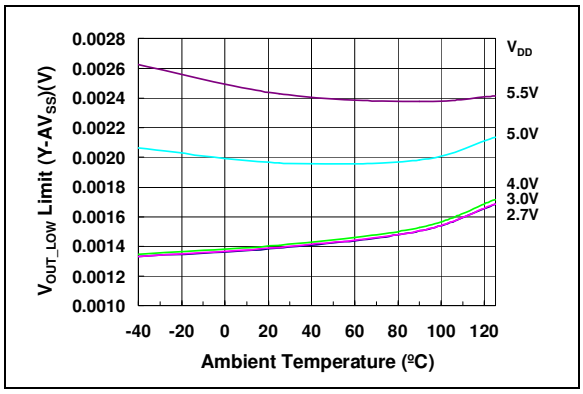


FIGURE 2-26: *V_{OUT} Low Limit vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Gain = 2, R_L = 5 kΩ, C_L = 100 pF.

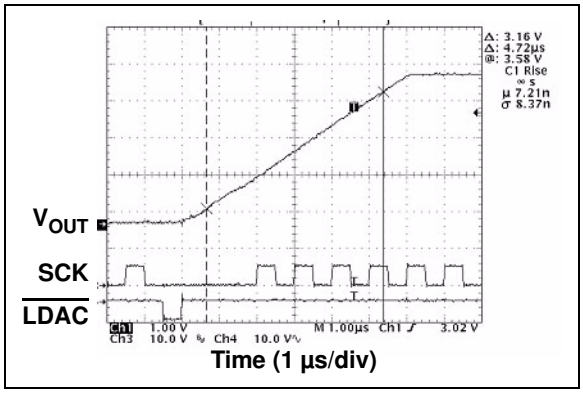


FIGURE 2-29: *V_{OUT} Rise Time.*

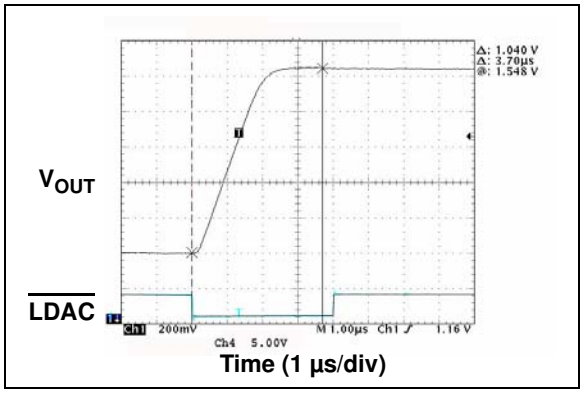


FIGURE 2-32: *V_{OUT} Rise Time.*

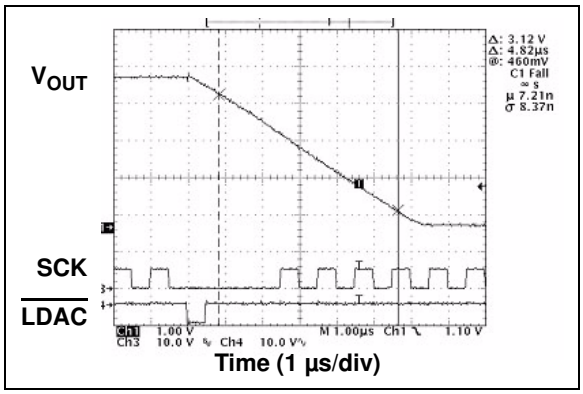


FIGURE 2-30: *V_{OUT} Fall Time.*

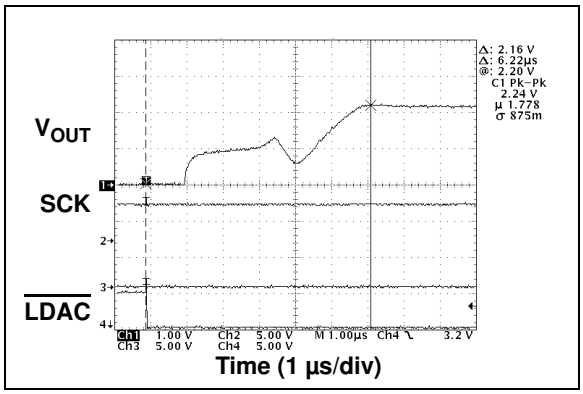


FIGURE 2-33: *V_{OUT} Rise Time Exit Shutdown.*

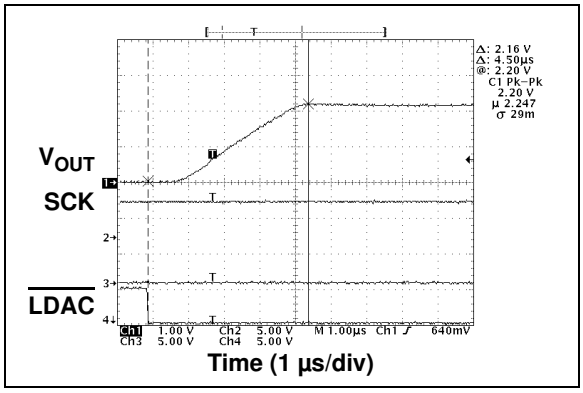


FIGURE 2-31: *V_{OUT} Rise Time.*

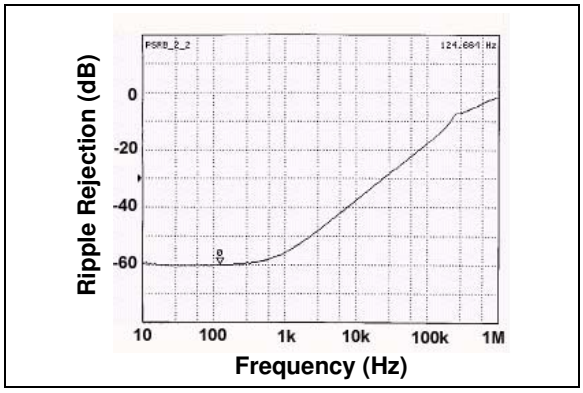


FIGURE 2-34: *PSRR vs. Frequency.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE FOR MCP4801/4811/4821

MCP4801/4811/4821		Symbol	Description
MSOP, PDIP, SOIC, DFN	DFN		
1	1	V_{DD}	Supply Voltage Input (2.7V to 5.5V)
2	2	$\overline{CS}$	Chip Select Input
3	3	SCK	Serial Clock Input
4	4	SDI	Serial Data Input
5	5	$\overline{LDAC}$	DAC Output Synchronization Input. This pin is used to transfer the input register (DAC settings) to the output register (V_{OUT})
6	6	$\overline{SHDN}$	Hardware Shutdown Input
7	7	V_{SS}	Ground reference point for all circuitry on the device
8	8	V_{OUT}	DAC Analog Output
—	9	EP	Exposed thermal pad. This pad must be connected to V_{SS} in application

3.1 Supply Voltage Pins (V_{DD}, V_{SS})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS} and can range from 2.7V to 5.5V. The power supply at the V_{DD} pin should be as clean as possible for good DAC performance. Using an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground is recommended. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high-frequency noise present in application boards.

V_{SS} is the analog ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application Printed Circuit Board (PCB), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.2 Chip Select ($\overline{CS}$)

$\overline{CS}$ is the Chip Select input pin, which requires an active low to enable serial clock and data functions.

3.3 Serial Clock Input (SCK)

SCK is the SPI compatible serial clock input pin.

3.4 Serial Data Input (SDI)

SDI is the SPI compatible serial data input pin.

3.5 Latch DAC Input ($\overline{LDAC}$)

$\overline{LDAC}$ (latch DAC synchronization input) pin is used to transfer the input latch register to the DAC register (output latches, V_{OUT}). When this pin is low, V_{OUT} is updated with input register content. This pin can be tied to low (V_{SS}) if the V_{OUT} update is desired at the rising edge of the $\overline{CS}$ pin. This pin can be driven by an external control device such as an MCU I/O pin.

3.6 Analog Output (V_{OUT})

V_{OUT} is the DAC analog output pin. The DAC output has an output amplifier. The full-scale range of the DAC output is from V_{SS} to $G*V_{REF}$, where G is the gain selection option (1x or 2x). The DAC analog output cannot go higher than the supply voltage (V_{DD}).

3.7 Exposed Thermal Pad (EP)

There is an internal electrical connection between the exposed thermal pad (EP) and the V_{SS} pin. They must be connected to the same potential on the PCB.

NOTES:

4.0 GENERAL OVERVIEW

The MCP4801, MCP4811 and MCP4821 are single channel voltage-output 8-bit, 10-bit and 12-bit DAC devices, respectively. These devices include rail-to-rail output amplifier, internal voltage reference, shutdown and reset-management circuitry. The devices use an SPI serial communication interface and operate with a single supply voltage from 2.7V to 5.5V.

The DAC input coding of these devices is straight binary. Equation 4-1 shows the DAC analog output voltage calculation.

EQUATION 4-1: ANALOG OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{(2.048V \times D_n)}{2^n} \times G$$

Where:

2.048V	=	Internal voltage reference
D_n	=	DAC input code
G	=	Gain selection
	=	2 for <$\overline{GA}$> bit = 0
	=	1 for <$\overline{GA}$> bit = 1
n	=	DAC Resolution
	=	8 for MCP4801
	=	10 for MCP4811
	=	12 for MCP4821

The ideal output range of each device is:

- **MCP4801 (n = 8)**

(a) 0.0V to 255/256 * 2.048V when gain setting = `1x`.

(b) 0.0V to 255/256 * 4.096V when gain setting = `2x`.

- **MCP4811 (n = 10)**

(a) 0.0V to 1023/1024 * 2.048V when gain setting = `1x`.

(b) 0.0V to 1023/1024 * 4.096V when gain setting = `2x`.

- **MCP4821 (n = 12)**

(a) 0.0V to 4095/4096 * 2.048V when gain setting = `1x`.

(b) 0.0V to 4095/4096 * 4.096V when gain setting = `2x`.

Note: See the output swing voltage specification in **Section 1.0 "Electrical Characteristics"**.

1 LSb is the ideal voltage difference between two successive codes. Table 4-1 illustrates the LSb calculation of each device.

TABLE 4-1: LSb OF EACH DEVICE

Device	Gain Selection	LSb Size
MCP4801 (n = 8)	1x	2.048V/256 = 8 mV
	2x	4.096V/256 = 16 mV
MCP4811 (n = 10)	1x	2.048V/1024 = 2 mV
	2x	4.096V/1024 = 4 mV
MCP4821 (n = 12)	1x	2.048V/4096 = 0.5 mV
	2x	4.096V/4096 = 1 mV

4.0.1 INL ACCURACY

Integral Non-Linearity (INL) error is the maximum deviation between an actual code transition point and its corresponding ideal transition point once offset and gain errors have been removed. The two endpoints method (from 0x000 to 0xFFF) is used for the calculation. Figure 4-1 shows the details.

A positive INL error represents transition(s) later than ideal. A negative INL error represents transition(s) earlier than ideal.

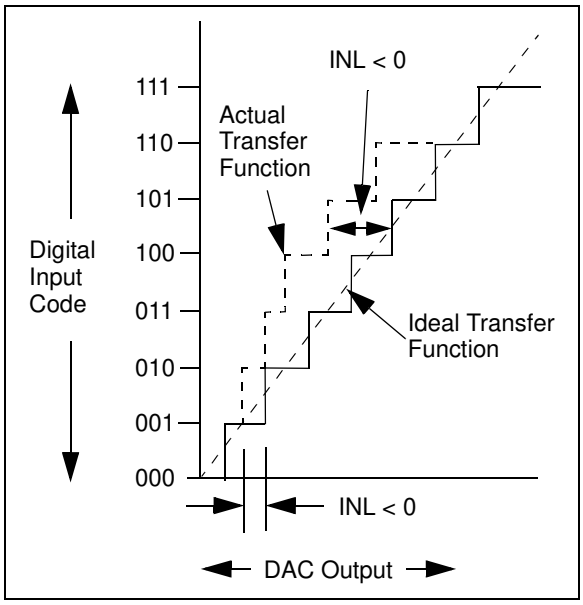


FIGURE 4-1: *Example for INL Error.*

4.0.2 DNL ACCURACY

A Differential Non-Linearity (DNL) error is the measure of the variations in code widths from the ideal code width. A DNL error of zero indicates that every code is exactly 1 LSb wide.

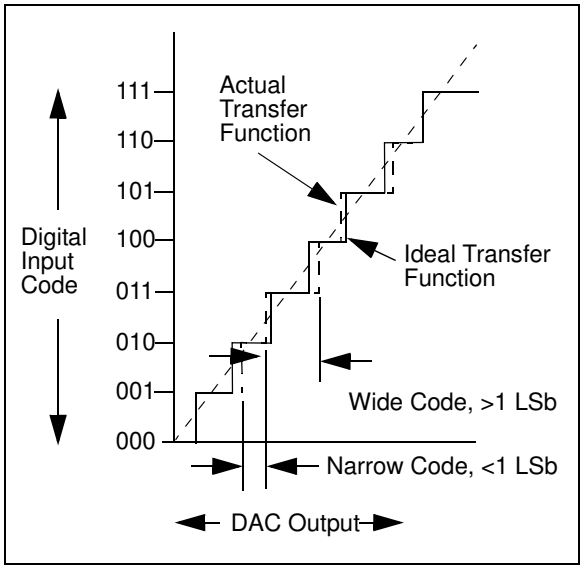


FIGURE 4-2: *Example for DNL Error.*

4.0.3 OFFSET ERROR

Offset error is the deviation from zero voltage output when the digital input code is zero.

4.0.4 GAIN ERROR

Gain error is the deviation from the ideal output, V_{REF} – 1 LSb, excluding the effects of offset error.

4.1 Circuit Descriptions

4.1.1 OUTPUT AMPLIFIER

The analog DAC output is buffered with a low-power, precision CMOS amplifier. This amplifier provides low offset voltage and low noise. The output stage enables the device to operate with output voltages close to the power supply rails. Refer to **Section 1.0 "Electrical Characteristics"** for the analog output voltage range and load conditions.

In addition to resistive load-driving capability, the amplifier will also drive high capacitive loads without oscillation. The amplifier's strong output allows V_{OUT} to be used as a programmable voltage reference in a system.

4.1.1.1 Programmable Gain Block

The rail-to-rail output amplifier has two configurable gain options: a gain of 1x (<$\overline{GA}$> = 1) or a gain of 2x (<$\overline{GA}$> = 0). The default setting is a gain of 2x. This results in an ideal full-scale output of 0.000V to 4.096V due to the internal reference (V_{REF} = 2.048V).

4.1.2 VOLTAGE REFERENCE

The MCP4801/4811/4821 devices utilize internal 2.048V voltage reference. The voltage reference has a low temperature coefficient and low noise characteristics. Refer to **Section 1.0 "Electrical Characteristics"** for the voltage reference specifications.

4.1.3 POWER-ON RESET CIRCUIT

The internal Power-on Reset (POR) circuit monitors the power supply voltage (V_{DD}) during the device operation. The circuit also ensures that the DAC powers up with high output impedance (<$\overline{SHDN}$> = 0, typically 500 kΩ). The devices will continue to have a high-impedance output until a valid write command is received, and the $\overline{LDAC}$ pin meets the input low threshold.

If the power supply voltage is less than the POR threshold (V_{POR} = 2.0V, typical), the DAC will be held in the Reset state. It will remain in that state until $V_{DD} > V_{POR}$ and a subsequent write command is received.

Figure 4-3 shows a typical power supply transient pulse and the duration required to cause a reset to occur, as well as the relationship between the duration and trip voltage. A 0.1 µF decoupling capacitor, mounted as close as possible to the V_{DD} pin, can provide additional transient immunity.

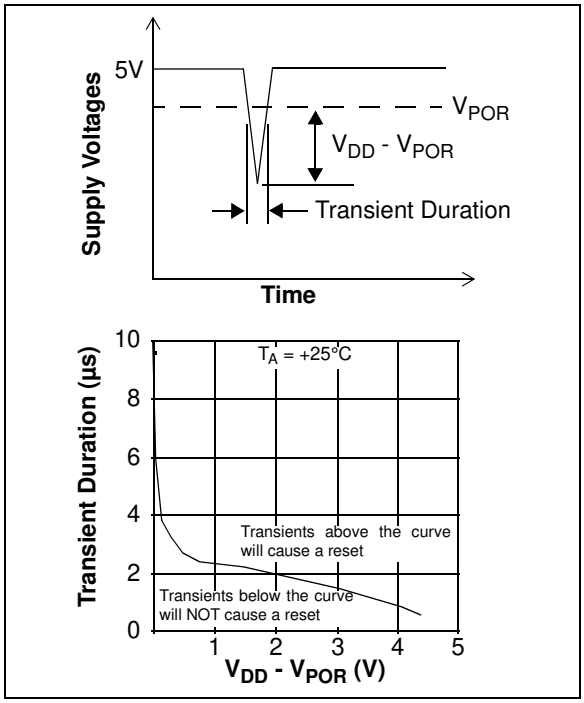


FIGURE 4-3: *Typical Transient Response.*

4.1.4 SHUTDOWN MODE

The user can shut down the device using a software command (<$\overline{SHDN}$> = 0) or $\overline{SHDN}$ pin. During shutdown mode, most of the internal circuits, including the output amplifier, are turned off for power savings. The internal reference is not affected by the shutdown command. The serial interface also remains active, allowing a write command to bring the device out of Shutdown mode. There will be no analog output at the V_{OUT} pin, which is internally switched to a known resistive load (500 kΩ, typical). Figure 4-4 shows the analog output stage during Shutdown mode.

The condition of the Power-on Reset circuit during Shutdown is as follows:

a) Turned off if shutdown occurred from the $\overline{SHDN}$ pin

b) Remains turned on if the shutdown occurred through software

The device will remain in Shutdown mode until the <$\overline{SHDN}$> bit = 1 is latched into the device or $\overline{SHDN}$ pin is changed to logic high. When the device is changed from Shutdown to Active mode, the output settling time takes < 10 µs, but greater than the standard active mode settling time (4.5 µs).

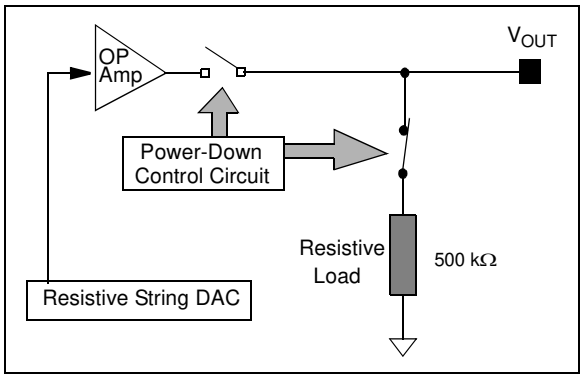


FIGURE 4-4: *Output Stage for Shutdown Mode.*

NOTES:

5.0 SERIAL INTERFACE

5.1 Overview

The MCP4801/4811/4821 devices are designed to interface directly with the Serial Peripheral Interface (SPI) port, available on many microcontrollers, and supports Mode 0,0 and Mode 1,1. Commands and data are sent to the device via the SDI pin, with data being clocked-in on the rising edge of SCK. The communications are unidirectional and, thus, data cannot be read out of the MCP4801/4811/4821 devices. The $\overline{CS}$ pin must be held low for the duration of a write command. The write command consists of 16 bits and is used to configure the DAC's control and data latches. Register 5-1 to Register 5-3 detail the input register that is used to configure and load the DAC register for each device. Figure 5-1 to Figure 5-3 show the write command for each device.

Refer to Figure 1-1 and the SPI Timing Specifications Table for detailed input and output timing specifications for both Mode 0,0 and Mode 1,1 operation.

5.2 Write Command

The write command is initiated by driving the $\overline{CS}$ pin low, followed by clocking the four Configuration bits and the 12 data bits into the SDI pin on the rising edge of SCK. The $\overline{CS}$ pin is then raised, causing the data to be latched into the DAC's input register.

The MCP4801/4811/4821 devices utilize a double-buffered latch structure to allow the DAC output to be synchronized with the $\overline{LDAC}$ pin, if desired.

By bringing down the $\overline{LDAC}$ pin to a low state, the content stored in the DAC's input register is transferred into the DAC's output register (V_{OUT}), and V_{OUT} is updated.

All writes to the MCP4801/4811/4821 devices are 16-bit words. Any clocks after the first 16th clock will be ignored. The Most Significant four bits are Configuration bits. The remaining 12 bits are data bits. No data can be transferred into the device with $\overline{CS}$ high. The data transfer will only occur if 16 clocks have been transferred into the device. If the rising edge of $\overline{CS}$ occurs prior, shifting of data into the input register will be aborted.

REGISTER 5-1: WRITE COMMAND REGISTER FOR MCP4821 (12-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
0	—	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15															bit 0

REGISTER 5-2: WRITE COMMAND REGISTER FOR MCP4811 (10-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
0	—	$\overline{GA}$	$\overline{SHDN}$	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	x	x
bit 15															bit 0

REGISTER 5-3: WRITE COMMAND REGISTER FOR MCP4801 (8-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
0	—	$\overline{GA}$	$\overline{SHDN}$	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x
bit 15															bit 0

Where:

bit 15 **(1)** 0 = Write to DAC register
1 = Ignore this command

bit 14 — Don't Care

bit 13 **$\overline{GA}$:** Output Gain Selection bit
1 = 1x ($V_{OUT} = V_{REF} * D/4096$)
0 = 2x ($V_{OUT} = 2 * V_{REF} * D/4096$), where internal V_{REF} = 2.048V.

bit 12 **$\overline{SHDN}$:** Output Shutdown Control bit
1 = Active mode operation. V_{OUT} is available.
0 = Shutdown the device. Analog output is not available. V_{OUT} pin is connected to 500 kΩ (typical).

bit 11-0 **D11:D0:** DAC Input Data bits. Bit x is ignored.

Legend			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

Note 1: This bit must be '0'. The device ignores the write command if this MSB bit is not '0'.

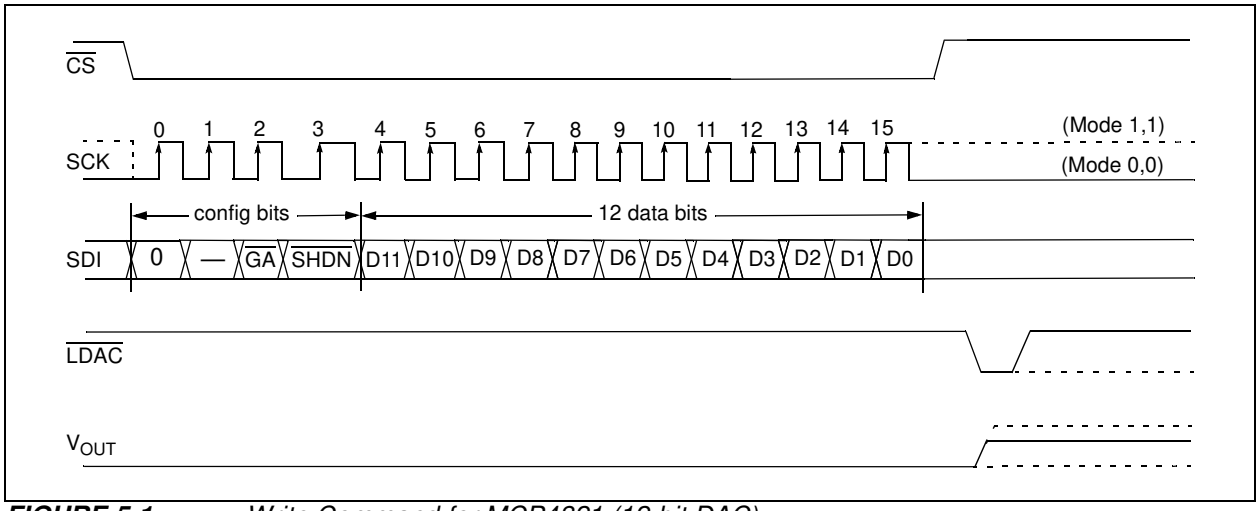
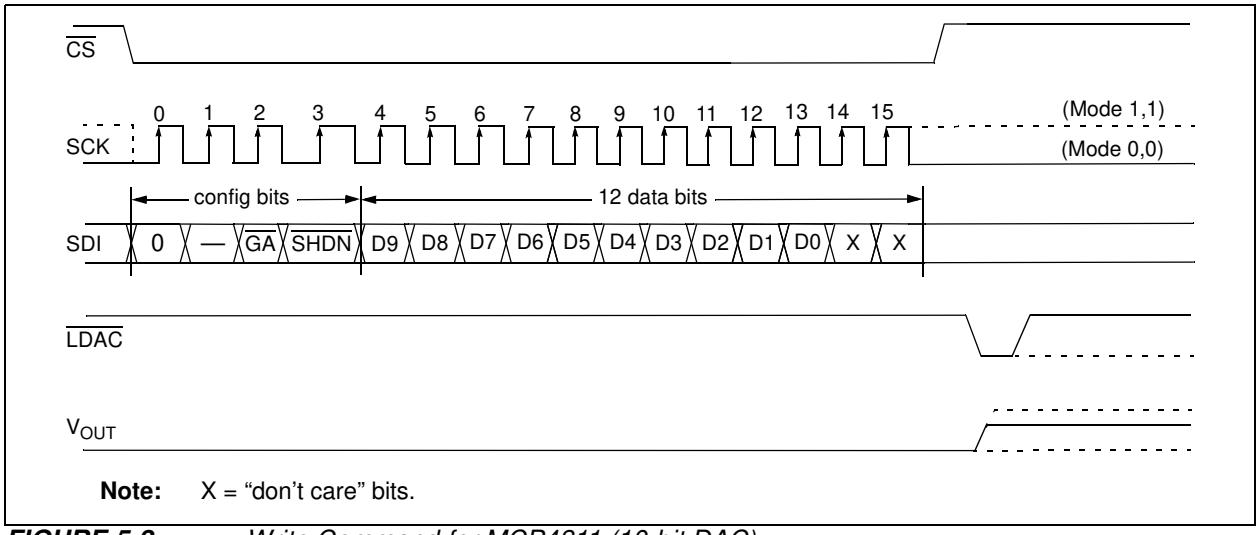
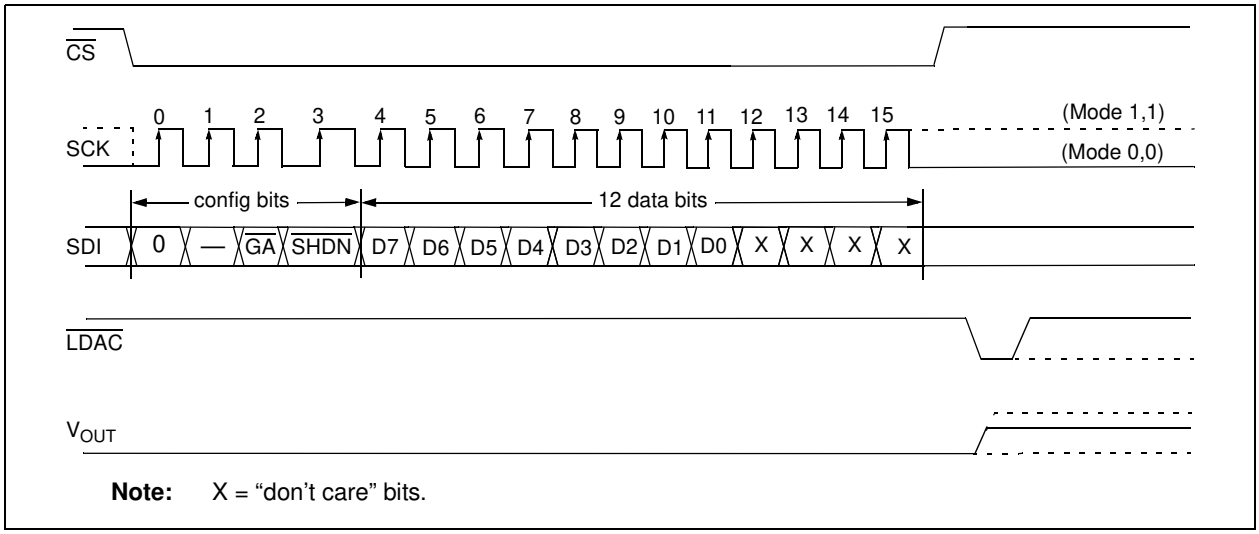


FIGURE 5-1: *Write Command for MCP4821 (12-bit DAC).*



Note: X = “don’t care” bits.

FIGURE 5-2: *Write Command for MCP4811 (10-bit DAC).*



Note: X = “don’t care” bits.

FIGURE 5-3: *Write Command for MCP4801 (8-bit DAC).*

NOTES:

6.0 TYPICAL APPLICATIONS

The MCP4801/4811/4821 family of devices are general purpose, single channel voltage output DACs for various applications where a precision operation with low-power and internal voltage reference is required.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Precision Selectable Voltage Reference
- Portable Instrumentation (Battery-Powered)
- Calibration of Optical Communication Devices

6.1 Digital Interface

The MCP4801/4811/4821 devices utilize a 3-wire synchronous serial protocol to transfer the DAC's setup and input codes from the digital devices. The serial protocol can be interfaced to SPI or Microwire peripherals which are common on many microcontroller units (MCUs), including Microchip's PIC® MCUs and dsPIC® DSCs.

In addition to the three serial connections ($\overline{CS}$, SCK and SDI), the $\overline{LDAC}$ signal synchronizes the DAC output with $\overline{LDAC}$ pin event. By bringing the $\overline{LDAC}$ pin down "low", the DAC input codes and settings in the DAC input register are latched into the output register, and the DAC analog output is updated. Figure 6-1 shows an example of the pin connections. Note that the $\overline{LDAC}$ pin can be tied low (V_{SS}) to reduce the required connections from 4 to 3 I/O pins. In this case, the DAC output can be immediately updated when a valid 16 clock transmission has been received and the $\overline{CS}$ pin has been raised.

6.2 Power Supply Considerations

The typical application will require a bypass capacitor to filter out noise in the power supply traces. The noise can be induced onto the power supply's traces from various events such as digital switching or as a result of changes on the DAC's output. The bypass capacitor helps minimize the effect of these noise sources. Figure 6-1 illustrates an appropriate bypass strategy. In this example, two bypass capacitors are used in parallel: (a) 0.1 µF (ceramic) and (b)10 µF (tantalum). These capacitors should be placed as close to the device power pin (V_{DD}) as possible (within 4 mm).

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} of the device should reside on the analog plane.

6.3 Output Noise Considerations

The voltage noise density (in µV/√Hz) is illustrated in Figure 2-13. This noise appears at V_{OUT}, and is primarily a result of the internal reference voltage. Its 1/f corner (f_{CORNER}) is approximately 400 Hz.

Figure 2-14 illustrates the voltage noise (in mV_{RMS} or mV_{P-P}). A small bypass capacitor on V_{OUT} is an effective method to produce a single-pole Low-Pass Filter (LPF) that will reduce this noise. For instance, a bypass capacitor sized to produce a 1 kHz LPF would result in an E_{NREF} of about 100 μV_{RMS}. This would be necessary when trying to achieve the low DNL error performance (at G = 1x) that the MCP4801/4811/4821 devices are capable of. The tested range for stability is .001 µF through 4.7 µF.

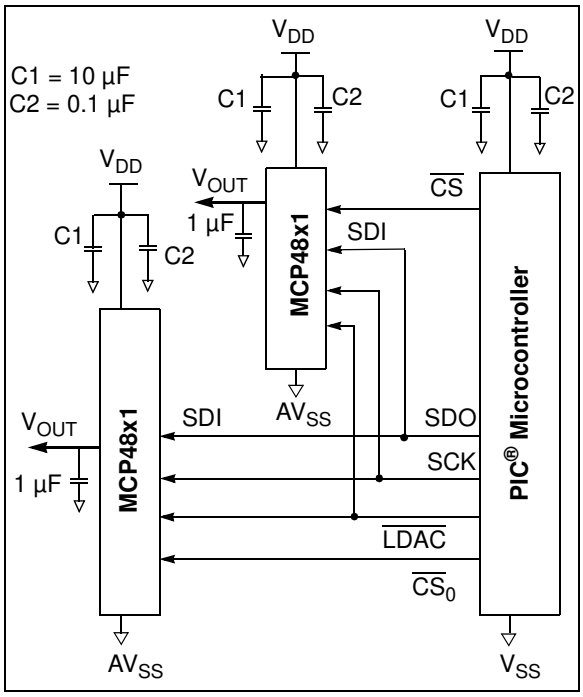


FIGURE 6-1: *Typical Connection Diagram.*

6.4 Layout Considerations

Inductively-coupled AC transients and digital switching noises can degrade the output signal integrity, and potentially reduce the device performance. Careful board layout will minimize these effects and increase the Signal-to-Noise Ratio (SNR). Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs and isolated outputs with proper decoupling, is critical for the best performance. Particularly harsh environments may require shielding of critical signals.

Breadboards and wire-wrapped boards are not recommended if low noise is desired.