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MCP48FEBXX

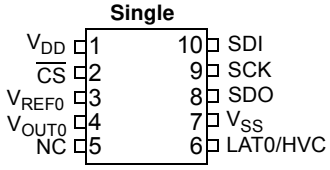
8-/10-/12-Bit Single/Dual Voltage Output Nonvolatile Digital-to-Analog Converters with SPI Interface

Features

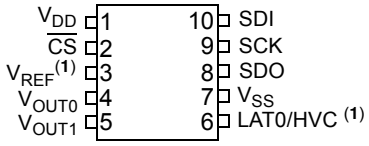
- Operating Voltage Range:
  - 2.7V to 5.5V - full specifications
  - 1.8V to 2.7V - reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: **MCP48FEB0X** (256 Steps)
  - 10-bit: **MCP48FEB1X** (1024 Steps)
  - 12-bit: **MCP48FEB2X** (4096 Steps)
- Rail-to-Rail Output
- Fast Settling Time of 7.8 µs (typical)
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal Band Gap (1.22V typical)
- Output Gain Options:
  - Unity (1x)
  - 2x
- Nonvolatile Memory (EEPROM):
  - User-programmed Power-on Reset (POR)/Brown-out Reset (BOR) output setting, recall and device configuration bits
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power-Down)
- Power-on/Brown-out Reset Protection
- Power-Down Modes:
  - Disconnects output buffer (High Impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- Low Power Consumption:
  - Normal operation: <180 µA (Single), 380 µA (Dual)
  - Power-down operation: 650 nA typical
  - EEPROM write cycle (1.9 mA maximum)
- SPI Interface:
  - Supports '00' and '11' modes
  - Up to 20 MHz writes and 10 MHz reads
  - Input buffers support interfacing to low-voltage digital devices
- Package Types: 10-lead MSOP
- Extended Temperature Range: -40°C to +125°C

Package Types

MCP48FEBx1
MSOP
Single



MCP48FEBx2
MSOP
Dual



Note 1: Associated with both DAC0 and DAC1

General Description

The MCP48FEBXX are Single- and Dual-channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an SPI serial interface.

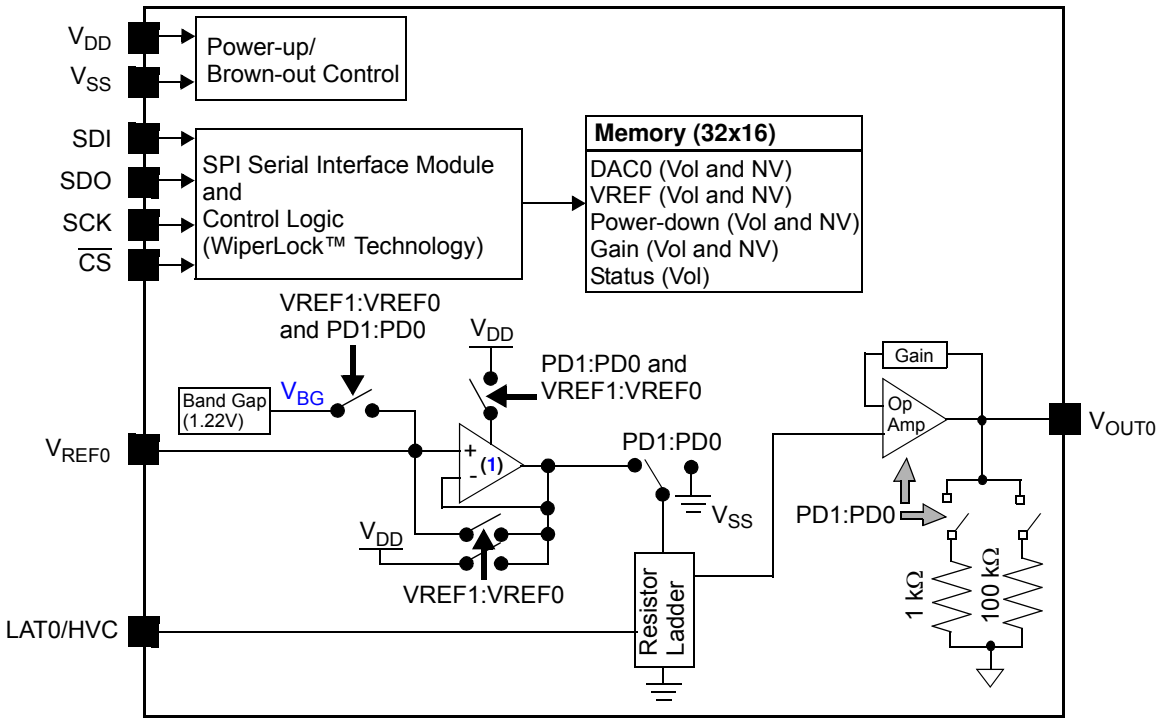
The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is connected internally to the DAC reference circuit. When the V_{REF} pin is used, the user can select the output buffer's gain to be 1 or 2. When the gain is 2, the V_{REF} pin voltage should be limited to a maximum of $V_{DD}/2$.

These devices have an SPI-compatible serial interface. Write commands are supported up to 20 MHz while read commands are supported up to 10 MHz.

Applications

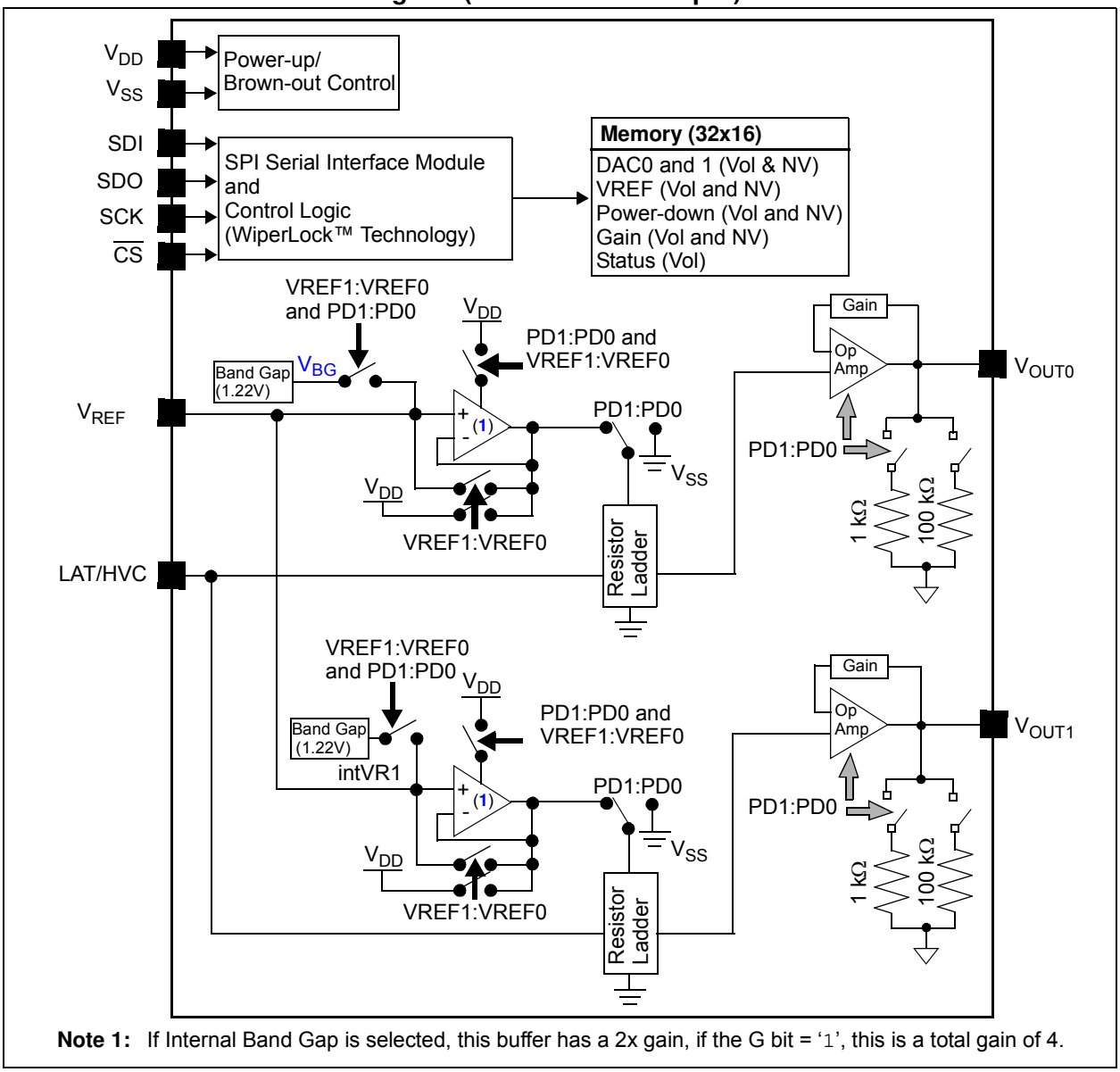
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

MCP48FEBX1 Device Block Diagram (Single-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain. If the G bit = '1', this is a total gain of 4.

MCP48FEBX2 Device Block Diagram (Dual-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain, if the G bit = '1', this is a total gain of 4.

Device Features

Device	# of Channels	Resolution (bits)	Control Interface	DAC Output POR/BOR Setting (1)	# of VREF Inputs	Internal band gap ?	# of LAT Inputs	Memory	Specified Operating Range (V_{DD}) (2)
MCP48FEB01	1	8	SPI	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB11	1	10	SPI	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB21	1	12	SPI	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB02	2	8	SPI	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB12	2	10	SPI	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP48FEB22	2	12	SPI	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FVB01	1	8	I²C™	7Fh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB11	1	10	I²C	1FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB21	1	12	I²C	7FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB02	2	8	I²C	7Fh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB12	2	10	I²C	1FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FVB22	2	12	I²C	7FFh	1	Yes	1	RAM	1.8V to 5.5V
MCP47FEB01	1	8	I²C	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB11	1	10	I²C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB21	1	12	I²C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB02	2	8	I²C	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB12	2	10	I²C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB22	2	12	I²C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V

Note 1: Factory Default value. The DAC output POR/BOR value can be modified via the nonvolatile DAC output register(s) (available only on nonvolatile devices (MCP4XFEBXX)).

2: Analog output performance specified from 2.7V to 5.5V.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Voltage on V_{DD} with respect to V_{SS} ..... -0.6V to +6.5V

Voltage on all pins with respect to V_{SS} ..... -0.6V to V_{DD}+0.3V

Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV pins) ..... ±20 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA

Maximum current out of V_{SS} pin (Single) ..... 50 mA
(Dual) ..... 100 mA

Maximum current into V_{DD} pin (Single) ..... 50 mA
(Dual) ..... 100 mA

Maximum current sourced by the V_{OUT} pin ..... 20 mA

Maximum current sunk by the V_{OUT} pin ..... 20 mA

Maximum current sunk by the V_{REF} pin ..... 125 µA

Maximum input current source/sunk by SDI, SCK, and $\overline{CS}$ pins ..... 2 mA

Maximum output current sunk by SDO Output pin ..... 25 mA

Total power dissipation (1) ..... 400 mW

Package power dissipation (T_A = +50°C, T_J = +150°C)
MSOP-10 ..... 490 mW

ESD protection on all pins ..... ≥ ±4 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±1.5 kV (CDM)

Latch-Up (per JEDEC JESD78A) @ +125°C ..... ±100 mA

Storage temperature ..... -65°C to +150°C

Ambient temperature with power applied ..... -55°C to +125°C

Soldering temperature of leads (10 seconds) ..... +300°C

Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and Serial Interface
V_{DD} Voltage (rising) to ensure device Power-on Reset	$V_{POR/BOR}$	—	—	1.7	V	RAM retention voltage (V_{RAM}) < V_{POR} V_{DD} voltages greater than $V_{POR/BOR}$ limit Ensure that device is out of reset.
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 3**)			V/ms	
High-Voltage Commands Voltage Range (HVC pin)	V_{HV}	V_{SS}	—	12.5	V	The HVC pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}) [(1)]
High-Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	—	V	Threshold for Entry into WiperLock Technology
High-Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V	V	**(Note 2)**
Power-on Reset to Output-Driven Delay	T_{PORD}	—	25	50	µs	V_{DD} rising, V_{DD} > V_{POR}

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 3 POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Supply Current	I_{DD}	—	—	320	µA	Single	1MHz (2)	Serial Interface Active (Not High-Voltage Command) VRxB:VRxA = '01' (6) V_{OUT} is unloaded, V_{DD} = 5.5V Volatile DAC Register = 000h
		—	—	910	µA		10MHz (2)	
		—	—	1.7	mA		20MHz	
		—	—	510	µA	Dual	1MHz (2)	
		—	—	1.1	mA		10MHz (2)	
		—	—	1.85	mA		20MHz	
		—	—	250	µA	Single	1MHz (2)	Serial Interface Active (Not High-Voltage Command) VRxB:VRxA = '10' (4) V_{OUT} is unloaded. V_{REF} = V_{DD} = 5.5V Volatile DAC Register = 000h
		—	—	840	µA		10MHz (2)	
		—	—	1.65	mA		20MHz (2)	
		—	—	380	µA	Dual	1MHz (2)	
		—	—	970	µA		10MHz (2)	
		—	—	1.75	mA		20MHz (2)	
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command) VRxB:VRxA = '00' SCK = SDI = V_{SS} V_{OUT} is unloaded. Volatile DAC Register = 000h	
		—	—	380	µA	Dual		
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command) VRxB:VRxA = '11', V_{REF} = V_{DD} SCK = SDI = V_{SS} V_{OUT} is unloaded. Volatile DAC Register = 000h	
		—	—	380	µA	Dual		
		—	—	1.9	mA	EE Write Current V_{REF} = V_{DD} = 5.5V (After write, Serial Interface is Inactive.) Write all 0's to non-volatile DAC 0 (address 10h). V_{OUT} pins are unloaded.		
		—	145	180	µA	Single	HVC = 12.5V (High-Voltage Command) Serial Interface Inactive V_{REF} = V_{DD} = 5.5V, LAT/HVC = V_{IHH} DAC registers = 000h V_{OUT} pins are unloaded.	
		—	260	400	µA	Dual		
Power-Down Current	I_{DDP}	—	0.65	3.8	µA	PDxB:PDxA = '01' (5), V_{OUT} not connected		

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = '10'.

Note 5 The PDxB:PDxA = '01', '10', and '11' configurations should have the same current.

Note 6 By design, this is the worst-case current mode.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Resistor Ladder Resistance	R_L	100	140	180	kΩ	1.8V ≤ V_{DD} ≤ 5.5V V_{REF} ≥ 1.0V (7)
Resolution (# of Resistors and # of Taps) (see **B.1 "Resolution"**)	N	256			Taps	8-bit — No Missing Codes
		1024			Taps	10-bit — No Missing Codes
		4096			Taps	12-bit — No Missing Codes
Nominal V_{OUT} Match (11)	$\lvert V_{OUT} - V_{OUTMEAN} \rvert / V_{OUTMEAN}$	—	0.5	1.0	%	2.7V ≤ V_{DD} ≤ 5.5V (2)
		—	—	1.2	%	1.8V (2)
V_{OUT} Tempco (see **B.19 "V_{OUT} Temperature Coefficient"**)	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (7Fh, 1FFh or 7FFh)
V_{REF} pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V (1)

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 7 Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP48FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.

Note 11 Variation of one output voltage to mean output voltage.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Zero-Scale Error (see **B.5 "Zero-Scale Error (EZS)"**) (Code = 000h)	E_{ZS}	—	—	0.75	LSb	8-bit	VRxB:VRxA = '11', Gx = '0' V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0' V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0', No Load
		—	—	3	LSb	10-bit	VRxB:VRxA = '11', Gx = '0' V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0' V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0' No Load
		—	—	12	LSb	12-bit	VRxB:VRxA = '11', Gx = '0' V_{REF} = V_{DD}, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', Gx = '0' V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0', No Load
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01', Gx = '0' No Load
Offset Error (see **B.7 "Offset Error (EOS)"**)	E_{OS}	-15	±1.5	+15	mV	VRxB:VRxA = '00' Gx = '0' No Load	
Offset Voltage Temperature Coefficient	V_{OSTC}	—	±10	—	µV/°C		

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Full-Scale Error (see **B.4 "Full-Scale Error (EFS)"**)	E_{FS}	—	—	4.5	LSb	8-bit	Code = FFh, VRxB:VRxA = '11' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFh, VRxB:VRxA = '10' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFh, VRxB:VRxA = '01' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFh, VRxB:VRxA = '00' No Load
		—	—	18	LSb	10-bit	Code = 3FFh, VRxB:VRxA = '11' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = 3FFh, VRxB:VRxA = '10' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = 3FFh, VRxB:VRxA = '01' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = 3FFh, VRxB:VRxA = '00' No Load
		—	—	70	LSb	12-bit	Code = FFFh, VRxB:VRxA = '11' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFFh, VRxB:VRxA = '10' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFFh, VRxB:VRxA = '01' Gx = '0', V_{REF} = 2.048V, No Load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Code = FFFh, VRxB:VRxA = '00' No Load

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Gain Error (see **B.9 "Gain Error (EG)"**)[8]	E_G	-1.0	±0.1	+1.0	% of FSR	8-bit	Code = 250, No Load VRxB:VRxA = '00' Gx = '0'
		-1.0	±0.1	+1.0	% of FSR	10-bit	Code = 1000, No Load VRxB:VRxA = '00' Gx = '0'
		-1.0	±0.1	+1.0	% of FSR	12-bit	Code = 4000, No Load VRxB:VRxA = '00' Gx = '0'
Gain-Error Drift (see **B.10 "Gain-Error Drift (EGD)"**)	ΔG/°C	—	-3	—	ppm/°C		

Note 2 This parameter is ensured by characterization.

Note 8 This gain error does not include offset error.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Integral Nonlinearity (see **B.11 "Integral Nonlinearity (INL)"**) (10)	INL	-0.5	±0.1	+0.5	LSb	8-bit	VRxB:VRxA = '10' (codes: 6 to 250) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V V_{REF} = 1.0V
		-1.5	±0.4	+1.5	LSb	10-bit	VRxB:VRxA = '10' (codes: 25 to 1000) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"** (2)			LSb		V_{DD} = 1.8V V_{REF} = 1.0V
		-6	±1.5	+6	LSb	12-bit	VRxB:VRxA = '10' (codes: 100 to 4000) V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V V_{REF} = 1.0V

Note 2 This parameter is ensured by characterization.

Note 10 Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Differential Nonlinearity (see **B.12 "Differential Nonlinearity (DNL)"**)(10)	DNL	-0.25	±0.0125	+0.25	LSb	8-bit	VRxB:VRxA = '10' (codes: 6 to 250) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V
		-0.5	±0.05	+0.5	LSb	10-bit	VRxB:VRxA = '10' (codes: 25 to 1000) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V
		-1.0	±0.2	+1.0	LSb	12-bit	VRxB:VRxA = '10' (codes: 100 to 4000) V_{DD} = V_{REF} = 5.5V
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '00', '01', '11'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '01' V_{DD} = 5.5V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		Char: VRxB:VRxA = '10', '11' V_{REF} = 1.0V, Gx = '1'
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		V_{DD} = 1.8V

Note 2 This parameter is ensured by characterization.

Note 10 Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
-3 dB Bandwidth (see **B.16 "-3 dB Bandwidth"**)	BW	—	200	—	kHz	V_{REF} = 2.048V ± 0.1V VRxB:VRxA = '10', Gx = '0'
		—	100	—	kHz	V_{REF} = 2.048V ± 0.1V VRxB:VRxA = '10', Gx = '1'
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	1.8V ≤ V_{DD} < 5.5V Output Amplifier's minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.04	—	V	1.8V ≤ V_{DD} < 5.5V Output Amplifier's maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF R_L = ∞
Slew Rate (9)	SR	—	0.44	—	V/µs	R_L = 5 kΩ
Short-Circuit Current	I_{SC}	3	9	14	mA	DAC code = Full Scale
Internal Band Gap						
Band Gap Voltage	V_{BG}	1.18	1.22	1.26	V	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	15	—	ppm/°C	
Operating Range (V_{DD})		2.0	—	5.5	V	V_{REF} pin voltage stable
		2.2	—	5.5	V	V_{OUT} output linear
External Reference (V_{REF})						
Input Range (1)	V_{REF}	V_{SS}	—	V_{DD} – 0.04	V	VRxB:VRxA = '11' (Buffered mode)
		V_{SS}	—	V_{DD}	V	VRxB:VRxA = '10' (Unbuffered mode)
Input Capacitance	C_{REF}	—	1	—	pF	VRxB:VRxA = '10' (Unbuffered mode)
Total Harmonic Distortion (1)	THD	—	-64	—	dB	V_{REF} = 2.048V ± 0.1V VRxB:VRxA = '10', Gx = '0' Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **B.14 "Major-Code Transition Glitch"**)		—	45	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **B.15 "Digital Feed-through"**)		—	<10	—	nV-s	

Note 1 This parameter is ensured by design.

Note 9 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Inputs/Outputs ($\overline{CS}$, SCK, SDI, SDO, $\overline{LAT0}$/HVC)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V
		0.5 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low-Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Output Low Voltage	V_{OL}	V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 5 mA, V_{DD} = 5.5V
		V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 1 mA, V_{DD} = 1.8V
Output High Voltage	V_{OH}	0.7V_{DD}	—	V_{DD}	V	I_{OH} = -2.5 mA, V_{DD} = 5.5V
		0.7V_{DD}	—	V_{DD}	V	I_{OH} = -1 mA, V_{DD} = 1.8V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 20 MHz

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
RAM Value							
Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	3FFh	hex	10-bit	
		0h	—	FFFh	hex	12-bit	
DAC Register POR/BOR Value	N	See **Table 4-2**			hex	8-bit	
		See **Table 4-2**			hex	10-bit	
		See **Table 4-2**			hex	12-bit	
PDCON Initial Factory Setting		See **Table 4-2**			hex		
EEPROM							
Endurance	EN_{EE}	—	1M	—	Cycles	**Note 1**, **Note 2**	
Data Retention	DR_{EE}	—	200	—	Years	At +25°C (1), (2)	
EEPROM Range	N	0h	—	FFh	hex	8-bit	DACx Register(s)
		0h	—	3FFh	hex	10-bit	DACx Register(s)
		0h	—	FFFh	hex	12-bit	DACx Register(s)
Initial Factory Setting	N	See **Table 4-2**					
EEPROM Programming Write Cycle Time	t_{WC}	—	11	16	ms	V_{DD} = +1.8V to 5.5V	
Power Requirements							
Power Supply Sensitivity (**B.17 "Power-Supply Sensitivity (PSS)"**)	PSS	—	0.002	0.005	%/%	8-bit	Code = 7Fh
		—	0.002	0.005	%/%	10-bit	Code = 1FFh
		—	0.002	0.005	%/%	12-bit	Code = 7FFh

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = '10'.
5. The PDxB:PDxA = '01', '10', and '11' configurations should have the same current.
6. By design, this is the worst-case current mode.
7. Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP48FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.
8. This gain error does not include offset error.
9. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
10. Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.
11. Variation of one output voltage to mean output voltage.

1.1 Reset, Power-Down, and SPI Mode Timing Waveforms and Requirements

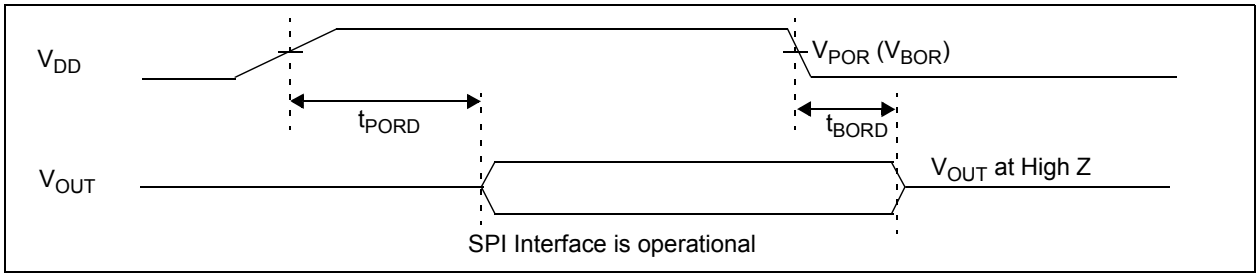


FIGURE 1-1: *Power-on and Brown-out Reset Waveforms.*

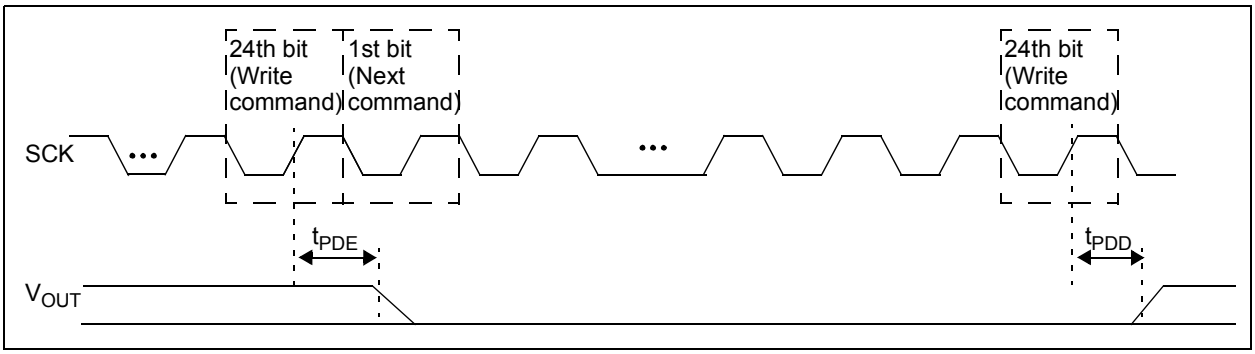


FIGURE 1-2: *SPI Power-Down Command Waveforms.*

TABLE 1-1: RESET AND POWER-DOWN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +1.8V to 5.5V, V_{SS} = 0V R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power-on Reset Delay	t_{PORD}	—	60	—	µs	
Brown-out Reset Delay	t_{BORD}	—	45	—	µs	V_{DD} transitions from $V_{DD(MIN)} \rightarrow > V_{POR}$ V_{OUT} driven to V_{OUT} disabled
Power-Down Output Disable Time Delay	T_{PDD}	—	10.5	—	µs	PDxB:PDxA = '11', '10', or '01' → "00" started from falling edge of the SCK at the end of the 24th clock cycle. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.
Power-Down Output Enable Time Delay	T_{PDE}	—	1	—	µs	PDxB:PDxA = "00" → '11', '10', or '01' started from falling edge of the SCK at the end of the 24th clock cycle. V_{OUT} = V_{OUT} - 10 mV. V_{OUT} not connected.

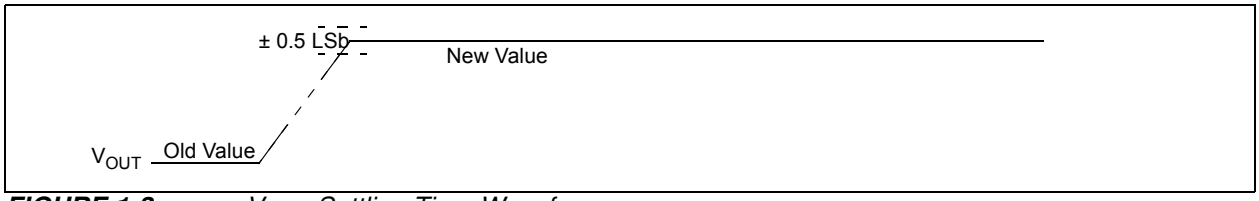


FIGURE 1-3: *V_{OUT} Settling Time Waveform.*

TABLE 1-2: V_{OUT} SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +1.8V to 5.5V, V_{SS} = 0V R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (±0.5LSb error band, C_L = 100 pF) (see **B.13 "Settling Time"**)	t_S	—	7.8	—	µs	8-bit	Code = 40h → C0h; C0h → 40h (3)
		—	7.8	—	µs	10-bit	Code = 100h → 300h; 300h → 100h (3)
		—	7.8	—	µs	12-bit	Code = 400h → C00h; C00h → 400h (3)

Note 3 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

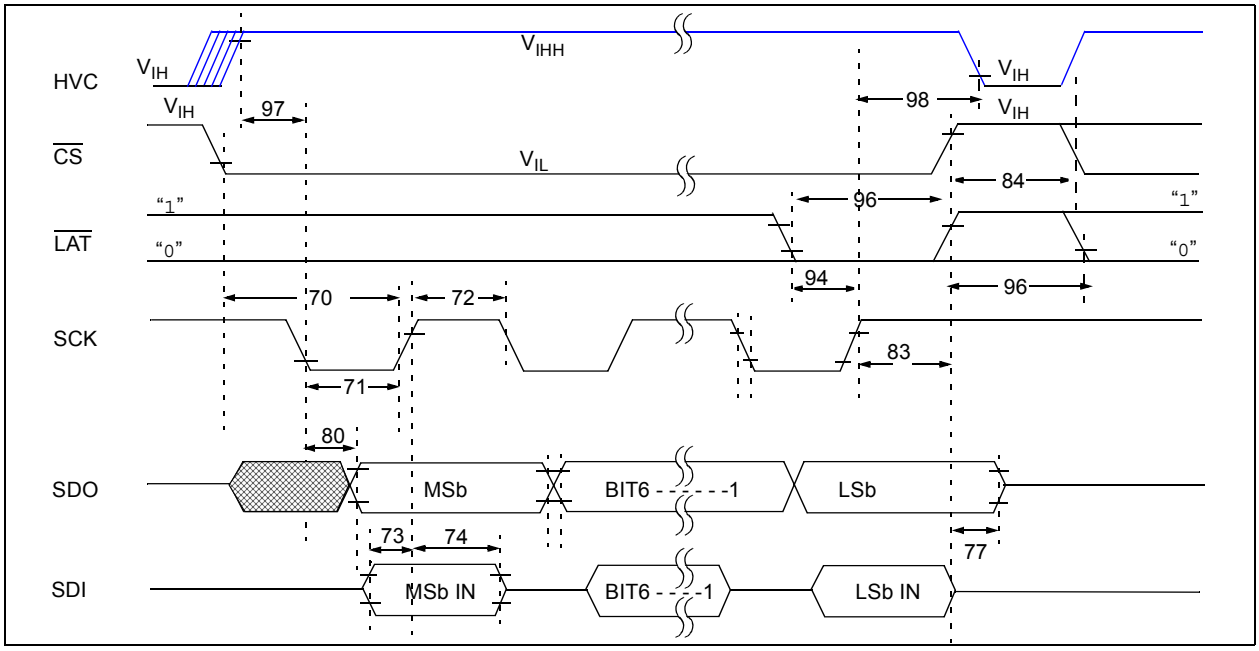


FIGURE 1-4: *SPI Timing (Mode = 11) Waveforms.*

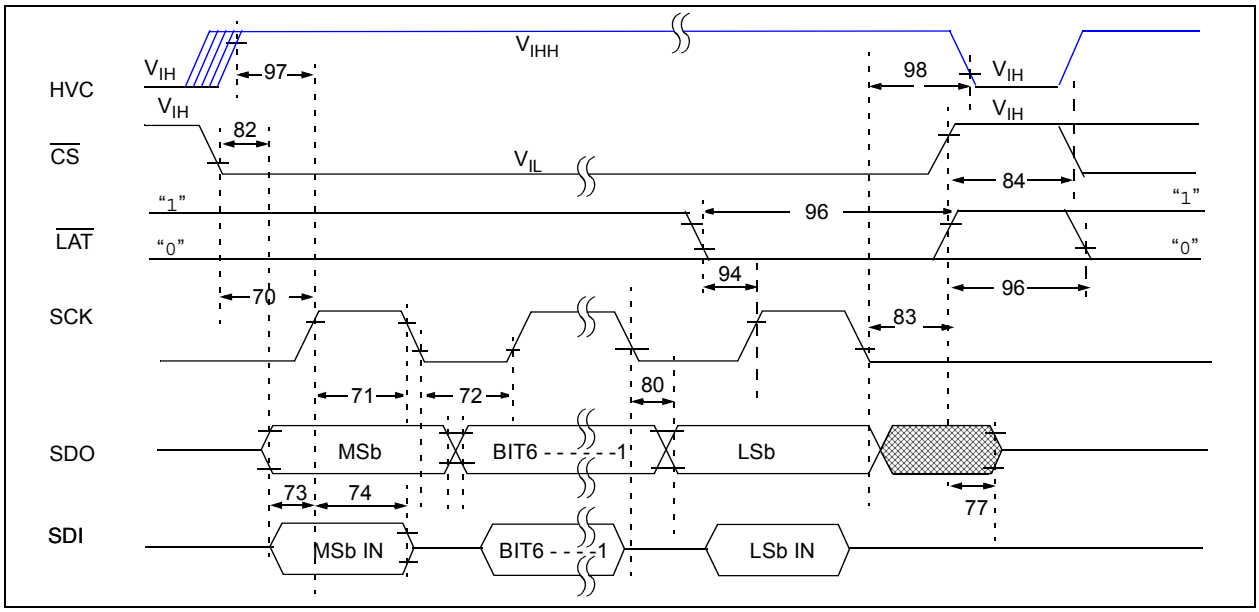


FIGURE 1-5: *SPI Timing (Mode = 00) Waveforms.*

TABLE 1-3: SPI REQUIREMENTS (MODE = 11)

SPI AC Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**.				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	F_{SCK}	SCK input frequency	—	10	MHz	V_{DD} = 2.7V to 5.5V (Read Command)
			—	20	MHz	V_{DD} = 2.7V to 5.5V (All Other Commands)
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	TcsA2scH	$\overline{CS}$ Active (V_{IL}) to command's 1st SCK↑ input	60	—	ns	
71	TscH	SCK input high time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
72	TscL	SCK input low time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
73	TdiV2scH	Setup time of SDI input to SCK↑ edge	10	—	ns	
74	TscH2diL	Hold time of SDI input from SCK↑ edge	20	—	ns	
77	TcsH2DOZ	$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	—	50	ns	**Note 1**
80	TscL2doV	SDO data output valid after SCK↓ edge	—	45	ns	V_{DD} = 2.7V to 5.5V
			—	170	ns	V_{DD} = 1.8V to 2.7V
83	TscH2csL	$\overline{CS}$ Inactive (V_{IH}) after SCK↑ edge	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		µs	V_{DD} = 1.8V to 2.7V
84	TcsH	$\overline{CS}$ high time (V_{IH})	50	—	ns	
94	T_{LATSU}	$\overline{LAT}$ ↓ to SCK↑ (write data 24th bit) setup time	20	—	ns	Write Data transferred (4)
96	T_{LAT}	$\overline{LAT}$ high or low time	20	—	ns	
97	T_{HVCSU}	HVC ↑ to SCK ↓ (1st data bit) (HVC setup time)	0	—	ns	High-Voltage Commands(1)
98	T_{HVCHD}	SCK ↑ (last bit of command (8th or 24th bit)) to HVC ↓ (HVC hold time)	25	—	ns	High-Voltage Commands(1)

Note 1 This parameter is ensured by design.

Note 4 The transition of the LAT signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (VOUT) before the register is overwritten with the new value.

TABLE 1-4: SPI REQUIREMENTS (MODE = 00)

SPI AC Characteristics			Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**.			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
	F_{SCK}	SCK input frequency	—	10	MHz	V_{DD} = 2.7V to 5.5V (Read Command)
			—	20	MHz	V_{DD} = 2.7V to 5.5V (All Other Commands)
			—	1	MHz	V_{DD} = 1.8V to 2.7V
70	TcsA2scH	$\overline{CS}$ Active (V_{IL}) to SCK↑ input	60	—	ns	
71	TscH	SCK input high time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
72	TscL	SCK input low time	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
73	TDIV2scH	Setup time of SDI input to SCK↑ edge	10	—	ns	
74	TscH2DIL	Hold time of SDI input from SCK↑ edge	20	—	ns	
77	TcsH2DOZ	$\overline{CS}$ Inactive (V_{IH}) to SDO output hi-impedance	—	50	ns	**Note 1**
80	TscL2DOV	SDO data output valid after SCK↓ edge	—	45	ns	V_{DD} = 2.7V to 5.5V
			—	170	ns	V_{DD} = 1.8V to 2.7V
82	TssL2doV	$\overline{SDO}$ data output valid after $\overline{CS}$ Active (V_{IL})	—	70	ns	
83	TscH2csL	$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		µs	V_{DD} = 1.8V to 2.7V
84	TcsH	$\overline{CS}$ high time (V_{IH})	50	—	ns	
94	T_{LATSU}	$\overline{LAT}$ ↓ to SCK↑ (write data 24th bit) setup time	10	—	ns	Write Data transferred (4)
96	T_{LAT}	$\overline{LAT}$ high or low time	50	—	ns	
97	T_{HVCSU}	HVC ↑ to SCK ↑ (1st data bit) (HVC setup time)	0	—	ns	High-Voltage Commands (1)
98	T_{HVCHD}	SCK ↓ (last bit of command (8th or 24th bit)) to HVC ↓ (HVC hold time)	25	—	ns	High-Voltage Commands (1)

Note 1 This parameter is ensured by design.

Note 4 The transition of the LAT signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (VOUT) before the register is overwritten with the new value.

Timing Table Notes:

1. This parameter is ensured by design.
2. This parameter ensured by characterization.
3. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
4. The transition of the LAT signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (V_{OUT}) before the register is overwritten with the new value.

Temperature Specifications

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 10LD-MSOP	θ_{JA}	—	202	—	°C/W	

Note 1: The MCP48FEBXX devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note: The device Performance Curves are available in a separate document. This is done to keep the file size of this PDF document less than the 10 MB file attachment limit of many mail servers.
The MCP48FXBXX Performance Curves document is literature number **DS20005440**, and can be found on the Microchip website. Look on the MCP48FEBXX product page under “Documentation and Software”, in the Data Sheets category.