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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP606/7/8/9

2.5V to 6.0V Micropower CMOS Op Amp

Features

- Low Input Offset Voltage: 250 µV (maximum)
- Rail-to-Rail Output
- Low Input Bias Current: 80 pA (maximum at +85°C)
- Low Quiescent Current: 25 µA (maximum)
- Power Supply Voltage: 2.5V to 6.0V
- Unity-Gain Stable
- Chip Select ($\overline{CS}$) Capability: **MCP608**
- Industrial Temperature Range: -40°C to +85°C
- No Phase Reversal
- Available in Single, Dual and Quad Packages

Typical Applications

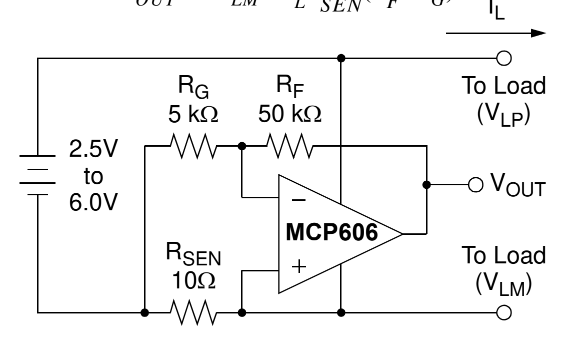
- Battery Power Instruments
- High-Impedance Applications
- Strain Gauges
- Medical Instruments
- Test Equipment

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application

$$V_{OUT} = V_{LM} + I_L R_{SEN}(R_F / R_G)$$



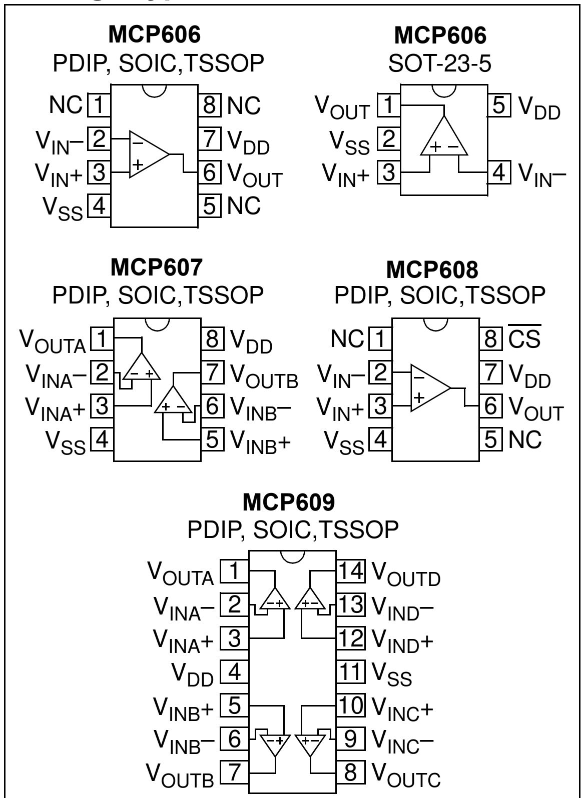
Low-Side Battery Current Sensor

Description

The MCP606/7/8/9 family of operational amplifiers (op amps) from Microchip Technology Inc. are unity-gain stable with low offset voltage (250 µV, maximum). Performance characteristics include rail-to-rail output swing capability and low input bias current (80 pA at +85°C, maximum). These features make this family of op amps well suited for single-supply, precision, high-impedance, battery-powered applications.

The single is available in standard 8-lead PDIP, SOIC and TSSOP packages, as well as in a SOT-23-5 package. The single MCP608 with Chip Select ($\overline{CS}$) is offered in the standard 8-lead PDIP, SOIC and TSSOP packages. The dual MCP607 is offered in the standard 8-lead PDIP, SOIC and TSSOP packages. Finally, the quad MCP609 is offered in the standard 14-lead PDIP, SOIC and TSSOP packages. All devices are fully specified from -40°C to +85°C, with power supplies from 2.5V to 6.0V.

Package Types



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V

Current at Input Pins ....±2 mA

Analog Inputs ($V_{IN}+$, $V_{IN}-$) †† .... V_{SS} – 1.0V to V_{DD} + 1.0V

All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V

Difference Input Voltage .... $|V_{DD} - V_{SS}|$

Output Short Circuit Current ....Continuous

Current at Output and Supply Pins ....±30 mA

Storage Temperature ....–65° C to +150° C

Maximum Junction Temperature (T_J)........................+150° C

ESD Protection On All Pins (HBM; MM)............. ≥ 3 kV; 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-250	—	+250	µV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±1.8	—	µV/°C	T_A = -40°C to +85°C
Power Supply Rejection Ratio	PSRR	80	93	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
At Temperature	I_B	—	—	80	pA	T_A = +85°C
Input Offset Bias Current	I_{OS}	—	1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}‖6	—	Ω‖pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}‖6	—	Ω‖pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3		V_{DD} – 1.1	V	CMRR ≥ 75 dB
Common Mode Rejection Ratio	CMRR	75	91	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 3.9V
Open-Loop Gain						
DC Open-Loop Gain (Large-signal)	A_{OL}	105	121	—	dB	R_L = 25 kΩ to V_L, V_{OUT} = 50 mV to V_{DD} – 50 mV
DC Open-Loop Gain (Large-signal)	A_{OL}	100	118	—	dB	R_L = 5 kΩ to V_L, V_{OUT} = 0.1V to V_{DD} – 0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 20	mV	R_L = 25 kΩ to V_L, 0.5V input overdrive
	V_{OL}, V_{OH}	V_{SS} + 45	—	V_{DD} – 60	mV	R_L = 5 kΩ to V_L, 0.5V input overdrive
Linear Output Voltage Range	V_{OUT}	V_{SS} + 50	—	V_{DD} – 50	mV	R_L = 25 kΩ to V_L, A_{OL} ≥ 105 dB
	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 5 kΩ to V_L, A_{OL} ≥ 100 dB
Output Short Circuit Current	I_{SC}	—	7	—	mA	V_{DD} = 2.5V
	I_{SC}	—	17	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	2.5	—	6.0	V	
Quiescent Current per Amplifier	I_Q	—	18.7	25	µA	I_O = 0

Note 1: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 2.5V and 5.5V.

AC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
AC Response						
Gain Bandwidth Product	GBWP	—	155	—	kHz	
Phase Margin	PM	—	62	—	°	G = +1 V/V
Slew Rate	SR	—	0.08	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	2.8	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	38	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

MCP608 CHIP SELECT CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF, and $\overline{CS}$ is tied low (refer to Figure 1-2 and Figure 1-3).						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	-0.1	0.01	—	µA	$\overline{CS}$ = $0.2V_{DD}$
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.01	0.1	µA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current	I_{SS}	-2	-0.05	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage, $\overline{CS}$ High	$I_{O(LEAK)}$	—	10	—	nA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	9	100	µs	$\overline{CS}$ = $0.2V_{DD}$ to V_{OUT} = 0.9 $V_{DD}/2$, G = +1 V/V, R_L = 1 kΩ to V_{SS}
$\overline{CS}$ High to Amplifier Output Hi-Z	t_{OFF}	—	0.1	—	µs	$\overline{CS}$ = $0.8V_{DD}$ to V_{OUT} = 0.1 $V_{DD}/2$, G = +1 V/V, R_L = 1 kΩ to V_{SS}
$\overline{CS}$ Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5.0V

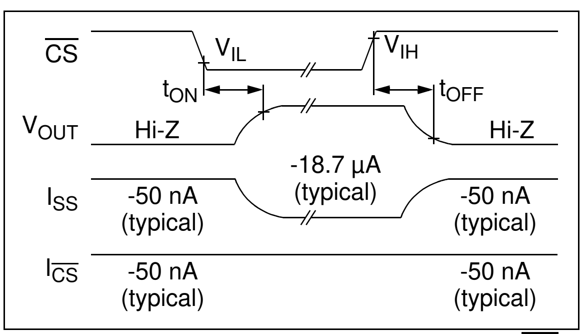


FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ Pin on the MCP608.*

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	139	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP606/7/8/9 operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in **Section 4.5 "Supply Bypass"**.

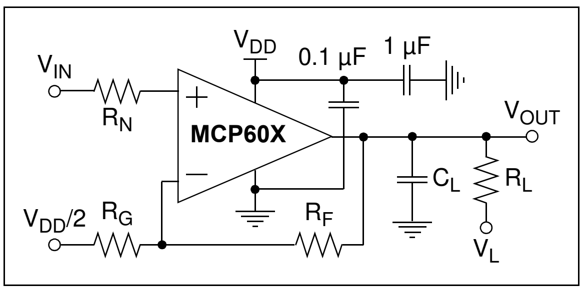


FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

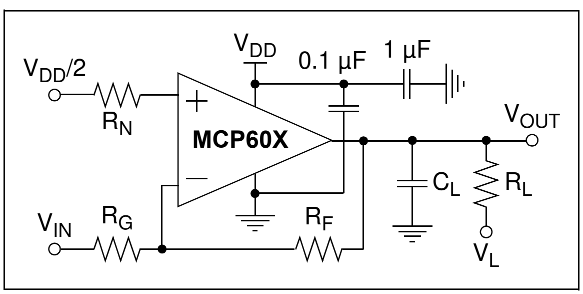


FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

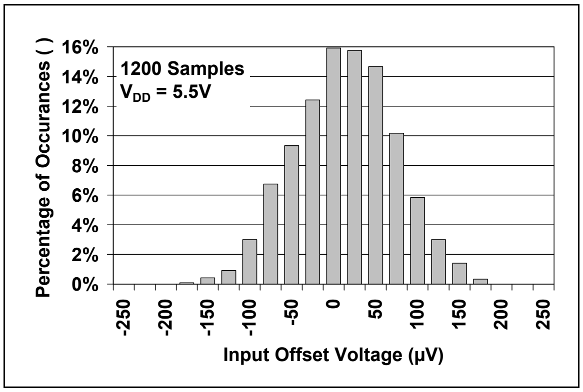


FIGURE 2-1: *Input Offset Voltage at V_{DD} = 5.5V.*

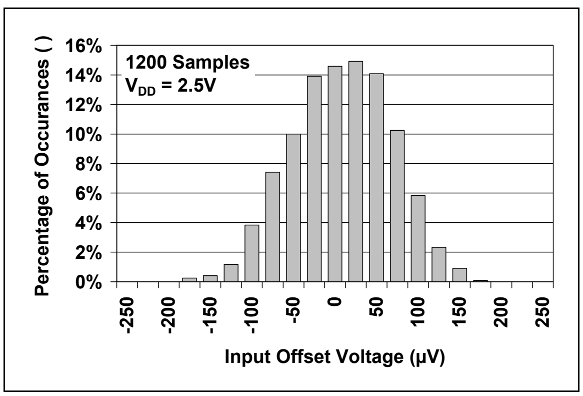


FIGURE 2-2: *Input Offset Voltage at V_{DD} = 2.5V.*

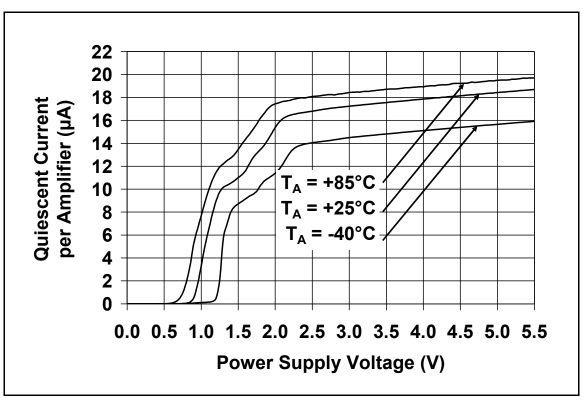


FIGURE 2-3: *Quiescent Current vs. Power Supply Voltage.*

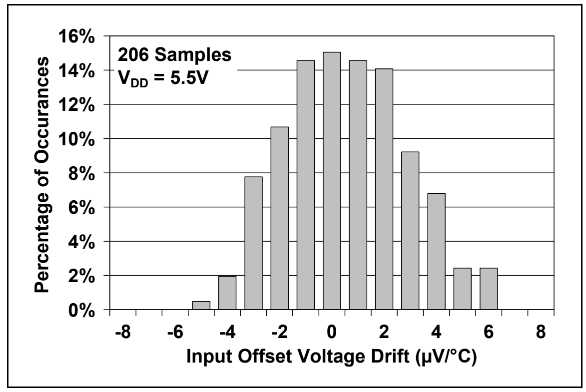


FIGURE 2-4: *Input Offset Voltage Drift Magnitude at V_{DD} = 5.5V.*

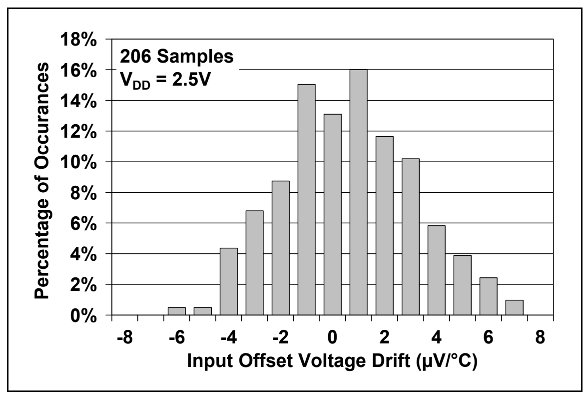


FIGURE 2-5: *Input Offset Voltage Drift Magnitude at V_{DD} = 2.5V.*

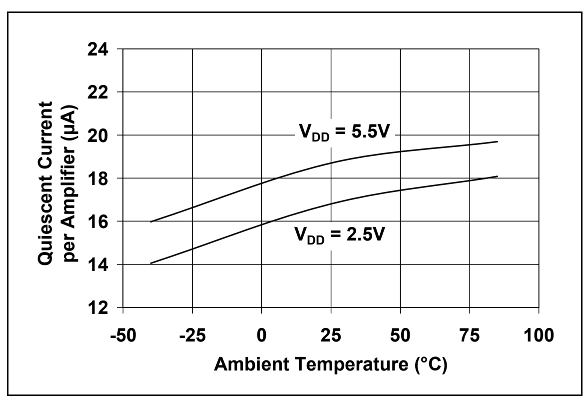


FIGURE 2-6: *Quiescent Current vs. Ambient Temperature.*

Note: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

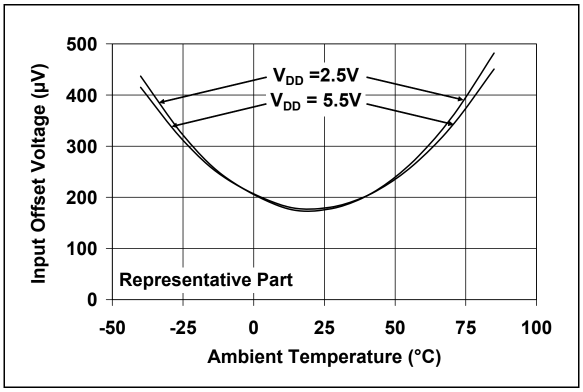


FIGURE 2-7: *Input Offset Voltage vs. Ambient Temperature.*

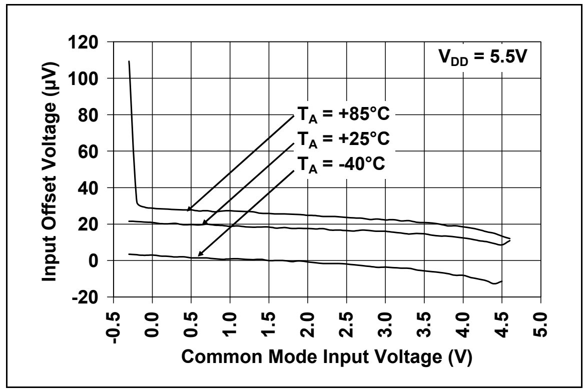


FIGURE 2-10: *Input Offset Voltage vs. Common Mode Input Voltage.*

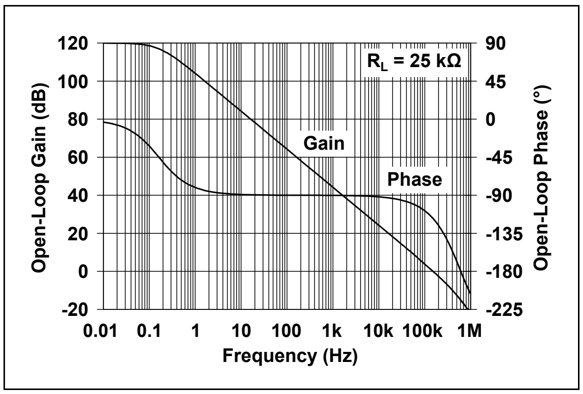


FIGURE 2-8: *Open-Loop Gain and Phase vs. Frequency.*

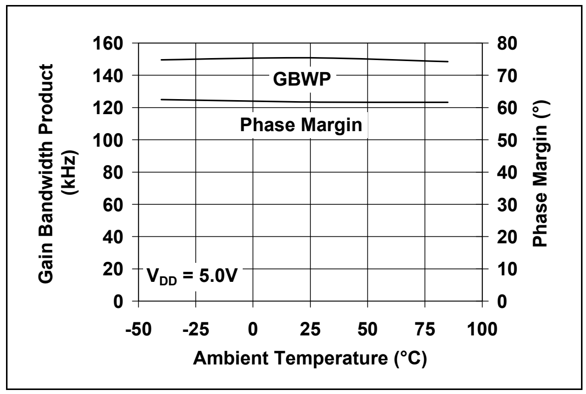


FIGURE 2-11: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

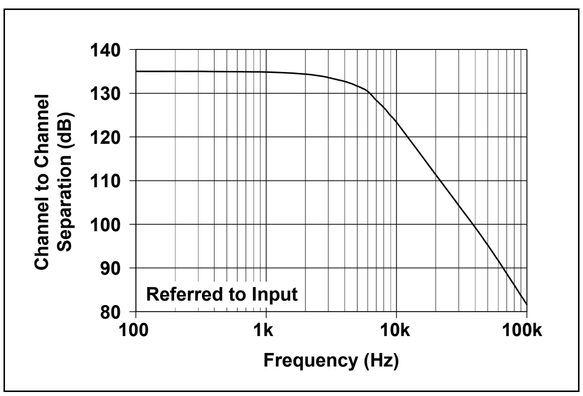


FIGURE 2-9: *Channel-to-Channel Separation (MCP607 and MCP609 only).*

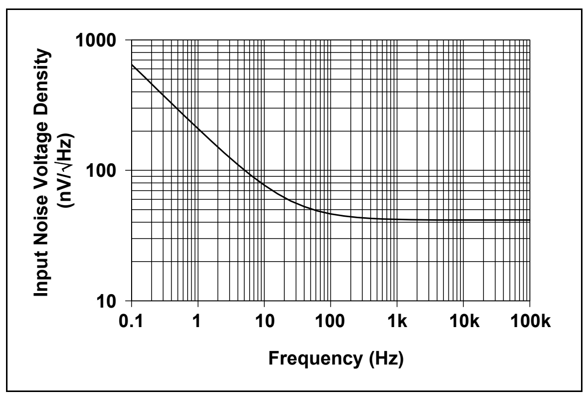


FIGURE 2-12: *Input Noise Voltage Density vs. Frequency.*

Note: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

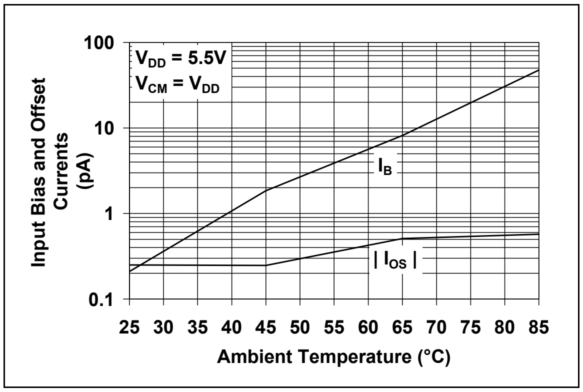


FIGURE 2-13: Input Bias Current, Input Offset Current vs. Ambient Temperature.

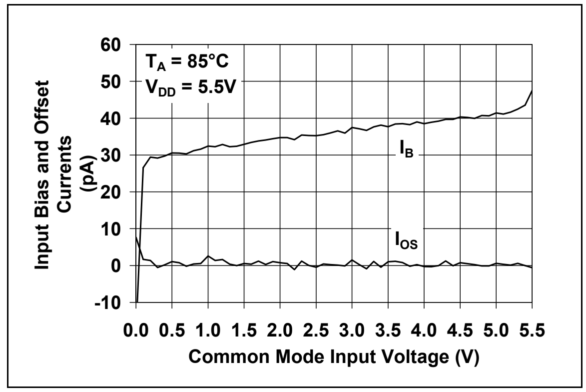


FIGURE 2-16: Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.

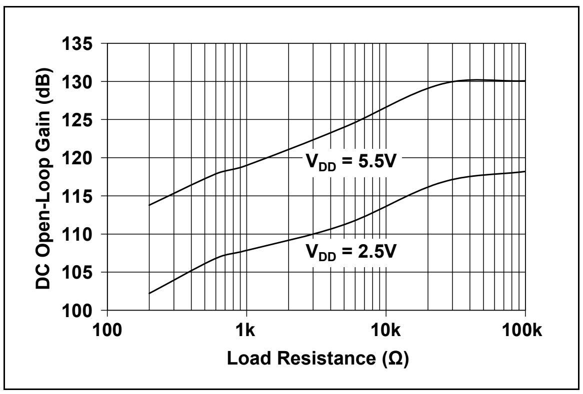


FIGURE 2-14: DC Open-Loop Gain vs. Load Resistance.

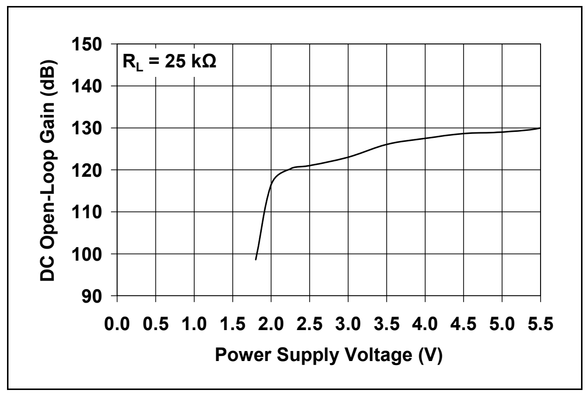


FIGURE 2-17: DC Open-Loop Gain vs. Power Supply Voltage.

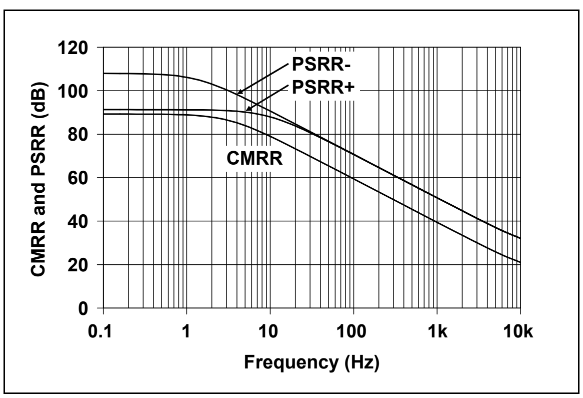


FIGURE 2-15: CMRR, PSRR vs. Frequency.

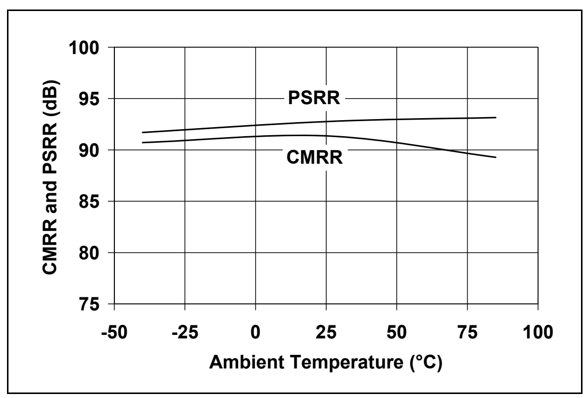


FIGURE 2-18: CMRR, PSRR vs. Ambient Temperature.

Note: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

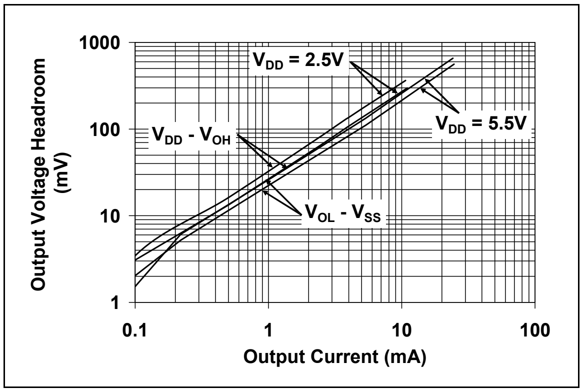


FIGURE 2-19: *Output Voltage Headroom vs. Output Current Magnitude.*

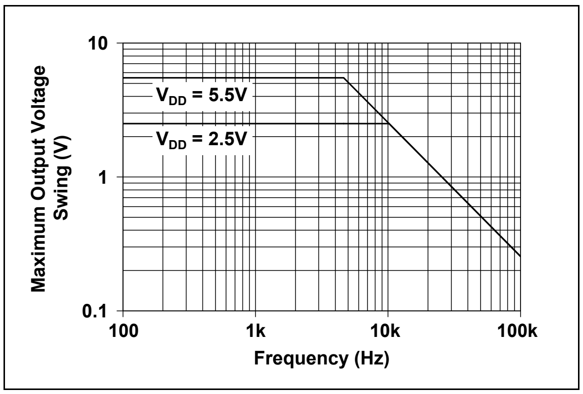


FIGURE 2-20: *Maximum Output Voltage Swing vs. Frequency.*

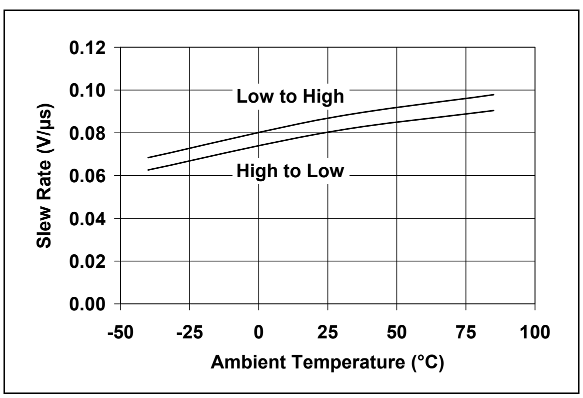


FIGURE 2-21: *Slew Rate vs. Ambient Temperature.*

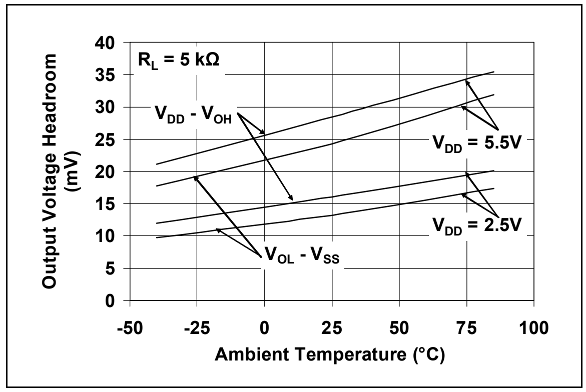


FIGURE 2-22: *Output Voltage Headroom vs. Ambient Temperature at R_L = 5 kΩ.*

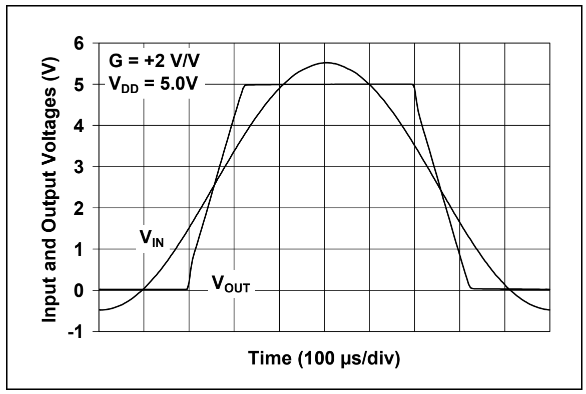


FIGURE 2-23: *The MCP606/7/8/9 Show No Phase Reversal.*

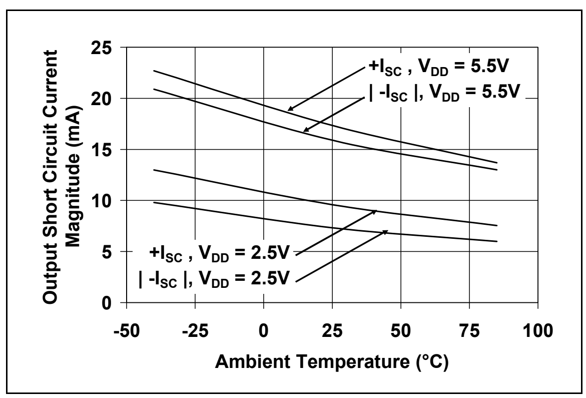


FIGURE 2-24: *Output Short Circuit Current Magnitude vs. Ambient Temperature.*

Note: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

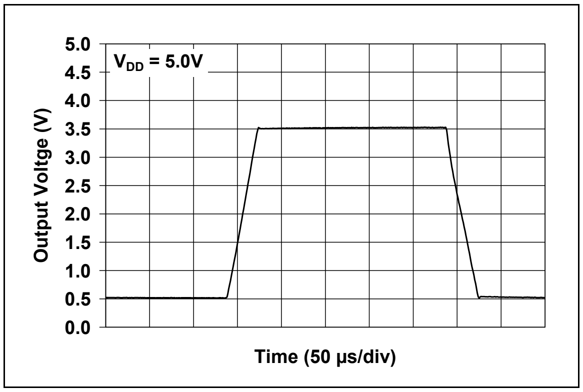


FIGURE 2-25: Large-signal, Non-inverting Pulse Response.

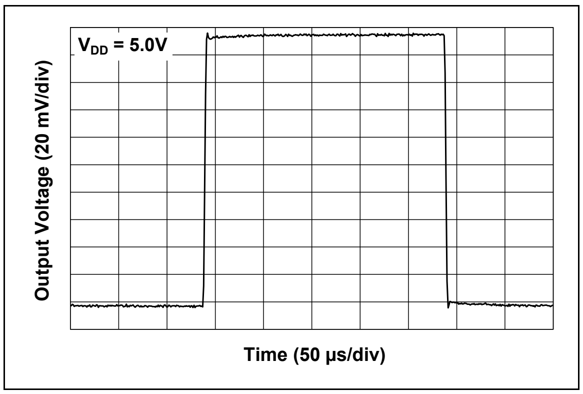


FIGURE 2-26: Small-signal, Non-inverting Pulse Response.

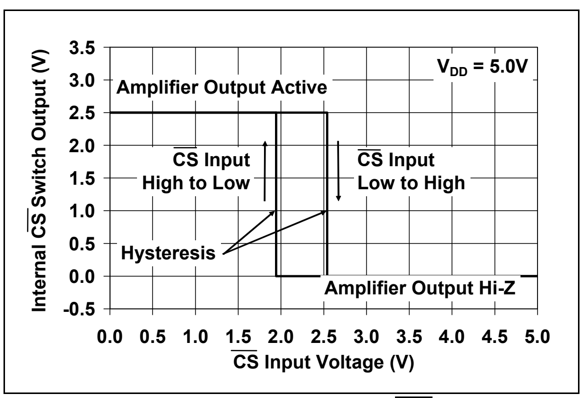


FIGURE 2-27: Chip Select ($\overline{CS}$) Hysteresis (MCP608 only).

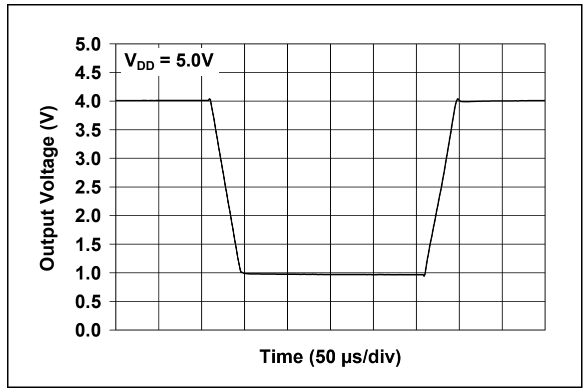


FIGURE 2-28: Large-signal, Inverting Pulse Response.

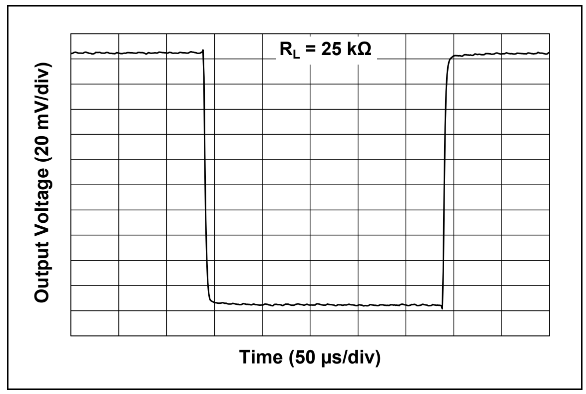


FIGURE 2-29: Small-signal, Inverting Pulse Response.

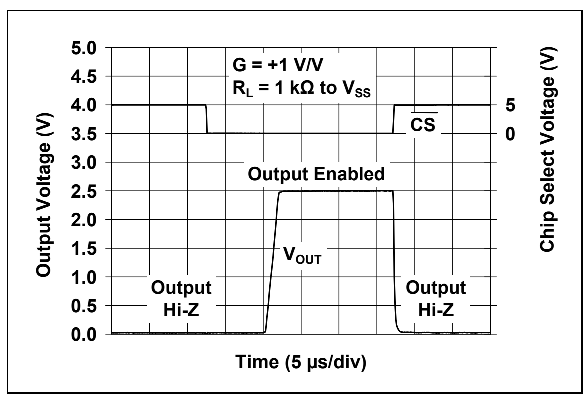


FIGURE 2-30: Amplifier Output Response Times vs. Chip Select ($\overline{CS}$) Pulse (MCP608 only).

Note: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ is tied low.

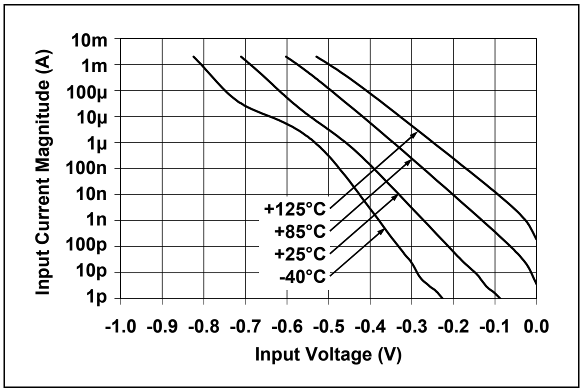


FIGURE 2-31: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP606		MCP607	MCP608	MCP609	Symbol	Description
PDIP, SOIC, TSSOP	SOT-23-5					
6	1	1	6	1	V_{OUT}, V_{OUTA}	Output (op amp A)
2	4	2	2	2	$V_{IN}–$, $V_{INA}–$	Inverting Input (op amp A)
3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
7	5	8	7	4	V_{DD}	Positive Power Supply
—	—	5	—	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	6	—	6	$V_{INB}–$	Inverting Input (op amp B)
—	—	7	—	7	V_{OUTB}	Output (op amp B)
—	—	—	—	8	V_{OUTC}	Output (op amp B)
—	—	—	—	9	$V_{INC}–$	Inverting Input (op amp C)
—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	2	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	13	$V_{IND}–$	Inverting Input (op amp D)
—	—	—	—	14	V_{OUTD}	Output (op amp D)
—	—	—	8	—	$\overline{CS}$	Chip Select
1, 5, 8	—	—	1, 5	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Chip Select Digital Input

The Chip Select ($\overline{CS}$) pin is a Schmitt-triggered, CMOS logic input. It is used to place the MCP608 op amp in a Low-power mode, with the output(s) in a Hi-Z state.

3.4 Power Supply Pins

The positive power supply pin (V_{DD}) is 2.5V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the output pins are at voltages between V_{SS} and V_{DD}; while the input pins are at voltages between V_{SS} – 0.3V and V_{DD} + 0.3V.

Typically, these parts are used in a single-supply (positive) configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors .

NOTES:

4.0 APPLICATIONS INFORMATION

The MCP606/7/8/9 family of op amps is manufactured using Microchip's state-of-the-art CMOS process These op amps are unity-gain stable and suitable for a wide range of general purpose applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP606/7/8/9 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-23 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

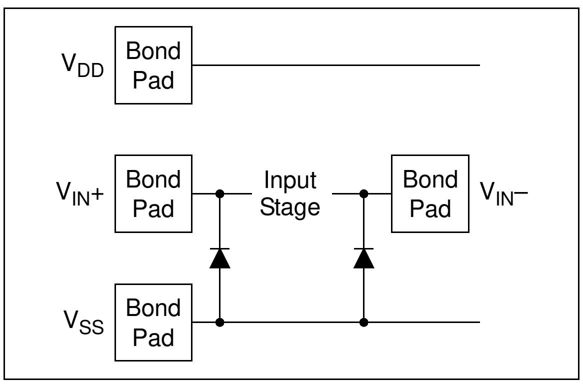
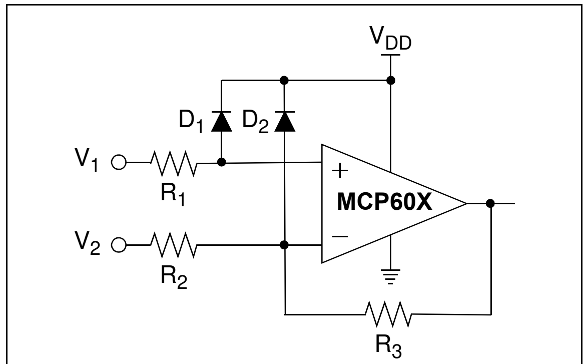


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the $V_{IN}+$ and $V_{IN}–$ pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\text{ mA}}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\text{ mA}}$$

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}–$) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-31. Applications that are high impedance may need to limit the useable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP606/7/8/9 op amps use a PMOS input stage. It operates at low common mode input voltage (V_{CM}), including ground. WIth this topology, the device operates with V_{CM} up to V_{DD} –1.1V and 0.3V below V_{SS}.

Figure 4-3 shows a unity gain buffer. Since V_{OUT} is the same voltage as the inverting input, V_{OUT} must be kept below V_{DD}–1.2V for correct operation.

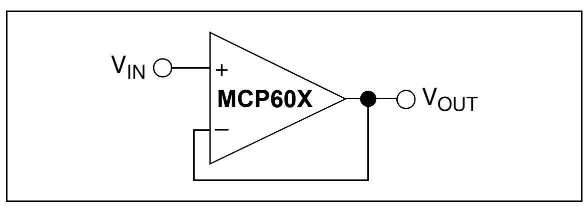


FIGURE 4-3: *Unity Gain Buffer has a Limited V_{OUT} Range.*

4.2 Rail-to-Rail Output

There are two specifications that describe the output-swing capability of the MCP606/7/8/9 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 kΩ load to $V_{DD}/2$. Figure 2-23 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output-swing capability of these amplifiers (Linear Output Voltage Range) defines the maximum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large-signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} conditions in the specification table.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage-feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain-peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

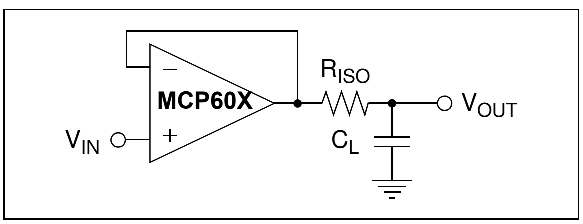


FIGURE 4-4: *Output Resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-5 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

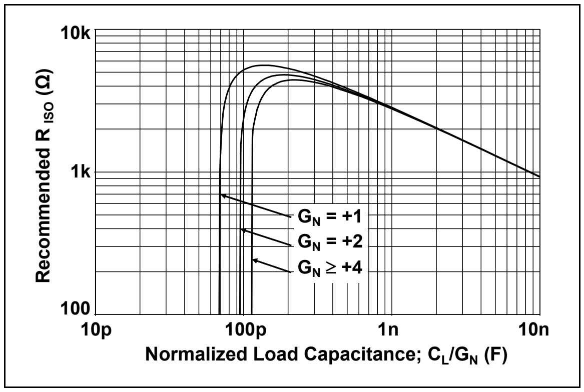


FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP606/7/8/9 SPICE macro model are helpful.

4.4 MCP608 Chip Select

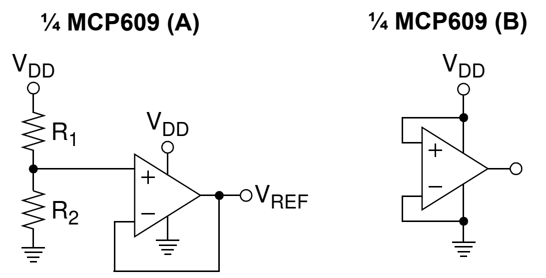
The MCP608 is a single op amp with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 50 nA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. The $\overline{CS}$ pin has an internal 5 MΩ (typical) pull-down resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pins is left floating. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.5 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts.

4.6 Unused Op Amps

An unused op amp in a quad package (MCP609) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



$$V_{REF} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}$$

FIGURE 4-6: *Unused Op Amps.*

4.7 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP606/7/8/9 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

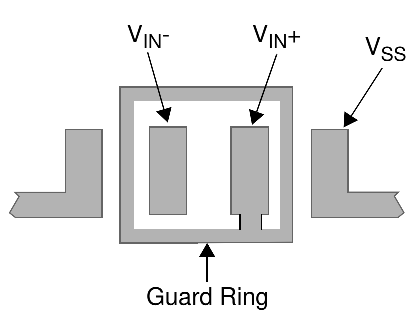


FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-gain Buffer:
   a) Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.

4.8 Application Circuits

4.8.1 LOW-SIDE BATTERY CURRENT SENSOR

The MCP606/7/8/9 op amps can be used to sense the load current on the low-side of a battery using the circuit in Figure 4-8. In this circuit, the current from the power supply (minus the current required to power the MCP606) flows through a sense resistor (R_{SEN}), which converts it to voltage. This is gained by the the amplifier and resistors, R_G and R_F. Since the non-inverting input of the amplifier is at the load's negative supply (V_{LM}), the gain from R_{SEN} to V_{OUT} is R_F/R_G.

$$V_{OUT} = V_{LM} + I_L R_{SEN}(R_F/R_G)$$

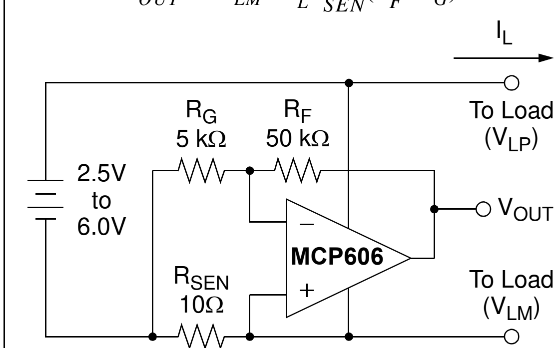


FIGURE 4-8: *Low Side Battery Current Sensor.*

Since the input bias current and input offset voltage of the MCP606 are low, and the input is capable of swinging below ground, there is very little error generated by the amplifier. The quiescent current is very low, which helps conserve battery power. The rail-to-rail output makes it possible to read very low currents.

4.8.2 PHOTODIODE AMPLIFIERS

Sensors that produce an output current and have high output impedance can be connected to a transimpedance amplifier. The transimpedance amplifier converts the current into voltage. Photodiodes are one sensor that produce an output current.

The key op amp characteristics that are needed for these circuits are: low input offset voltage, low input bias current, high input impedance and an input common mode range that includes ground. The low input offset voltage and low input bias current support a very low voltage drop across the photodiode; this gives the best photodiode linearity. Since the photodiode is biased at ground, the op amp's input needs to function well both above and below ground.

4.8.2.1 Photo-Voltaic Mode

Figure 4-9 shows a transimpedance amplifier with a photodiode (D_1) biased in the Photo-voltaic mode (0V across D_1), which is used for precision photodiode sensing.

As light impinges on D_1, charge is generated, causing a current to flow in the reverse bias direction of D_1. The op amp's negative feedback forces the voltage across the D_1 to be nearly 0V. Resistor R_2 converts the current into voltage. Capacitor C_2 limits the bandwidth and helps stabilize the circuit when D_1's junction capacitance is large.

$$V_{OUT} = I_{D1}R_2$$

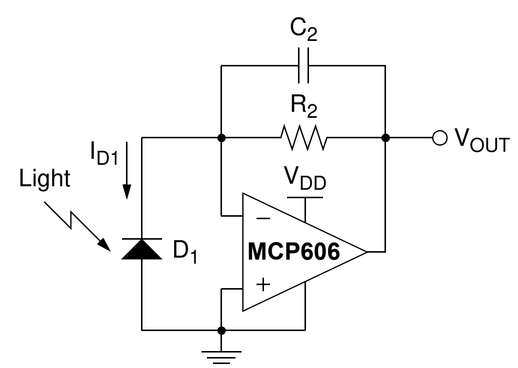


FIGURE 4-9: *Photodiode (in Photo-voltaic mode) and Transimpedance Amplifier.*

4.8.2.2 Photo-Conductive Mode

Figure 4-9 shows a transimpedance amplifier with a photodiode (D_1) biased in the Photo-conductive mode (D_1 is reverse biased), which is used for high-speed applications.

As light impinges on D_1, charge is generated, causing a current to flow in the reverse bias direction of D_1. Placing a negative bias on D_1 significantly reduces its junction capacitance, which allows the circuit to operate at a much higher speed. This reverse bias also increases the dark current and current noise, however. Resistor R_2 converts the current into voltage. Capacitor C_2 limits the bandwidth and helps stabilize the circuit when D_1's junction capacitance is large.

$$V_B < 0$$
$$V_{OUT} = I_{D1}R_2$$

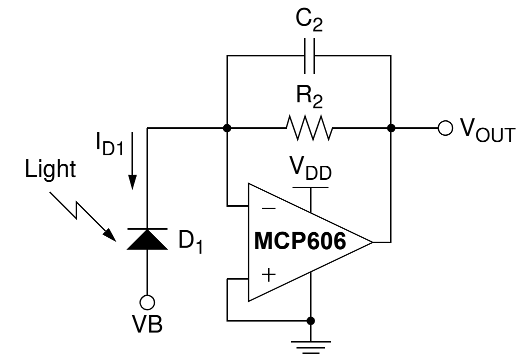


FIGURE 4-10: *Photodiode (in Photo-conductive mode) and Transimpedance Amplifier.*

4.8.3 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two op amp instrumentation amplifier shown in Figure 4-11 serves the function of taking the difference of two input voltages, level-shifting it and gaining it to the output. This configuration is best suited for higher gains (i.e., gain > 3 V/V). The reference voltage (V_{REF}) is typically at mid-supply ($V_{DD}/2$) in a single-supply environment.

$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

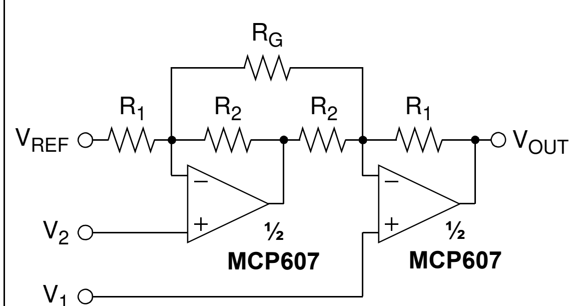


FIGURE 4-11: *Two Op Amp Instrumentation Amplifier.*

The key specifications that make the MCP606/7/8/9 family appropriate for this application circuit are low input bias current, low offset voltage and high common-mode rejection.

4.8.4 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three op amp instrumentation amplifier is illustrated in Figure 4-12. The two input op amps provide differential signal gain and a common mode gain of +1. The output op amp is a difference amplifier, which converts its input signal from differential to a single ended output; it rejects common mode signals at its input. The gain of this circuit is simply adjusted with one resistor (R_G). The reference voltage (V_{REF}) is typically referenced to mid-supply ($V_{DD}/2$) in single-supply applications.

$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{2R_2}{R_G}\right)\left(\frac{R_4}{R_3}\right) + V_{REF}$$

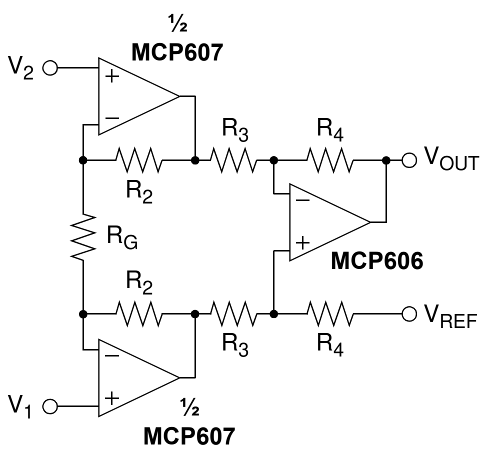


FIGURE 4-12: *Three Op Amp Instrumentation Amplifier.*

4.8.5 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 4-13, the MCP606 op amps, R_1 and R_2 provide a high gain to the input signal (V_{IN}). The MCP606's low offset voltage makes this an accurate circuit.

The MCP601 is configured as a unity-gain buffer. It isolates the MCP606's output from the load, increasing the high-gain stage's precision. Since the MCP601 has a higher output current, with the two amplifiers being housed in separate packages, there is minimal change in the MCP606's offset voltage due to loading effect.

$$V_{OUT} = V_{IN}(1 + R_2 / R_1)$$

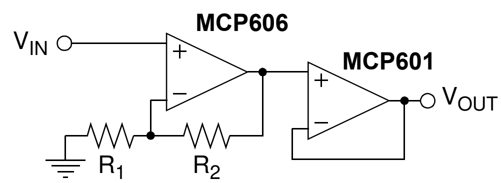


FIGURE 4-13: *Precision Gain with Good Load Isolation.*

NOTES:

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP606/7/8/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP606/7/8/9 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparasion reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990

These application notes and others are listed in the design guide:

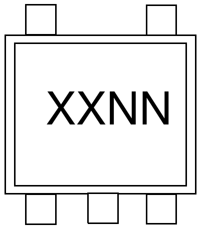
"Signal Chain Design Guide", DS21825

NOTES:

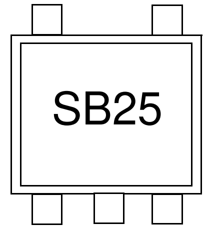
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

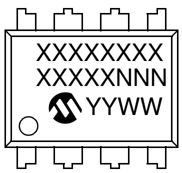
5-Lead SOT-23 (**MCP606**)



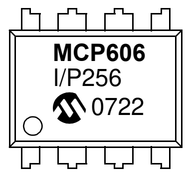
Example:



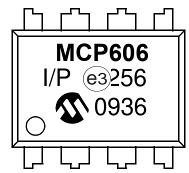
8-Lead PDIP (300 mil)



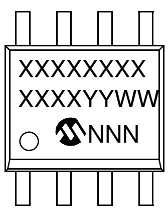
Example:



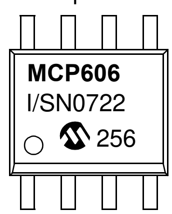
OR



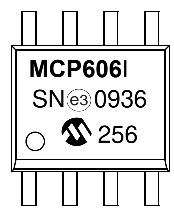
8-Lead SOIC (150 mil)



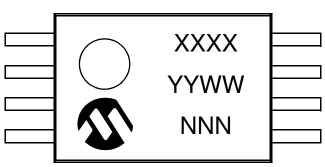
Example:



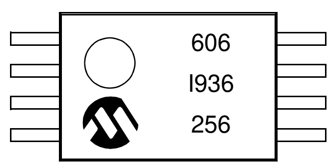
OR



8-Lead TSSOP



Example:

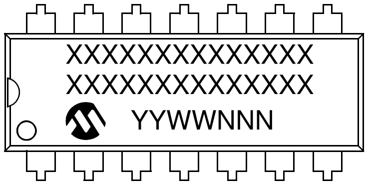


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

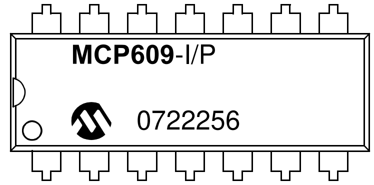
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

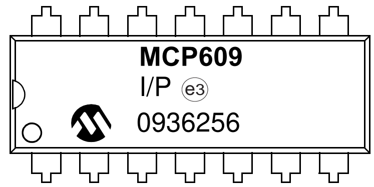
14-Lead PDIP (300 mil) (**MCP609**)



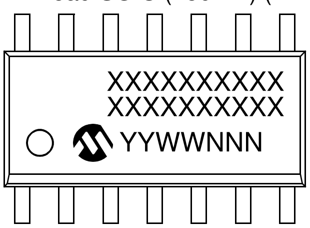
Example:



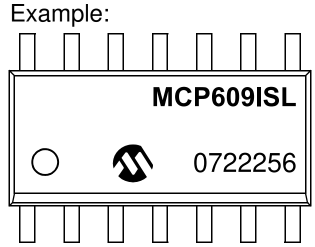
OR



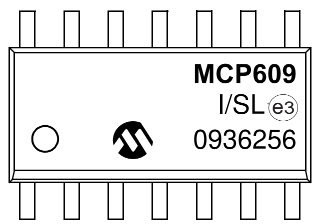
14-Lead SOIC (150 mil) (**MCP609**)



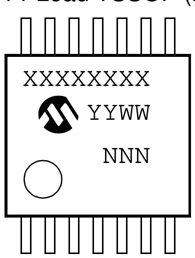
Example:



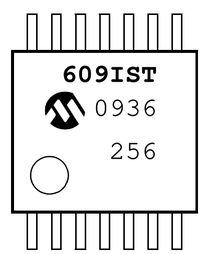
OR



14-Lead TSSOP (**MCP609)**

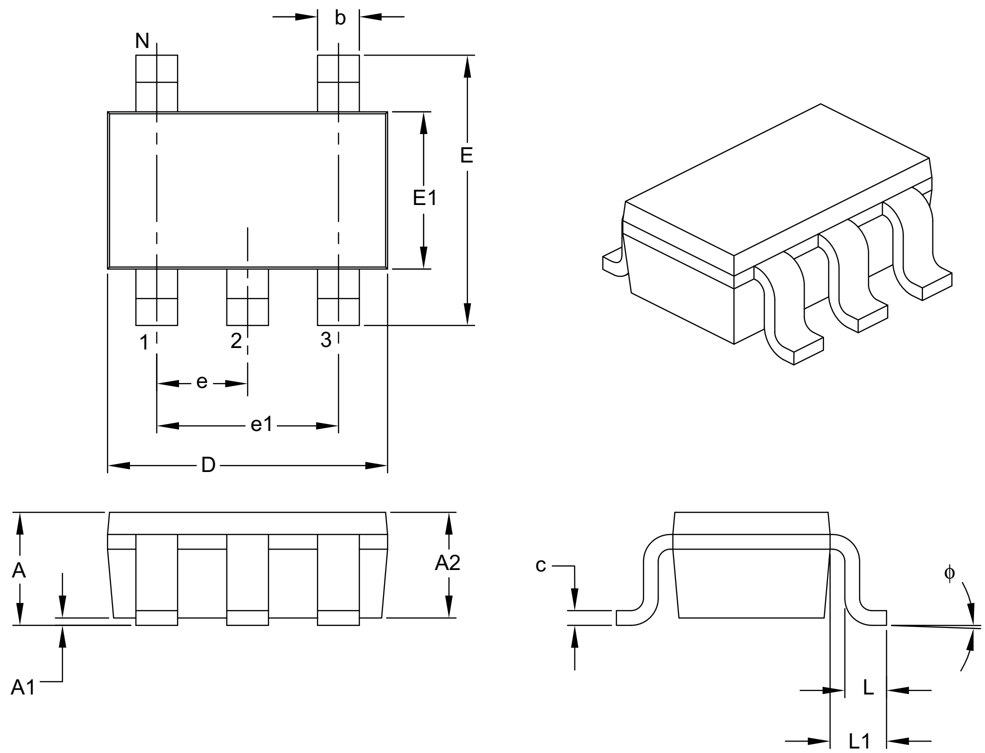


Example:



5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

