MCP6231/1R/1U/2/4

20 µA, 300 kHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 300 kHz (typical)
- Supply Current: I_Q = 20 µA (typical)
- Supply Voltage: 1.8V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to +125°C
- Available in 5-Pin SC70 and SOT-23 packages

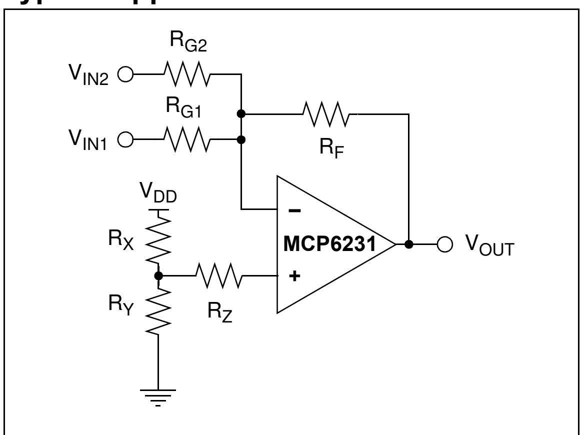
Applications

- Automotive
- Portable Equipment
- Transimpedance amplifiers
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application

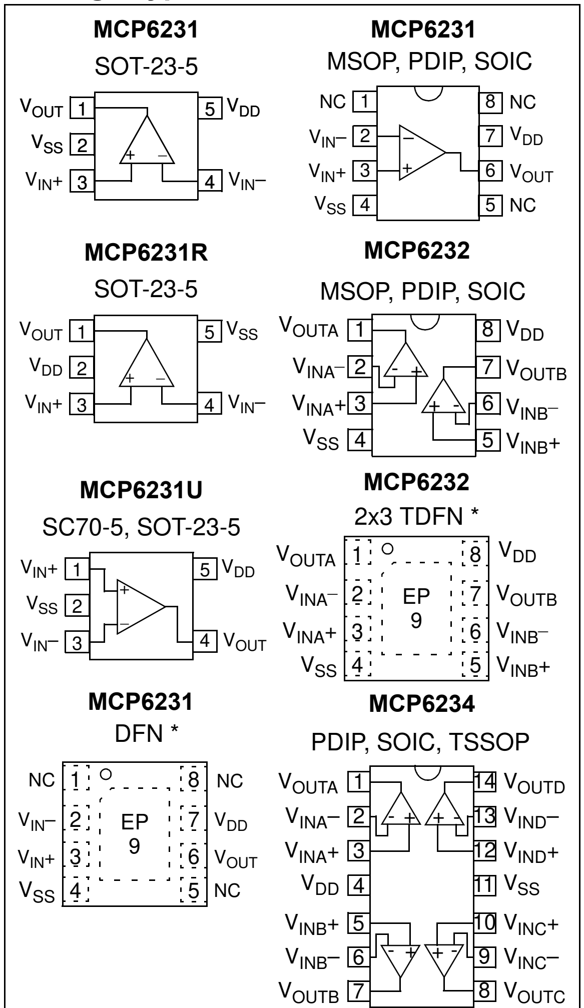


Summing Amplifier Circuit

Description

The Microchip Technology Inc. MCP6231/1R/1U/2/4 operational amplifiers (op amps) provide wide bandwidth for the quiescent current. The MCP6231/1R/1U/2/4 family has a 300 kHz gain bandwidth product and 65°C (typical) phase margin. This family operates from a single supply voltage as low as 1.8V, while drawing 20 µA (typical) quiescent current. In addition, the MCP6231/1R/1U/2/4 family supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. These op amps are designed in one of Microchip's advanced CMOS processes.

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 7.0V

Current at Analog Input Pins (V_{IN}+, V_{IN}–)....................±2 mA

Analog Inputs (V_{IN}+, V_{IN}–) †† .... V_{SS} – 1.0V to V_{DD} + 1.0V

All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V

Difference Input Voltage .... $|V_{DD} – V_{SS}|$

Output Short Circuit Current ....Continuous

Current at Output and Supply Pins ....±30 mA

Storage Temperature ....–65°C to +150°C

Maximum Junction Temperature (T_J)......................... .+150°C

ESD Protection On All Pins (HBM; MM) .... ≥ 4 kV; 300V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage and Current Limits”**.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and $V_{OUT} \approx V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-5.0	—	+5.0	mV	$V_{CM} = V_{SS}$
Extended Temperature	V_{OS}	-7.0	—	+7.0	mV	T_A = -40°C to +125°C, $V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3.0	—	µV/°C	T_A= -40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	83	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	±1.0	—	pA	
At Temperature	I_B	—	20	—	pA	T_A = +85°C
At Temperature	I_B	—	1100	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	61	75	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	90	110	—	dB	V_{OUT} = 0.3V to V_{DD} – 0.3V, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 35	—	V_{DD} – 35	mV	R_L =10 kΩ, 0.5V Input Overdrive
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
	I_{SC}	—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	6.0	V	
Quiescent Current per Amplifier	I_Q	10	20	30	µA	I_O = 0, $V_{CM} = V_{DD}$ – 0.5V

Note 1: The SC70 package is only tested at +25°C.

2: All parts with date codes February 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V

AC ELECTRICAL CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.						
AC Response						
Gain Bandwidth Product	GBWP	—	300	—	kHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	0.15	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	6.0	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	52	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Temperature Ranges						
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-DFN	θ_{JA}	—	84.5	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-TDFN	θ_{JA}	—	41	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-1 and Figure 1-1. The bypass capacitors are laid out according to the rules discussed in **Section 4.6 "PCB Surface Leakage"**.

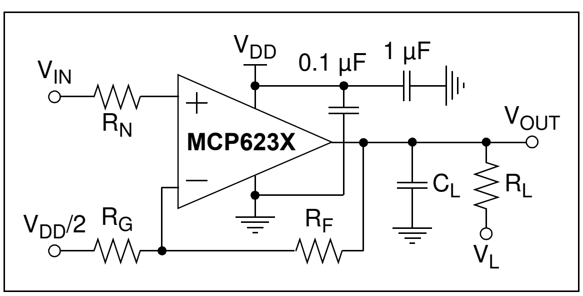


FIGURE 1-1: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

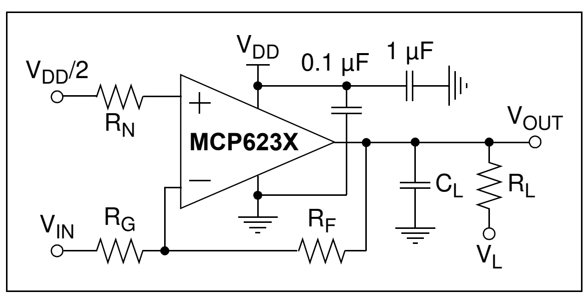


FIGURE 1-2: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 60 pF.

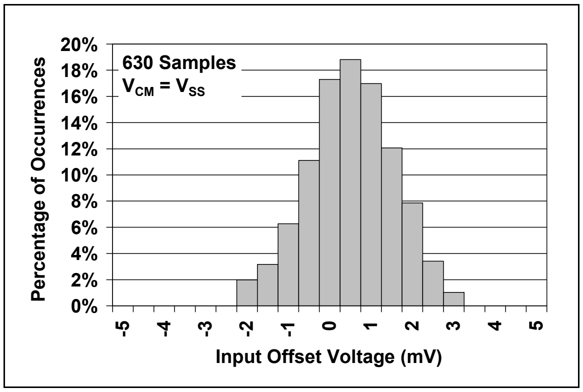


FIGURE 2-1: *Input Offset Voltage.*

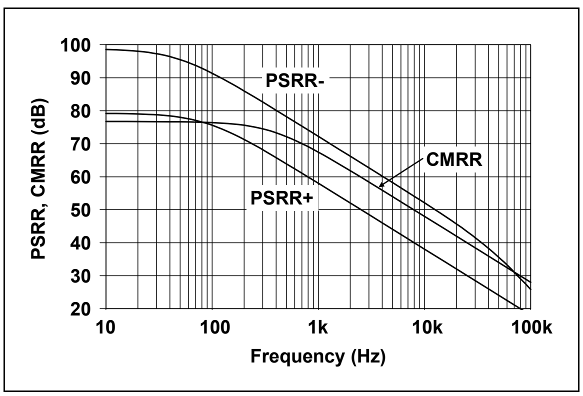


FIGURE 2-2: *PSRR, CMRR vs. Frequency.*

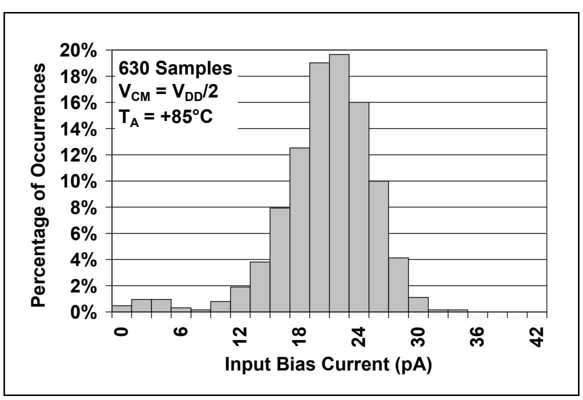


FIGURE 2-3: *Input Bias Current at +85°C.*

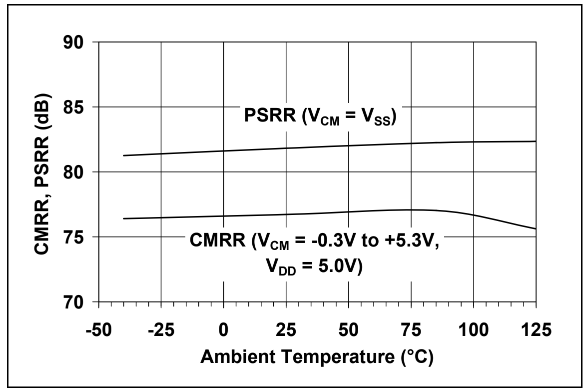


FIGURE 2-4: *CMRR, PSRR vs. Ambient Temperature.*

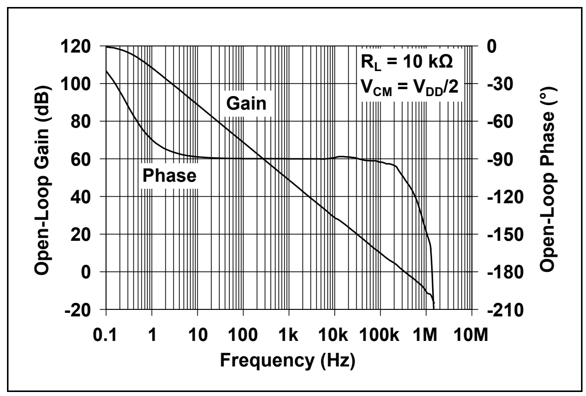


FIGURE 2-5: *Open-Loop Gain, Phase vs. Frequency.*

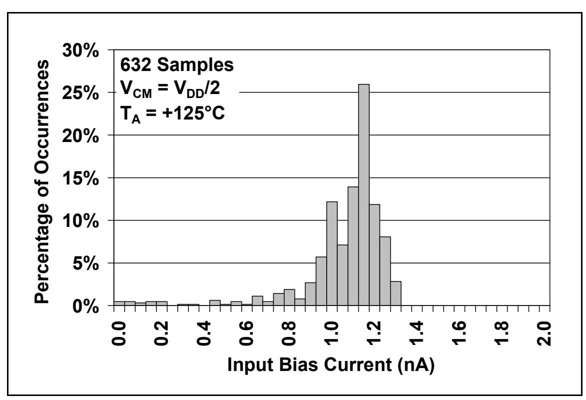


FIGURE 2-6: *Input Bias Current at +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 60 pF.

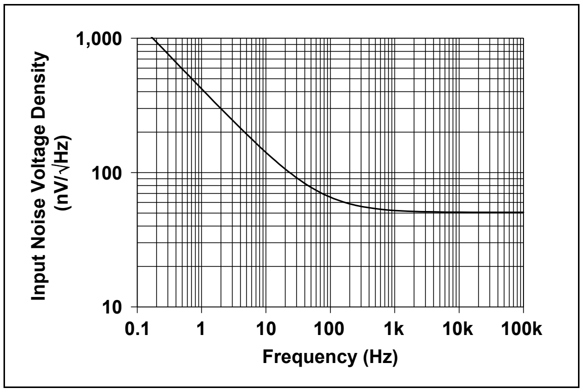


FIGURE 2-7: *Input Noise Voltage Density vs. Frequency.*

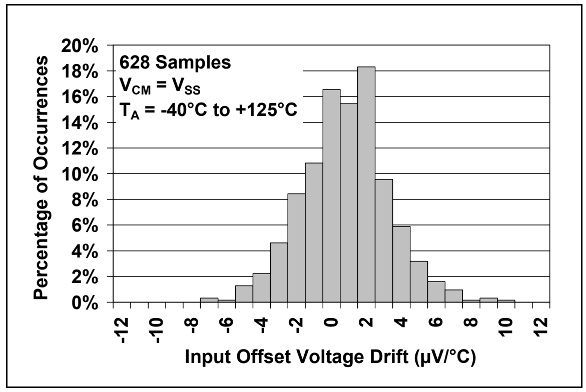


FIGURE 2-10: *Input Offset Voltage Drift.*

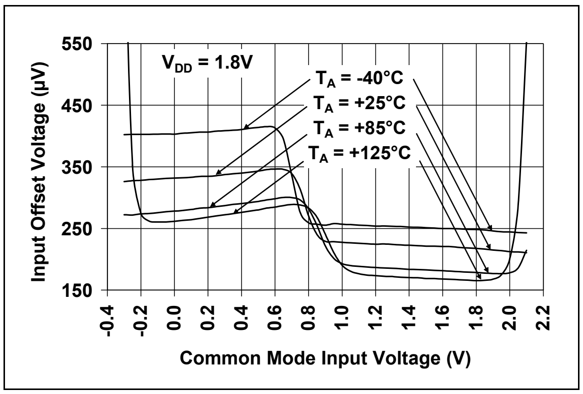


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.8V.*

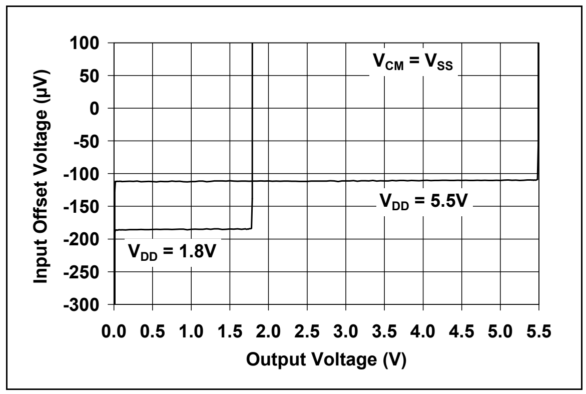


FIGURE 2-11: *Input Offset Voltage vs. Output Voltage.*

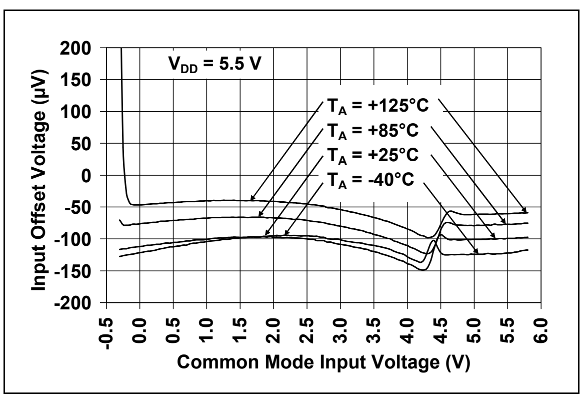


FIGURE 2-9: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

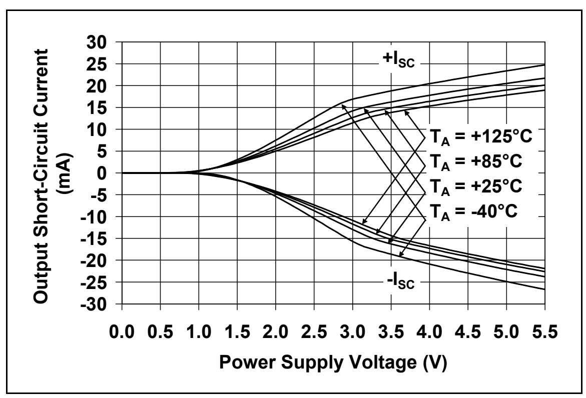


FIGURE 2-12: *Output Short-Circuit Current vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 60 pF.

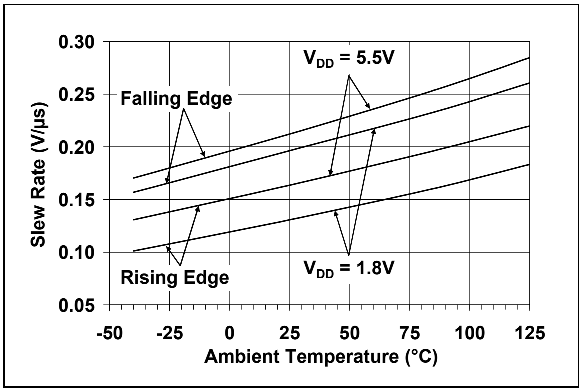


FIGURE 2-13: *Slew Rate vs. Ambient Temperature.*

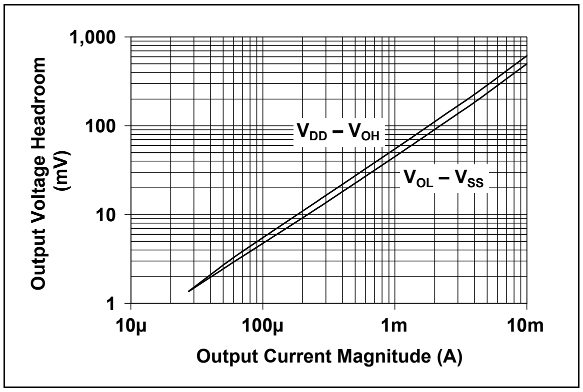


FIGURE 2-14: *Output Voltage Headroom vs. Output Current Magnitude.*

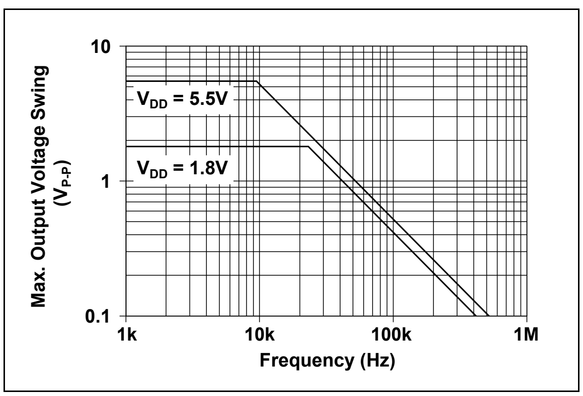


FIGURE 2-15: *Maximum Output Voltage Swing vs. Frequency.*

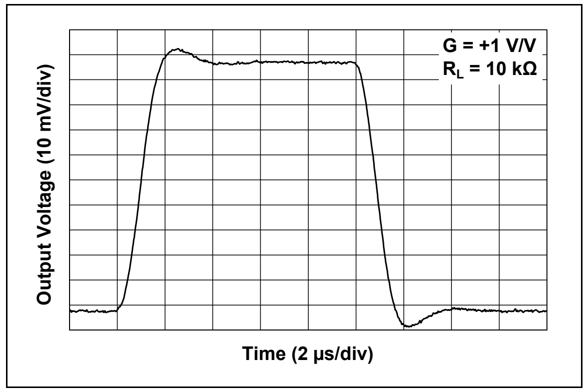


FIGURE 2-16: *Small-Signal, Non-Inverting Pulse Response.*

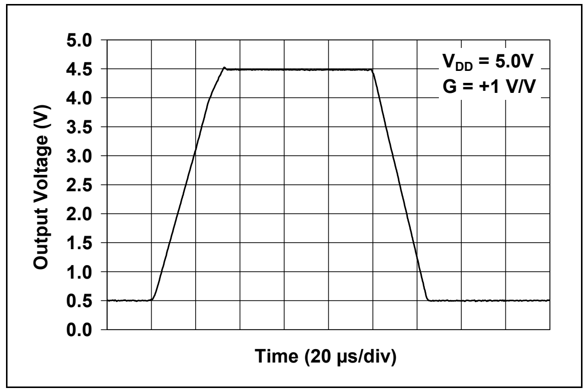


FIGURE 2-17: *Large-Signal, Non-Inverting Pulse Response.*

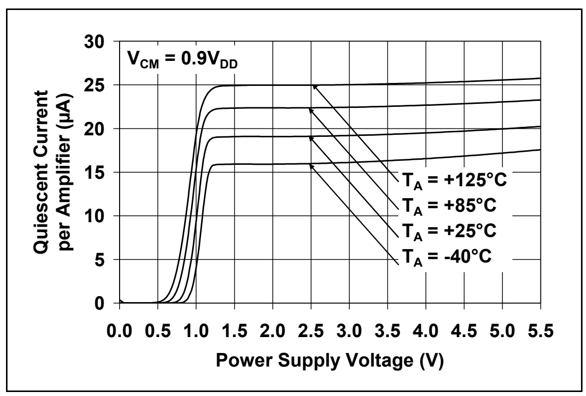


FIGURE 2-18: *Quiescent Current vs. Power Supply Voltage.*

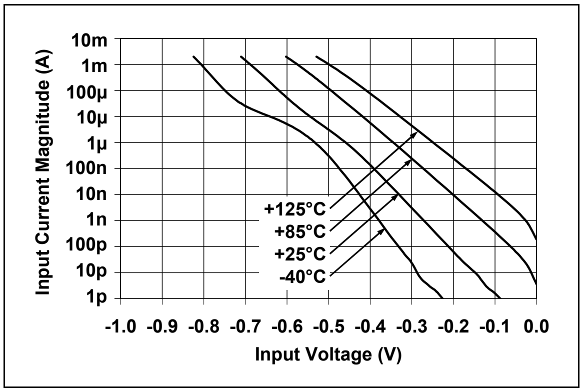


FIGURE 2-19: *Measured Input Current vs. Input Voltage (below V_{SS}).*

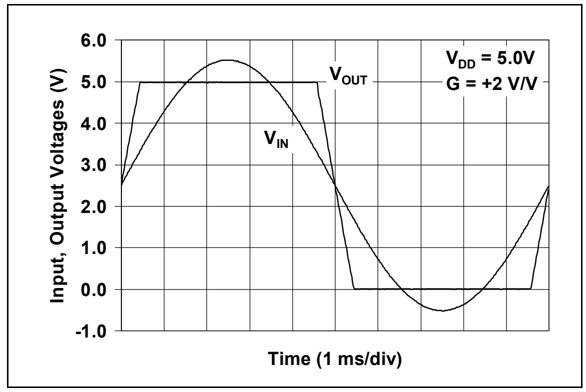


FIGURE 2-20: *The MCP6231/1R/1U/2/4 Show No Phase Reversal.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1 (single op amps) and Table 3-2 (dual and quad op amps).

TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

MCP6231		MCP6231R	MCP6231U	Symbol	Description
DFN, MSOP, PDIP, SOIC	SOT-23-5	SOT-23-5	SOT-23-5 SC70		
6	1	1	4	V_{OUT}	Analog Output
2	4	4	3	$V_{IN}-$	Inverting Input
3	3	3	1	$V_{IN}+$	Non-inverting Input
7	5	2	5	V_{DD}	Positive Power Supply
4	2	5	2	V_{SS}	Negative Power Supply
1, 5, 8	—	—	—	NC	No Internal Connection
9	—	—	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS

MCP6232	MCP6234	Symbol	Description
MSOP, PDIP, SOIC, TDFN	PDIP, SOIC, TSSOP		
1	1	V_{OUTA}	Analog Output (op amp A)
2	2	$V_{INA}-$	Inverting Input (op amp A)
3	3	$V_{INA}+$	Non-inverting Input (op amp A)
8	4	V_{DD}	Positive Power Supply
5	5	$V_{INB}+$	Non-inverting Input (op amp B)
6	6	$V_{INB}-$	Inverting Input (op amp B)
7	7	V_{OUTB}	Analog Output (op amp B)
—	8	V_{OUTC}	Analog Output (op amp C)
—	9	$V_{INC}-$	Inverting Input (op amp C)
—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	11	V_{SS}	Negative Power Supply
—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	13	$V_{IND}-$	Inverting Input (op amp D)
—	14	V_{OUTD}	Analog Output (op amp D)
9	—	—	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply (V_{SS} and V_{DD})

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

NOTES:

4.0 APPLICATION INFORMATION

The MCP6231/1R/1U/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6231/1R/1U/2/4 ideal for battery-powered applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6231/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 4-1 shows the input voltage exceeding the supply voltage without any phase reversal.

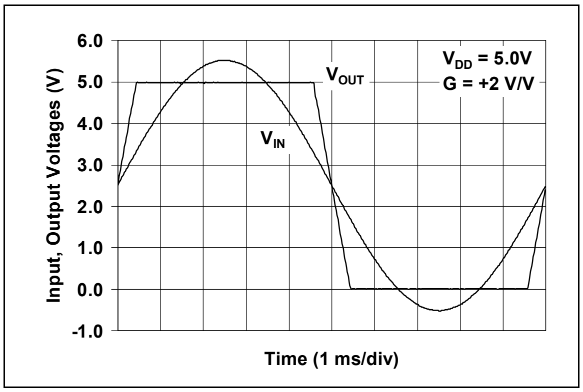


FIGURE 4-1: *The MCP6231/1R/1U/2/4 Show No Phase Reversal.*

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

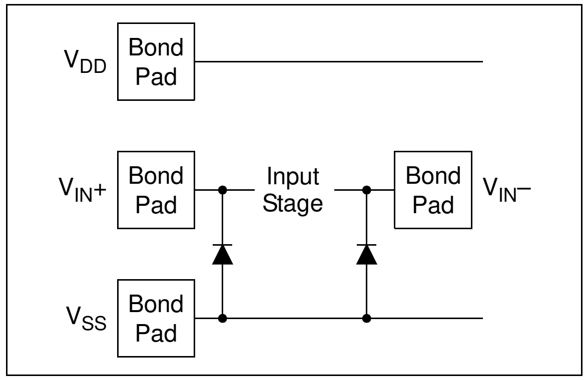
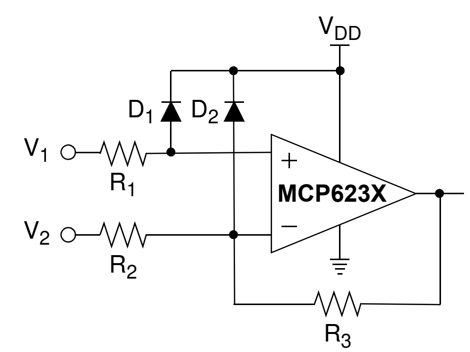


FIGURE 4-2: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the $V_{IN}+$ and $V_{IN}–$ pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\ mA}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\ mA}$$

FIGURE 4-3: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}–$) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-19. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6231/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}), while the other operates at high V_{CM}. WIth this topology, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS}.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6231/1R/1U/2/4 op amps is V_{DD} – 35 mV (maximum) and V_{SS} + 35 mV (minimum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-14 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, but all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

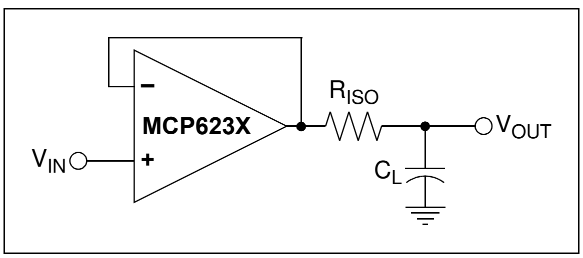


FIGURE 4-4: *Output resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-5 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the signal gain are equal. For inverting gains, G_N is 1 + |Signal Gain| (e.g., –1 V/V gives G_N = +2 V/V).

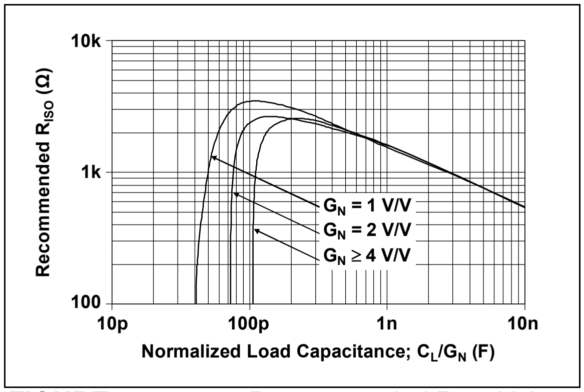


FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

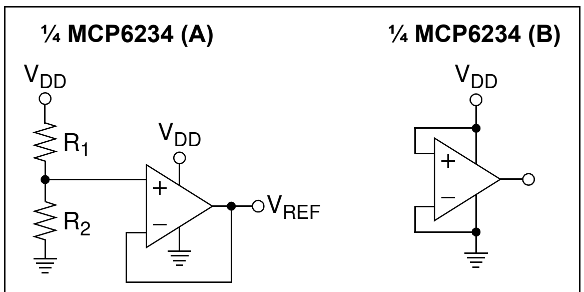
After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Evaluation on the bench and simulations with the MCP6231/1R/1U/2/4 SPICE macro model are very helpful. Modify R_{ISO}'s value until the response is reasonable.

4.4 Supply Bypass

With this op amp, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6234) should be configured as shown in Figure 4-6. Both circuits prevent the output from toggling and causing crosstalk. Circuit A can use any reference voltage between the supplies, provides a buffered DC voltage and minimizes the supply current draw of the unused op amp. Circuit B minimizes the number of components, but may draw a little more supply current for the unused op amp.



$$V_{REF} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}$$

FIGURE 4-6: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6231/1R/1U/2/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

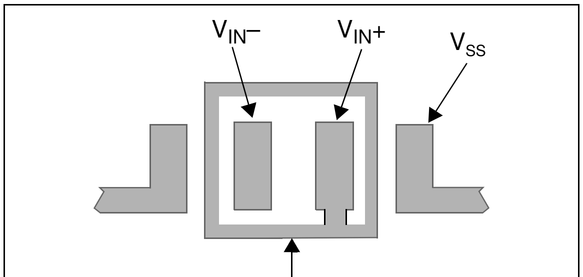


FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b. Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 MATCHING THE IMPEDANCE AT THE INPUTS

To minimize the effect of input bias current in an amplifier circuit (this is important for very high source-impedance applications, such as pH meters and transimpedance amplifiers), the impedances at the inverting and non-inverting inputs need to be matched. This is done by choosing the circuit resistor values so that the total resistance at each input is the same. Figure 4-8 shows a summing amplifier circuit.

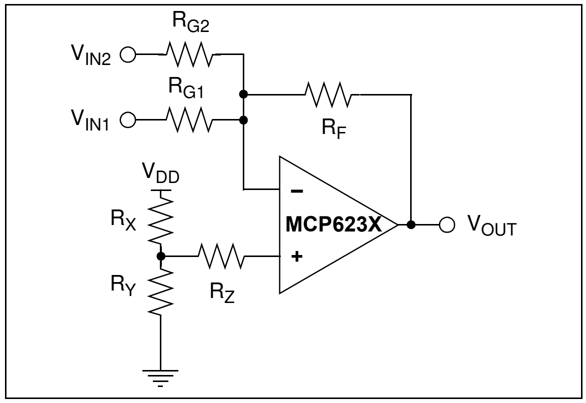


FIGURE 4-8: *Summing Amplifier Circuit.*

To match the inputs, set all voltage sources to ground and calculate the total resistance at the input nodes. In this summing amplifier circuit, the resistance at the inverting input is calculated by setting V_{IN1}, V_{IN2} and V_{OUT} to ground. In this case, R_{G1}, R_{G2} and R_F are in parallel. The total resistance at the inverting input is:

EQUATION 4-1:

$$R_{VIN-} = \frac{1}{\left(\frac{1}{R_{G1}} + \frac{1}{R_{G2}} + \frac{1}{R_F}\right)}$$

Where:

R_{VIN-} = total resistance at the inverting input

At the non-inverting input, V_{DD} is the only voltage source. When V_{DD} is set to ground, both R_x and R_y are in parallel. The total resistance at the non-inverting input is:

EQUATION 4-2:

$$R_{VIN+} = \frac{1}{\left(\frac{1}{R_X} + \frac{1}{R_Y}\right)} + R_Z$$

Where:

R_{VIN+} = total resistance at the inverting input

To minimize output offset voltage and increase circuit accuracy, the resistor values need to meet the conditions:

EQUATION 4-3:

$$R_{VIN^+} = R_{VIN^-}$$

4.7.2 COMPENSATING FOR THE PARASITIC CAPACITANCE

In analog circuit design, the PCB parasitic capacitance can compromise the circuit behavior; Figure 4-9 shows a typical scenario. If the input of an amplifier sees parasitic capacitance of several picofarad (C_{PARA}, which includes the common mode capacitance of 6 pF, typical), and large R_F and R_G, the frequency response of the circuit will include a zero. This parasitic zero introduces gain-peaking and can cause circuit instability.

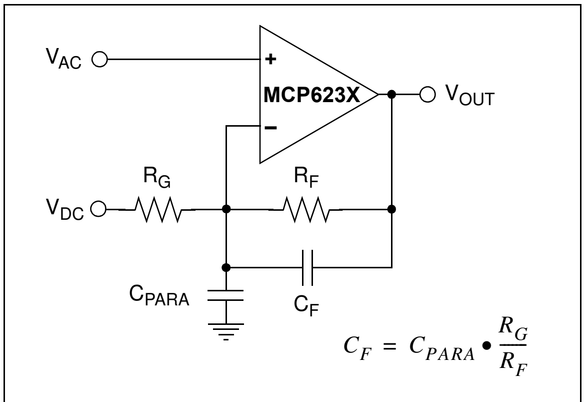


FIGURE 4-9: *Effect of Parasitic Capacitance at the Input.*

One solution is to use smaller resistor values to push the zero to a higher frequency. Another solution is to compensate by introducing a pole at the point at which the zero occurs. This can be done by adding C_F in parallel with the feedback resistor (R_F). C_F needs to be selected so that the ratio $C_{PARA}:C_F$ is equal to the ratio of $R_F:R_G$.

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6231/1R/1U/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6231/1R/1U/2/4 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at:

www.microchip.com/analogtools

Two of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990

These application notes and others are listed in the design guide:

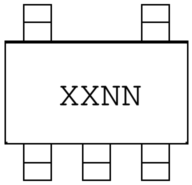
- *"Signal Chain Design Guide",* DS21825

NOTES:

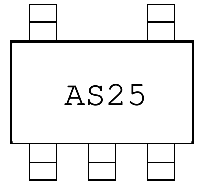
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

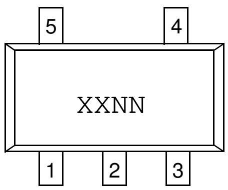
5-Lead SC70 **(MCP6231U Only)**



Example:



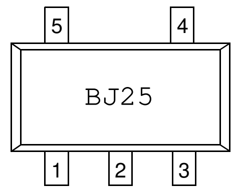
5-Lead SOT-23



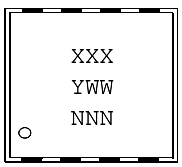
Device	Code
MCP6231	BJNN
MCP6231R	BKNN
MCP6231U	BLNN

Note: Applies to 5-Lead SOT-23.

Example:

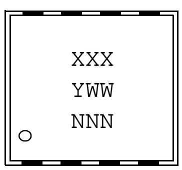


8-Lead DFN (2 x 3) (**MCP6231**)



Example:

8-Lead TDFN (2 x 3) (**MCP6232**)



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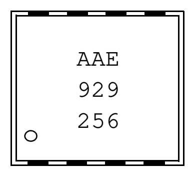
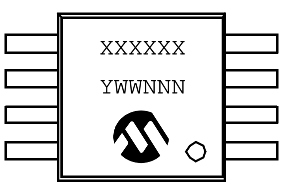


8-Lead MSOP



Example:

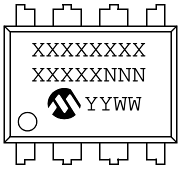
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

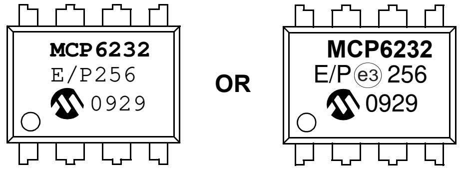
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

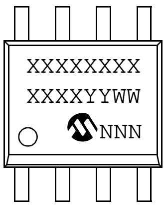
8-Lead PDIP (300 mil)



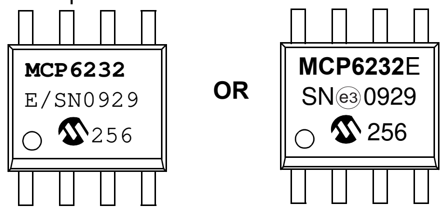
Example:



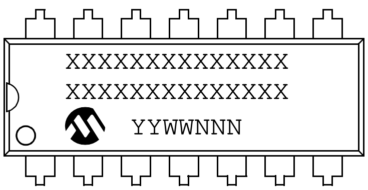
8-Lead SOIC (150 mil)



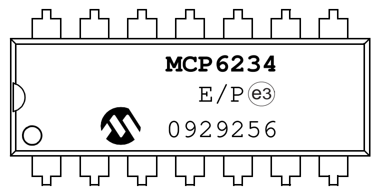
Example:



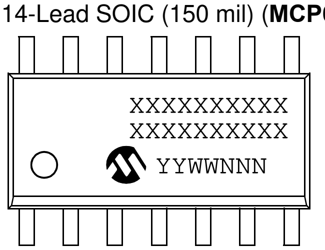
14-Lead PDIP (300 mil) (**MCP6234**)



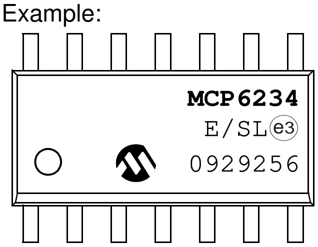
Example:



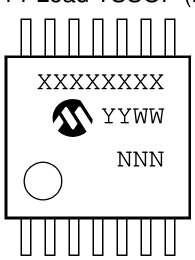
14-Lead SOIC (150 mil) (**MCP6234**)



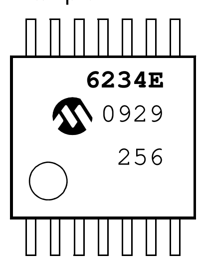
Example:



14-Lead TSSOP (**MCP6234**)

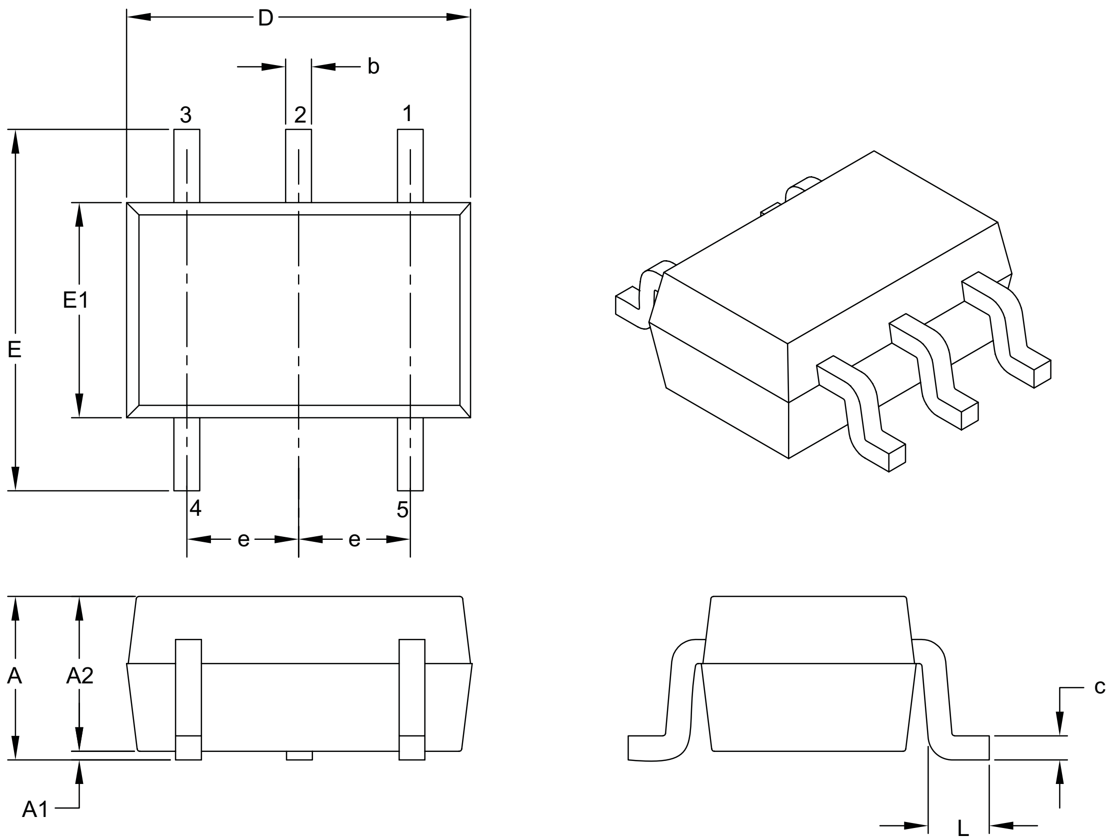


Example:



5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

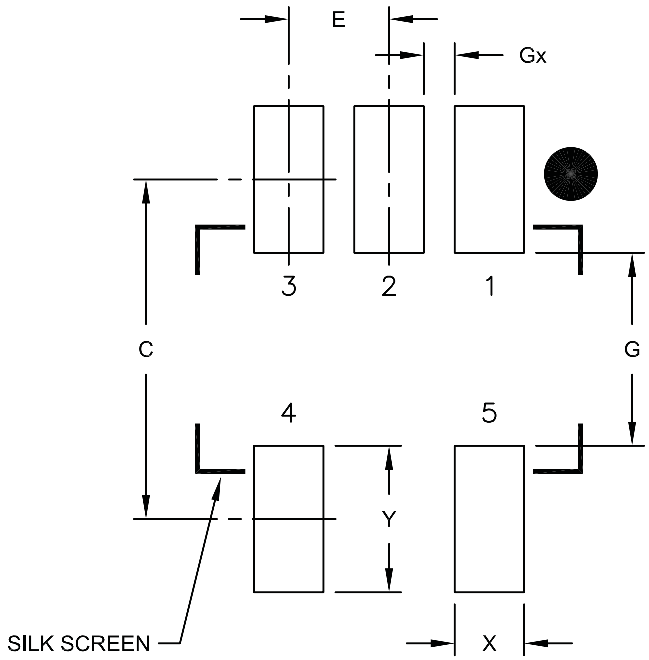
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

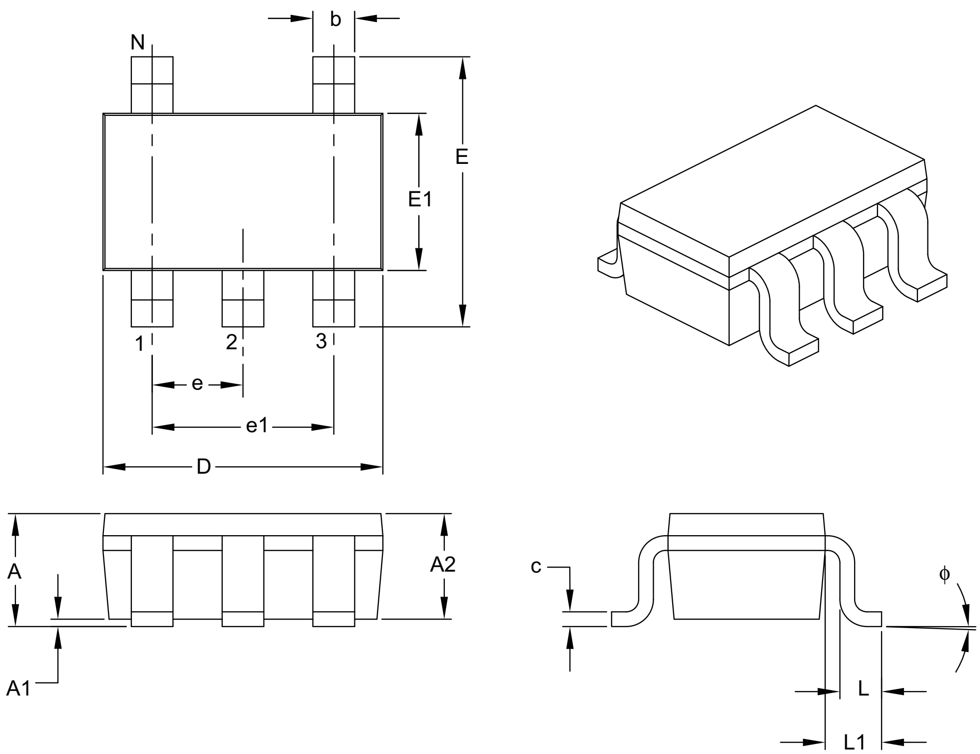
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

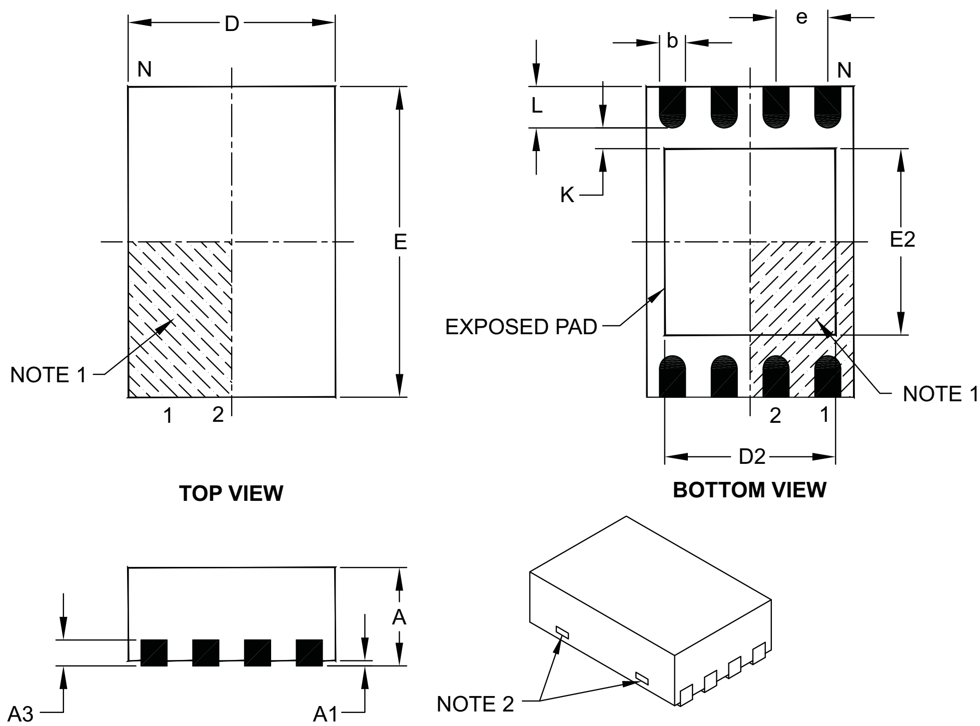
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



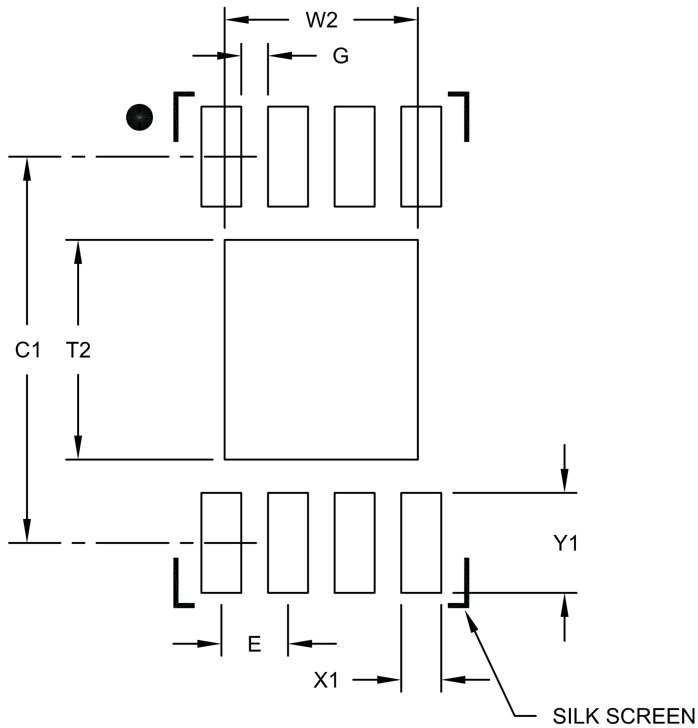
		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

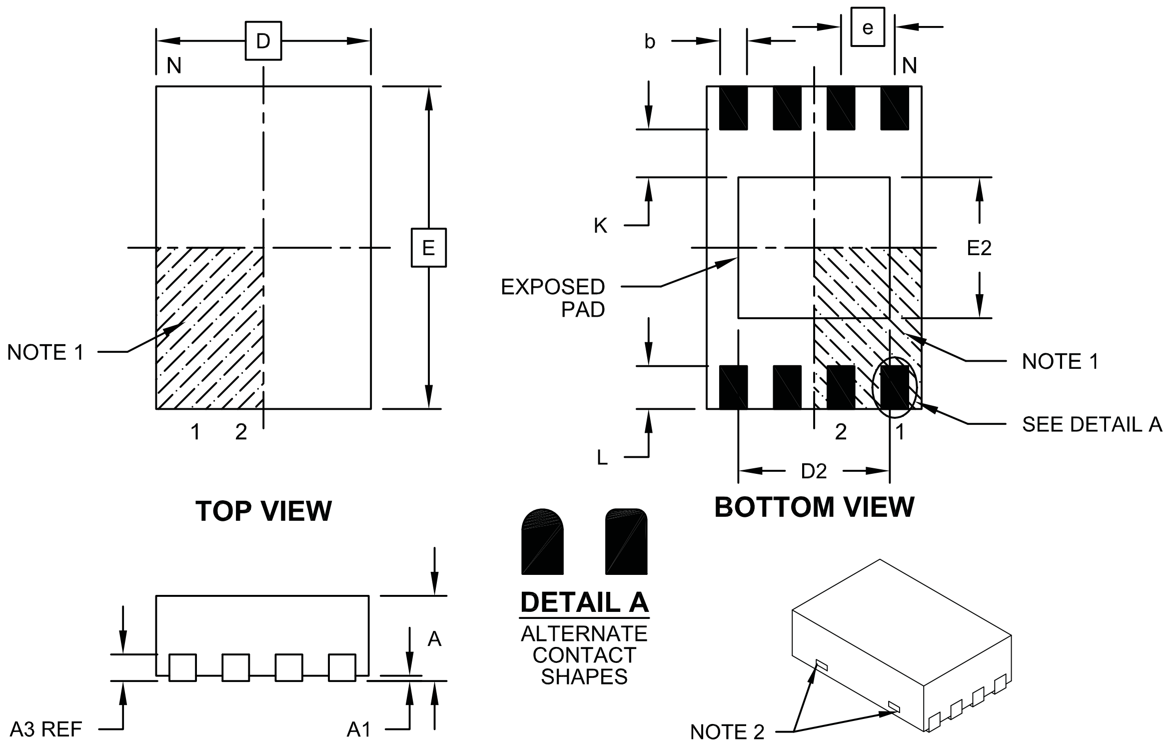
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

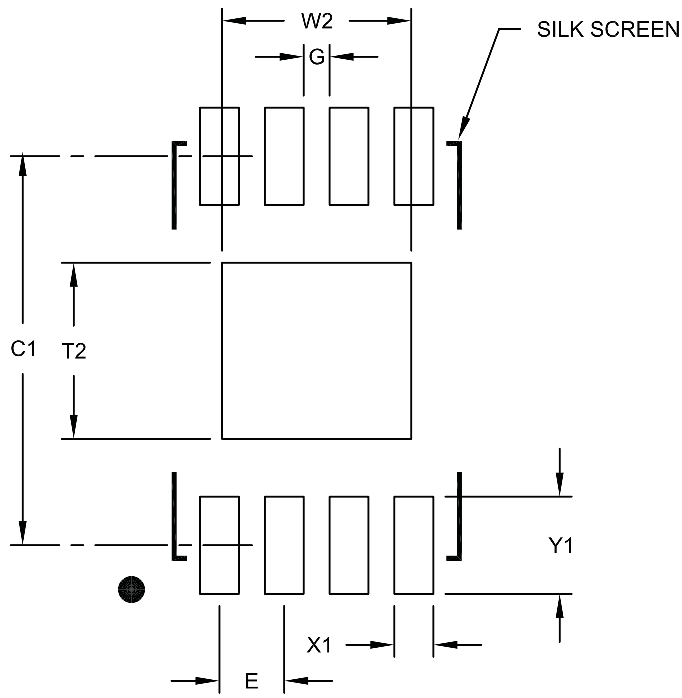
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129B

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A