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MCP6401/1R/1U/2/4/6/7/9

1 MHz, 45 µA Op Amps

Features

- Low Quiescent Current: 45 µA (typical)
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input and Output
- Supply Voltage Range: 1.8V to 6.0V
- Unity Gain Stable
- Extended Temperature Ranges:
  - -40°C to +125°C (E temp)
  - -40°C to +150°C (H temp)
- No Phase Reversal

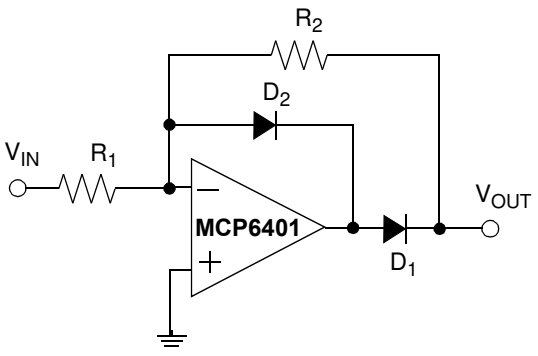
Applications

- Portable Equipment
- Battery Powered System
- Medical Instrumentation
- Automotive Electronics
- Data Acquisition Equipment
- Sensor Conditioning
- Analog Active Filters

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



Precision Half-Wave Rectifier

Description

The Microchip Technology Inc. MCP6401/1R/1U/2/4/6/7/9 family of operational amplifiers (op amps) has low quiescent current (45 µA, typical) and rail-to-rail input and output operation. This family is unity gain stable and has a gain bandwidth product of 1 MHz (typical). These devices operate with a power supply voltage of 1.8V to 6.0V. These features make the family of op amps well suited for single-supply, battery-powered applications.

The MCP6401/1R/1U/2/4/6/7/9 family is designed with Microchip's advanced CMOS process and offered in single, dual and quad packages. The devices are available in two extended temperature ranges (E temp and H temp) with different package types, which makes them well-suited for automotive and industrial applications.

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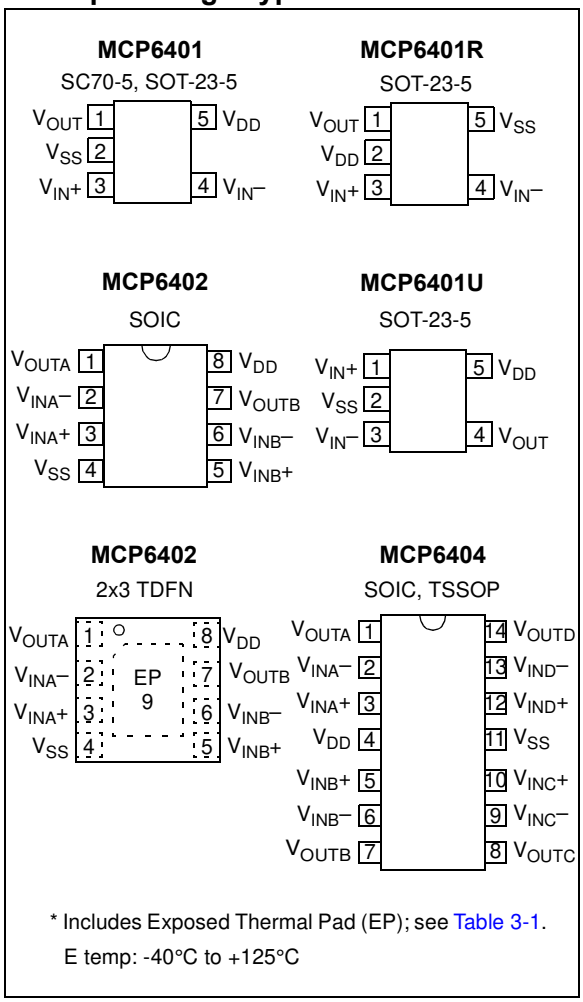
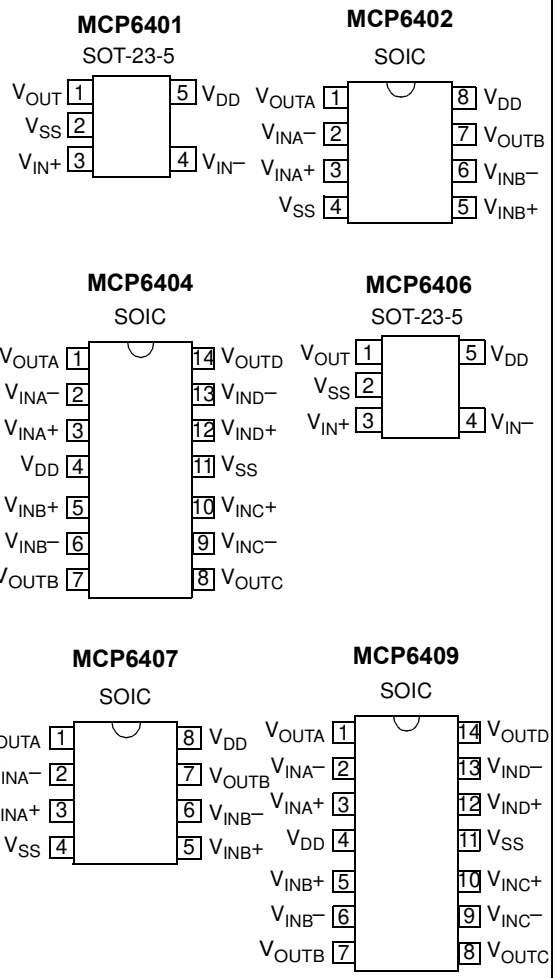
E Temp Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

E temp: -40°C to +125°C

H Temp Package Types



H temp: -40°C to +150°C

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN+}, V_{IN-})†† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Maximum Junction Temperature (T_J) ..... +155°C
ESD Protection on All Pins (HBM; MM; CDM) ....≥ 4 kV; 300V, 1500V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage Limits".**

1.2 MCP6401/1R/1U/2/4 Electrical Specifications

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8v to +6.0v, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}D/2$ and R_L = 100 kΩ to V_L (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Temp	Parts (Note 1)	Conditions
Input Offset								
Input Offset Voltage	V_{OS}	-4.5	±0.8	+4.5	mV		E, H	$V_{CM} = V_{SS}$
		—	±1.0	—	mV	+125°C	E	
		—	±1.5	—	mV	+150°C	H	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	-40°C to +125°C	E	$V_{CM} = V_{SS}$
		—	±2.5	—	µV/°C	-40°C to +150°C	H	
Power Supply Rejection Ratio	PSRR	63	78	—	dB		E, H	$V_{CM} = V_{SS}$
		—	75	—	dB	+125°C	E	
		—	73	—	dB	+150°C	H	
Input Bias Current and Impedance								
Input Bias Current	I_B	—	1	100	pA		E, H	
		—	30	—	pA	+85°C	E, H	
		—	800	—	pA	+125°C	E	
		—	7	—	nA	+150°C	H	
Input Offset Current	I_{OS}	—	1	—	pA		E, H	
		—	5	—	pA	+85°C	E, H	
		—	20	—	pA	+125°C	E	
		—	45	—	pA	+150°C	H	

Note 1: E part stands for the one whose operating temperature range is from -40°C to +125°C and H part stands for the one whose operating temperature range is from -40°C to +150°C.

2: Figure 2-14 shows how V_{CMR} changes across temperature.

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DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8v to +6.0v, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}D/2 and R_L = 100 kΩ to V_L (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Temp	Parts (Note 1)	Conditions
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF		E, H	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF		E, H	
Common Mode								
Common Mode Input Voltage Range (Note 2)	V_{CMR}	V_{SS}-0.20	—	V_{DD}+0.20	V		E, H	V_{DD} = 1.8V
		V_{SS}-0.05	—	V_{DD}+0.05	V	+125°C	E	
		V_{SS}	—	V_{DD}	V	+150°C	H	
		V_{SS}-0.30	—	V_{DD}+0.30	V		E, H	V_{DD} = 6.0V
		V_{SS}-0.15	—	V_{DD}+0.15	V	+125°C	E	
		V_{SS}-0.10	—	V_{DD}+0.10	V	+150°C	H	
Common Mode Rejection Ratio	CMRR	56	71	—	dB		E, H	V_{CM} = -0.2V to 2.0V, V_{DD} = 1.8V
		—	68	—	dB	+125°C	E	V_{CM} = -0.05V to 1.85V, V_{DD} = 1.8V
		—	65	—	dB	+150°C	H	V_{CM} = 0V to 1.8V, V_{DD} = 1.8V
		63	78	—	dB		E, H	V_{CM} = -0.3V to 6.3V, V_{DD} = 6.0V
		—	76	—	dB	+125°C	E	V_{CM} = -0.15V to 6.15V, V_{DD} = 6.0V
		—	75	—	dB	+150°C	H	V_{CM} = -0.1V to 6.1V, V_{DD} = 6.0V
Open-Loop Gain								
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB		E, H	V_{OUT} = 0.3V to V_{DD}-0.3V, V_{CM} = V_{SS}
		—	105	—	dB	+125°C	E	
		—	100	—	dB	+150°C	H	
Output								
High-Level Output Voltage	V_{OH}	1.790	1.792	—	V		E, H	V_{DD} = 1.8V, R_L = 10 kΩ, 0.5V input overdrive
		—	1.788	—	V	+125°C	E	
		—	1.785	—	V	+150°C	H	
		5.980	5.985	—	V		E, H	V_{DD} = 6.0V, R_L = 10 kΩ, 0.5V input overdrive
		—	5.980	—	V	+125°C	E	
		—	5.975	—	V	+150°C	H	
Low-Level Output Voltage	V_{OL}	—	0.008	0.010	V		E, H	V_{DD} = 1.8V, R_L = 10 kΩ, 0.5V input overdrive
		—	0.012	—	V	+125°C	E	
		—	0.015	—	V	+150°C	H	
		—	0.015	0.020	V		E, H	V_{DD} = 6.0V, R_L = 10 kΩ, 0.5V input overdrive
		—	0.020	—	V	+125°C	E	
		—	0.025	—	V	+150°C	H	

Note 1: E part stands for the one whose operating temperature range is from -40°C to +125°C and H part stands for the one whose operating temperature range is from -40°C to +150°C.

2: Figure 2-14 shows how V_{CMR} changes across temperature.

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DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8v to +6.0v, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}D/2$ and R_L = 100 kΩ to V_L (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Temp	Parts (Note 1)	Conditions
Output Short-Circuit Current	I_{SC}	—	±5	—	mA		E, H	V_{DD} = 1.8V
		—	±15	—	mA		E, H	V_{DD} = 6.0V
Power Supply								
Supply Voltage	V_{DD}	1.8	—	6.0	V		E, H	
Quiescent Current per Amplifier	I_Q	20	45	70	µA		E, H	I_O = 0, V_{DD} = 5.0V $V_{CM} = 0.2V_{DD}$
		—	55	—	µA	+125°C	E	
		—	60	—	µA	+150°C	H	

Note 1: E part stands for the one whose operating temperature range is from -40°C to +125°C and H part stands for the one whose operating temperature range is from -40°C to +150°C.

2: Figure 2-14 shows how V_{CMR} changes across temperature.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to +6.0V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 100 kΩ to V_L and C_L = 60 pF (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Parts	Conditions
AC Response							
Gain Bandwidth Product	GBWP	—	1	—	MHz	E, H	
Phase Margin	PM	—	65	—	°	E, H	G = +1 V/V
Slew Rate	SR	—	0.5	—	V/µs	E, H	
Noise							
Input Noise Voltage	E_{ni}	—	3.6	—	µVp-p	E, H	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	E, H	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	E, H	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +6.0V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	E temp parts (Note 1)
	T_A	-40	—	+150	°C	H temp parts (Note 1)
Storage Temperature Range	T_A	-65	—	+155	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	52.5	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +155°C.

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1.3 MCP6406/7/9 Electrical Specifications

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 100 kΩ to V_L (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Temp	Parts (Note 1)	Conditions
Input Offset								
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV		E, H	$V_{CM} = V_{SS}$
		-5.0	±1.0	+5.0	mV	+125°C	E	
		-5.5	±1.5	+5.5	mV	+150°C	H	
Input Offset Drift with Temperature	$\Delta V_{OS}/DT_A$	—	±2.0	—	µV/°C	-40°C to +125°C	E	$V_{CM} = V_{SS}$
		—	±2.5	—	µV/°C	-40°C to +150°C	H	
Power Supply Rejection Ratio	PSRR	63	78	—	dB		E, H	$V_{CM} = V_{SS}$
		60	75	—	dB	+125°C	E	
		58	73	—	dB	+150°C	H	
Input Bias Current and Impedance								
Input Bias Current	I_B	—	±1	100	pA		E, H	
		—	30	—	pA	+85°C	E, H	
		—	800	2000	pA	+125°C	E	
		—	7	12	nA	+150°C	H	
Input Offset Current	I_{OS}	—	1	—	pA		E, H	
		—	5	—	pA	+85°C	E, H	
		—	20	—	pA	+125°C	E	
		—	45	—	pA	+150°C	H	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF		E, H	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF		E, H	
Common Mode								
Common Mode Input Voltage Range (Note 2)	V_{CMR}	V_{SS}-0.20	—	V_{DD}+0.20	V		E, H	V_{DD} = 1.8V
		V_{SS}-0.05	—	V_{DD}+0.05	V	+125°C	E	
		V_{SS}	—	V_{DD}	V	+150°C	H	
		V_{SS}-0.30	—	V_{DD}+0.30	V		E, H	V_{DD} = 6.0V
		V_{SS}-0.15	—	V_{DD}+0.15	V	+125°C	E	
		V_{SS}-0.10	—	V_{DD}+0.10	V	+150°C	H	

Note 1: E part stands for the one whose operating temperature range is from -40°C to +125°C and H part stands for the one whose operating temperature range is from -40°C to +150°C.

2: Figure 2-14 shows how V_{CMR} changes across temperature.

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DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} » V_{DD}/2, V_L = V_{DD}/2 and R_L = 100 kΩ to V_L (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Temp	Parts (Note 1)	Conditions
Common Mode Rejection Ratio	CMRR	56	71	—	dB		E, H	V_{CM} = -0.2V to 2.0V, V_{DD} = 1.8V
		53	68	—	dB	+125°C	E	V_{CM} = -0.05V to 1.85V, V_{DD} = 1.8V
		50	65	—	dB	+150°C	H	V_{CM} = 0V to 1.8V, V_{DD} = 1.8V
		63	78	—	dB		E, H	V_{CM} = -0.3V to 6.3V, V_{DD} = 6.0V
		61	76	—	dB	+125°C	E	V_{CM} = -0.15V to 6.15V, V_{DD} = 6.0V
		60	75	—	dB	+150°C	H	V_{CM} = -0.1V to 6.1V, V_{DD} = 6.0V
Open-Loop Gain								
DC Open-Loop Gain (Large Signal)	A_{OL}	90	110	—	dB		E, H	V_{OUT} = 0.3V to V_{DD}-0.3V, V_{CM} = V_{SS}
		88	105	—	dB	+125°C	E	
		85	100	—	dB	+150°C	H	
Output								
High-Level Output Voltage	V_{OH}	1.790	1.792	—	V		E, H	V_{DD} = 1.8V R_L = 10 kΩ 0.5V input overdrive
		1.785	1.788	—	V	+125°C	E	
		1.782	1.785	—	V	+150°C	H	
		5.980	5.985	—	V		E, H	V_{DD} = 6.0V R_L = 10 kΩ 0.5V input overdrive
		5.970	5.980	—	V	+125°C	E	
		5.965	5.975	—	V	+150°C	H	
Low-Level Output Voltage	V_{OL}	—	0.008	0.010	V		E, H	V_{DD} = 1.8V R_L = 10 kΩ 0.5V input overdrive
		—	0.012	0.015	V	+125°C	E	
		—	0.015	0.018	V	+150°C	H	
		—	0.015	0.020	V		E, H	V_{DD} = 6.0V R_L = 10 kΩ 0.5V input overdrive
		—	0.020	0.030	V	+125°C	E	
		—	0.025	0.035	V	+150°C	H	
Output Short-Circuit Current	I_{SC}	—	±5	—	mA		E, H	V_{DD} = 1.8V
		—	±15	—	mA		E, H	V_{DD} = 6.0V
Power Supply								
Supply Voltage	V_{DD}	1.8	—	6.0	V		E, H	
Quiescent Current per Amplifier	I_Q	20	45	70	µA		E, H	I_O = 0, V_{DD} = 5.0V V_{CM} = 0.2V_{DD}
		30	55	80	µA	+125°C	E	
		35	60	90	µA	+150°C	H	

Note 1: E part stands for the one whose operating temperature range is from -40°C to +125°C and H part stands for the one whose operating temperature range is from -40°C to +150°C.

2: Figure 2-14 shows how V_{CMR} changes across temperature.

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AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Part	Conditions
AC Response							
Gain Bandwidth Product	GBWP	—	1	—	MHz	E, H	
Phase Margin	PM	—	65	—	°	E, H	G = +1 V/V
Slew Rate	SR	—	0.5	—	V/µs	E, H	
Noise							
Input Noise Voltage	E_{ni}	—	3.6	—	µVp-p	E, H	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	E, H	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	E, H	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +6.0V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	E temp parts **(Note 1)**
	T_A	-40	—	+150	°C	H temp parts **(Note 1)**
Storage Temperature Range	T_A	-65	—	+155	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +155°C.

1.4 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's Common Mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM} =	Differential Mode Gain	(V/V)
V_{CM} =	Op Amp's Common Mode Input Voltage	(V)
V_{OST} =	Op Amp's Total Input Offset Voltage	(mV)

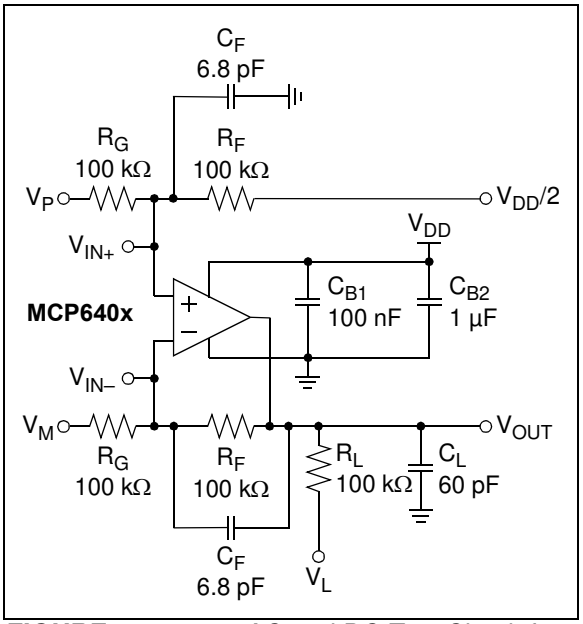

FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

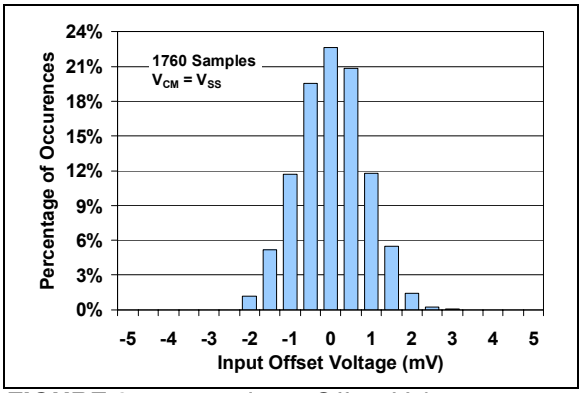

FIGURE 2-1: *Input Offset Voltage.*

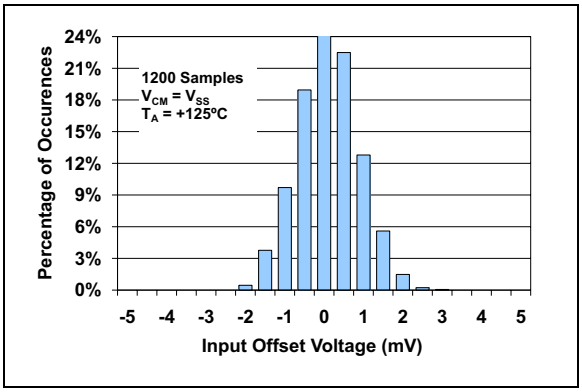

FIGURE 2-2: *Input Offset Voltage.*

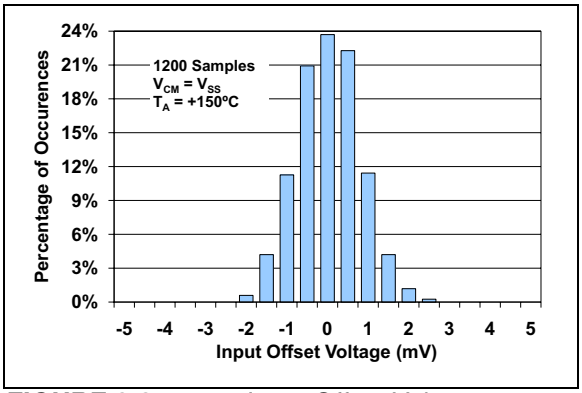

FIGURE 2-3: *Input Offset Voltage.*

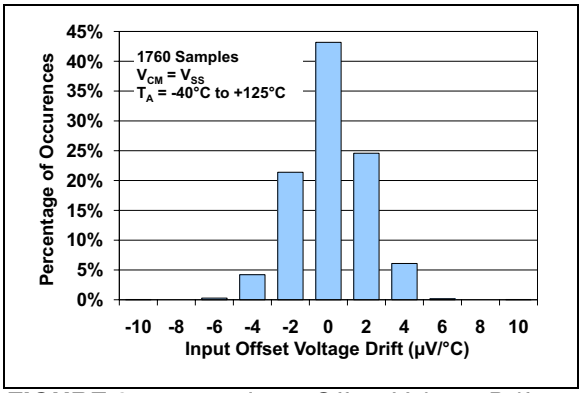

FIGURE 2-4: *Input Offset Voltage Drift.*

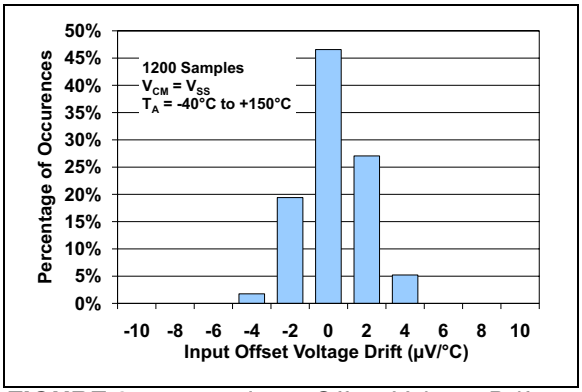

FIGURE 2-5: *Input Offset Voltage Drift.*

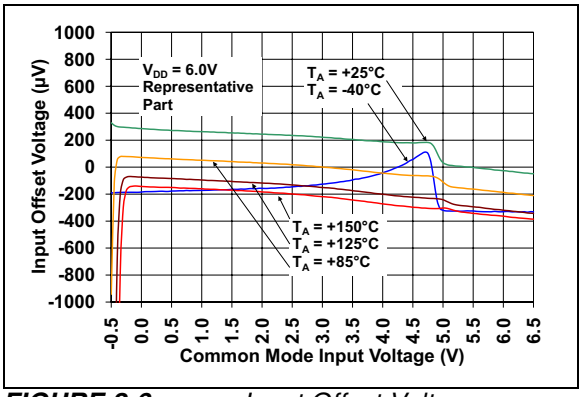

FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 6.0V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

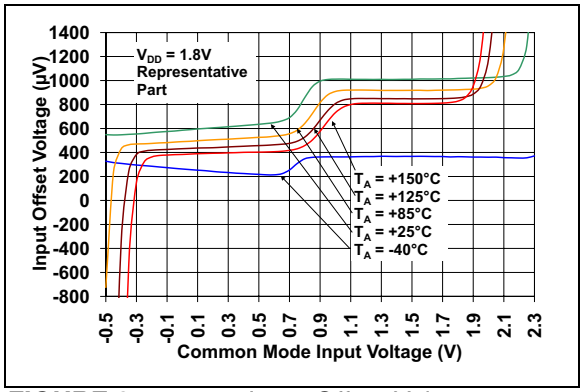

FIGURE 2-7: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 1.8V.*

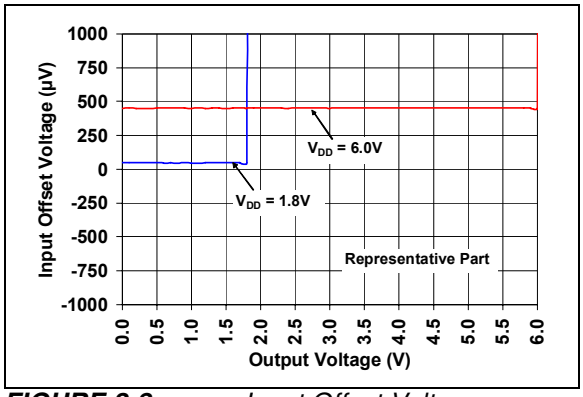

FIGURE 2-8: *Input Offset Voltage vs. Output Voltage.*

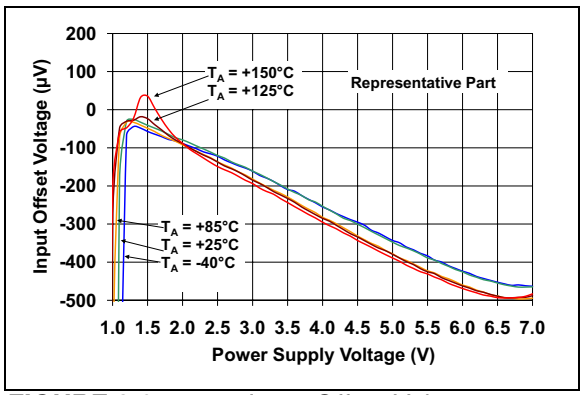

FIGURE 2-9: *Input Offset Voltage vs. Power Supply Voltage.*

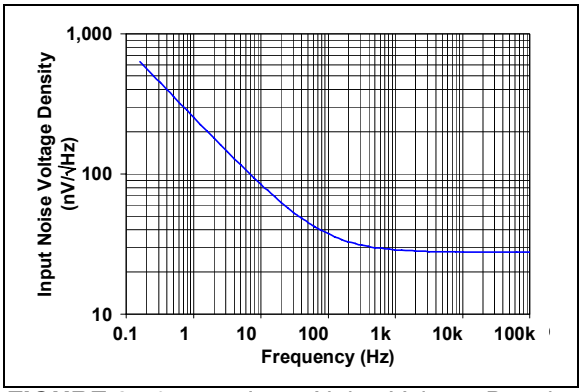

FIGURE 2-10: *Input Noise Voltage Density vs. Frequency.*

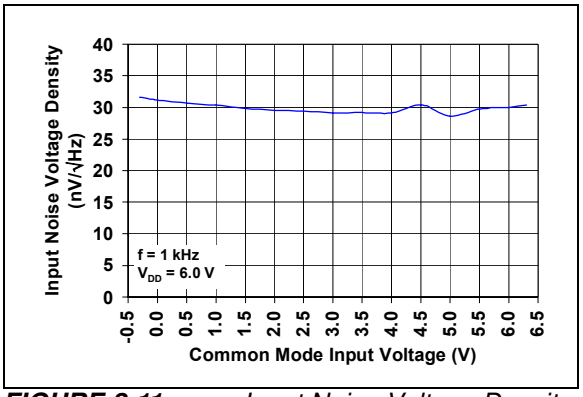

FIGURE 2-11: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

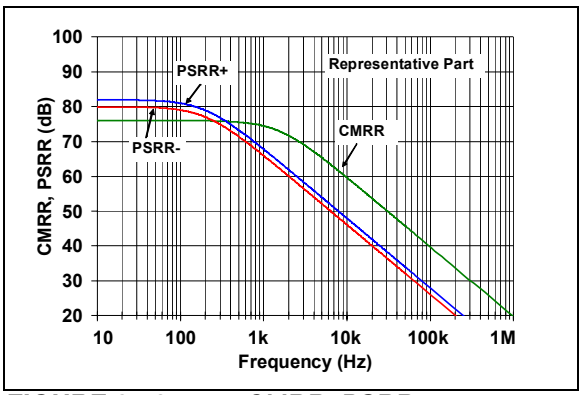

FIGURE 2-12: *CMRR, PSRR vs. Frequency.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

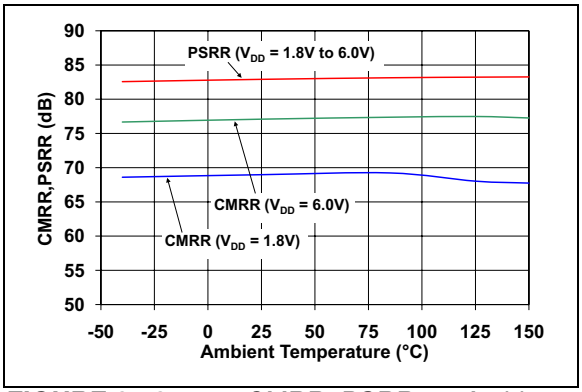

FIGURE 2-13: *CMRR, PSRR vs. Ambient Temperature.*

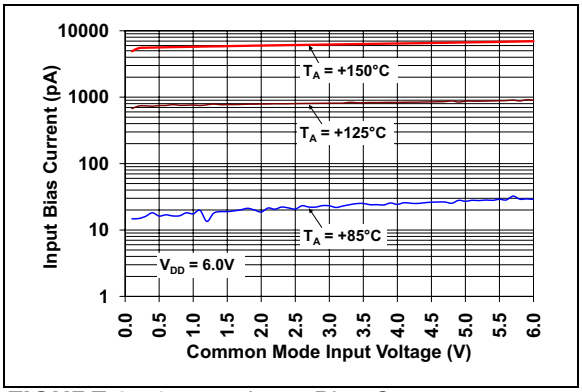

FIGURE 2-16: *Input Bias Current vs. Common Mode Input Voltage.*

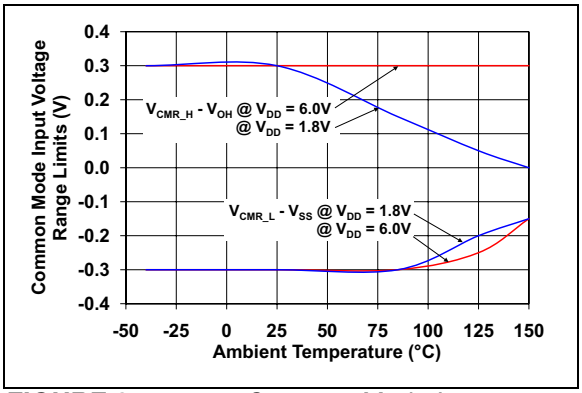

FIGURE 2-14: *Common Mode Input Voltage Range Limits vs. Ambient Temperature.*

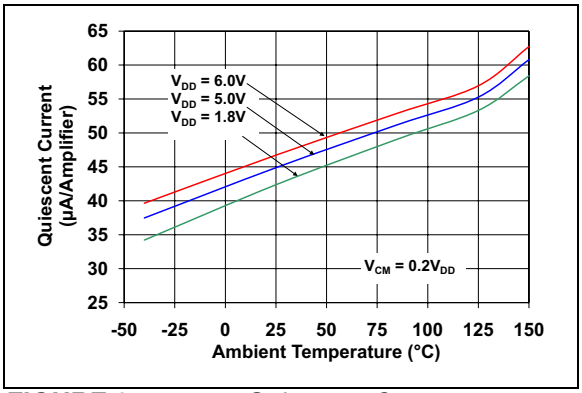

FIGURE 2-17: *Quiescent Current vs. Ambient Temperature.*

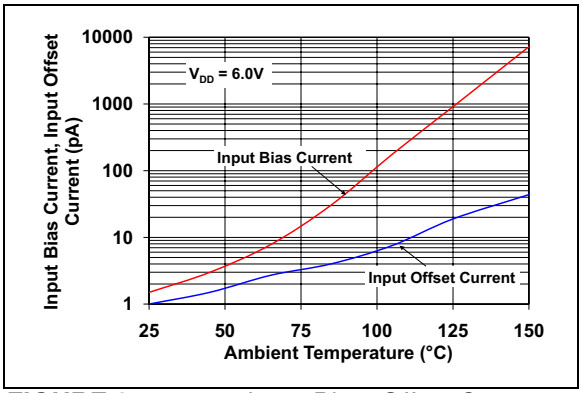

FIGURE 2-15: *Input Bias, Offset Current vs. Ambient Temperature.*

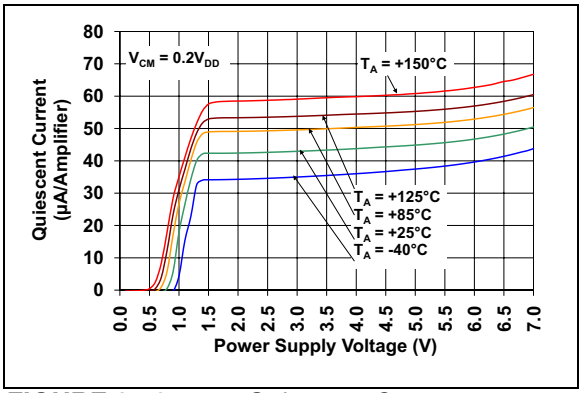

FIGURE 2-18: *Quiescent Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

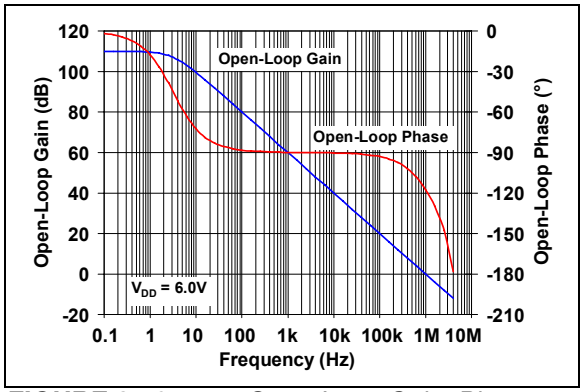

FIGURE 2-19: *Open-Loop Gain, Phase vs. Frequency.*

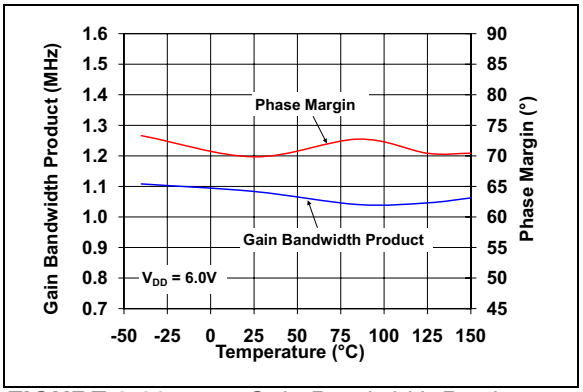

FIGURE 2-22: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

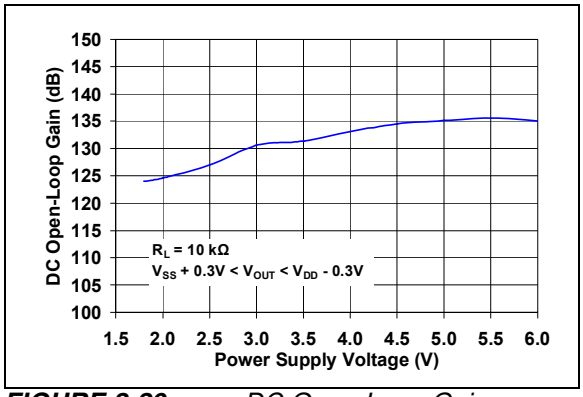

FIGURE 2-20: *DC Open-Loop Gain vs. Power Supply Voltage.*

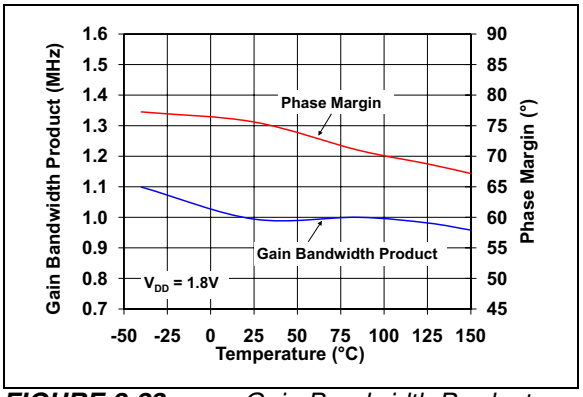

FIGURE 2-23: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

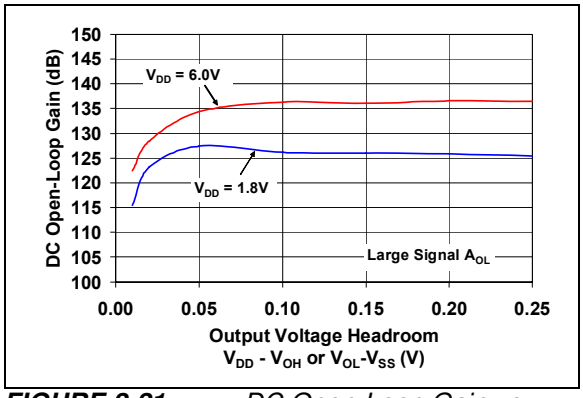

FIGURE 2-21: *DC Open-Loop Gain vs. Output Voltage Headroom.*

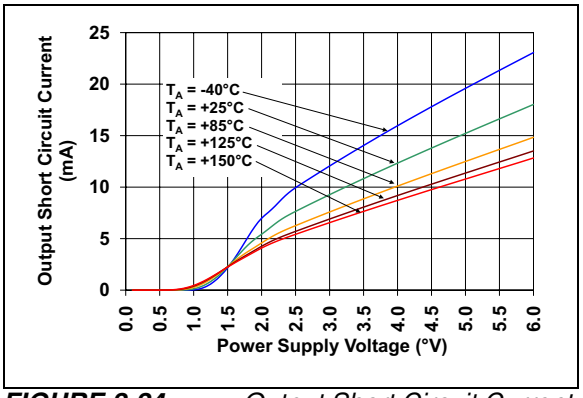

FIGURE 2-24: *Output Short Circuit Current vs. Power Supply Voltage.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

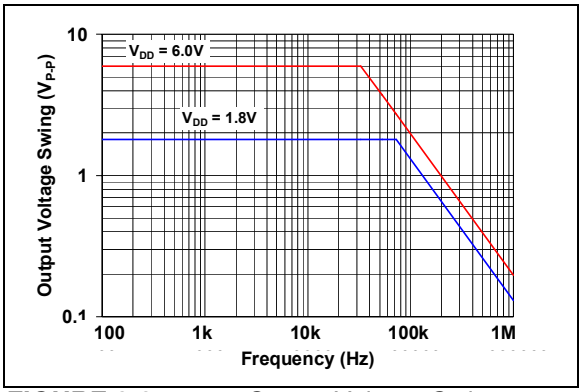

FIGURE 2-25: *Output Voltage Swing vs. Frequency.*

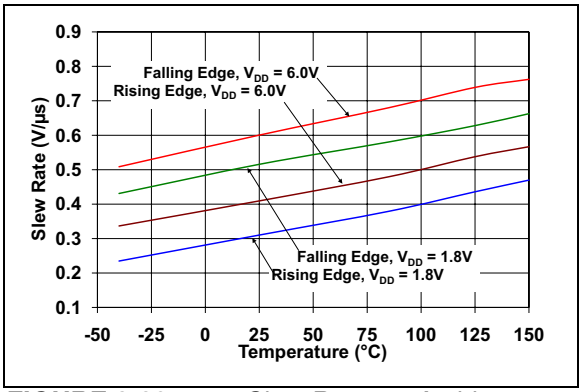

FIGURE 2-28: *Slew Rate vs. Ambient Temperature.*

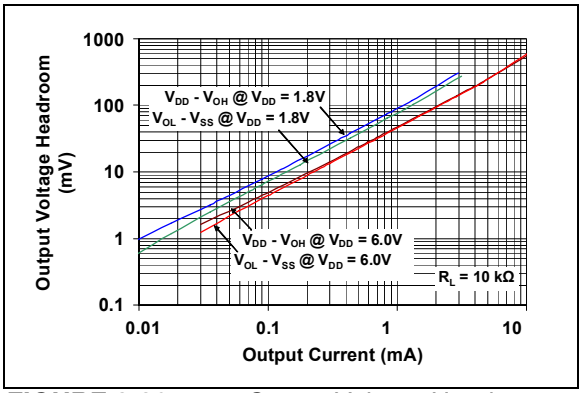

FIGURE 2-26: *Output Voltage Headroom vs. Output Current.*

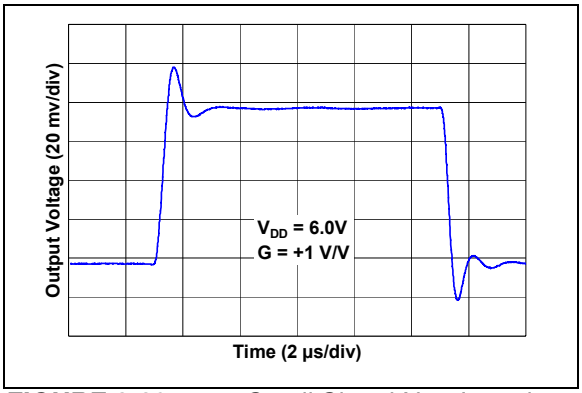

FIGURE 2-29: *Small Signal Non-Inverting Pulse Response.*

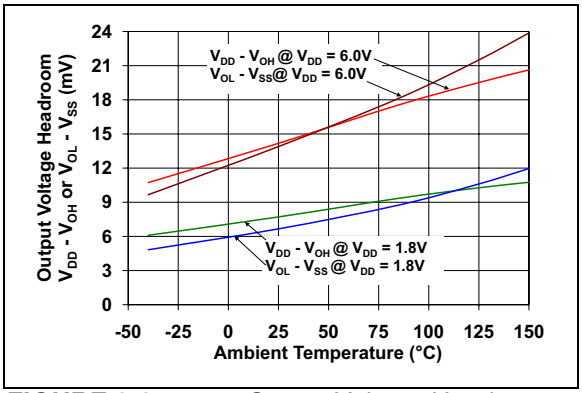

FIGURE 2-27: *Output Voltage Headroom vs. Ambient Temperature.*

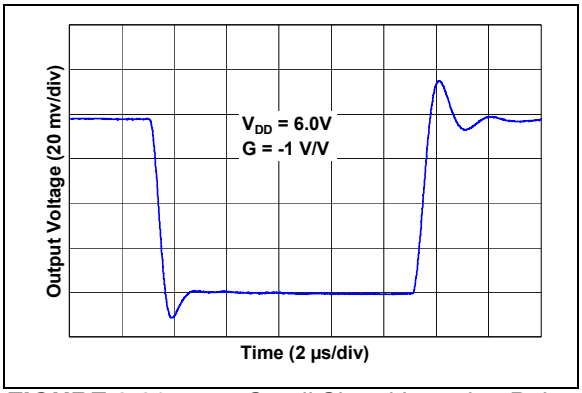

FIGURE 2-30: *Small Signal Inverting Pulse Response.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +6.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 60 pF.

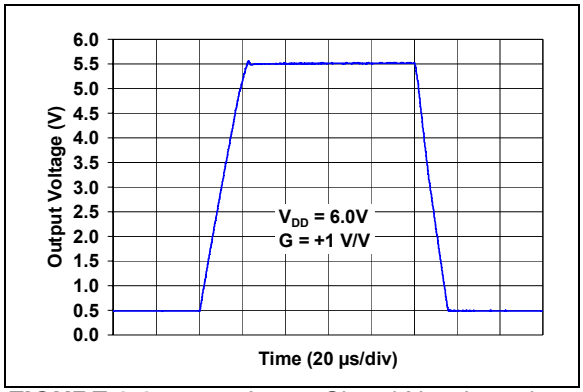

FIGURE 2-31: *Large Signal Non-Inverting Pulse Response.*

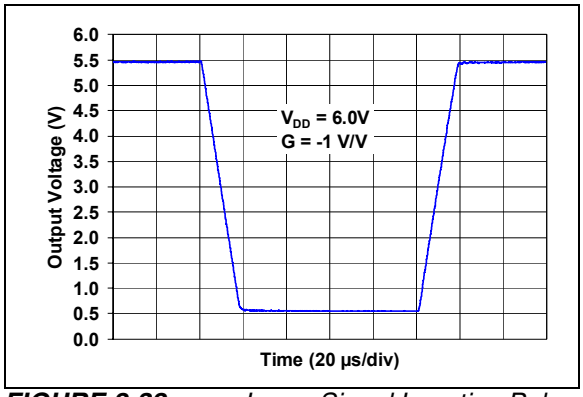

FIGURE 2-32: *Large Signal Inverting Pulse Response.*

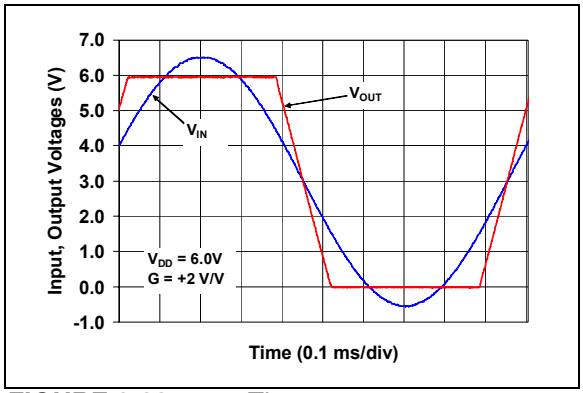

FIGURE 2-33: *The MCP6401/1R/1U/2/4/6/7/9 Shows No Phase Reversal.*

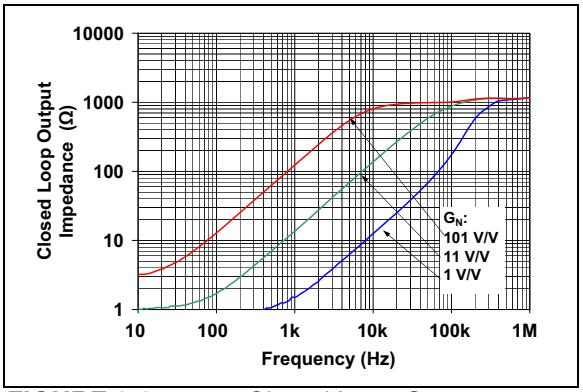

FIGURE 2-34: *Closed Loop Output Impedance vs. Frequency.*

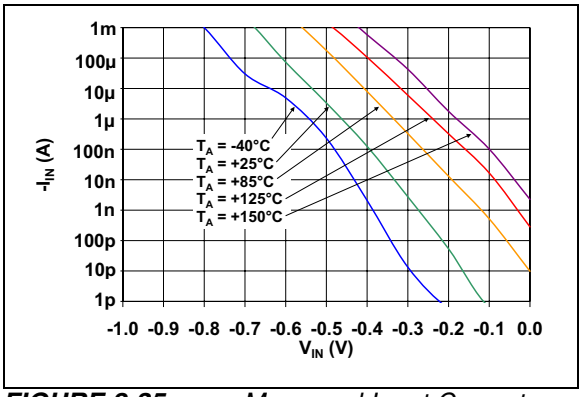

FIGURE 2-35: *Measured Input Current vs. Input Voltage (below V_{SS}).*

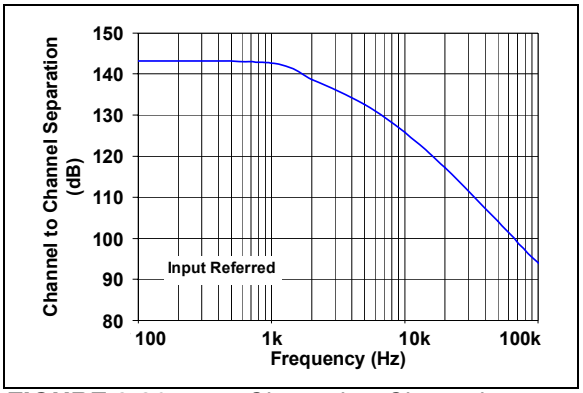

FIGURE 2-36: *Channel-to-Channel Separation vs. Frequency (MCP6402/4/7/9 only).*

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE 1

MCP6401	MCP6401R	MCP6401U	MCP6402		MCP6404	MCP6406	MCP6407	MCP6409	Symbol	Description
SC70-5, SOT-23-5	SOT-23-5	SOT-23-5	SOIC	2x3 TDFN	SOIC, TSSOP	SOT-23-5	SOIC	SOIC		
1	1	4	1	1	1	1	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	4	3	2	2	2	4	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	1	3	3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
5	2	5	8	8	4	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	5	—	5	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	6	6	—	6	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	7	—	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	—	8	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	—	9	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	10	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
2	5	2	4	4	11	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	12	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	13	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	14	—	—	14	V_{OUTD}	Analog Output (op amp D)
—	—	—	—	9	—	—	—	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

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3.1 Analog Output (V_{OUT})

The output pin is low-impedance voltage source.

3.2 Analog Inputs (V_{IN}+, V_{IN}-)

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pin (V_{DD}, V_{SS})

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

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4.0 APPLICATION INFORMATION

The MCP6401/1R/1U/2/4/6/7/9 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power, high-precision applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The MCP6401/1R/1U/2/4/6/7/9 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-33 shows the input voltage exceeding the supply voltage with no phase reversal.

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**).

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many (but not all) over-voltage conditions, and to minimize the input bias current (I_B).

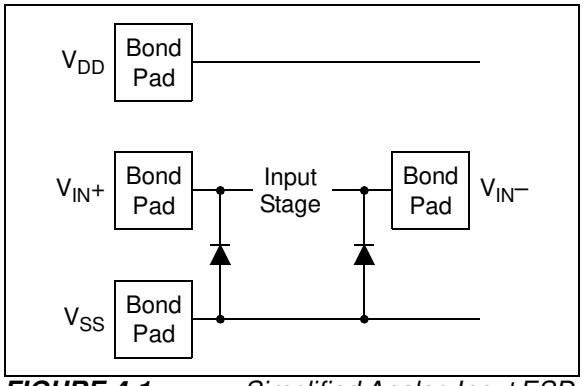

FIGURE 4-1: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V_{DD}) events. Very fast ESD events (that meet the spec) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-2 shows one approach to protecting these inputs.

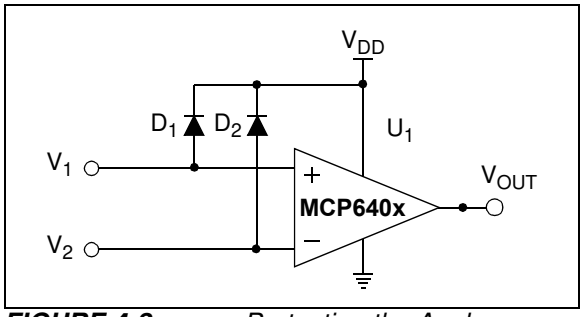

FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs when the Common Mode voltage (V_{CM}) is below ground (V_{SS}); See Figure 2-35.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**).

Figure 4-3 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins (and the ESD diodes, D_1 and D_2). The diode currents will go through either V_{DD} or V_{SS}.

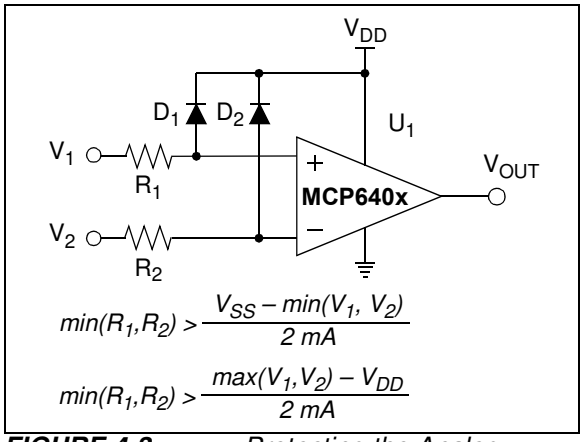

FIGURE 4-3: *Protecting the Analog Inputs.*

4.1.4 NORMAL OPERATION

The input stage of the MCP6401/1R/1U/2/4/6/7/9 op amps use two differential input stages in parallel. One operates at a low Common Mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS} (see Figure 2-14). The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The transition between the input stages occurs when V_{CM} is near $V_{DD} - 1.1V$ (see Figures 2-6 and 2-7). For the best distortion performance and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6401/1R/1U/2/4/6/7/9 op amps is V_{SS} + 20 mV (minimum) and V_{DD} – 20 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 6.0V. Refer to Figures 2-26 and 2-27 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

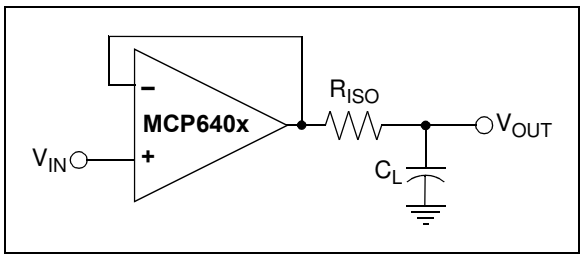

FIGURE 4-4: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-5 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

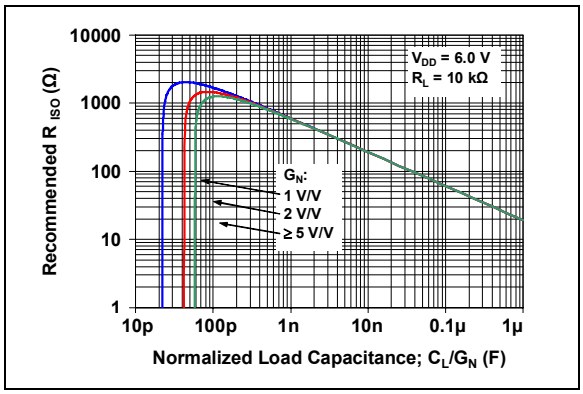

FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6401/1R/1U/2/4/6/7/9 SPICE macro model are very helpful.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 Unused Op Amps

An unused op amp in quad packages (MCP6404 or MCP6409) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp, which buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

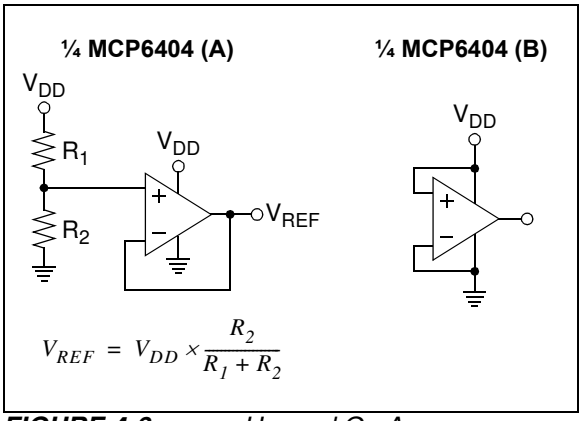

FIGURE 4-6: *Unused Op Amps.*

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4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6401/1R/1U/2/4/6/7/9 family's bias current at +25°C (±1.0 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

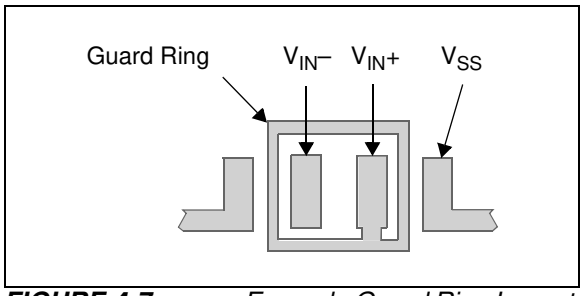

FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the Common Mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 PRECISION HALF-WAVE RECTIFIER

The precision half-wave rectifier, which is also known as a super diode, is a configuration obtained with an operational amplifier in order to have a circuit behave like an ideal diode and rectifier. It effectively cancels the forward voltage drop of the diode so that very low level signals can still be rectified with minimal error. This can be useful for high-precision signal processing. The MCP6401/1R/1U/2/4/6/7/9 op amps have high input impedance, low input bias current and rail-to-rail input/output, which makes this device suitable for precision rectifier applications.

Figure 4-8 shows a precision half-wave rectifier and its transfer characteristic. The rectifier's input impedance is determined by the input resistor R_1. To avoid loading effect, it must be driven from a low-impedance source.

When V_{IN} is greater than zero, D_1 is OFF, D_2 is ON, and V_{OUT} is zero. When V_{IN} is less than zero, D_1 is ON, D_2 is OFF, and V_{OUT} is the V_{IN} with an amplification of $-R_2/R_1$.

The rectifier circuit shown in Figure 4-8 has the benefit that the op amp never goes in saturation, so the only thing affecting its frequency response is the amplification and the gain bandwidth product.

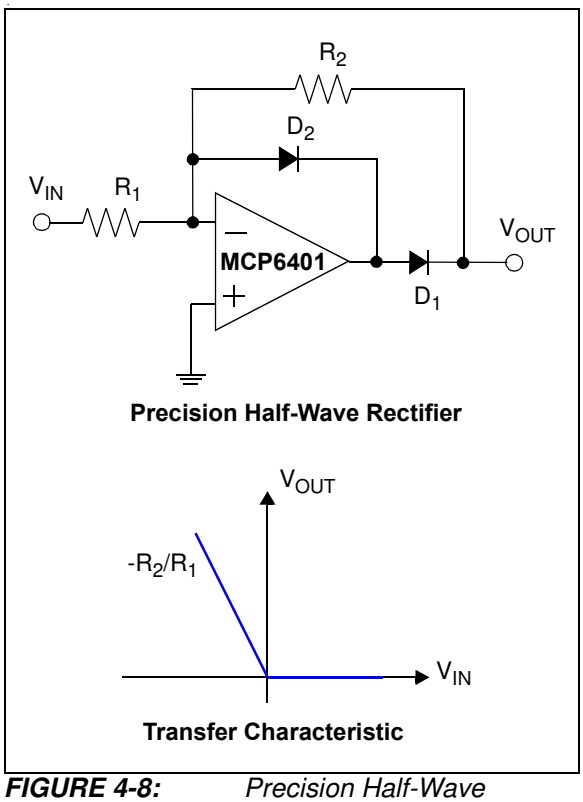

FIGURE 4-8: *Precision Half-Wave Rectifier.*

4.7.2 BATTERY CURRENT SENSING

The MCP6401/1R/1U/2/4/6/7/9 op amps' Common Mode Input Range, which goes 0.3V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The low quiescent current (45 µA, typical) helps prolong battery life, and the rail-to-rail output supports detection of low currents.

Figure 4-9 shows a high-side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common Mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, which is within its Maximum Output Voltage Swing specification.

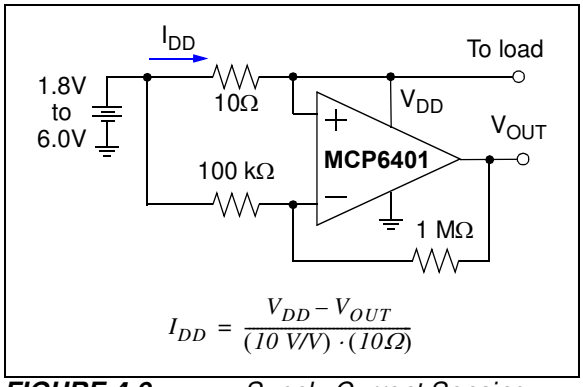

FIGURE 4-9: *Supply Current Sensing.*

4.7.3 INSTRUMENTATION AMPLIFIER

The MCP6401/1R/1U/2/4/6/7/9 op amps are well suited for conditioning sensor signals in battery-powered applications. Figure 4-10 shows a two op amp instrumentation amplifier, using the MCP6402, that works well for applications requiring rejection of Common Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low impedance source. In single supply applications, V_{REF} is typically $V_{DD}/2$.

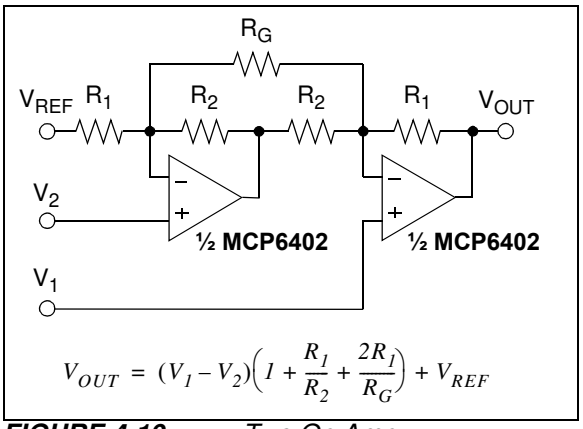

FIGURE 4-10: *Two Op Amp Instrumentation Amplifier.*

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5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6401/1R/1U/2/4/6/7/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6401/1R/1U/2/4/6/7/9 op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in official Orcad (Cadence) owned PSPICE. For other simulators, translation may be required.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot be guaranteed to match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit www.microchip.com/analogtools, the Microchip web site.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

5.5 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits"*, DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications"*, DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications"*, DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors"*, DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise"*, DS01228
- **AN1297:** *"Microchip's Op Amp SPICE Macro Models"*, DS01297
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals"*, DS01332

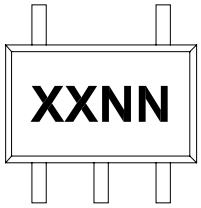
These application notes and others are listed in the design guide:

- *"Signal Chain Design Guide"*, DS21825

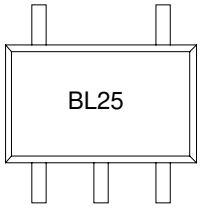
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

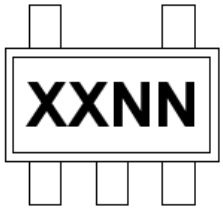
5-Lead SC70 **(MCP6401 only)**



Example:

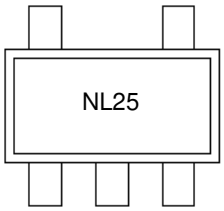


5-Lead SOT-23
(MCP6401/1R/1U, MCP6406)



Part Number	Code
MCP6401T-E/OT	NLNN
MCP6401T-H/OT	U8NN
MCP6401RT-E/OT	NMNN
MCP6401RT-H/OT	U9NN
MCP6401UT-E/OT	NPNN
MCP6401UT-H/OT	V8NN
MCP6406T-E/OT	ZXNN
MCP6406T-H/OT	ZYNN

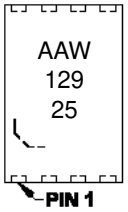
Example:



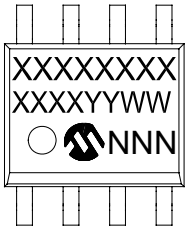
8-Lead TDFN (2 x 3)**(MCP6402 only)**

Part Number	Code
MCP6402T-E/MNY	AAW

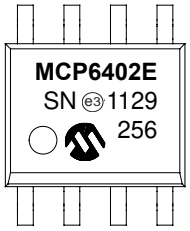
Example:



8-Lead SOIC (150 mil)**(MCP6401, MCP6402, MCP6407)**



Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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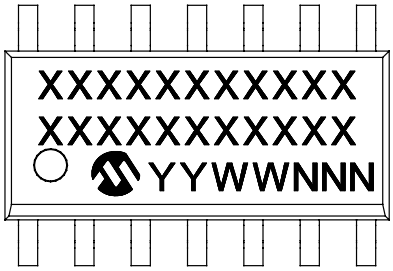
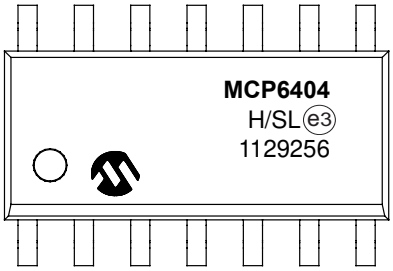
Package Marking Information (Continued)

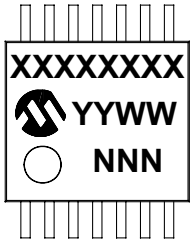
14-Lead SOIC (150 mil) (**MCP6404, MCP6409**)



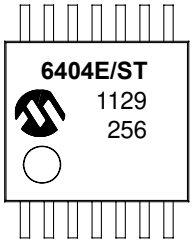
Example:



14-Lead TSSOP (**MCP6404 only**)



Example:

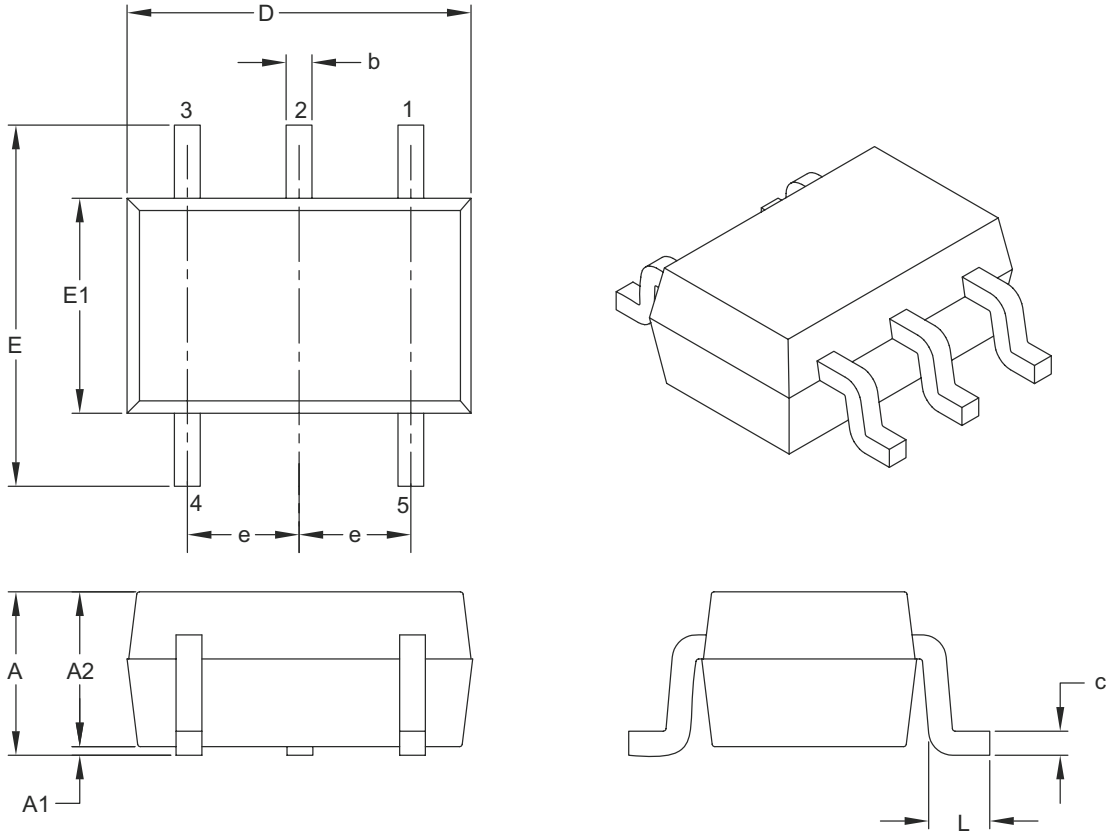


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

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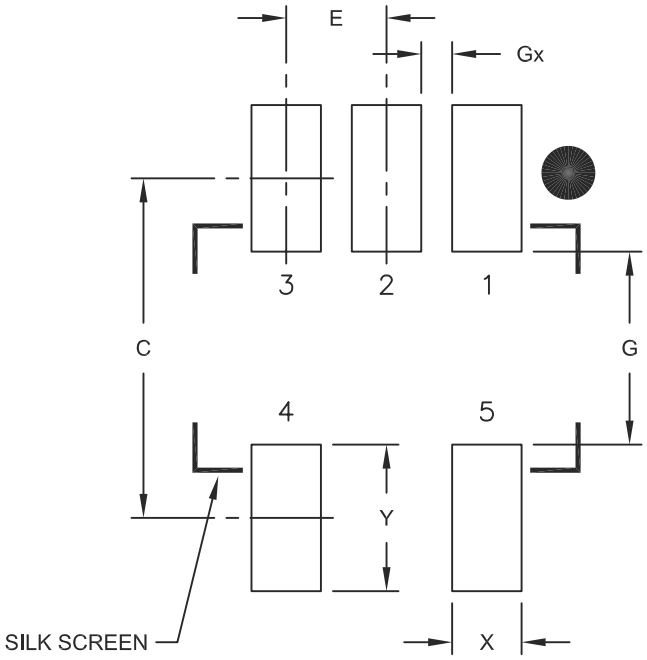
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A