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MCP651/1S/2/3/4/5/9

50 MHz, 200 µV Op Amps with mCal

Features:

- Gain-Bandwidth Product: 50 MHz
- Slew Rate: 30 V/µs
- Low Input Offset: ±200 µV (maximum)
- Low Input Bias Current: 6 pA (typical)
- Noise: 7.5 nV/√Hz, at 1 MHz
- Ease-of-Use:
  - Unity-Gain Stable
  - Rail-to-Rail Output
  - Input Range incl. Negative Rail
  - No Phase Reversal
- Supply Voltage Range: +2.5V to +5.5V
- High Output Current: ±100 mA
- Supply Current: 6.0 mA/Ch (typical)
- Low-Power Mode: 5 µA/Ch
- Small Packages: SOT23-5, DFN
- Extended Temperature Range: -40°C to +125°C

Typical Applications:

- Driving A/D Converters
- Fast Low-side Current Sensing
- Power Amplifier Control Loops
- Optical Detector Amplifier
- Barcode Scanners
- Multi-Pole Active Filter
- Consumer Audio

Design Aids:

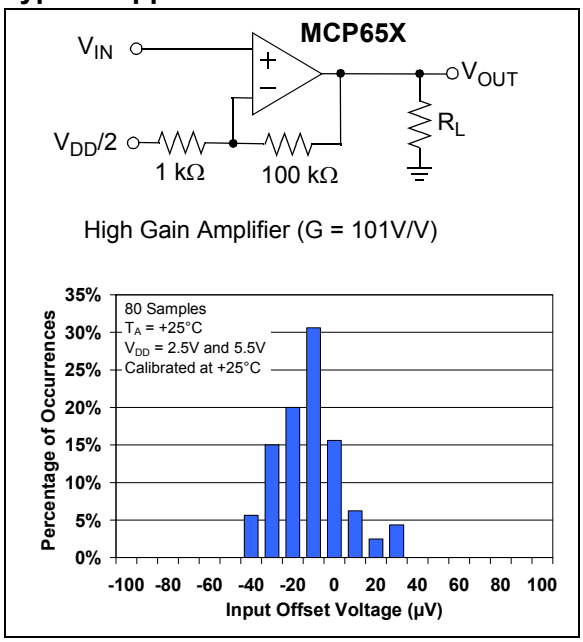
- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
  - MCP651EV-VOS
- Application Notes

Description:

The Microchip Technology Inc. MCP651/1S/2/3/4/5/9 family of high bandwidth and high slew rate operational amplifiers features low offset. At power-up, these op amps are self-calibrated using mCal. Some package options also provide a Calibration/Chip Select pin (CAL/$\overline{CS}$) that supports a Low-Power mode of operation, with offset calibration at the time normal operation is re-started. These amplifiers are optimized for high speed, low noise and distortion, single-supply operation with rail-to-rail output and an input that includes the negative rail.

This family is offered in single (MCP651 and MCP651S), single with CAL/$\overline{CS}$ pin (MCP653), dual (MCP652), dual with CAL/$\overline{CS}$ pins (MCP655), quad (MCP654) and quad with CAL/$\overline{CS}$ pins (MCP659). All devices are fully specified from -40°C to +125°C.

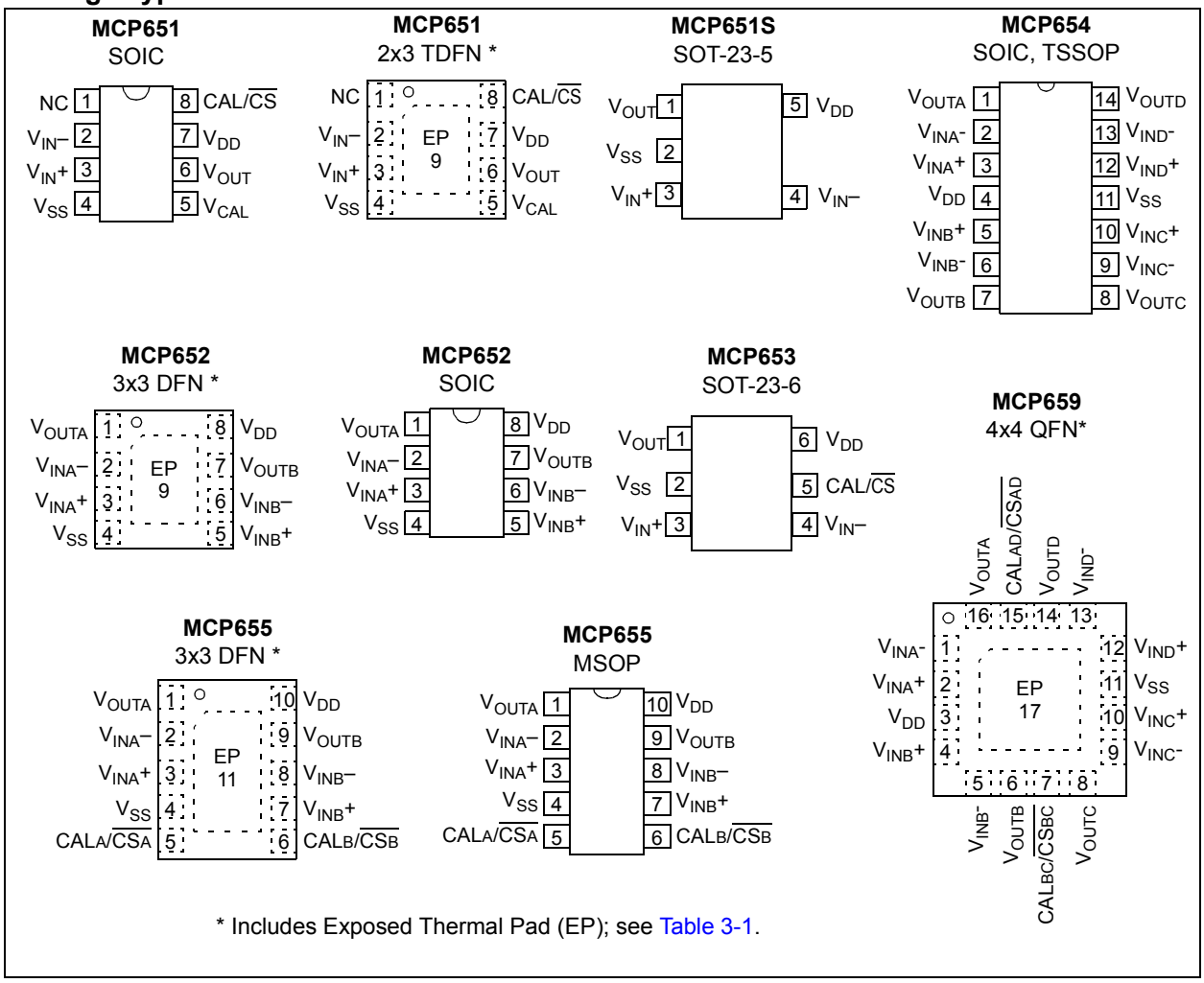
Typical Application Circuit



High Gain-Bandwidth Op Amp Portfolio

Model Family	Channels/Package	Gain-Bandwidth	V_{OS} (max.)	I_Q/Ch (typ.)
MCP621/1S/2/3/4/5/9	1, 2, 4	20 MHz	0.2 mV	2.5 mA
MCP631/2/3/4/5/9	1, 2, 4	24 MHz	8.0 mV	2.5 mA
MCP651/1S/2/3/4/5/9	1, 2, 4	50 MHz	0.2 mV	6.0 mA
MCP660/1/2/3/4/5/9	1, 2, 3, 4	60 MHz	8.0 mV	6.0 mA

Package Types



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† . V_{SS} – 1.0V to V_{DD} + 1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±150 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, MM) .....≥ 1 kV, 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.2 "Input Voltage and Current Limits"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-200	—	+200	µV	After calibration (**Note 1**)
Input Offset Voltage Trim Step	V_{OSTRM}	—	37	200	µV	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A= -40°C to +125°C
Power Supply Rejection Ratio	PSRR	61	76	—	dB	
Input Current and Impedance						
Input Bias Current	I_B	—	6	—	pA	
Across Temperature	I_B	—	130	—	pA	T_A= +85°C
Across Temperature	I_B	—	1700	5,000	pA	T_A= +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||9	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.3	V	(**Note 2**)
Common Mode Rejection Ratio	CMRR	65	81	—	dB	V_{DD} = 2.5V, V_{CM} = -0.3 to 1.2V
	CMRR	68	84	—	dB	V_{DD} = 5.5V, V_{CM} = -0.3 to 4.2V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	88	114	—	dB	V_{DD} = 2.5V, V_{OUT} = 0.3V to 2.2V
	A_{OL}	94	123	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.3V to 5.2V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 2.5V, G = +2, 0.5V Input Overdrive
	V_{OL}, V_{OH}	V_{SS} + 50	—	V_{DD} – 50	mV	V_{DD} = 5.5V, G = +2, 0.5V Input Overdrive
Output Short-Circuit Current	I_{SC}	±50	±95	±145	mA	V_{DD} = 2.5V (**Note 3**)
	I_{SC}	±50	±100	±150	mA	V_{DD} = 5.5V (**Note 3**)

Note 1: Describes the offset (under the specified conditions) right after power-up, or just after the CAL/$\overline{CS}$ pin is toggled. Thus, 1/f noise effects (an apparent wander in V_{OS}; see Figure 2-35) are not included.
2: See Figure 2-6 and Figure 2-7 for temperature effects.
3: The I_{SC} specifications are for design guidance only; they are not tested.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/3$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Calibration Input						
Calibration Input Voltage Range	V_{CALRNG}	V_{SS} + 0.1	—	V_{DD} – 1.4	mV	V_{CAL} pin externally driven
Internal Calibration Voltage	V_{CAL}	0.31V_{DD}	0.33V_{DD}	0.35V_{DD}		V_{CAL} pin open
Input Impedance	Z_{CAL}	—	100 || 5	—	kΩ||pF	
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	3	6	9	mA	I_O = 0
POR Input Threshold, Low	V_{PRL}	1.15	1.40	—	V	
POR Input Threshold, High	V_{PRH}	—	1.40	1.65	V	

Note 1: Describes the offset (under the specified conditions) right after power-up, or just after the CAL/$\overline{CS}$ pin is toggled. Thus, 1/f noise effects (an apparent wander in V_{OS}; see Figure 2-35) are not included.

2: See Figure 2-6 and Figure 2-7 for temperature effects.

3: The I_{SC} specifications are for design guidance only; they are not tested.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L, C_L = 20 pF and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain-Bandwidth Product	GBWP	—	50	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1
Open-Loop Output Impedance	R_{OUT}	—	20	—	Ω	
AC Distortion						
Total Harmonic Distortion plus Noise	THD+N	—	0.0012	—	%	G = +1, V_{OUT} = 4V_{P-P}, f = 1 kHz, V_{DD} = 5.5V, BW = 80 kHz
Step Response						
Rise Time, 10% to 90%	t_r	—	6	—	ns	G = +1, V_{OUT} = 100 mV_{P-P}
Slew Rate	SR	—	30	—	V/µs	G = +1
Noise						
Input Noise Voltage	E_{ni}	—	17	—	µV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	7.5	—	nV/√Hz	f = 1 MHz
Input Noise Current Density	i_{ni}		4	—	fA/√Hz	f = 1 kHz

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L, C_L = 20 pF and CAL/$\overline{CS}$ = V_{SS} (refer to Figure 1-1 and Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
CAL/$\overline{CS}$ Low Specifications						
CAL/$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2V_{DD}	V	
CAL/$\overline{CS}$ Input Current, Low	I_{CSL}	—	0	—	nA	CAL/$\overline{CS}$ = 0V
CAL/$\overline{CS}$ High Specifications						
CAL/$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8V_{DD}		V_{DD}	V	
CAL/$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	—	µA	CAL/$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	-3.5	-1.8	—	µA	Single, CAL/$\overline{CS}$ = V_{DD} = 2.5V
	I_{SS}	-8	-4	—	µA	Single, CAL/$\overline{CS}$ = V_{DD} = 5.5V
	I_{SS}	-5	-2.5	—	µA	Dual, CAL/$\overline{CS}$ = V_{DD} = 2.5V
	I_{SS}	-10	-5	—	µA	Dual, CAL/$\overline{CS}$ = V_{DD} = 5.5V
CAL/$\overline{CS}$ Internal Pull-Down Resistor	R_{PD}	—	5	—	MΩ	
Amplifier Output Leakage	$I_{O(LEAK)}$	—	50	—	nA	CAL/$\overline{CS}$ = V_{DD}
POR Dynamic Specifications						
V_{DD} Low to Amplifier Off Time (output goes High Z)	t_{POFF}	—	200	—	ns	G = +1 V/V, V_L = V_{SS}, V_{DD} = 2.5V to 0V step to V_{OUT} = 0.1 (2.5V)
V_{DD} High to Amplifier On Time (including calibration)	t_{PON}	100	200	300	ms	G = +1 V/V, V_L = V_{SS}, V_{DD} = 0V to 2.5V step to V_{OUT} = 0.9 (2.5V)
CAL/$\overline{CS}$ Dynamic Specifications						
CAL/$\overline{CS}$ Input Hysteresis	V_{HYST}	—	0.25	—	V	
CAL/$\overline{CS}$ Setup Time (between CAL/$\overline{CS}$ edges)	t_{CSU}	1	—	—	µs	G = +1 V/V, V_L = V_{SS} **(Notes 2, 3, 4)** CAL/$\overline{CS}$ = 0.8V_{DD} to V_{OUT} = 0.1 (V_{DD}/2)
CAL/$\overline{CS}$ High to Amplifier Off Time (output goes High Z)	t_{COFF}	—	200	—	ns	G = +1 V/V, V_L = V_{SS}, CAL/$\overline{CS}$ = 0.8V_{DD} to V_{OUT} = 0.1 (V_{DD}/2)
CAL/$\overline{CS}$ Low to Amplifier On Time (including calibration)	t_{CON}	—	3	4	ms	G = +1 V/V, V_L = V_{SS}, MCP651 and MCP655, CAL/$\overline{CS}$ = 0.2V_{DD} to V_{OUT} = 0.9 (V_{DD}/2)
	t_{CON}	—	6	8	ms	G = +1 V/V, V_L = V_{SS}, MCP659, CAL/$\overline{CS}$ = 0.2V_{DD} to V_{OUT} = 0.9 (V_{DD}/2)

Note 1: The MCP652 single, MCP653 single, MCP655 dual and MCP659 quad have their CAL/$\overline{CS}$ inputs internally pulled down to V_{SS} (0V).

2: This time ensures that the internal logic recognizes the edge. However, for the rising edge case, if CAL/$\overline{CS}$ is raised before the calibration is complete, the calibration will be aborted and the part will return to Low-Power mode.

3: For the MCP655 dual, there is an additional constraint. CALA/$\overline{CS}$A and CALB/$\overline{CS}$B can be toggled simultaneously (within a time much smaller than t_{CSU}) to make both op amps perform the same function simultaneously. If they are toggled independently, then CALA/$\overline{CS}$A (CALB/$\overline{CS}$B) cannot be allowed to toggle while op amp B (op amp A) is in Calibration mode; allow more than the maximum t_{CON} time (4 ms) before the other side is toggled.

4: For the MCP659 quad, there is an additional constraint. CALAD/$\overline{CS}$AD and CALBC/$\overline{CS}$BC can be toggled simultaneously (within a time much smaller than t_{CSU}) to make all four op amps perform the same function simultaneously, and the maximum t_{CON} time is approximately doubled (8 ms). If they are toggled independently, then CALAD/$\overline{CS}$AD (CALBC/$\overline{CS}$BC) cannot be allowed to toggle while op amps B and C (op amps A and D) are in Calibration mode; allow more than the maximum t_{CON} time (8 ms) before the other side is toggled.

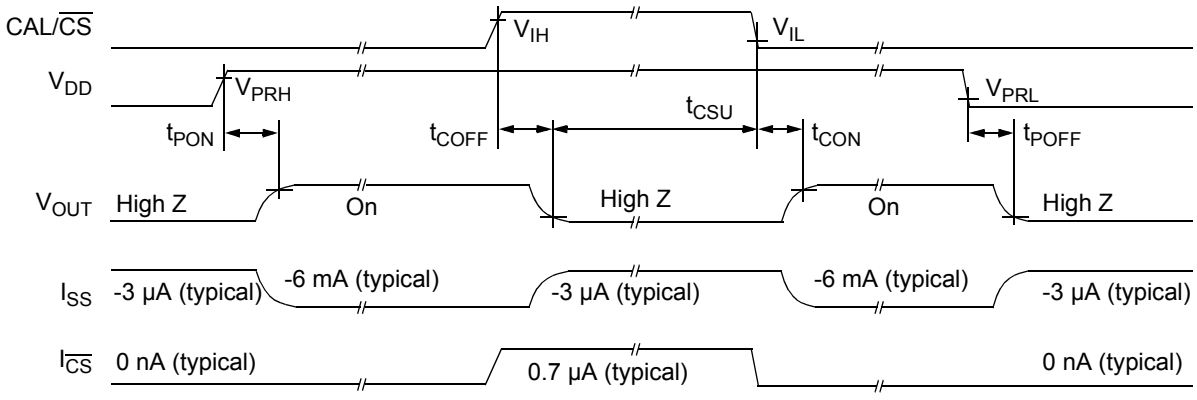
TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +2.5V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-2×3 SOT	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 6L-2×3 SOT	θ_{JA}	—	190.5	—	°C/W	
Thermal Resistance, 8L-2×3 TDFN	θ_{JA}	—	52.5	—	°C/W	
Thermal Resistance, 8L-3×3 DFN	θ_{JA}	—	63	—	°C/W	**(Note 2)**
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 10L-3×3 DFN	θ_{JA}	—	71	—	°C/W	**(Note 2)**
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-4x4-QFN	θ_{JA}	—	46	—	°C/W	**(Note 2)**

Note 1: Operation must not cause T_J to exceed Maximum Junction Temperature specification (150°C).

2: Measured on a standard JC51-7, four-layer printed circuit board with ground plane and vias.

1.3 Timing Diagram



Note: For the MCP655 dual and the MCP659 quad, there is an additional constraint on toggling the two CAL/$\overline{CS}$ pins close together; see the T_{CON} specification in Table 1-3.

FIGURE 1-1: *Timing Diagram.*

1.4 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-2. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's Common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F/R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

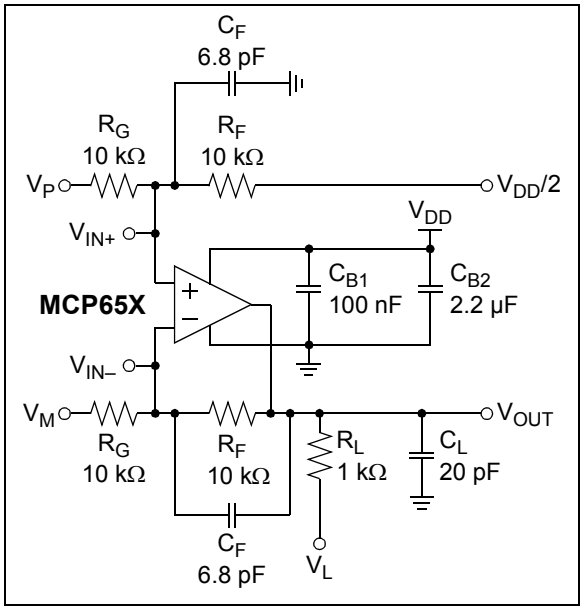


FIGURE 1-2: *AC and DC Test Circuit for Most Specifications.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.1 DC Signal Inputs

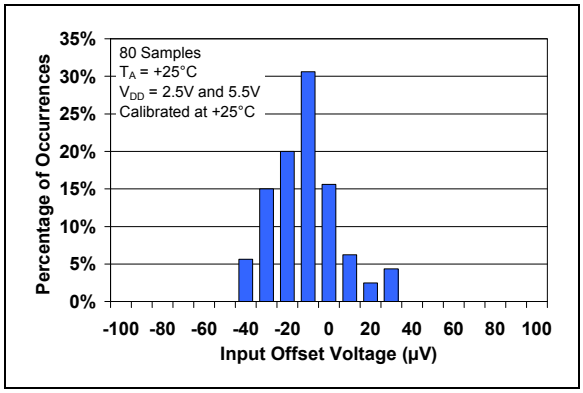


FIGURE 2-1: *Input Offset Voltage.*

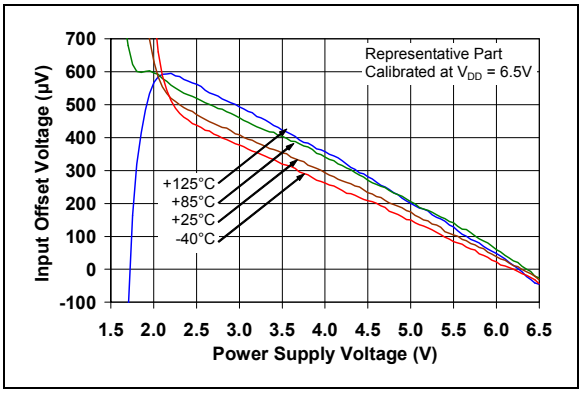


FIGURE 2-4: *Input Offset Voltage vs. Power Supply Voltage.*

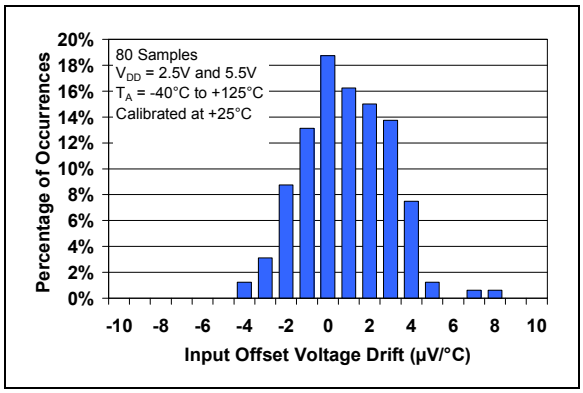


FIGURE 2-2: *Input Offset Voltage Drift.*

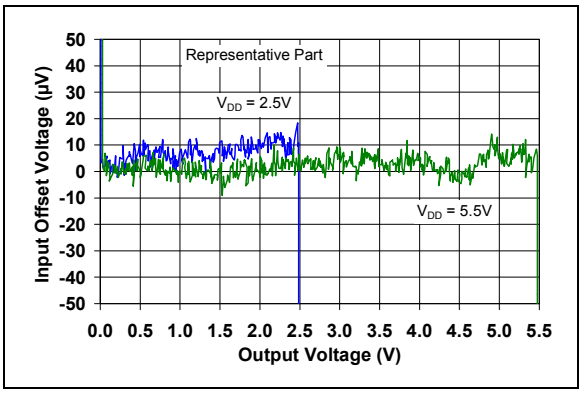


FIGURE 2-5: *Input Offset Voltage vs. Output Voltage.*

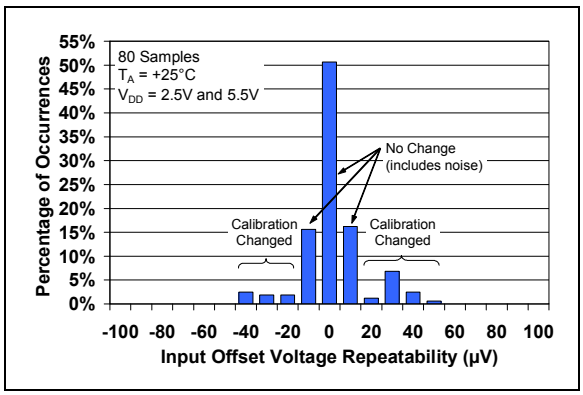


FIGURE 2-3: *Input Offset Voltage Repeatability (repeated calibration).*

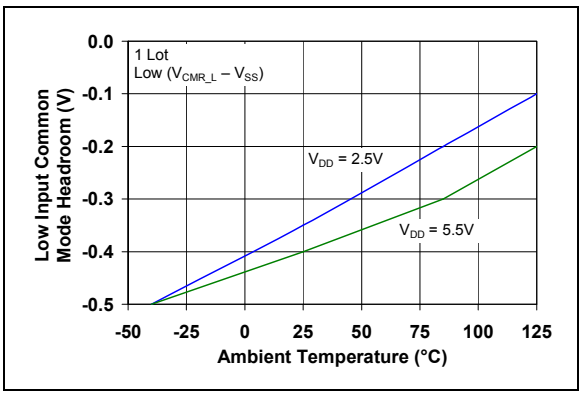


FIGURE 2-6: *Low-Input Common Mode Voltage Headroom vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

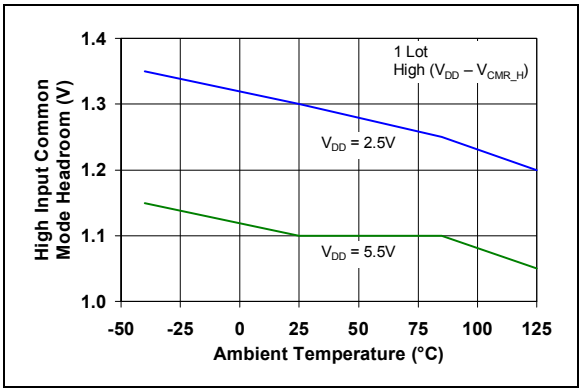


FIGURE 2-7: *High-Input Common Mode Voltage Headroom vs. Ambient Temperature.*

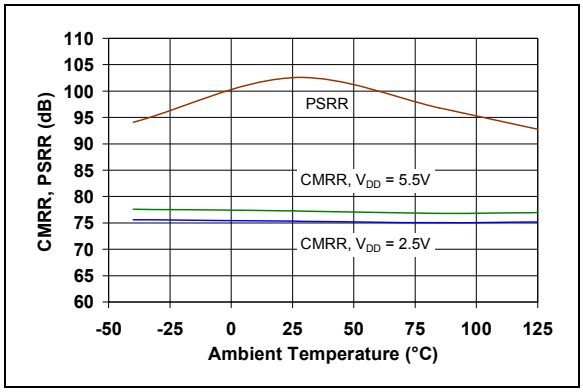


FIGURE 2-10: *CMRR and PSRR vs. Ambient Temperature.*

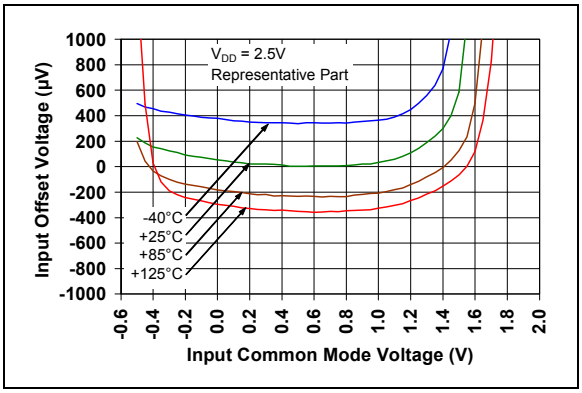


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 2.5V.*

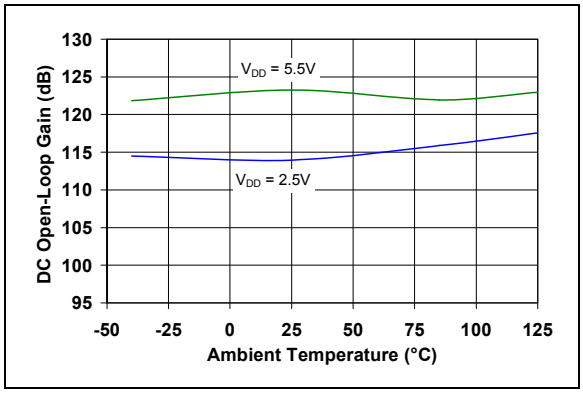


FIGURE 2-11: *DC Open-Loop Gain vs. Ambient Temperature.*

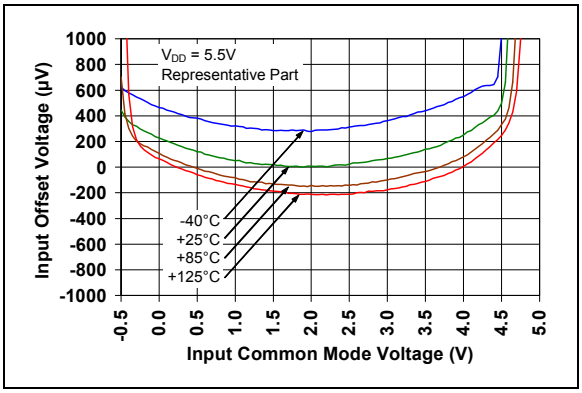


FIGURE 2-9: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 5.5V.*

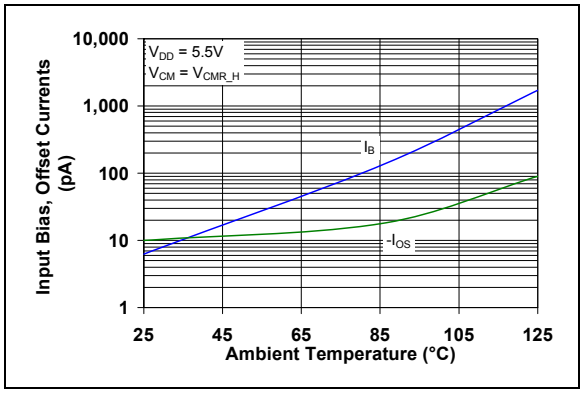


FIGURE 2-12: *Input Bias and Offset Currents vs. Ambient Temperature with V_{DD} = +5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

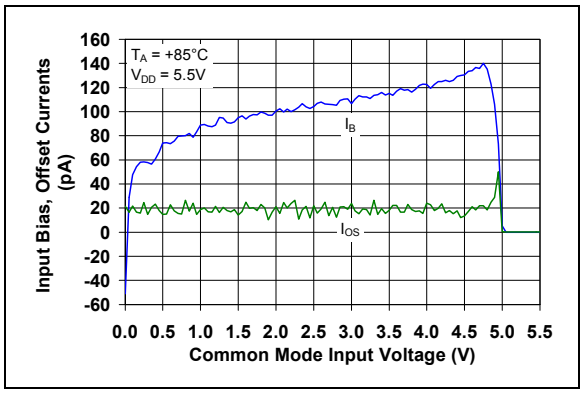


FIGURE 2-13: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +85°C.*

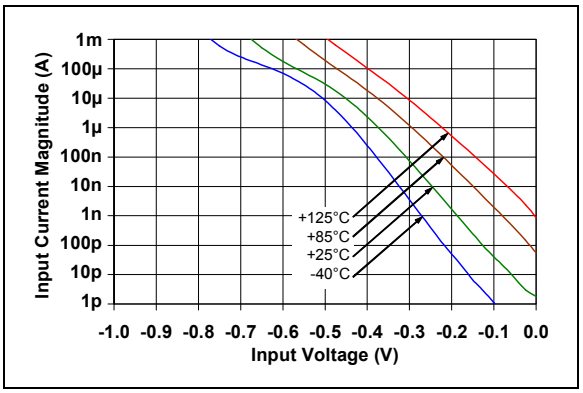


FIGURE 2-15: *Input Bias Current vs. Input Voltage (below V_{SS}).*

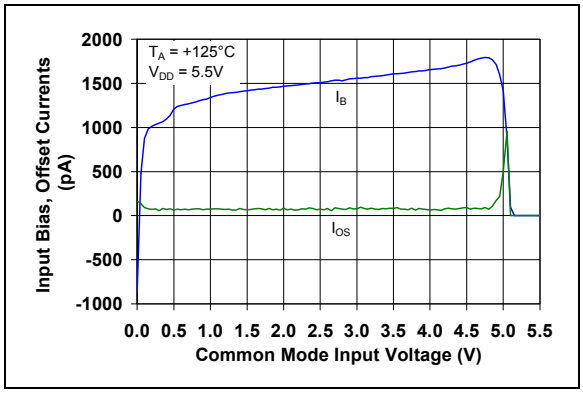


FIGURE 2-14: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.2 Other DC Voltages and Currents

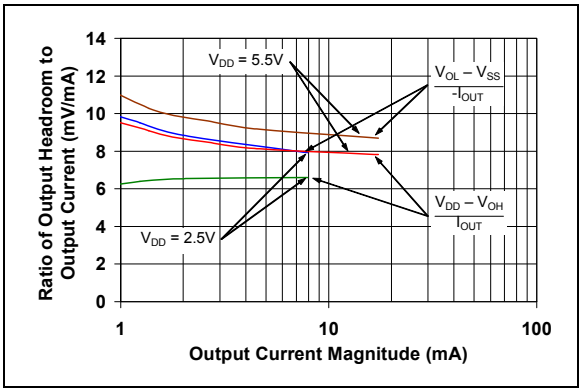


FIGURE 2-16: *Ratio of Output Voltage Headroom to Output Current.*

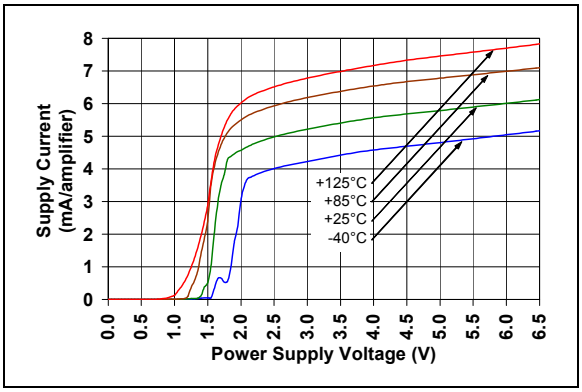


FIGURE 2-19: *Supply Current vs. Power Supply Voltage.*

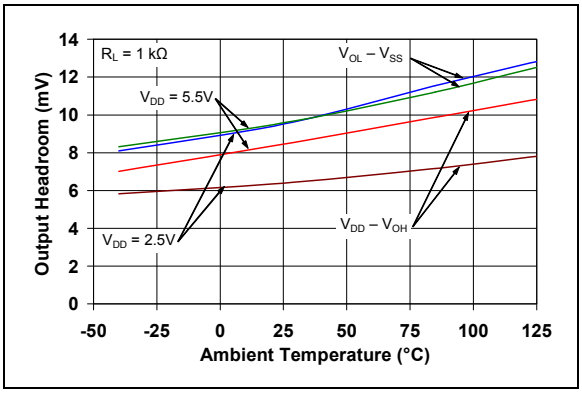


FIGURE 2-17: *Output Voltage Headroom vs. Ambient Temperature.*

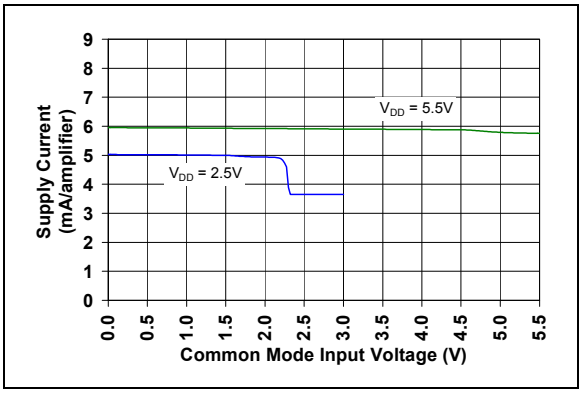


FIGURE 2-20: *Supply Current vs. Common Mode Input Voltage.*

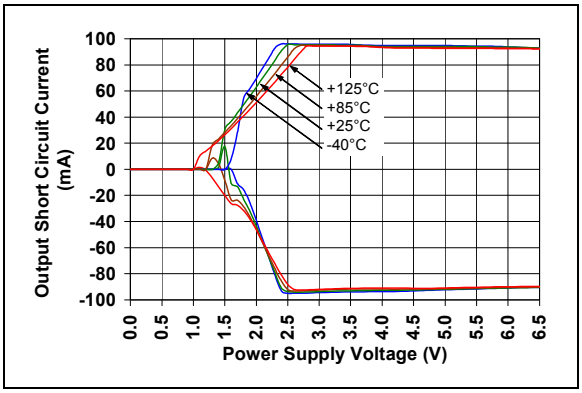


FIGURE 2-18: *Output Short-Circuit Current vs. Power Supply Voltage.*

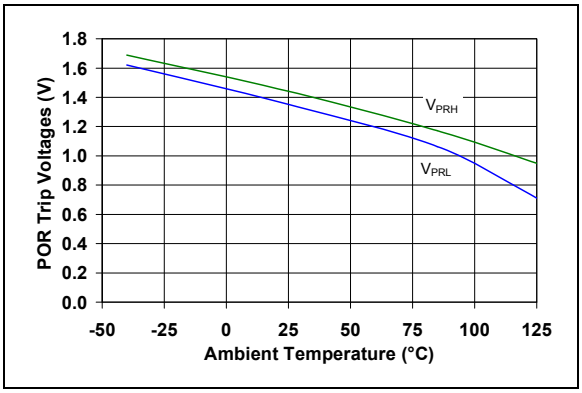


FIGURE 2-21: *Power-On Reset Voltages vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

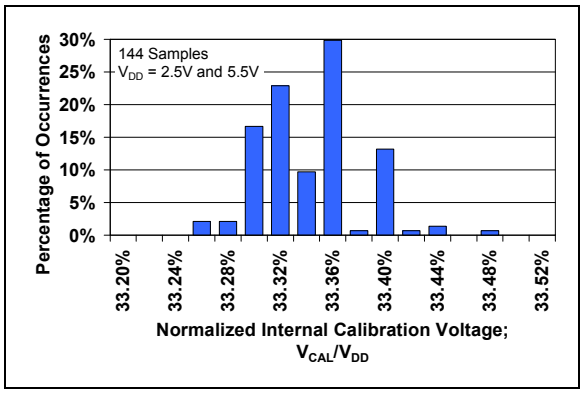


FIGURE 2-22: *Normalized Internal Calibration Voltage.*

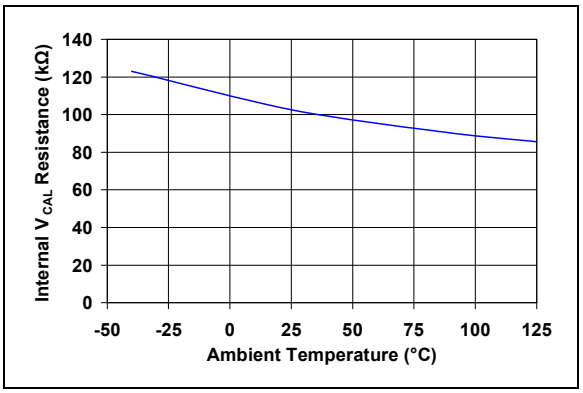


FIGURE 2-23: *V_{CAL} Input Resistance vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.3 Frequency Response

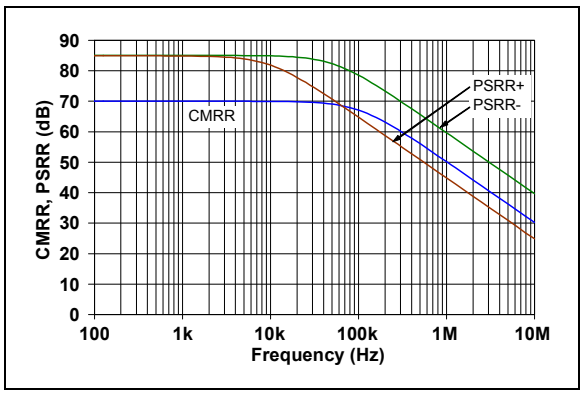


FIGURE 2-24: *CMRR and PSRR vs. Frequency.*

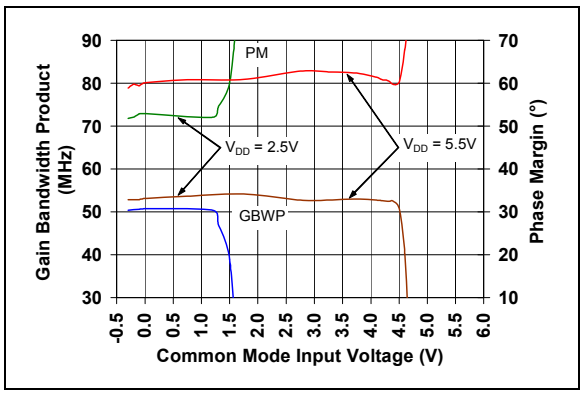


FIGURE 2-27: *Gain-Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.*

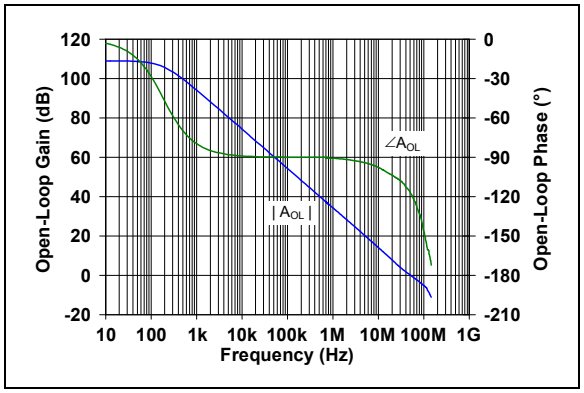


FIGURE 2-25: *Open-Loop Gain vs. Frequency.*

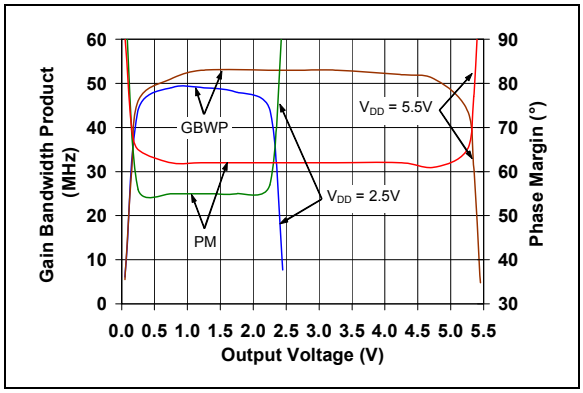


FIGURE 2-28: *Gain-Bandwidth Product and Phase Margin vs. Output Voltage.*

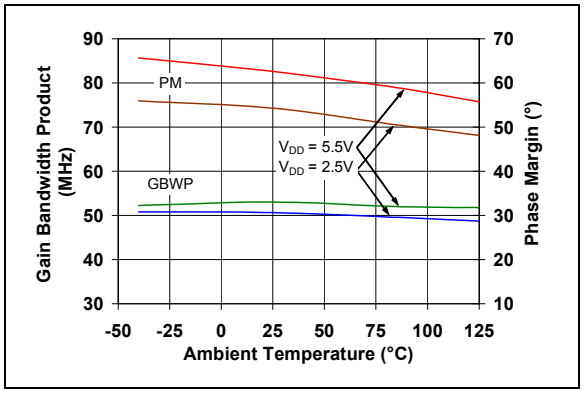


FIGURE 2-26: *Gain-Bandwidth Product and Phase Margin vs. Ambient Temperature.*

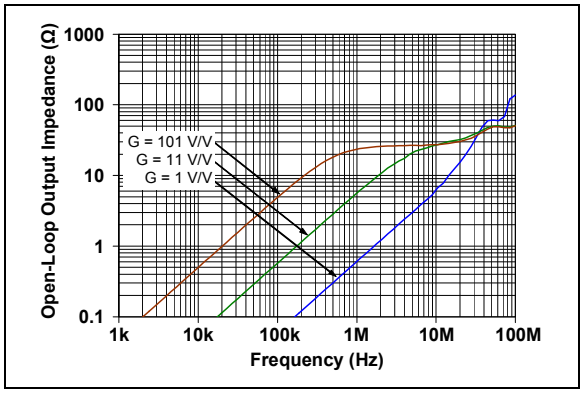


FIGURE 2-29: *Closed-Loop Output Impedance vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

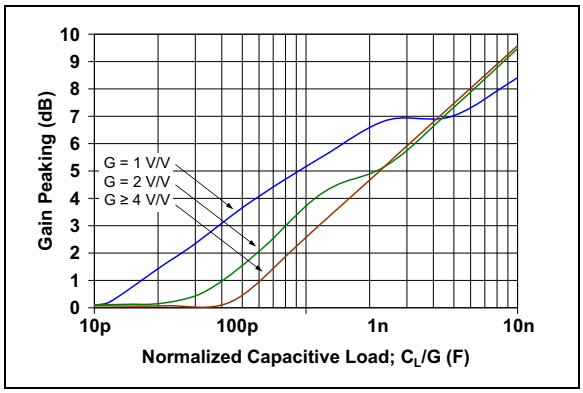


FIGURE 2-30: *Gain Peaking vs. Normalized Capacitive Load.*

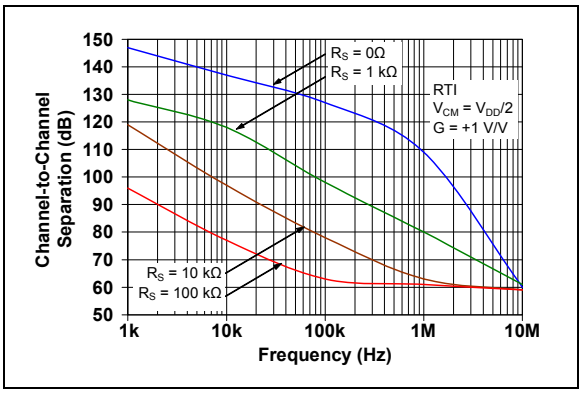


FIGURE 2-31: *Channel-to-Channel Separation vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.4 Input Noise and Distortion

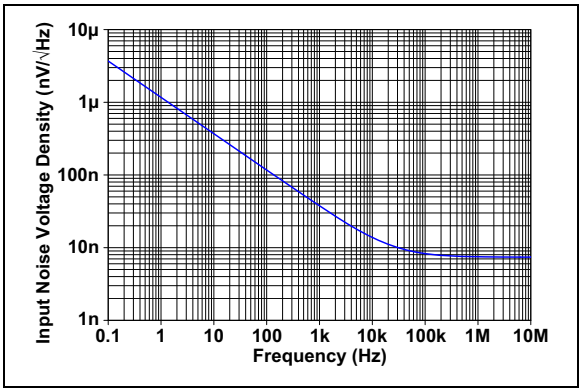


FIGURE 2-32: *Input Noise Voltage Density vs. Frequency.*

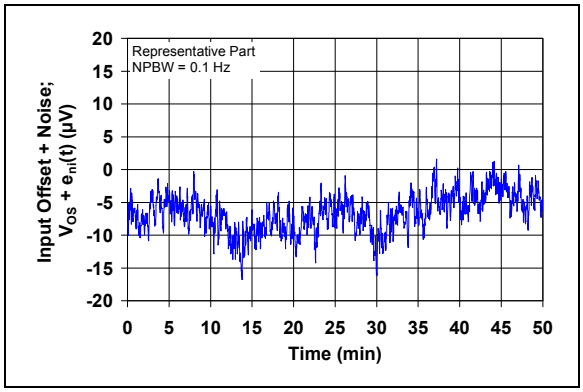


FIGURE 2-35: *Input Noise plus Offset vs. Time with 0.1 Hz Filter.*

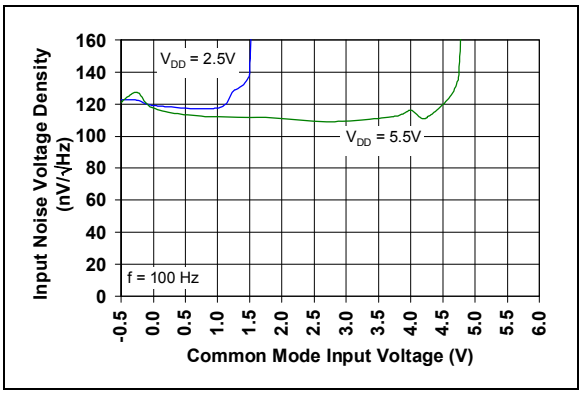


FIGURE 2-33: *Input Noise Voltage Density vs. Input Common Mode Voltage with f = 100 Hz.*

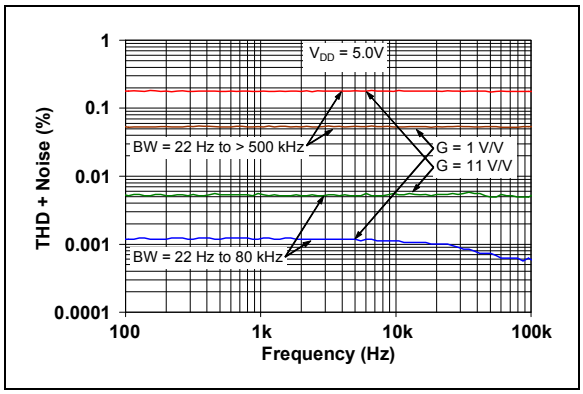


FIGURE 2-36: *THD+N vs. Frequency.*

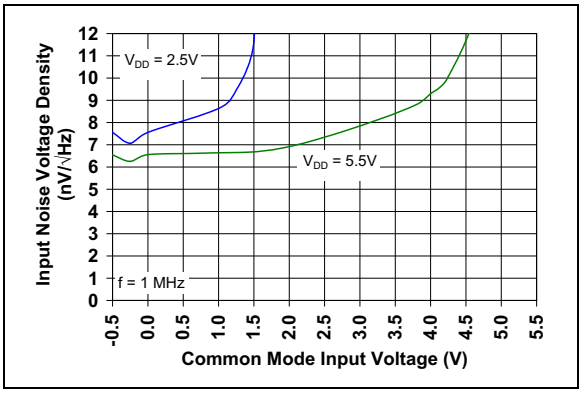


FIGURE 2-34: *Input Noise Voltage Density vs. Input Common Mode Voltage with f = 1 MHz.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.5 Time Response

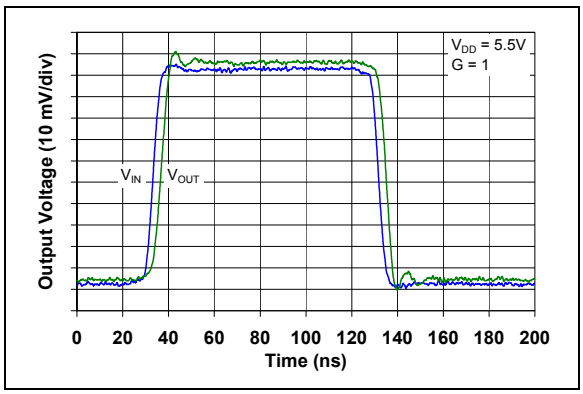


FIGURE 2-37: *Non-inverting Small Signal Step Response.*

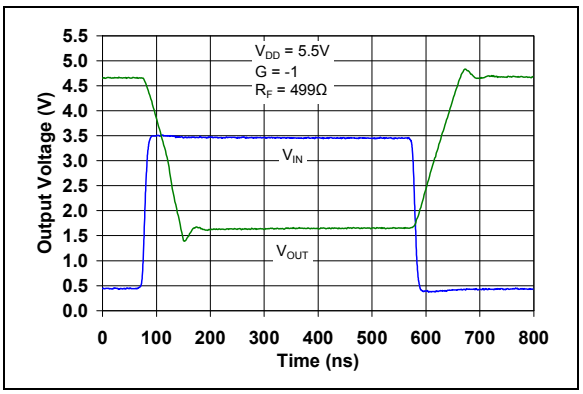


FIGURE 2-40: *Inverting Large Signal Step Response.*

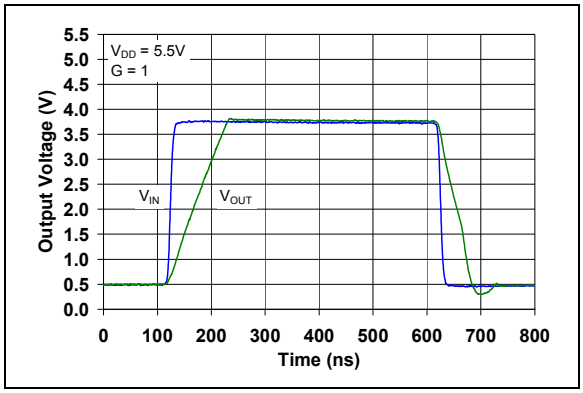


FIGURE 2-38: *Non-inverting Large Signal Step Response.*

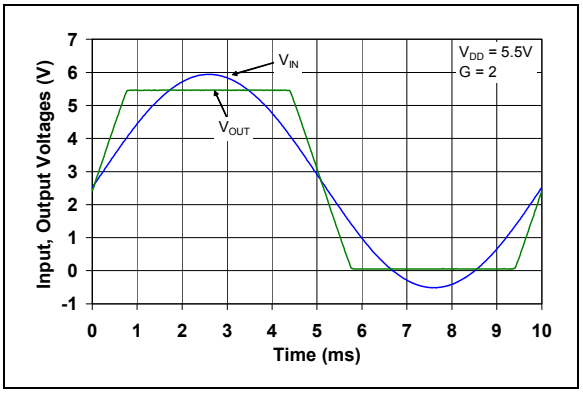


FIGURE 2-41: *The MCP651/1S/2/3/4/5/9 family shows no input phase reversal with overdrive.*

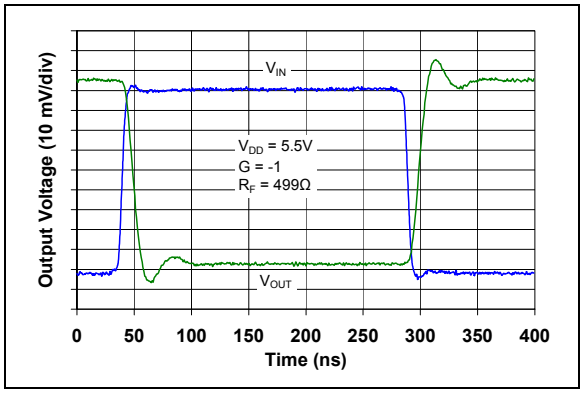


FIGURE 2-39: *Inverting Small Signal Step Response.*

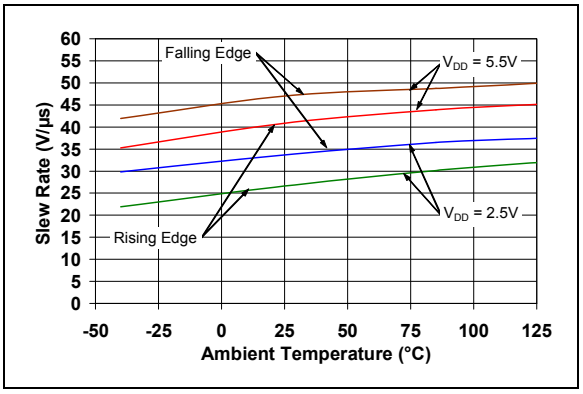


FIGURE 2-42: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

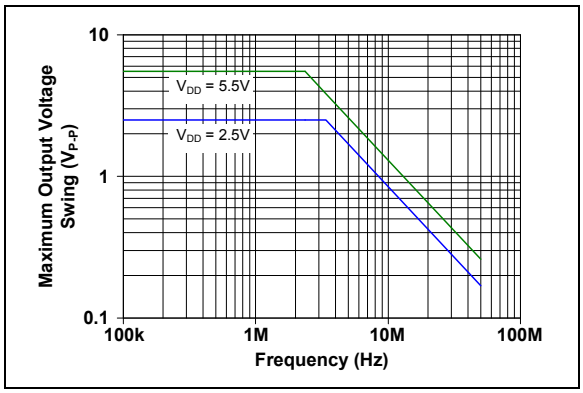


FIGURE 2-43: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

2.6 Calibration and Chip Select Response

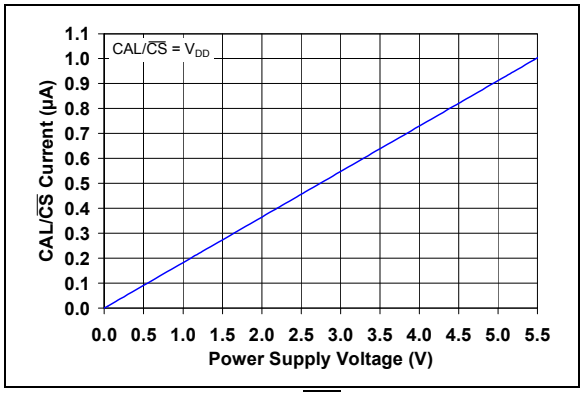


FIGURE 2-44: *CAL/$\overline{CS}$ Current vs. Power Supply Voltage.*

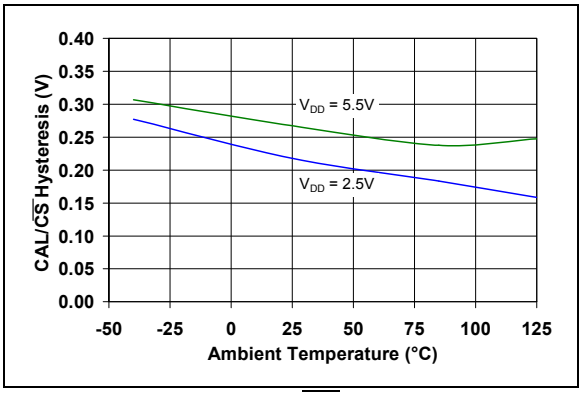


FIGURE 2-47: *CAL/$\overline{CS}$ Hysteresis vs. Ambient Temperature.*

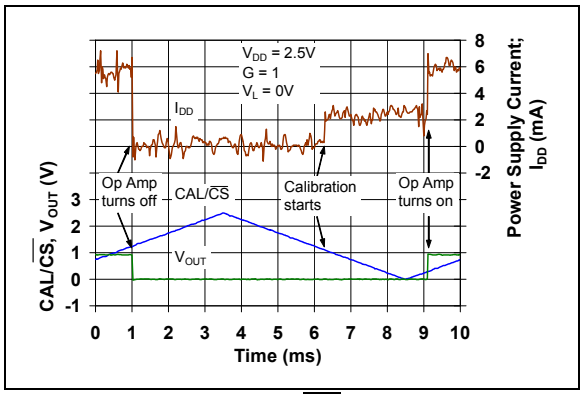


FIGURE 2-45: *CAL/$\overline{CS}$ Voltage, Output Voltage and Supply Current (for Side A) vs. Time with V_{DD} = 2.5V.*

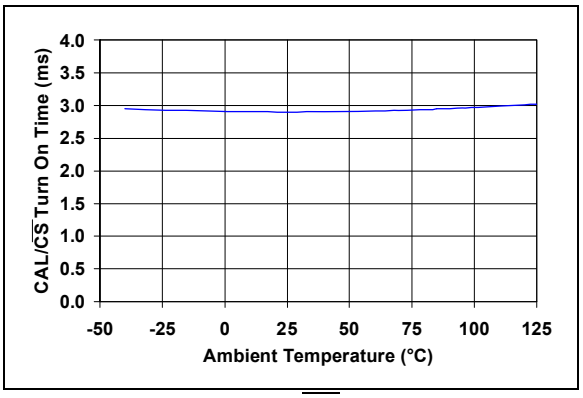


FIGURE 2-48: *CAL/$\overline{CS}$ Turn-On Time vs. Ambient Temperature.*

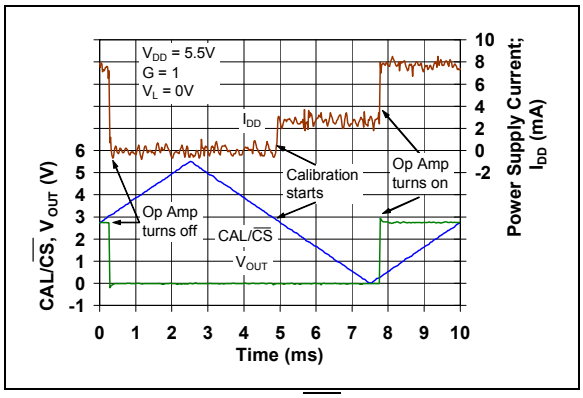


FIGURE 2-46: *CAL/$\overline{CS}$ Voltage, Output Voltage and Supply Current (for Side A) vs. Time with V_{DD} = 5.5V.*

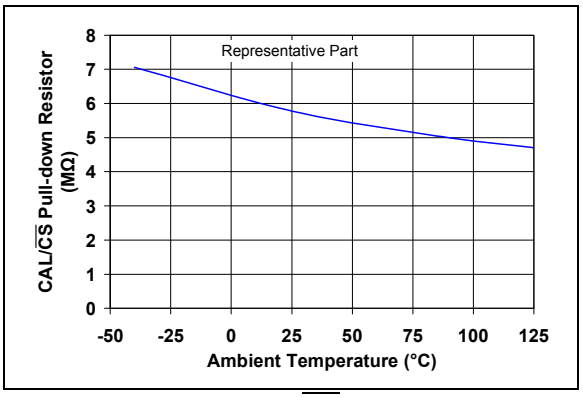


FIGURE 2-49: *CAL/$\overline{CS}$'s Pull-Down Resistor (R_{PD}) vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF, and CAL/$\overline{CS}$ = V_{SS}.

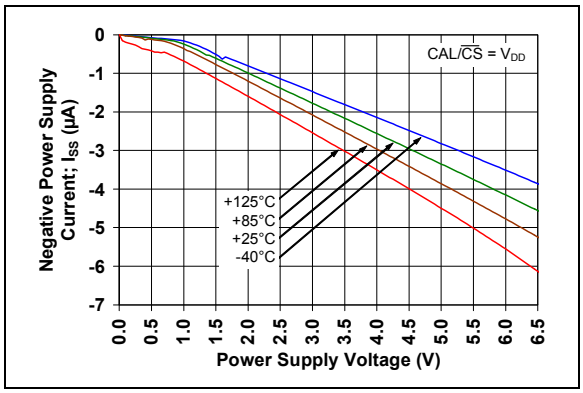


FIGURE 2-50: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

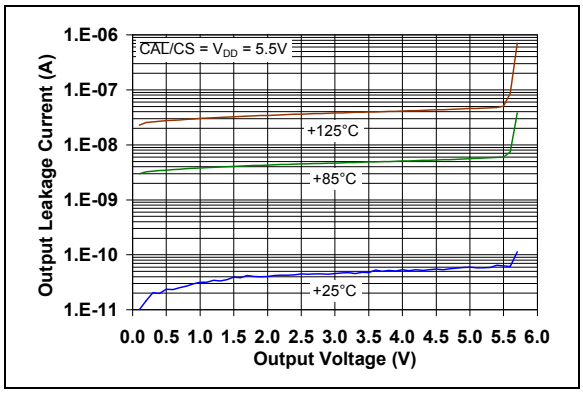


FIGURE 2-51: *Output Leakage Current vs. Output Voltage.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP651		MCP651S	MCP652		MCP653	MCP654		MCP655		MCP659	Symbol	Description
SOIC	TDFN	SOT	SOIC	DFN	SOT	SOIC	TSSOP	MSOP	DFN	QFN		
6	6	1	1	1	1	1	1	1	1	16	V_{OUT}, V_{OUTA}	Output (op amp A)
2	2	4	2	2	4	2	2	2	2	1	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	3	3	3	3	3	3	3	2	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
4	4	2	4	4	2	11	11	4	4	11	V_{SS}	Negative Power Supply
8	8	—	—	—	5	—	—	5	5	—	CAL/$\overline{CS}$, CAL$_A$/$\overline{CS_A}$	Calibrate/Chip Select Digital Input (op amp A)
—	—	—	—	—	—	—	—	6	6	—	CAL$_B$/$\overline{CS_B}$	Calibrate/Chip Select Digital Input (op amp B)
—	—	—	—	—	—	—	—	—	—	15	CALAD/ $\overline{CSAD}$	Calibrate/Chip Select Digital Input (op amps A and D)
—	—	—	—	—	—	—	—	—	—	7	CAL$_{BC}$/ $\overline{CSBC}$	Calibrate/Chip Select Digital Input (op amps B and C)
—	—	—	5	5	—	5	5	7	7	4	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	6	—	6	6	8	8	5	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	—	7	7	9	9	6	V_{OUTB}	Output (op amp B)
—	—	—	—	—	—	10	10	—	—	10	$V_{INC}+$	Non-inverting input (op amp C)
—	—	—	—	—	—	9	9	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	—	8	8	—	—	8	V_{OUTC}	Output (op amp C)
—	—	—	—	—	—	12	12	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	—	13	13	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	—	14	14	—	—	14	V_{OUTD}	Output (op amp D)
7	7	5	8	8	6	4	4	10	10	3	V_{DD}	Positive Power Supply
5	5	—	—	—	—	—	—	—	—	—	V_{CAL}	Calibration Common Mode Voltage Input
1	1	—	—	—	—	—	—	—	—	—	NC	No Internal Connection
—	9	—	—	9	—	—	—	—	11	17	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs ($V_{IN}+$, $V_{IN}–$, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.5V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Calibration Common Mode Voltage Input

A low-impedance voltage placed at this input (V_{CAL}) will set the op amps' Common mode input voltage during calibration. If this pin is left open, the Common mode input voltage during calibration is approximately $V_{DD}/3$. The internal resistor divider is disconnected from the supplies whenever the part is not in calibration.

3.5 Calibrate/Chip Select Digital Input

This input (CAL/$\overline{CS}$, …) is a CMOS, Schmitt-Triggered input that affects the Calibration and Low-Power modes of operation. When this pin goes high, the part is placed into a Low-Power mode and the output is High Z. When this pin goes low, a calibration sequence is started (which corrects V_{OS}). At the end of the calibration sequence, the output becomes low-impedance and the part resumes normal operation.

An internal POR triggers a calibration event when the part is powered on, or when the supply voltage drops too low. Thus, the MCP652 parts are calibrated, even though they do not have a CAL/$\overline{CS}$ pin.

3.6 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

4.0 APPLICATIONS

The MCP651/1S/2/3/4/5/9 family of self-zeroed op amps is manufactured using Microchip's state-of-the-art CMOS process. It is designed for low-cost, low-power and high-precision applications. Its low supply voltage, low quiescent current and wide bandwidth makes the MCP651/1S/2/3/4/5/9 ideal for battery-powered applications.

4.1 Calibration and Chip Select

These op amps include circuitry for dynamic calibration of the offset voltage (V_{OS}).

4.1.1 mCal CALIBRATION CIRCUITRY

The internal mCal circuitry, when activated, starts a delay timer (to wait for the op amp to settle to its new bias point), then calibrates the input offset voltage (V_{OS}). The mCal circuitry is triggered at power-up (and after some power brown-out events) by the internal POR, and by the memory's Parity Detector. The power-up time, when the mCal circuitry triggers the calibration sequence, is 200 ms (typical).

4.1.2 CAL/$\overline{CS}$ PIN

The CAL/$\overline{CS}$ pin gives the user a means to externally demand a Low-Power mode of operation, then to calibrate V_{OS}. Using the CAL/$\overline{CS}$ pin makes it possible to correct V_{OS} as it drifts over time (1/f noise and aging; see Figure 2-35) and across temperature.

The CAL/$\overline{CS}$ pin performs two functions: it places the op amp(s) in a Low-Power mode when it is held high, and starts a calibration event (correction of V_{OS}) after a rising edge.

While in the Low-Power mode, the quiescent current is quite small (I_{SS} = -3 µA, typical). The output is also in a High Z state.

During the calibration event, the quiescent current is near, but smaller than, the specified quiescent current (6 mA, typical). The output continues in the High Z state, and the inputs are disconnected from the external circuit, to prevent internal signals from affecting circuit operation. The op amp inputs are internally connected to a Common mode voltage buffer and feedback resistors. The offset is corrected (using a digital state machine, logic and memory), and the calibration constants are stored in memory.

Once the calibration event is completed, the amplifier is reconnected to the external circuitry. The turn-on time, when calibration is started with the CAL/$\overline{CS}$ pin, is 3 ms (typical).

There is an internal 5 MΩ pull-down resistor tied to the CAL/$\overline{CS}$ pin. If the CAL/$\overline{CS}$ pin is left floating, the amplifier operates normally.

For the MCP655 dual and the MCP659 quad, there is an additional constraint on toggling the two CAL/$\overline{CS}$ pins close together; see the t_{CON} specification in Table 1-3. If the two pins are toggled simultaneously, or if they are toggled separately with an adequate delay between them (greater than t_{CON}), then the CAL/$\overline{CS}$ inputs are accepted as valid. If one of the two pins toggles while the other pin's calibration routine is in progress, then an invalid input occurs and the result is unpredictable.

4.1.3 INTERNAL POR

This part includes an internal Power-On Reset (POR) to protect the internal calibration memory cells. The POR monitors the power supply voltage (V_{DD}). When the POR detects a low V_{DD} event, it places the part into the Low-Power mode of operation. When the POR detects a normal V_{DD} event, it starts a delay counter, then triggers an calibration event. The additional delay gives a total POR turn-on time of 200 ms (typical); this is also the power-up time (since the POR is triggered at power-up).

4.1.4 PARITY DETECTOR

A parity error detector monitors the memory contents for any corruption. In the rare event that a parity error is detected (e.g., corruption from an alpha particle), a POR event is automatically triggered. This will cause the input offset voltage to be re-corrected, and the op amp will not return to normal operation for a period of time (the POR turn-on time, t_{PON}).

4.1.5 CALIBRATION INPUT PIN

A V_{CAL} pin is available in some options (e.g., the single MCP651) for those applications that need the calibration to occur at an internally driven Common mode voltage other than $V_{DD}/3$.

Figure 4-1 shows the reference circuit that internally sets the op amp's Common mode reference voltage (V_{CM_INT}) during calibration (the resistors are disconnected from the supplies at other times). The 5 kΩ resistor provides over-current protection for the buffer.

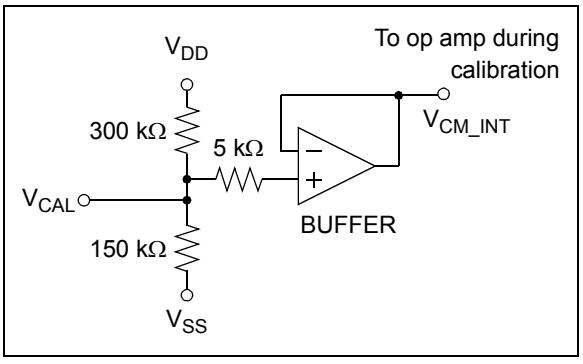


FIGURE 4-1: *Common-Mode Reference's Input Circuitry.*

When the V_{CAL} pin is left open, the internal resistor divider generates a V_{CM_INT} of approximately $V_{DD}/3$, which is near the center of the input Common mode voltage range. It is recommended that an external capacitor from V_{CAL} to ground be added to improve noise immunity.

When the V_{CAL} pin is driven by an external voltage source, which is within its specified range, the op amp will have its input offset voltage calibrated at that Common mode input voltage. Make sure that V_{CAL} is within its specified range.

It is possible to use an external resistor voltage divider to modify V_{CM_INT}; see Figure 4-2. The internal circuitry at the V_{CAL} pin looks like 100 kΩ tied to $V_{DD}/3$. The parallel equivalent of R_1 and R_2 should be much smaller than 100 kΩ to minimize differences in matching and temperature drift between the internal and external resistors. Again, make sure that V_{CAL} is within its specified range.

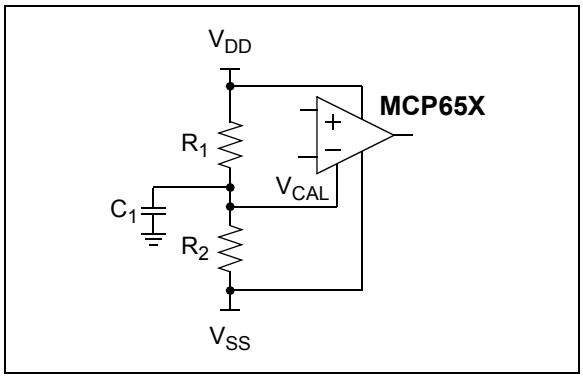


FIGURE 4-2: *Setting V_{CM} with External Resistors.*

For instance, a design goal to set V_{CM_INT} = 0.1V when V_{DD} = 2.5V could be met with: R_1 = 24.3 kΩ, R_2 = 1.00 kΩ and C_1 = 100 nF. This will keep V_{CAL} within its range for any V_{DD}, and should be close enough to 0V for ground-based applications.

4.2 Input

4.2.1 PHASE REVERSAL

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-41 shows an input voltage exceeding both supplies with no phase inversion.

4.2.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-3. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

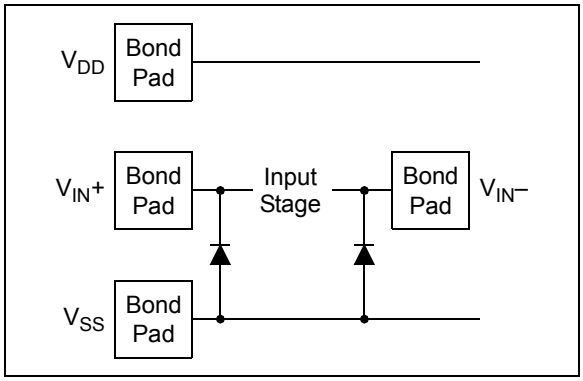


FIGURE 4-3: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). Figure 4-4 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}–) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

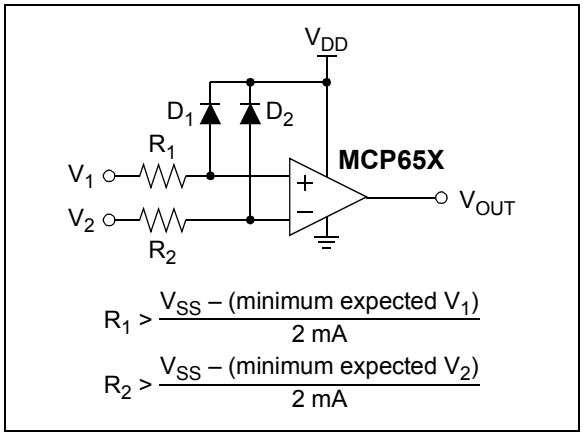


FIGURE 4-4: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the Common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-15. Applications that are high-impedance may need to limit the usable voltage range.

4.2.3 NORMAL OPERATION

The input stage of the MCP651/1S/2/3/4/5/9 op amps uses a differential PMOS input stage. It operates at low Common mode input voltage (V_{CM}), with V_{CM} up to V_{DD} – 1.3V and down to V_{SS} – 0.3V. The input offset voltage (V_{OS}) is measured at $V_{CM} = V_{SS} – 0.3V$ and V_{DD} – 1.3V to ensure proper operation. See Figure 2-6 and Figure 2-7 for temperature effects.

When operating at very low non-inverting gains, the output voltage is limited at the top by the V_{CM} range (< V_{DD} – 1.3V); see Figure 4-5.

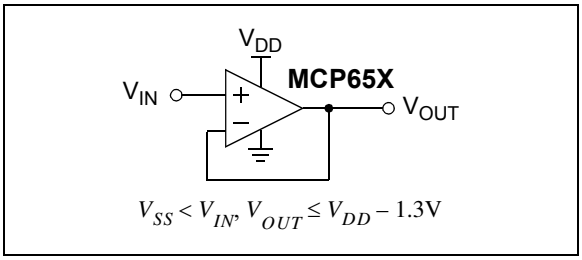


FIGURE 4-5: *Unity-Gain Voltage Limitations for Linear Operation.*

4.3 Rail-to-Rail Output

4.3.0.1 Maximum Output Voltage

The Maximum Output Voltage (see Figure 2-16 and Figure 2-17) describes the output range for a given load. For instance, the output voltage swings to within 15 mV of the negative rail with a 1 kΩ load tied to $V_{DD}/2$.

4.3.0.2 Output Current

Figure 4-6 shows the possible combinations of output voltage (V_{OUT}) and output current (I_{OUT}). I_{OUT} is positive when it flows out of the op amp into the external circuit.

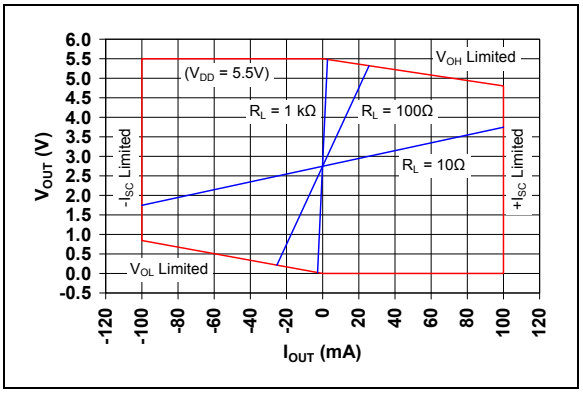


FIGURE 4-6: *Output Current.*

4.3.0.3 Power Dissipation

Since the output short circuit current (I_{SC}) is specified at ±100 mA (typical), these op amps are capable of both delivering and dissipating significant power. Two common loads, and their impact on the op amp's power dissipation, will be discussed.

Figure 4-7 shows a resistive load (R_L) with a DC output voltage (V_{OUT}). V_L is R_L's ground point, V_{SS} is usually ground (0V) and I_{OUT} is the output current. The input currents are assumed to be negligible.

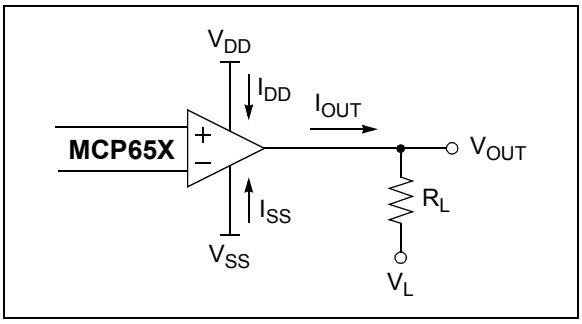


FIGURE 4-7: *Diagram for Resistive Load Power Calculations.*

The DC currents are:

EQUATION 4-1:

$$I_{OUT} = \frac{V_{OUT} - V_L}{R_L}$$
$$I_{DD} \approx I_Q + max(0, I_{OUT})$$
$$I_{SS} \approx -I_Q + min(0, I_{OUT})$$

Where:

I_Q = Quiescent supply current for one op amp (mA/amplifier)

V_{OUT} = A DC value (V)

The DC op amp power is:

EQUATION 4-2:

$$P_{OA} = I_{DD}(V_{DD} - V_{OUT}) + I_{SS}(V_{SS} - V_{OUT})$$

The maximum op amp power, for resistive loads at DC, occurs when V_{OUT} is halfway between V_{DD} and V_L or halfway between V_{SS} and V_L:

EQUATION 4-3:

$$max(P_{OA}) = I_{DD}(V_{DD} - V_{SS}) + \frac{max^2(V_{DD} - V_L, V_L - V_{SS})}{4R_L}$$

Figure 4-7 shows a capacitive load (C_L), which is driven by a sine wave with DC offset. The capacitive load causes the op amp to output higher currents at higher frequencies. Because the output rectifies I_{OUT}, the op amp's dissipated power increases (even though the capacitor does not dissipate power).

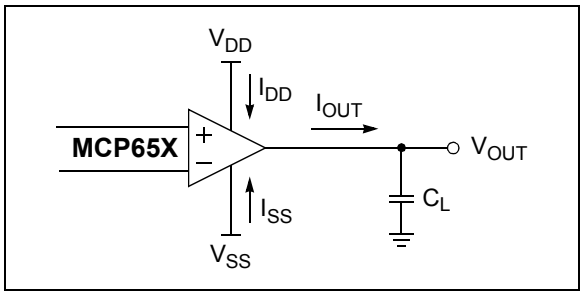


FIGURE 4-8: *Diagram for Capacitive Load Power Calculations.*

The output voltage is assumed to be:

EQUATION 4-4:

$$V_{OUT} = V_{DC} + V_{AC}sin(\omega t)$$

Where:

V_{DC} = DC offset (V)

V_{AC} = Peak output swing (V_{PK})

ω = Radian frequency ($2\pi f$) (rad/s)

The op amp's currents are:

EQUATION 4-5:

$$I_{OUT} = C_L \cdot \frac{dV_{OUT}}{dt} = V_{AC}\omega C_L cos(\omega t)$$
$$I_{DD} \approx I_Q + max(0, I_{OUT})$$
$$I_{SS} \approx -I_Q + min(0, I_{OUT})$$

Where:

I_Q = Quiescent supply current for one op amp (mA/amplifier)

The op amp's instantaneous power, average power and peak power are:

EQUATION 4-6:

$$P_{OA} = I_{DD}(V_{DD} - V_{OUT}) + I_{SS}(V_{SS} - V_{OUT})$$
$$ave(P_{OA}) = (V_{DD} - V_{SS})\left(I_Q + \frac{4V_{AC}fC_L}{\pi}\right)$$
$$max(P_{OA}) = (V_{DD} - V_{SS})(I_Q + 2V_{AC}fC_L)$$

The power dissipated in a package depends on the powers dissipated by each op amp in that package: