Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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MCP660/1/2/3/4/5/9

60 MHz, 32 V/µs Rail-to-Rail Output (RRO) Op Amps

Features:

- Gain-Bandwidth Product: 60 MHz (typical)
- Slew Rate: 32 V/µs (typical)
- Noise: 6.8 nV/√Hz (typical, at 1 MHz)
- Short Circuit Current: 90 mA (typical)
- Low Input Bias Current: 4 pA (typical)
- Ease of Use:
  - Unity-Gain Stable
  - Rail-to-Rail Output
  - Input Range including Negative Rail
  - No Phase Reversal
- Supply Voltage Range: +2.5V to +5.5V
- High Output Current: ±70 mA
- Supply Current: 6.0 mA/ch (typical)
- Low-Power Mode: 1 µA/ch
- Small Packages: SOT23-5, DFN
- Extended Temperature Range: -40°C to +125°C

Typical Applications:

- Multi-Pole Active Filter
- Driving A/D Converters
- Power Amplifier Control Loops
- Line Driver
- Video Amplifier
- Barcode Scanners
- Optical Detector Amplifier

Design Aids:

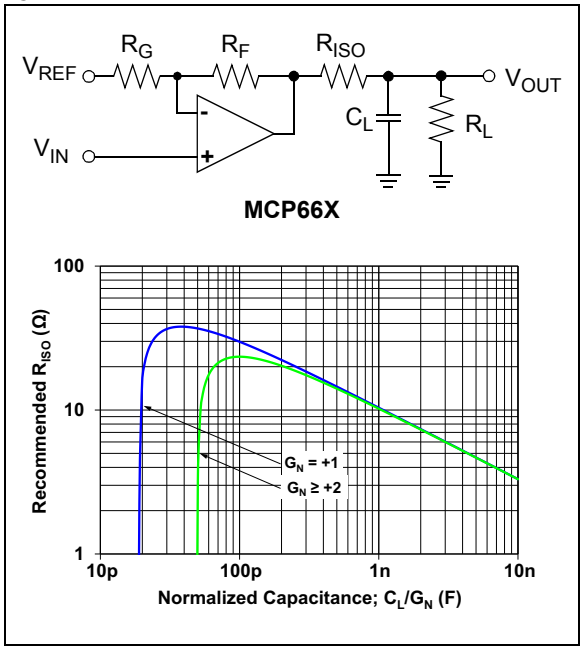
- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
  - MCP661DM-LD
- Application Notes

Description:

The Microchip Technology Inc. MCP660/1/2/3/4/5/9 family of operational amplifiers (op amps) features high gain-bandwidth product and high slew rate. Some also provide a Chip Select pin ($\overline{CS}$) that supports a low-power mode of operation. These amplifiers are optimized for high speed, low noise and distortion, single-supply operation with rail-to-rail output and an input that includes the negative rail.

This family is offered in single (MCP661), single with $\overline{CS}$ pin (MCP663), dual (MCP662) and dual with two $\overline{CS}$ pins (MCP665), triple (MCP660), quad (MCP664) and quad with two $\overline{CS}$ pins (MCP669). All devices are fully specified from -40°C to +125°C.

Typical Application Circuit

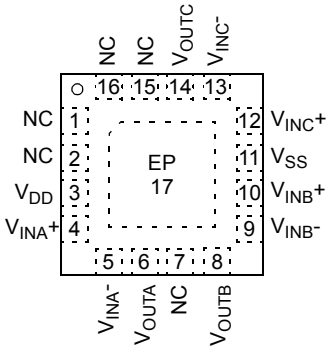


High Gain-Bandwidth Op Amp Portfolio

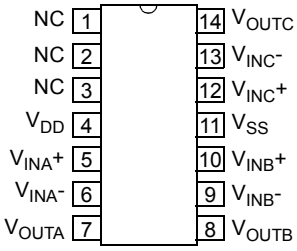
Model Family	Channels/Package	Gain-Bandwidth	V_{OS} (max.)	I_Q/Ch (typ.)
MCP621/1S/2/3/4/5/9	1, 2, 4	20 MHz	0.2 mV	2.5 mA
MCP631/2/3/4/5/9	1, 2, 4	24 MHz	8.0 mV	2.5 mA
MCP651/1S/2/3/4/5/9	1, 2, 4	50 MHz	0.2 mV	6.0 mA
MCP660/1/2/3/4/5/9	1, 2, 3, 4	60 MHz	8.0 mV	6.0 mA

Package Types

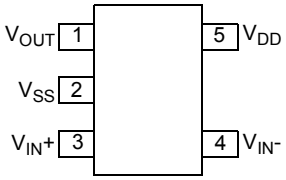
MCP660
4x4 QFN*



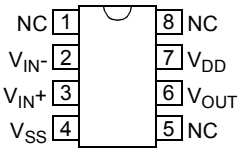
MCP660
SOIC, TSSOP



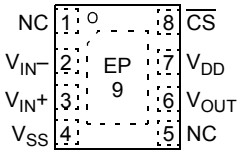
MCP661
SOT-23-5



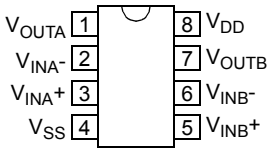
MCP661
SOIC



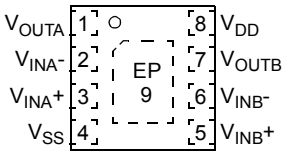
MCP661
2x3 TDFN*



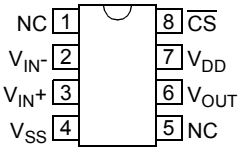
MCP662
MSOP, SOIC



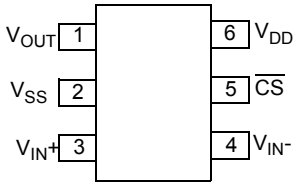
MCP662
3x3 DFN*



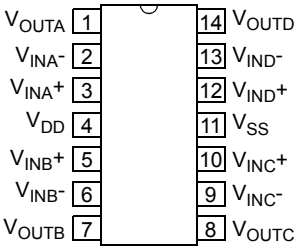
MCP663
SOIC



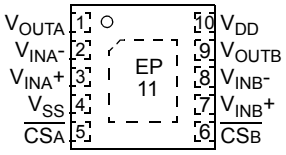
MCP663
SOT-23-6



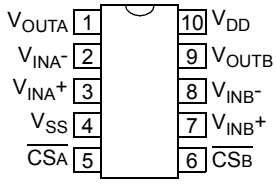
MCP664
SOIC, TSSOP



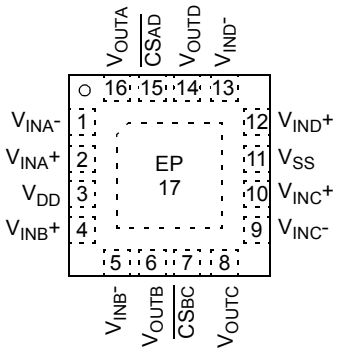
MCP665
3x3 DFN*



MCP665
MSOP



MCP669
4x4 QFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† . V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±150 mA
Storage Temperature .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
ESD protection on all pins (HBM, MM) .....≥ 1 kV, 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

1.2 Specifications

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, $V_{OUT} \approx V_{DD}/2$, V_L = V_{DD}/2, R_L = 1 kΩ to V_L and $\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-8	±1.8	+8	mV	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection Ratio	PSRR	61	76	—	dB	
Input Current and Impedance						
Input Bias Current	I_B	—	6	—	pA	
Across Temperature	I_B	—	130	—		T_A = +85°C
Across Temperature	I_B	—	1700	5000		T_A = +125°C
Input Offset Current	I_{OS}	—	±10	—	pA	
Common-Mode Input Impedance	Z_{CM}	—	10^{13}||9	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Common Mode						
Common-Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.3	V	**Note 1**
Common-Mode Rejection Ratio	CMRR	64	79	—	dB	V_{DD} = 2.5V, V_{CM} = -0.3V to 1.2V
		66	81	—	dB	V_{DD} = 5.5V, V_{CM} = -0.3V to 4.2V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	88	117	—	dB	V_{DD} = 2.5V, V_{OUT} = 0.3V to 2.2V
		94	126	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.3V to 5.2V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 2.5V, G = +2, 0.5V Input Overdrive
		V_{SS} + 50	—	V_{DD} – 50		V_{DD} = 5.5V, G = +2, 0.5V Input Overdrive
Output Short-Circuit Current	I_{SC}	±45	±90	±145	mA	V_{DD} = 2.5V **(Note 2)**
		±40	±80	±150		V_{DD} = 5.5V **(Note 2)**

Note 1: See Figure 2-5 for temperature effects.
2: The I_{SC} specifications are for design guidance only; they are not tested.

DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L and $\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	3	6	9	mA	No Load Current

Note 1: See Figure 2-5 for temperature effects.

2: The I_{SC} specifications are for design guidance only; they are not tested.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS} (refer to Figure 1-2).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain-Bandwidth Product	GBWP	—	60	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1
Open-Loop Output Impedance	R_{OUT}	—	10	—	Ω	
AC Distortion						
Total Harmonic Distortion plus Noise	THD + N	—	0.003	—	%	G = +1, V_{OUT} = $2V_{P-P}$, f = 1 kHz, V_{DD} = 5.5V, BW = 80 kHz
Differential Gain, Positive Video **(Note 1)**	DG	—	0.3	—	%	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to 0.7V
Differential Gain, Negative Video **(Note 1)**	DG	—	0.3	—	%	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to -0.7V
Differential Phase, Positive Video **(Note 1)**	DP	—	0.3	—	°	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to 0.7V
Differential Phase, Negative Video **(Note 1)**	DP	—	0.9	—	°	NTSC, V_{DD} = +2.5V, V_{SS} = -2.5V, G = +2, V_L = 0V, DC V_{IN} = 0V to -0.7V
Step Response						
Rise Time, 10% to 90%	t_r	—	5	—	ns	G = +1, V_{OUT} = 100 mV_{P-P}
Slew Rate	SR	—	32	—	V/µs	G = +1
Noise						
Input Noise Voltage	E_{ni}	—	14	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	6.8	—	nV/√Hz	f = 1 MHz
Input Noise Current Density	i_{ni}		4	—	fA/√Hz	f = 1 kHz

Note 1: These specifications are described in detail in **Section 4.3 "Distortion"**. (NTSC refers to a National Television Standards Committee signal.)

DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS} = V_{SS}$ (refer to Figures 1-1 and 2-1).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2V_{DD}$	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	-0.1	—	nA	$\overline{CS}$ = 0V
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	$0.8V_{DD}$	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	-0.7	—	µA	$\overline{CS} = V_{DD}$
GND Current	I_{SS}	-2	-1	—	µA	
$\overline{CS}$ Internal Pull-Down Resistor	R_{PD}	—	5	—	MΩ	
Amplifier Output Leakage	$I_{O(LEAK)}$	—	40	—	nA	$\overline{CS} = V_{DD}$, T_A = +125°C
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Input Hysteresis	V_{HYST}	—	0.25	—	V	
$\overline{CS}$ High to Amplifier Off Time (output goes High Z)	t_{OFF}	—	200	—	ns	G = +1 V/V, $V_L = V_{SS}$ $\overline{CS}$ = $0.8V_{DD}$ to $V_{OUT} = 0.1(V_{DD}/2)$
$\overline{CS}$ Low to Amplifier On Time	t_{ON}	—	2	10	µs	G = +1 V/V, $V_L = V_{SS}$ $\overline{CS}$ = $0.2V_{DD}$ to $V_{OUT} = 0.9(V_{DD}/2)$

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +2.5V to +5.5V, V_{SS} = GND.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	201.0	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	190.5	—	°C/W	
Thermal Resistance, 8L-3x3 DFN	θ_{JA}	—	56.7	—	°C/W	**Note 2**
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	52.5	—	°C/W	
Thermal Resistance, 10L-3x3 DFN	θ_{JA}	—	54.0	—	°C/W	**Note 2**
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	90.8	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-QFN	θ_{JA}	—	52.1	—	°C/W	

Note 1: Operation must not cause T_J to exceed the Maximum Junction Temperature specification (+150°C).

2: Measured on a standard JC51-7, four-layer printed circuit board with ground plane and vias.

1.3 Timing Diagram

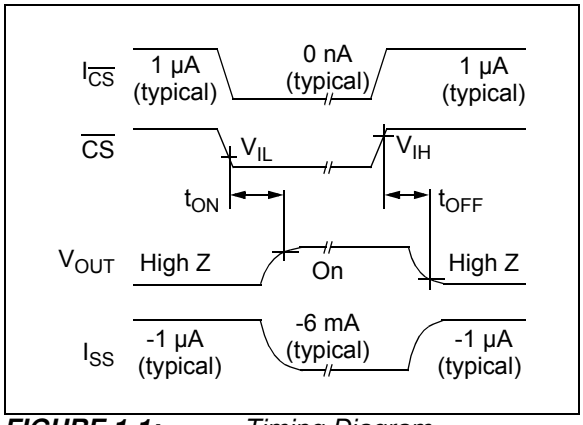


FIGURE 1-1: *Timing Diagram.*

1.4 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-2. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's common-mode voltage ((V_P + V_M)/2) and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = \frac{R_F}{R_G}$$

$$V_{CM} = \frac{V_P + \frac{V_{DD}}{2}}{2}$$

$$V_{OST} = V_{IN-} - V_{IN+}$$

$$V_{OUT} = \frac{V_{DD}}{2} + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common-Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

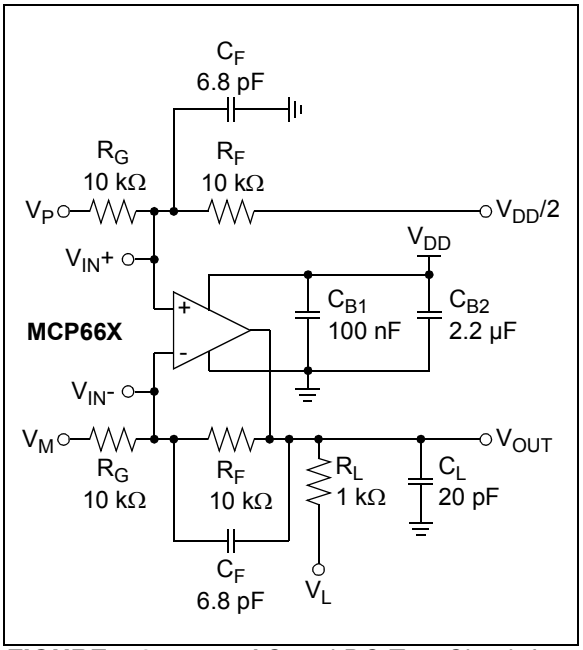


FIGURE 1-2: *AC and DC Test Circuit for Most Specifications.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.1 DC Signal Inputs

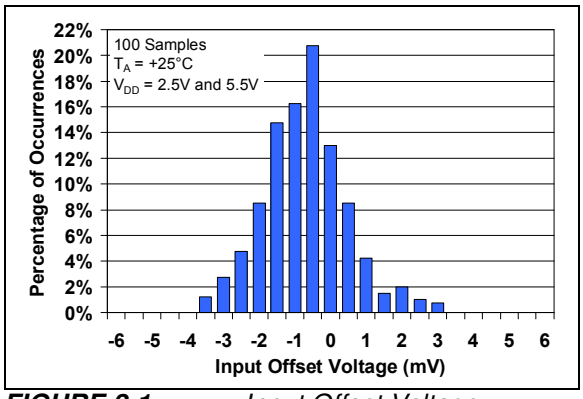


FIGURE 2-1: *Input Offset Voltage.*

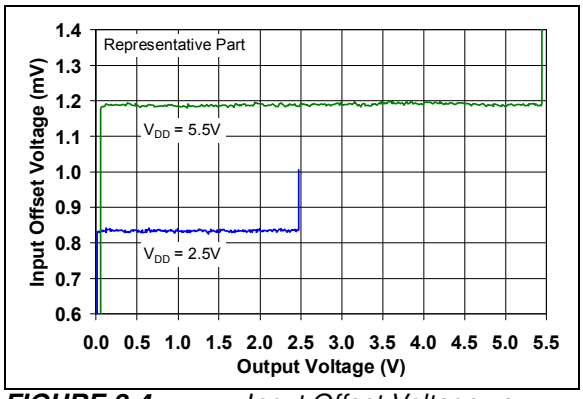


FIGURE 2-4: *Input Offset Voltage vs. Output Voltage.*

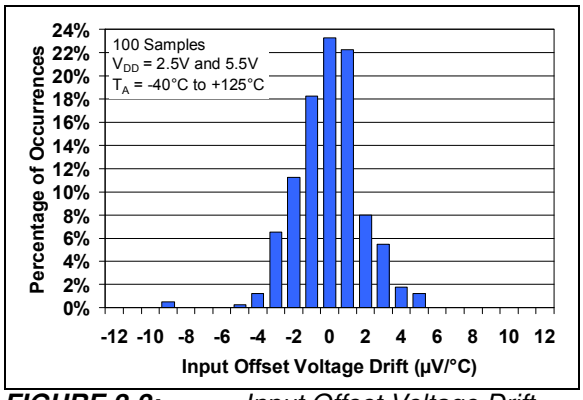


FIGURE 2-2: *Input Offset Voltage Drift.*

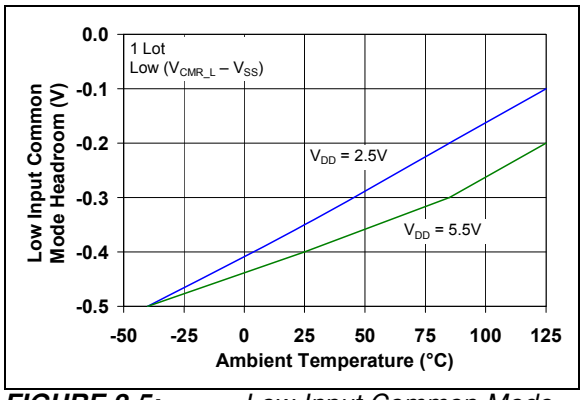


FIGURE 2-5: *Low-Input Common-Mode Voltage Headroom vs. Ambient Temperature.*

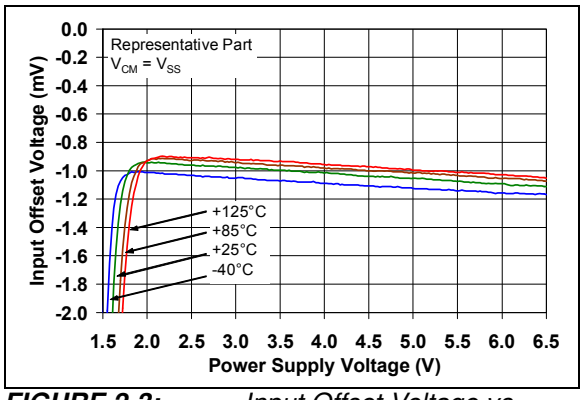


FIGURE 2-3: *Input Offset Voltage vs. Power Supply Voltage with V_{CM} = 0V.*

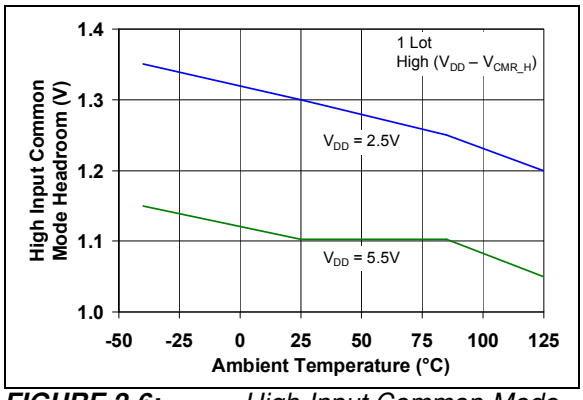


FIGURE 2-6: *High-Input Common-Mode Voltage Headroom vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

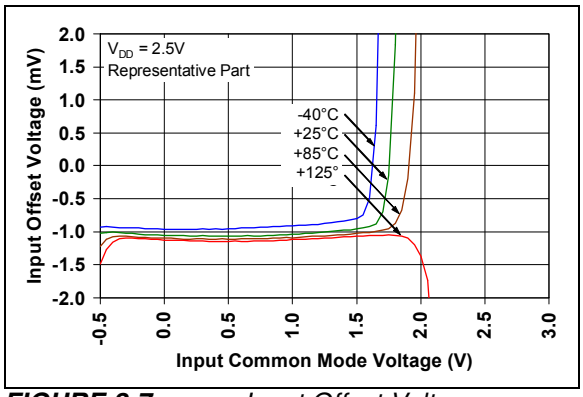


FIGURE 2-7: *Input Offset Voltage vs. Common-Mode Voltage with V_{DD} = 2.5V.*

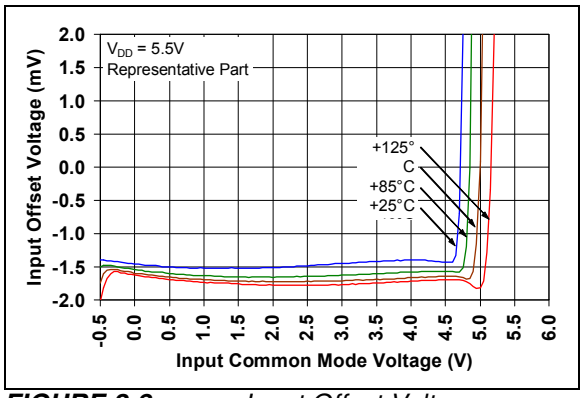


FIGURE 2-8: *Input Offset Voltage vs. Common-Mode Voltage with V_{DD} = 5.5V.*

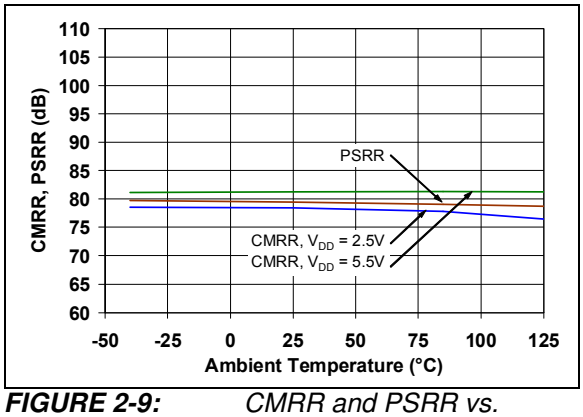


FIGURE 2-9: *CMRR and PSRR vs. Ambient Temperature.*

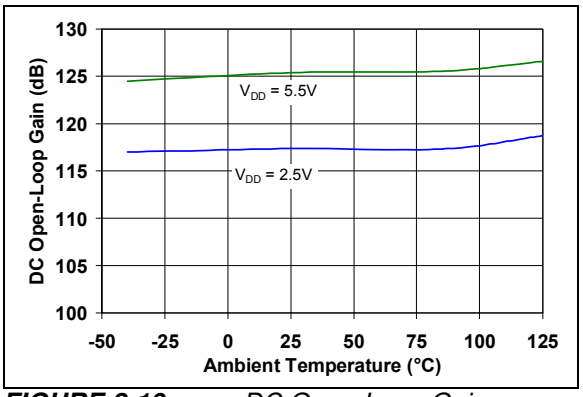


FIGURE 2-10: *DC Open-Loop Gain vs. Ambient Temperature.*

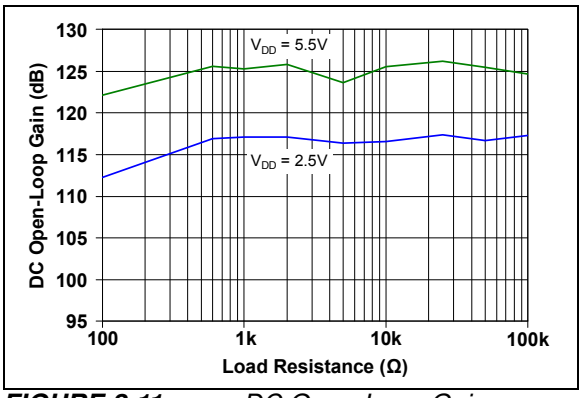


FIGURE 2-11: *DC Open-Loop Gain vs. Load Resistance.*

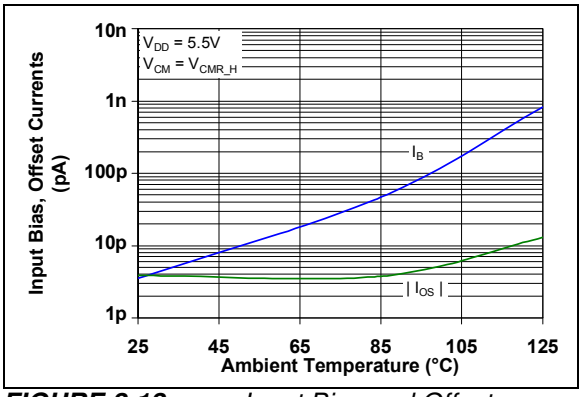


FIGURE 2-12: *Input Bias and Offset Currents vs. Ambient Temperature with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

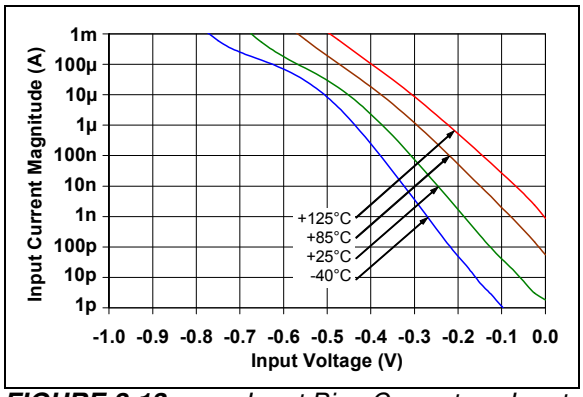


FIGURE 2-13: *Input Bias Current vs. Input Voltage (below V_{SS}).*

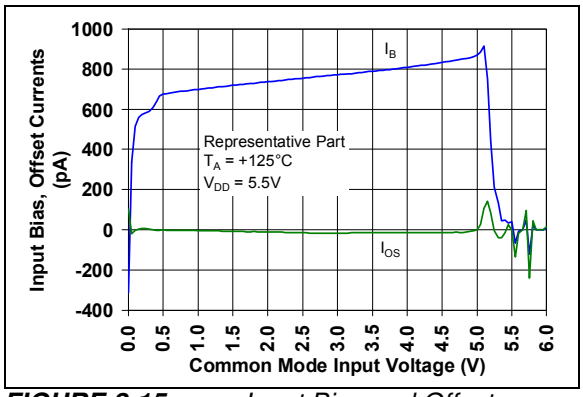


FIGURE 2-15: *Input Bias and Offset Currents vs. Common-Mode Input Voltage with T_A = +125°C.*

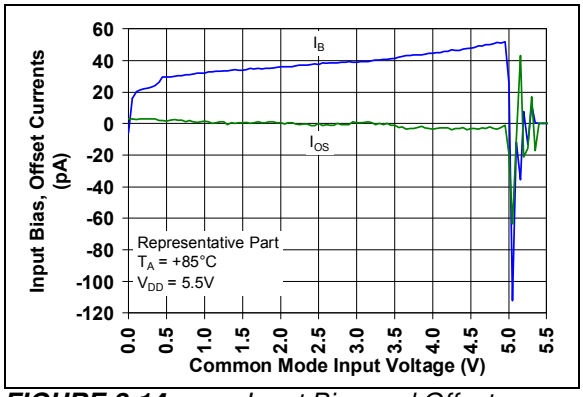


FIGURE 2-14: *Input Bias and Offset Currents vs. Common-Mode Input Voltage with T_A = +85°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.2 Other DC Voltages and Currents

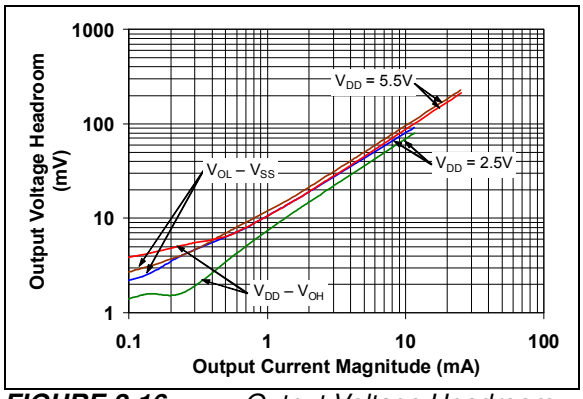


FIGURE 2-16: *Output Voltage Headroom vs. Output Current.*

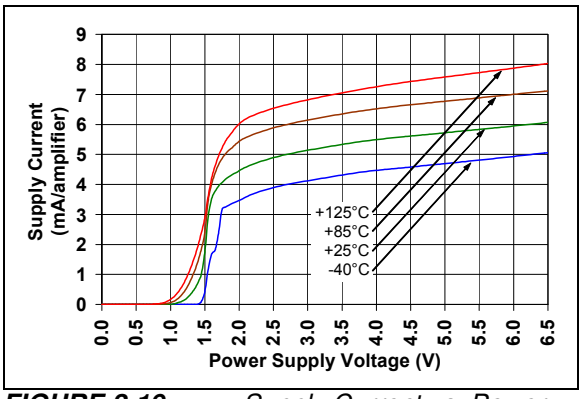


FIGURE 2-19: *Supply Current vs. Power Supply Voltage.*

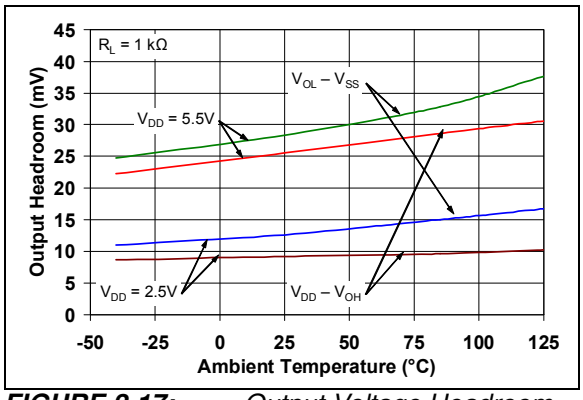


FIGURE 2-17: *Output Voltage Headroom vs. Ambient Temperature.*

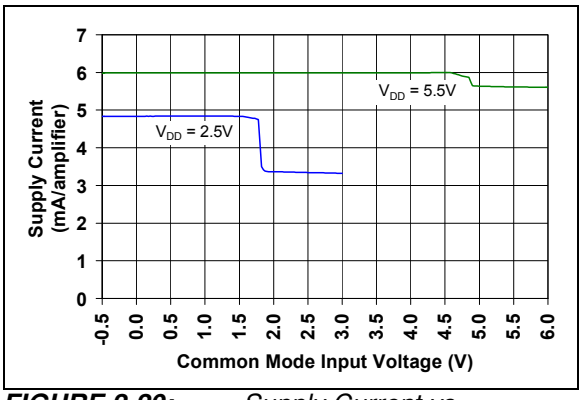


FIGURE 2-20: *Supply Current vs. Common-Mode Input Voltage.*

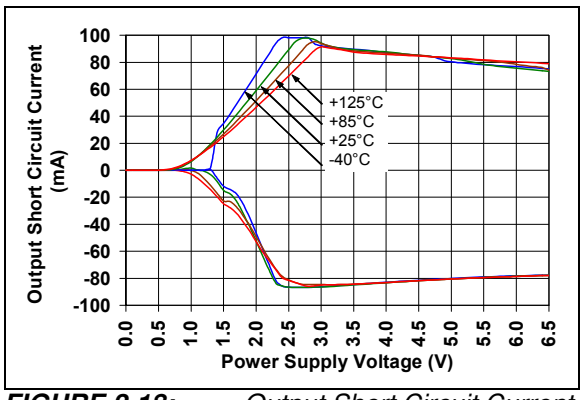


FIGURE 2-18: *Output Short Circuit Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.3 Frequency Response

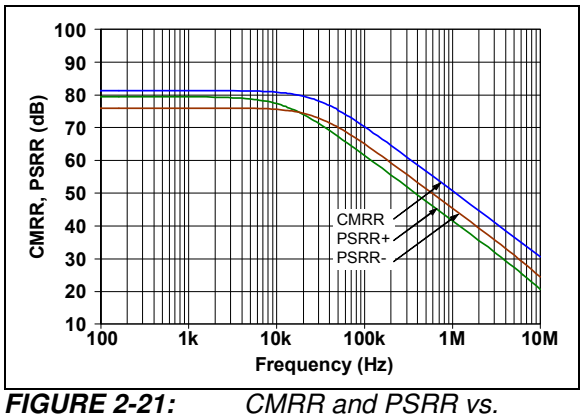


FIGURE 2-21: *CMRR and PSRR vs. Frequency.*

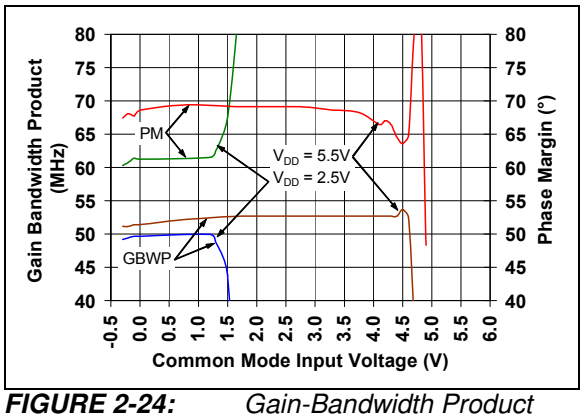


FIGURE 2-24: *Gain-Bandwidth Product and Phase Margin vs. Common-Mode Input Voltage.*

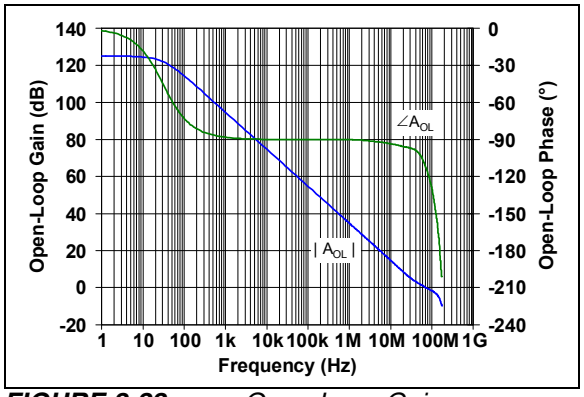


FIGURE 2-22: *Open-Loop Gain vs. Frequency.*

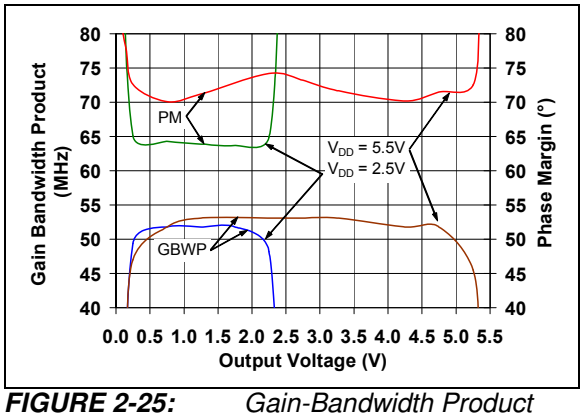


FIGURE 2-25: *Gain-Bandwidth Product and Phase Margin vs. Output Voltage.*

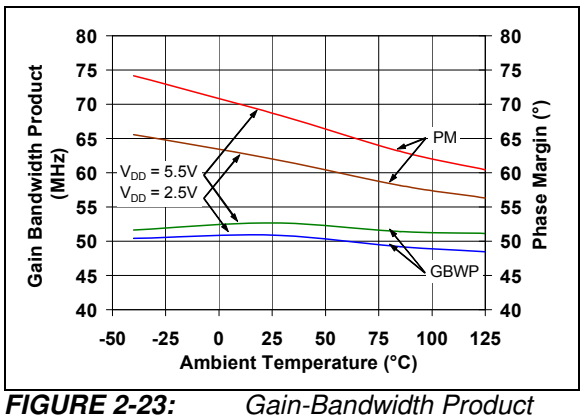


FIGURE 2-23: *Gain-Bandwidth Product and Phase Margin vs. Ambient Temperature.*

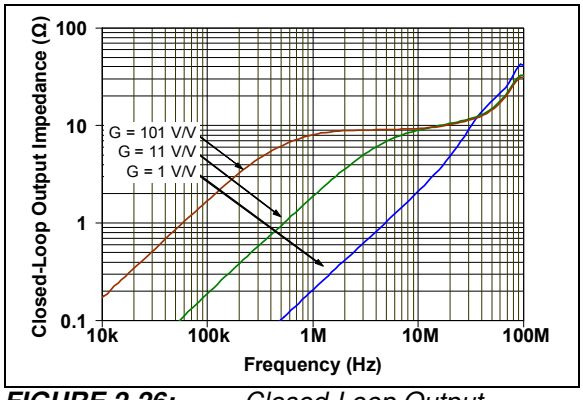


FIGURE 2-26: *Closed-Loop Output Impedance vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

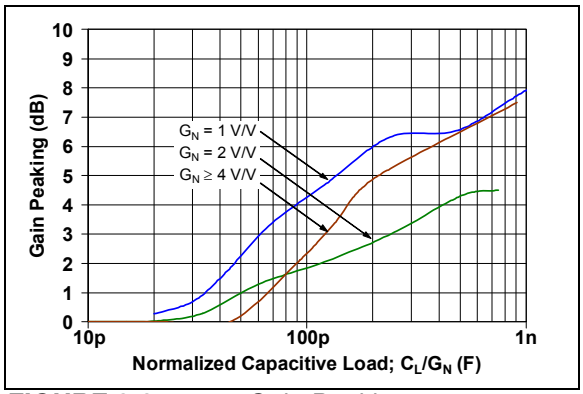


FIGURE 2-27: *Gain Peaking vs. Normalized Capacitive Load.*

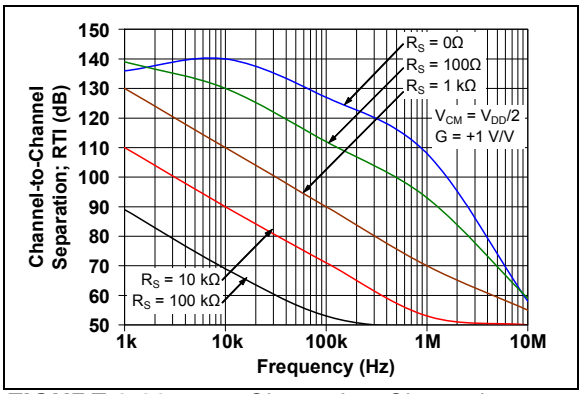


FIGURE 2-28: *Channel-to-Channel Separation vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.4 Noise and Distortion

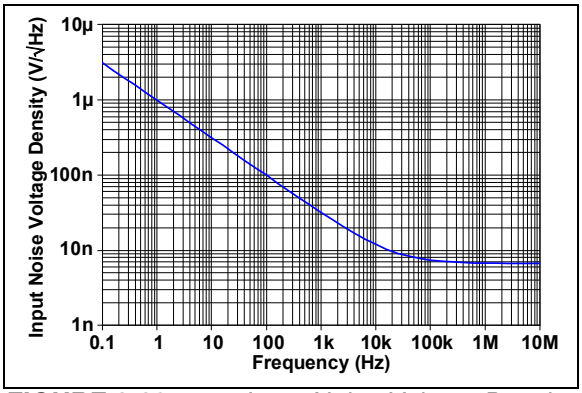


FIGURE 2-29: *Input Noise Voltage Density vs. Frequency.*

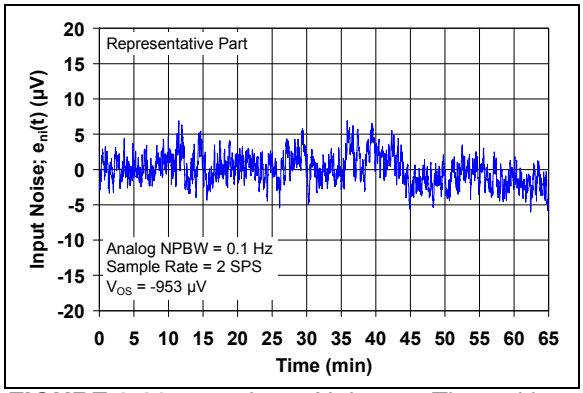


FIGURE 2-32: *Input Noise vs. Time with 0.1 Hz Filter.*

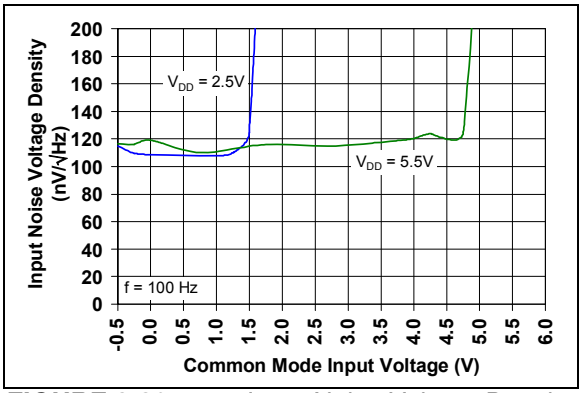


FIGURE 2-30: *Input Noise Voltage Density vs. Input Common-Mode Voltage with f = 100 Hz.*

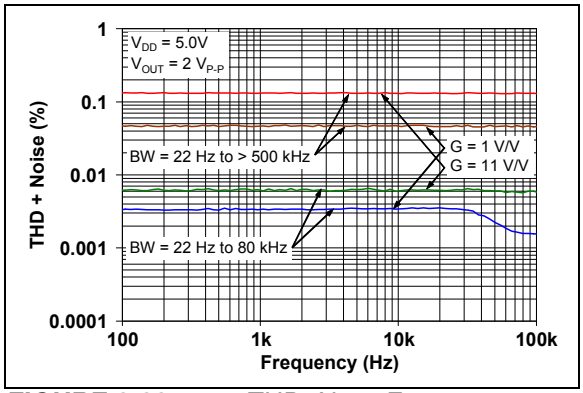


FIGURE 2-33: *THD+N vs. Frequency.*

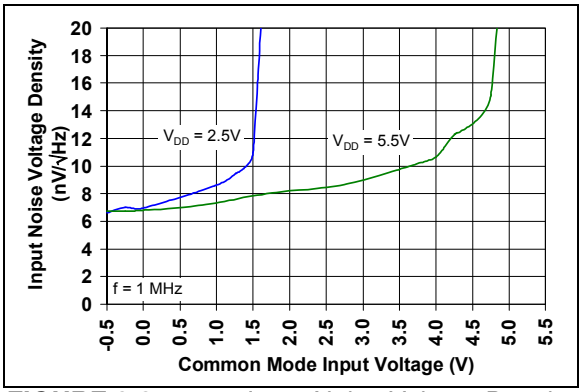


FIGURE 2-31: *Input Noise Voltage Density vs. Input Common-Mode Voltage with f = 1 MHz.*

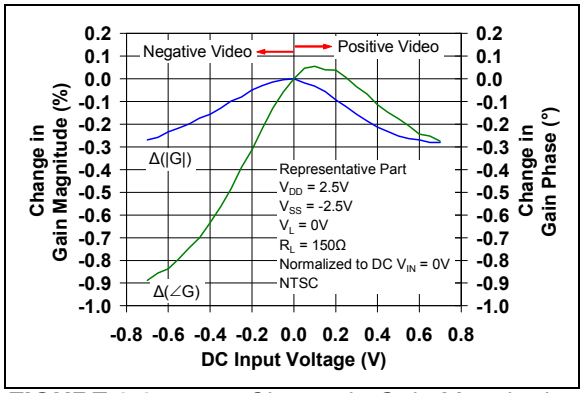


FIGURE 2-34: *Change in Gain Magnitude and Phase vs. DC Input Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.5 Time Response

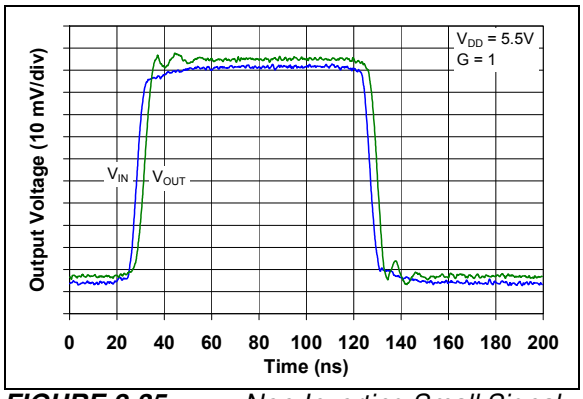


FIGURE 2-35: *Non-Inverting Small Signal Step Response.*

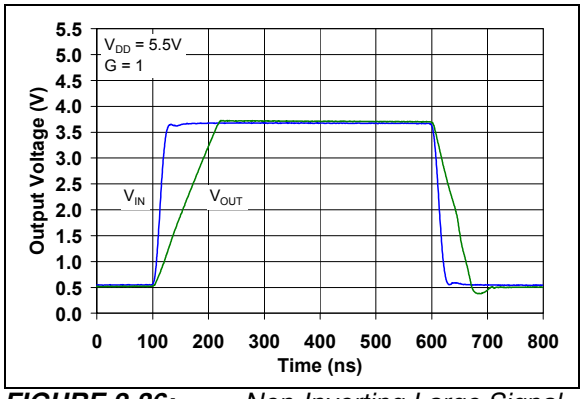


FIGURE 2-36: *Non-Inverting Large Signal Step Response.*

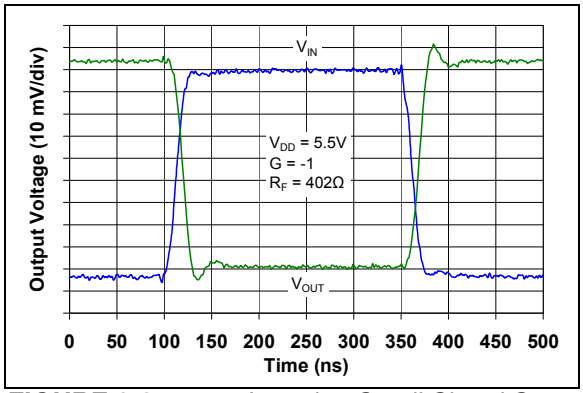


FIGURE 2-37: *Inverting Small Signal Step Response.*

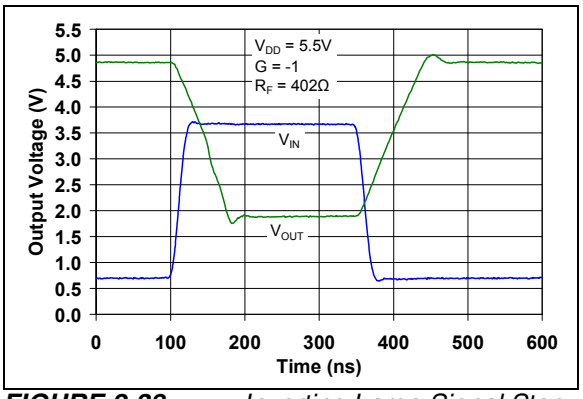


FIGURE 2-38: *Inverting Large Signal Step Response.*

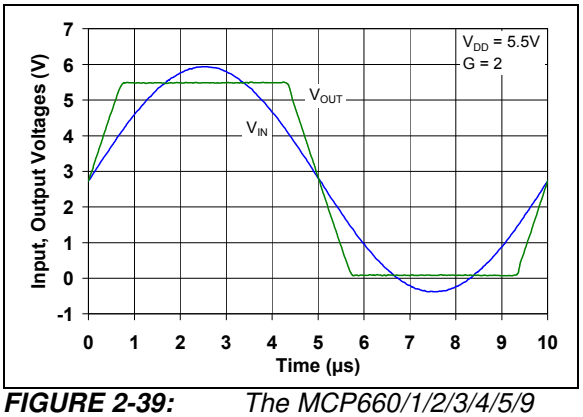


FIGURE 2-39: *The MCP660/1/2/3/4/5/9 Family Shows No Input Phase Reversal with Overdrive.*

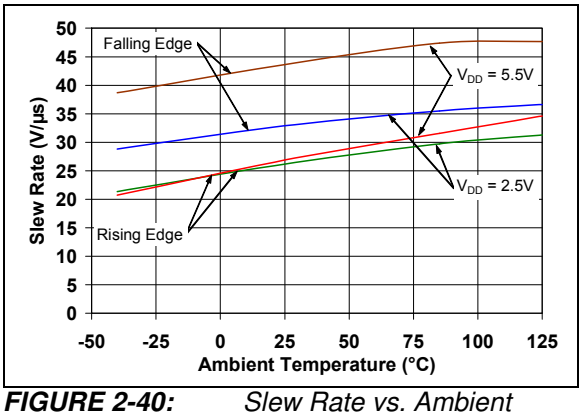


FIGURE 2-40: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

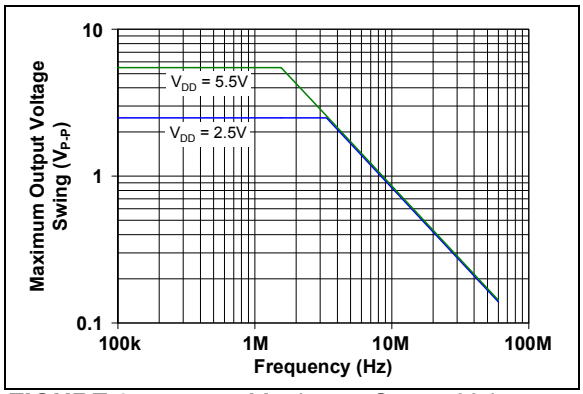


FIGURE 2-41: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

2.6 Chip Select Response

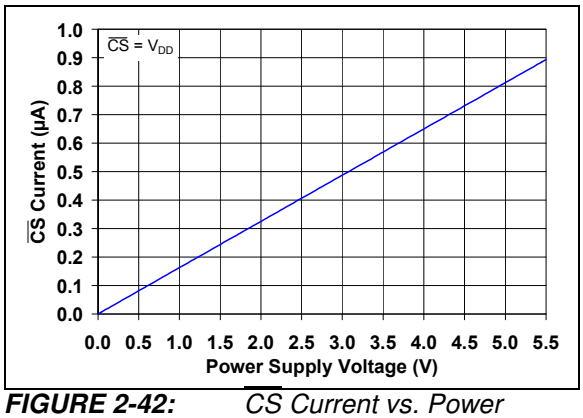


FIGURE 2-42: *$\overline{CS}$ Current vs. Power Supply Voltage.*

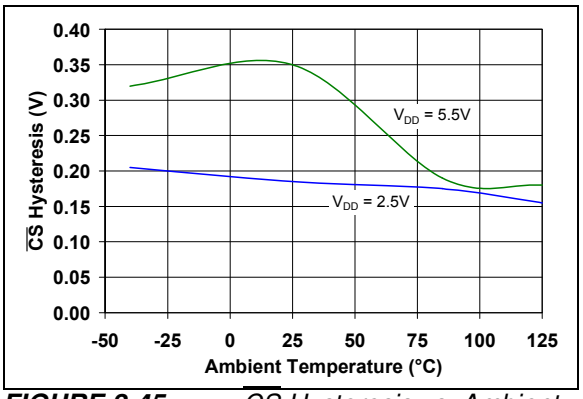


FIGURE 2-45: *$\overline{CS}$ Hysteresis vs. Ambient Temperature.*

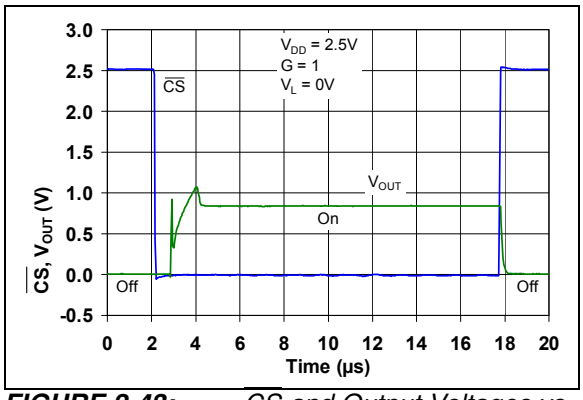


FIGURE 2-43: *$\overline{CS}$ and Output Voltages vs. Time with V_{DD} = 2.5V.*

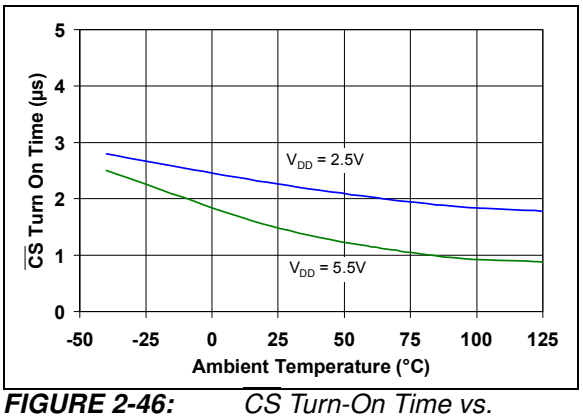


FIGURE 2-46: *$\overline{CS}$ Turn-On Time vs. Ambient Temperature.*

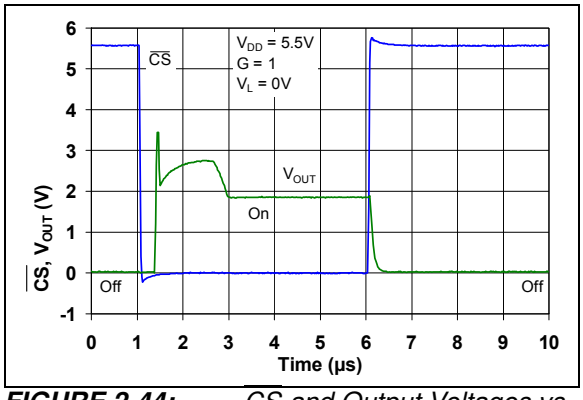


FIGURE 2-44: *$\overline{CS}$ and Output Voltages vs. Time with V_{DD} = 5.5V.*

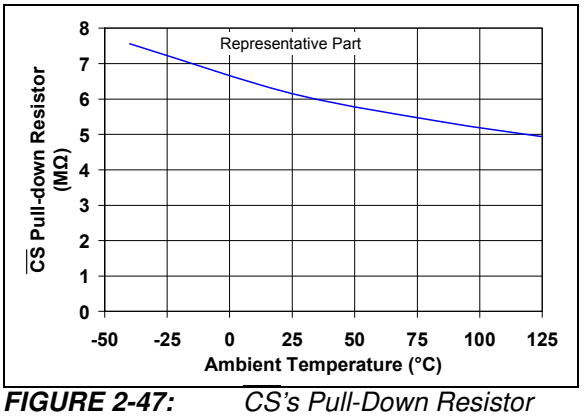


FIGURE 2-47: *$\overline{CS}$'s Pull-Down Resistor (R_{PD}) vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 kΩ to V_L, C_L = 20 pF and $\overline{CS}$ = V_{SS}.

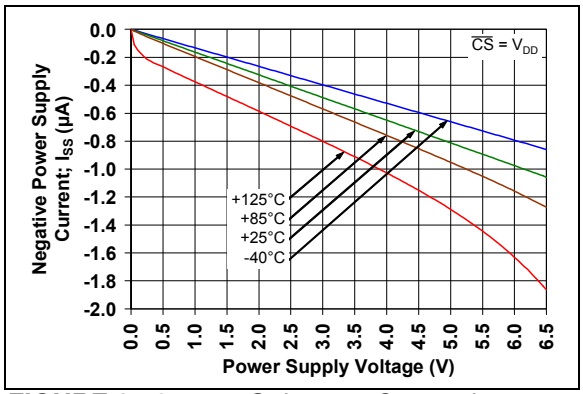


FIGURE 2-48: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

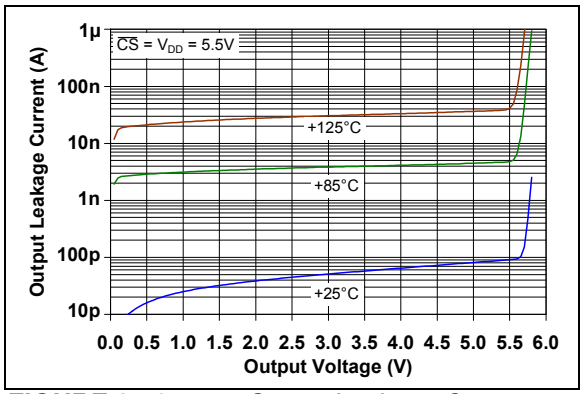


FIGURE 2-49: *Output Leakage Current vs. Output Voltage.*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP660		MCP661			MCP662		MCP663		MCP664	MCP665		MCP669	Symbol	Description
4x4 QFN	SOIC, TSSOP	SOIC	2x3 TDFN	SOT-23	MSOP, SOIC	DFN	SOIC	SOT-23	SOIC, TSSOP	MSOP	DFN	4x4 QFN		
5	6	2	2	4	2	2	2	4	2	2	2	1	V_{IN}-, V_{INA}-	Inverting Input (op amp A)
4	5	3	3	3	3	3	3	3	3	3	3	2	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
3	4	7	7	5	8	8	7	6	4	10	10	3	V_{DD}	Positive Power Supply
10	10	—	—	—	5	5	—	—	5	7	7	4	V_{INB}+	Non-inverting Input (op amp B)
9	9	—	—	—	6	6	—	—	6	8	8	5	V_{INB}-	Inverting Input (op amp B)
8	8	—	—	—	7	7	—	—	7	9	9	6	V_{OUTB}	Output (op amp B)
—	—	—	—	—	—	—	—	—	—	—	—	7	$\overline{CS_{BC}}$	Chip Select Digital Input (op amps B and C)
14	14	—	—	—	—	—	—	—	8	—	—	8	V_{OUTC}	Output (op amp C)
13	13	—	—	—	—	—	—	—	9	—	—	9	V_{INC}-	Inverting Input (op amp C)
12	12	—	—	—	—	—	—	—	10	—	—	10	V_{INC}+	Non-inverting Input (op amp C)
11	11	4	4	2	4	4	4	2	11	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	—	—	—	—	12	—	—	12	V_{IND}+	Inverting Input (op amp D)
—	—	—	—	—	—	—	—	—	13	—	—	13	V_{IND}-	Inverting Input (op amp D)
—	—	—	—	—	—	—	—	—	14	—	—	14	V_{OUTD}	Output (op amp D)
—	—	—	—	—	—	—	—	—	—	—	—	15	$\overline{CS_{AD}}$	Chip Select Digital Input (op amps A and D)
6	7	6	6	1	1	1	6	1	1	1	1	16	V_{OUT}, V_{OUTA}	Output (op amp A)
17	—	—	9	—	—	9	—	—	—	—	11	17	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}
—	—	—	8	—	—	—	8	5	—	5	5	—	$\overline{CS}$, $\overline{CS_A}$	Chip Select Digital Input (op amp A)
—	—	—	—	—	—	—	—	—	—	6	6	—	$\overline{CS_B}$	Chip Select Digital Input (op amp B)
1, 2, 7, 15, 16	1, 2, 3	1, 5, 8	1, 5	—	—	—	1, 5	—	—	—	—	—	NC	No Internal Connection

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs ($V_{IN}+$, $V_{IN}-$, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.5V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In that case, V_{SS} is connected to Ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Chip Select Digital Input ($\overline{CS}$)

The input ($\overline{CS}$) is a CMOS, Schmitt-triggered input that places the part into a low-power mode of operation.

3.5 Exposed Thermal Pad (EP)

There is an internal connection between the exposed thermal pad (EP) and the V_{SS} pin; they must be connected to the same potential on the printed circuit board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

4.0 APPLICATIONS

The MCP660/1/2/3/4/5/9 family is manufactured using the Microchip state-of-the-art CMOS process. It is designed for low-cost, low-power and high-speed applications. Its low supply voltage, low quiescent current and wide bandwidth make the MCP660/1/2/3/4/5/9 ideal for battery-powered applications.

4.1 Input

4.1.1 PHASE REVERSAL

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-39 shows an input voltage exceeding both supplies with no phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The electrostatic discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation and low enough to bypass quick ESD events within the specified limits.

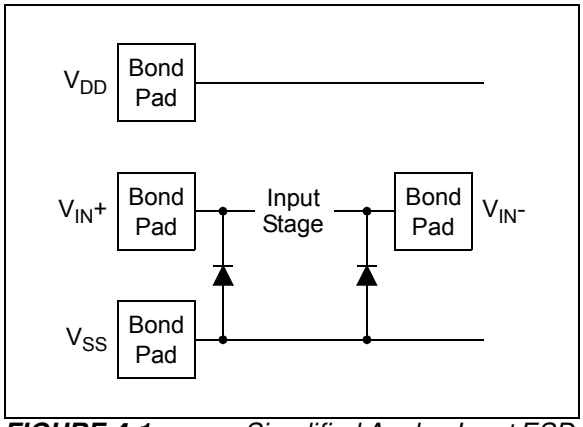


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). Figure 4-2 shows the recommended approach to protecting these inputs.

The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, while the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}-) from going too far above V_{DD} and dump any currents onto V_{DD}.

When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

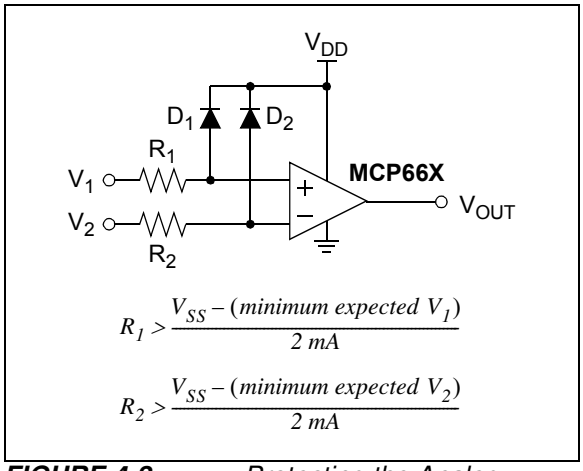


FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors R_1 and R_2. If so, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}-) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common-mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-13. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP660/1/2/3/4/5/9 op amps uses a differential PMOS input stage. It operates at low common-mode input voltages (V_{CM}), with V_{CM} between V_{SS} – 0.3V and V_{DD} – 1.3V. To ensure proper operation, the input offset voltage (V_{OS}) is measured at both $V_{CM} = V_{SS} – 0.3V$ and $V_{CM} = V_{DD} – 1.3V$. See Figures 2-5 and 2-6 for temperature effects.

When operating at very low non-inverting gains, the output voltage is limited at the top by the V_{CM} range ($< V_{DD} – 1.3V$); see Figure 4-3.

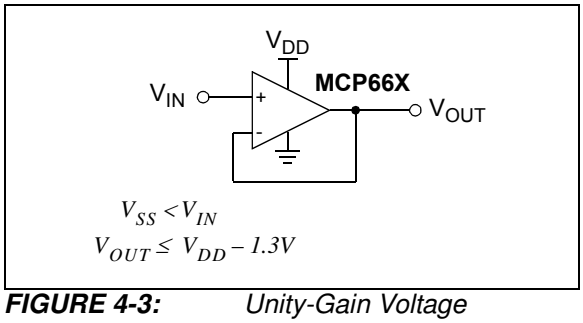


FIGURE 4-3: *Unity-Gain Voltage Limitations for Linear Operation.*

4.2 Rail-to-Rail Output

4.2.1 MAXIMUM OUTPUT VOLTAGE

The Maximum Output Voltage (see Figures 2-16 and 2-17) describes the output range for a given load. For example, the output voltage swings to within 50 mV of the negative rail with a 1 kΩ load tied to $V_{DD}/2$.

4.2.2 OUTPUT CURRENT

Figure 4-4 shows the possible combinations of output voltage (V_{OUT}) and output current (I_{OUT}), when V_{DD} = 5.5V.

I_{OUT} is positive when it flows out of the op amp into the external circuit.

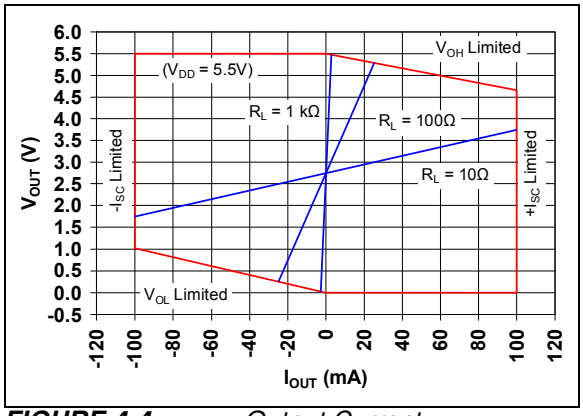


FIGURE 4-4: *Output Current.*

4.2.3 POWER DISSIPATION

Since the output short circuit current (I_{SC}) is specified at ±90 mA (typical), these op amps are capable of both delivering and dissipating significant power.

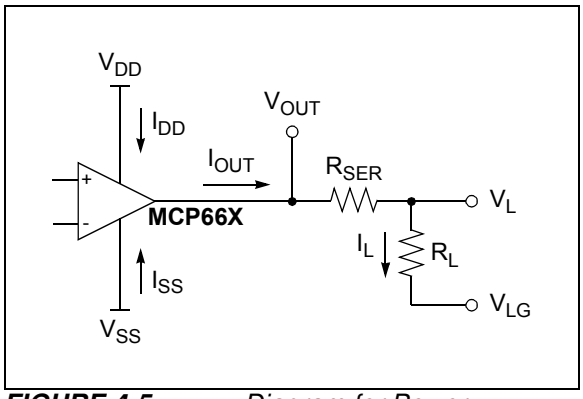


FIGURE 4-5: *Diagram for Power Calculations.*

Figure 4-5 shows the power calculations used for a single op amp:

- R_{SER} is 0Ω in most applications and can be used to limit I_{OUT}.
- V_{OUT} is the op amp's output voltage.
- V_L is the voltage at the load.
- V_{LG} is the load's ground point.
- V_{SS} is usually ground (0V).

The input currents are assumed to be negligible. The currents shown in Figure 4-5 can be approximated using Equation 4-1:

EQUATION 4-1:

$$I_{OUT} = I_L = \frac{V_{OUT} - V_{LG}}{R_{SER} + R_L}$$

$$I_{DD} \approx I_Q + max(0,\ I_{OUT})$$

$$I_{SS} \approx -I_Q + min(0,\ I_{OUT})$$

Where:

I_Q = Quiescent supply current

The instantaneous op amp power ($P_{OA}(t)$), R_{SER} power ($P_{RSER}(t)$) and load power ($P_L(t)$) are calculated in Equation 4-2:

EQUATION 4-2:

$$P_{OA}(t) = I_{DD}\,(V_{DD} - V_{OUT}) + I_{SS}\,(V_{SS} - V_{OUT})$$

$$P_{RSER}(t) = I_{OUT}{}^2 R_{SER}$$

$$P_L(t) = I_L{}^2 R_L$$

The maximum op amp power, for resistive loads, occurs when V_{OUT} is halfway between V_{DD} and V_{LG} or halfway between V_{SS} and V_{LG}.

EQUATION 4-3:

$$P_{OAmax} \le \frac{max^2(V_{DD} - V_{LG} - V_{SS})}{4(R_{SER} + R_L)}$$

The maximum ambient to junction temperature rise (ΔT_{JA}) and junction temperature (T_J) can be calculated using P_{OAmax}, the ambient temperature (T_A), the package thermal resistance (θ_{JA}, found in the Temperature Specifications table) and the number of op amps in the package (assuming equal power dissipations), as shown in Equation 4-4:

EQUATION 4-4:

$$\Delta T_{JA} = P_{OA}(t)\,\theta_{JA} \le nP_{OAmax}\,\theta_{JA}$$

$$T_J = T_A + \Delta T_{JA}$$

Where:

n = Number of op amps in the package (1, 2)

The power derating across temperature for an op amp in a particular package can be easily calculated (assuming equal power dissipations):

EQUATION 4-5:

$$P_{OAmax} \leq \frac{T_{Jmax} - T_A}{n\,\theta_{JA}}$$

Where:

T_{Jmax} = Absolute maximum junction temperature

Several techniques are available to reduce ΔT_{JA} for a given P_{OAmax}:

- Lower θ_{JA}
  - Use another package
  - PCB layout (ground plane, etc.)
  - Heat sinks and air flow
- Reduce P_{OAmax}
  - Increase R_L
  - Limit I_{OUT} (using R_{SER})
  - Decrease V_{DD}

4.3 Distortion

Differential gain (DG) and differential phase (DP) refer to the nonlinear distortion produced by an NTSC or a phase-alternating line (PAL) video component. The AC Electrical Specifications table and Figure 2-34 show the typical performance of the MCP661, configured as a gain of +2 amplifier (see Figure 4-10), when driving one back-matched video load (150Ω, for 75Ω cable). Microchip tests use a sine wave at NTSC's color sub-carrier frequency of 3.58 MHz, with a $0.286V_{P-P}$ magnitude. The DC input voltage is changed over a +0.7V range (positive video) or a -0.7V range (negative video).

DG is the peak-to-peak change in the AC gain magnitude (color hue), as the DC level (luminance) is changed, in percentile units (%). DP is the peak-to-peak change in the AC gain phase (color saturation), as the DC level (luminance) is changed, in degree (°) units.

4.4 Improving Stability

4.4.1 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the phase margin (stability) of the feedback loop decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 20 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-6) improves the phase margin of the feedback loop by making the output load resistive at higher frequencies. The bandwidth will generally be lower than bandwidth without the capacitive load.

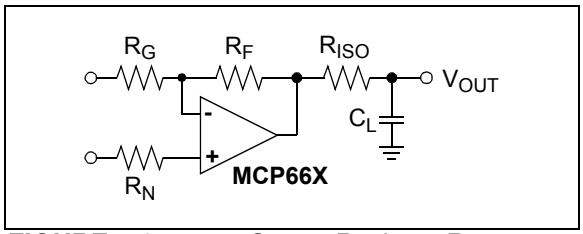


FIGURE 4-6: *Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads.*

Figure 4-7 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1 + |Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

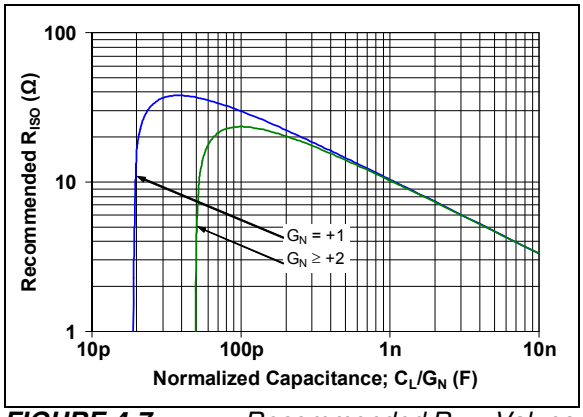


FIGURE 4-7: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for the circuit, double-check the resulting frequency response peaking and step response overshoot. Modify the value of R_{ISO} until the response is reasonable. Bench evaluation and simulations with the MCP660/1/2/3/4/5/9 SPICE macro model are helpful.

4.4.2 GAIN PEAKING

Figure 4-8 shows an op amp circuit that represents non-inverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp's common-mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel.

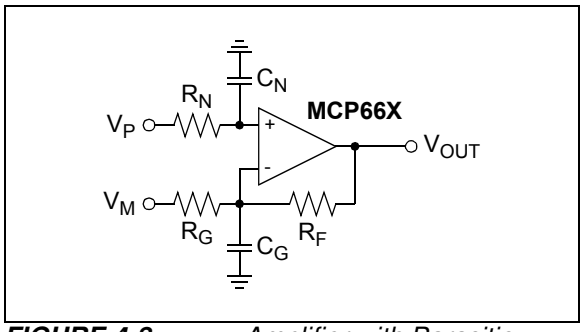


FIGURE 4-8: *Amplifier with Parasitic Capacitance.*

C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G or R_F.

C_N and R_N form a low-pass filter that affects the signal at V_P. This filter has a single real pole at $1/(2\pi R_N/C_N)$.

The largest value of R_F that should be used depends on the noise gain (see G_N in **Section 4.4.1 "Capacitive Loads"**), C_G and the open-loop gain's phase shift. Figure 4-9 shows the maximum recommended R_F for several C_G values. Some applications may modify these values to reduce either output loading or gain peaking (step response overshoot).

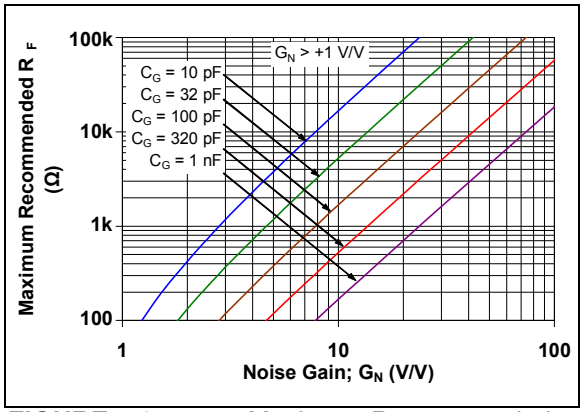


FIGURE 4-9: *Maximum Recommended R_F vs. Gain.*

Figures 2-35 and 2-36 show the small signal and large signal step responses at G = +1 V/V. The unity-gain buffer usually has $R_F = 0\Omega$ and R_G open.

Figures 2-37 and 2-38 show the small signal and large signal step responses at G = -1 V/V. Since the noise gain is 2 V/V and $C_G \approx 10$ pF, the resistors were chosen to be $R_F = R_G = 401\Omega$ and $R_N = 200\Omega$.

It is also possible to add a capacitor (C_F) in parallel with R_F to compensate for the destabilizing effect of C_G. This makes it possible to use larger values of R_F. The conditions for stability are summarized in Equation 4-6.

EQUATION 4-6:

Given:

$$G_{N1} = 1 + \frac{R_F}{R_G}$$

$$G_{N2} = 1 + \frac{C_G}{C_F}$$

$$f_F = \frac{1}{2\pi R_F C_F}$$

$$f_Z = f_F\left(\frac{G_{N1}}{G_{N2}}\right)$$

We need:

$$f_F \leq \frac{f_{GBWP}}{2G_{N2}},\ G_{N1} < G_{N2}$$

$$f_F \leq \frac{f_{GBWP}}{4G_{N1}},\ G_{N1} > G_{N2}$$

4.5 MCP663 and MCP665 Chip Select

The MCP663 is a single amplifier with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 1 µA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. The $\overline{CS}$ pin has an internal 5 MΩ (typical) pulldown resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pin is left floating. Figures 1-1, 2-43 and 2-44 show the output voltage and supply current response to a $\overline{CS}$ pulse.

The MCP665 is a dual amplifier with two $\overline{CS}$ pins; $\overline{CS_A}$ controls op amp A and $\overline{CS_B}$ controls op amp B. These op amps are controlled independently, with an enabled quiescent current (I_Q) of 6 mA/amplifier (typical) and a disabled I_Q of 1 µA/amplifier (typical). The I_Q seen at the supply pins is the sum of the two op amps' I_Q; the typical value for the I_Q of the MCP665 will be 2 µA, 6 mA or 12 mA when there are 0, 1 or 2 amplifiers enabled, respectively.

4.6 Power Supply

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. Surface mount, multilayer ceramic capacitors, or their equivalent, should be used.

These op amps require a bulk capacitor (i.e., 2.2 µF or larger) within 50 mm to provide large, slow currents. Tantalum capacitors, or their equivalent, may be a good choice. This bulk capacitor can be shared with other nearby analog parts as long as crosstalk through the power supplies does not prove to be a problem.

4.7 High Speed PCB Layout

These op amps are fast enough that a little extra care in the printed circuit board (PCB) layout can make a significant difference in performance. Good PC board layout techniques will help you achieve the performance shown in the specifications and typical performance curves; it will also help minimize electromagnetic compatibility (EMC) issues.

Use a solid ground plane. Connect the bypass local capacitor(s) to this plane with minimal length traces. This cuts down inductive and capacitive crosstalk.

Separate digital from analog, low-speed from high-speed and low-power from high-power. This will reduce interference.

Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high-frequency (low rise time) signals.

Sometimes, it helps to place guard traces next to victim traces. They should be on both sides of the victim trace and as close as possible. Connect guard traces to ground plane at both ends and in the middle for long traces.

Use coax cables, or low inductance wiring, to route signal and power to and from the PCB. Mutual and self inductance of power wires is often a cause of crosstalk and unusual behavior.