
Chipsmall
深圳市津利帝科技有限公司
Geelead Technology Limited
Chipsmall
采购部

MCP6H71/2/4

2.7 MHz, 12V Op Amps

Features:

- Input Offset Voltage: ±1 mV (typical)
- Quiescent Current: 480 µA (typical)
- Common Mode Rejection Ratio: 103 dB (typical)
- Power Supply Rejection Ratio: 105 dB (typical)
- Rail-to-Rail Output
- Supply Voltage Range:
  - Single-Supply Operation: 3.5V to 12V
  - Dual-Supply Operation: ±1.75V to ±6V
- Gain Bandwidth Product: 2.7 MHz (typical)
- Slew Rate: 2 V/µs (typical)
- Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C
- No Phase Reversal

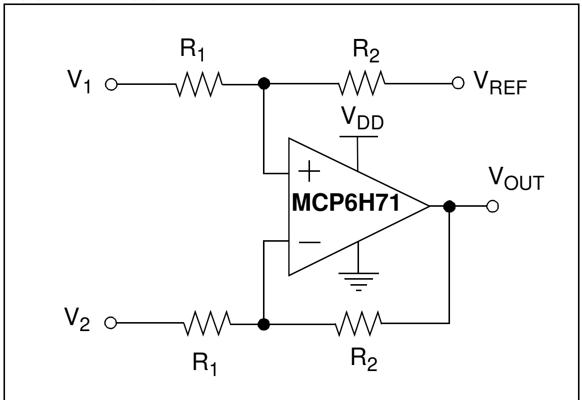
Applications:

- Automotive Power Electronics
- Industrial Control Equipment
- Battery Powered Systems
- Sensor Conditioning

Design Aids:

- SPICE Macro Models
- FilterLab® Software
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



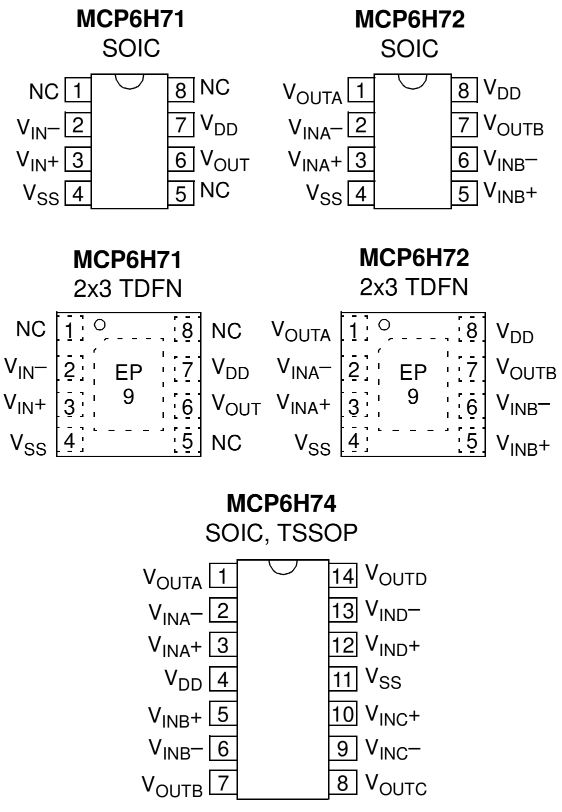
Difference Amplifier

Description:

Microchip's MCP6H71/2/4 family of operational amplifiers (op amps) has a wide supply voltage range of 3.5V to 12V and rail-to-rail output operation. This family is unity gain stable and has a gain bandwidth product of 2.7 MHz (typical). These devices operate with a single-supply voltage as high as 12V, while only drawing 480 µA/amplifier (typical) of quiescent current.

The MCP6H71/2/4 family is offered in single (MCP6H71), dual (MCP6H72) and quad (MCP6H74) configurations. All devices are fully specified in extended temperature range from -40°C to +125°C.

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$	13.2V
Current at Input Pins	±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)††	V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs	V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage	$V_{DD} – V_{SS}$
Output Short-Circuit Current	continuous
Current at Output and Supply Pins	±65 mA
Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
ESD protection on all pins (HBM; MM)	≥ 2 kV; 200V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2, Input Voltage Limits.**

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +3.5V to +12V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$ - 1.4V, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$ and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4	±1	4	mV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection Ratio	PSRR	82	105	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	10	—	pA	
		—	400	—	pA	T_A = +85°C
		—	9	25	nA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	$10^{13}\|\|6$	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13}\|\|6$	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 2.5	V	
Common Mode Rejection Ratio	CMRR	76	96	—	dB	V_{CM} = -0.3V to 1.0V, V_{DD} = 3.5V
		80	99	—	dB	V_{CM} = -0.3V to 2.5V, V_{DD} = 5V
		80	103	—	dB	V_{CM} = -0.3V to 9.5V, V_{DD} = 12V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	100	120	—	dB	0.2V < V_{OUT} <(V_{DD} – 0.2V)

DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +3.5V to +12V, V_{SS} = GND, T_A = +25°C, V_{CM} = V_{DD}/2 - 1.4V, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output						
High-Level Output Voltage	V_{OH}	3.490	3.495	—	V	V_{DD} = 3.5V 0.5V input overdrive
		4.985	4.993	—	V	V_{DD} = 5V 0.5V input overdrive
		11.970	11.980	—	V	V_{DD} = 12V 0.5V input overdrive
Low-Level Output Voltage	V_{OL}	—	0.005	0.010	V	V_{DD} = 3.5V 0.5 V input overdrive
		—	0.007	0.015	V	V_{DD} = 5V 0.5 V input overdrive
		—	0.020	0.030	V	V_{DD} = 12V 0.5 V input overdrive
Output Short-Circuit Current	I_{SC}	—	±32	—	mA	V_{DD} = 3.5V
		—	±50	—	mA	V_{DD} = 5V
		—	±53	—	mA	V_{DD} = 12V
Power Supply						
Supply Voltage	V_{DD}	3.5	—	12	V	Single-Supply operation
		±1.75	—	±6	V	Dual-Supply operation
Quiescent Current per Amplifier	I_Q	—	480	600	µA	I_O = 0, V_{CM} = V_{DD}/4

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +12V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF. (Refer to Figure 1-1).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	2.7	—	MHz	
Phase Margin	PM	—	57	—	°C	G = +1V/V
Slew Rate	SR	—	2	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	11	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	f = 1 kHz
		—	16	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	1.9	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +3.5V to +12V and V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	52.5	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.2 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT} (refer to Equation 1-1). Note that V_{CM} is not the circuit's common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$
\begin{aligned}
G_{DM} &= R_F / R_G \\
V_{CM} &= (V_P + V_{DD}/2)/2 \\
V_{OST} &= V_{IN-} - V_{IN+} \\
V_{OUT} &= (V_{DD}/2) + (V_P - V_M) + V_{OST} \cdot (1 + G_{DM})
\end{aligned}
$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

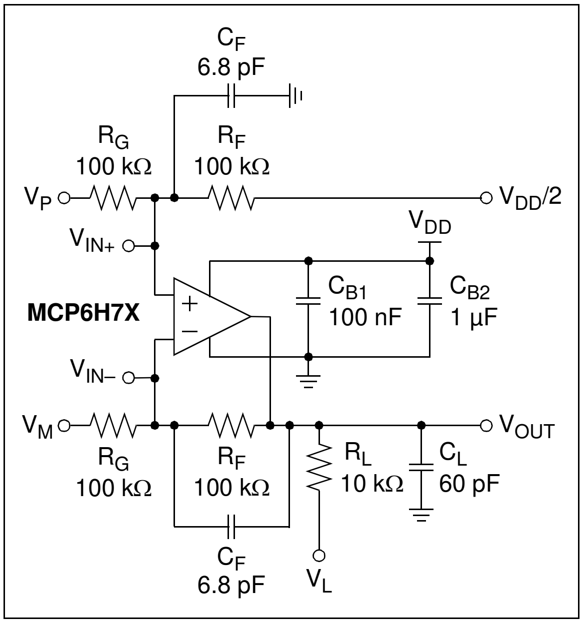


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +12V, V_{SS} = GND, $V_{CM} = V_{DD}/2 - 1.4V$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

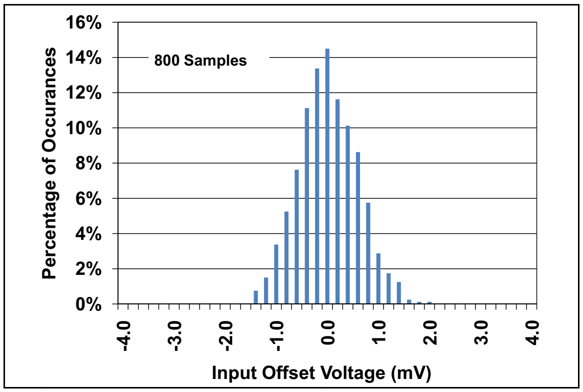


FIGURE 2-1: *Input Offset Voltage.*

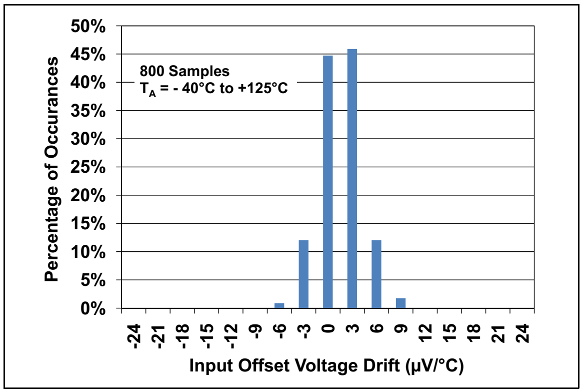


FIGURE 2-2: *Input Offset Voltage Drift.*

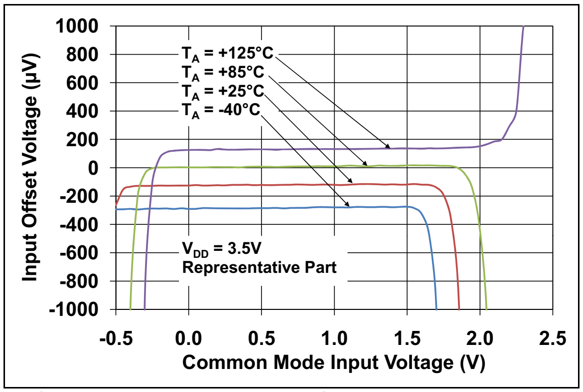


FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage.*

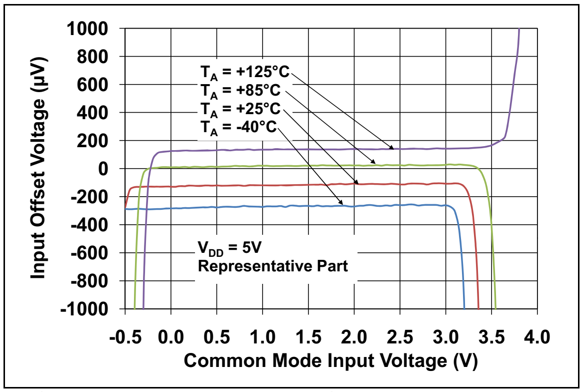


FIGURE 2-4: *Input Offset Voltage vs. Common Mode Input Voltage.*

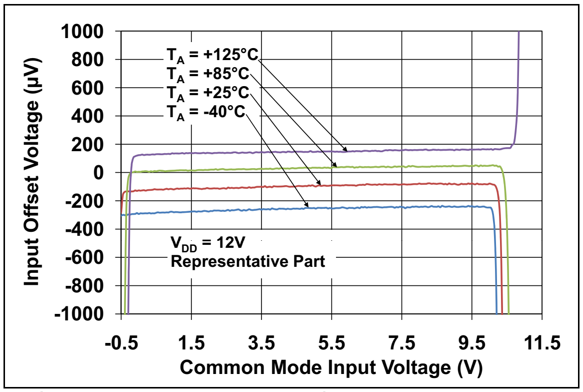


FIGURE 2-5: *Input Offset Voltage vs. Common Mode Input Voltage.*

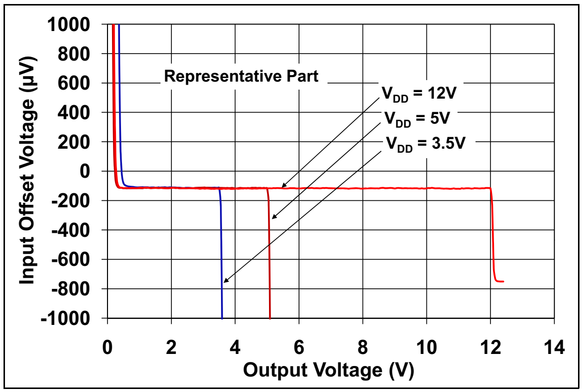


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +12V, V_{SS} = GND, $V_{CM} = V_{DD}/2 - 1.4V$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

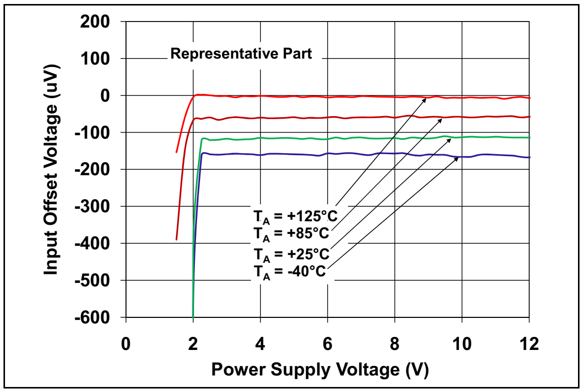


FIGURE 2-7: *Input Offset Voltage vs. Power Supply Voltage.*

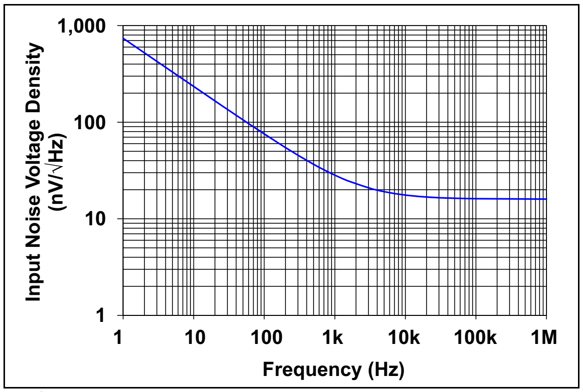


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

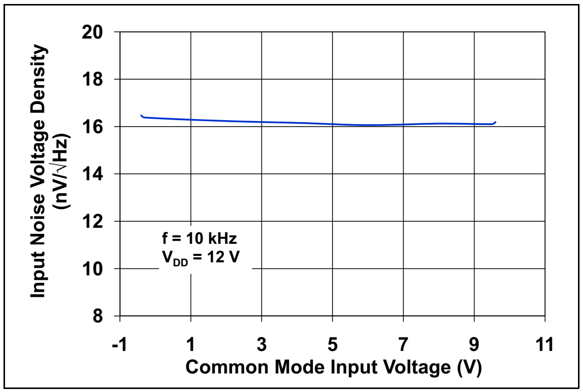


FIGURE 2-9: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

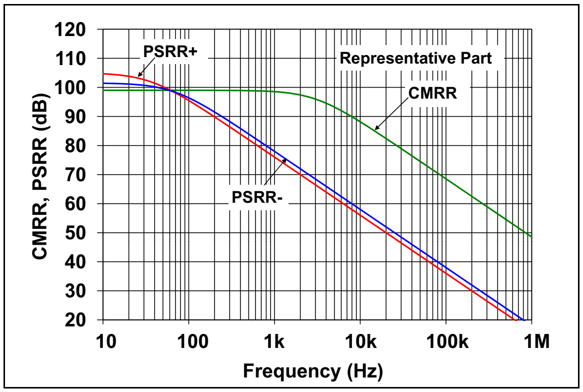


FIGURE 2-10: *CMRR, PSRR vs. Frequency.*

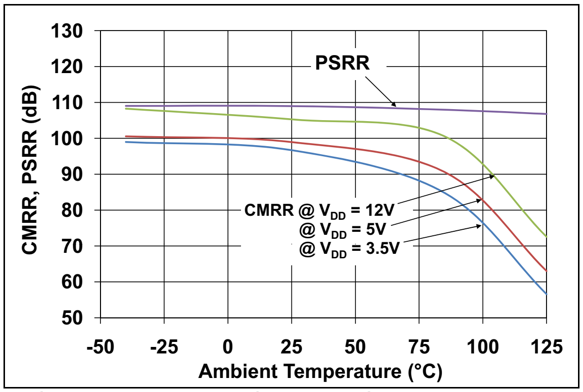


FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

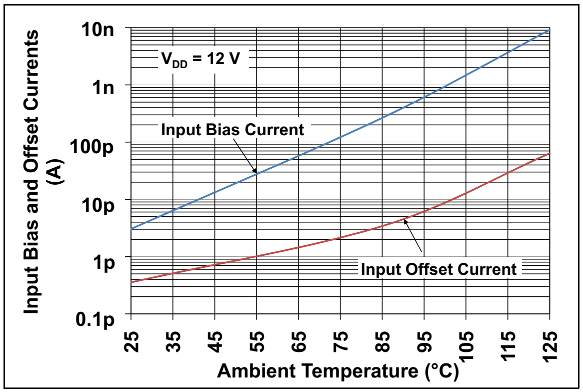


FIGURE 2-12: *Input Bias, Offset Currents vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +12V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

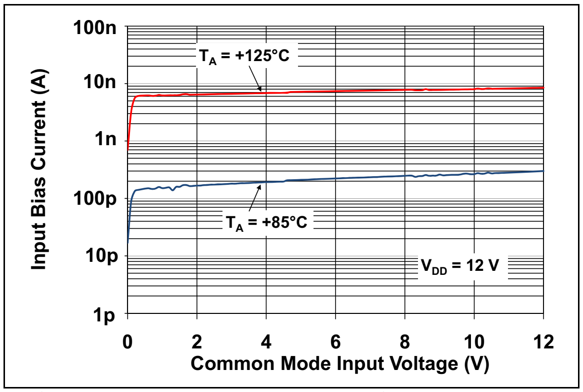


FIGURE 2-13: Input Bias Current vs. Common Mode Input Voltage.

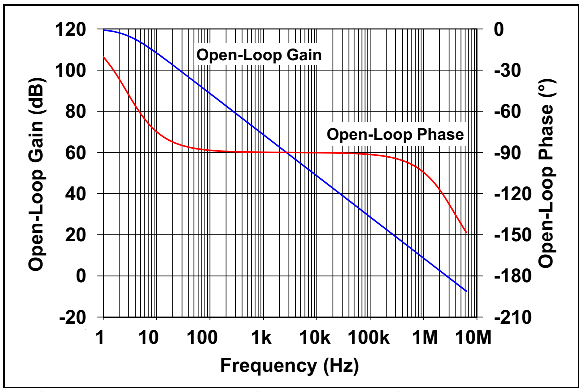


FIGURE 2-16: Open-Loop Gain, Phase vs. Frequency.

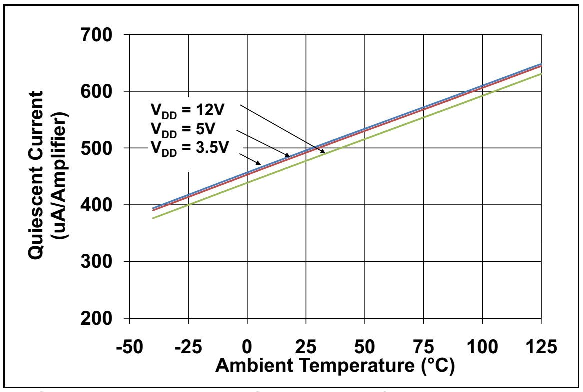


FIGURE 2-14: Quiescent Current vs. Ambient Temperature.

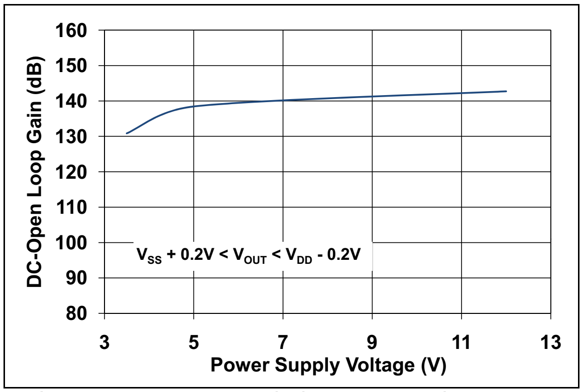


FIGURE 2-17: DC Open-Loop Gain vs. Power Supply Voltage.

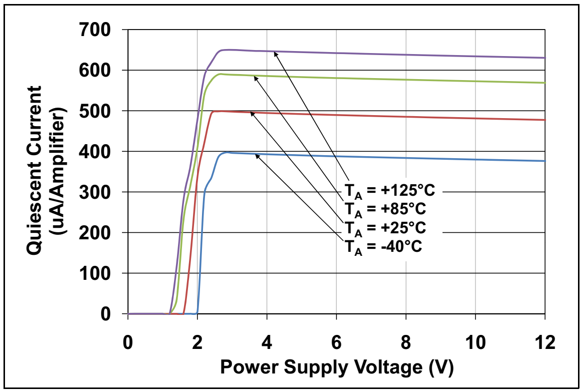


FIGURE 2-15: Quiescent Current vs. Power Supply Voltage.

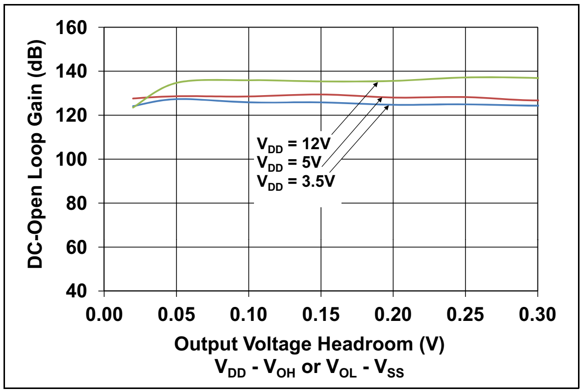


FIGURE 2-18: DC Open-Loop Gain vs. Output Voltage Headroom.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +12V, V_{SS} = GND, V_{CM} = $V_{DD}/2$ - 1.4V, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

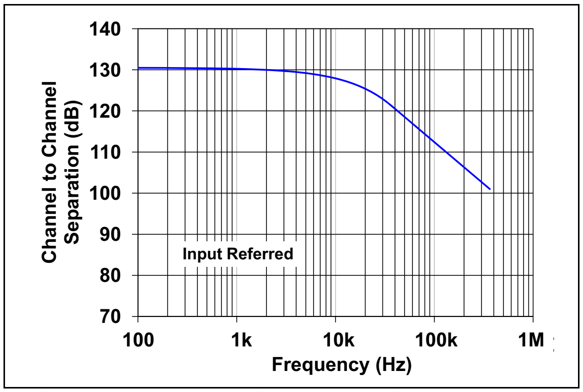


FIGURE 2-19: *Channel-to-Channel Separation vs. Frequency (MCP6H72/4 only).*

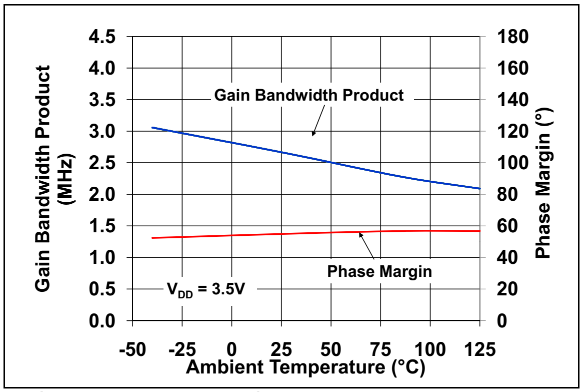


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

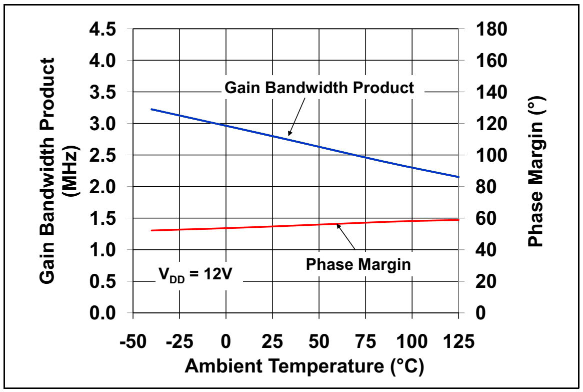


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

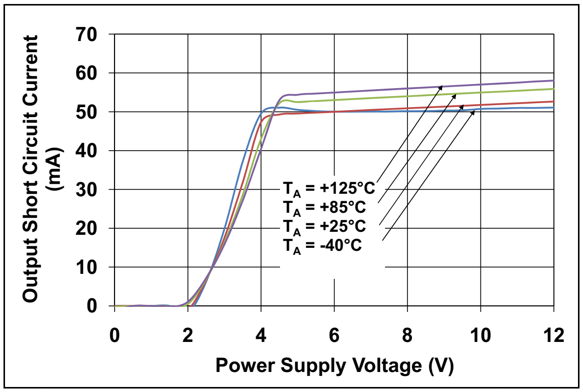


FIGURE 2-22: *Output Short Circuit Current vs. Power Supply Voltage.*

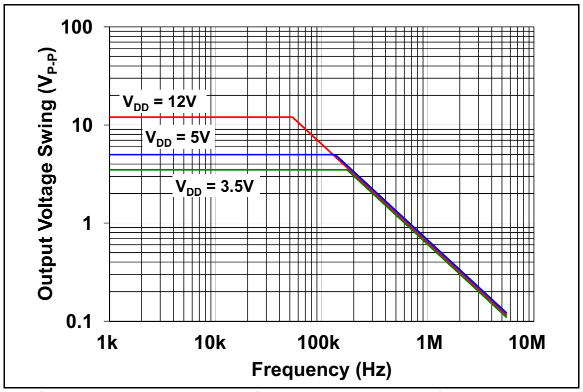


FIGURE 2-23: *Output Voltage Swing vs. Frequency.*

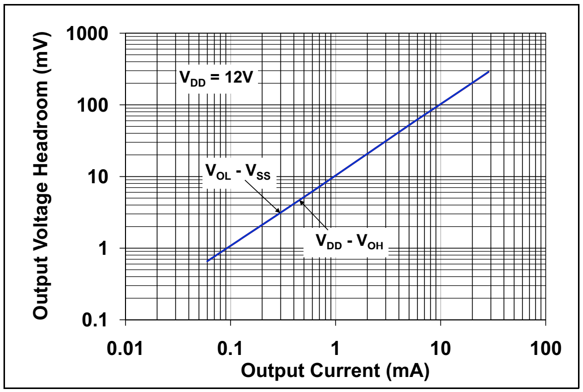


FIGURE 2-24: *Output Voltage Headroom vs. Output Current.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5V to +12V, V_{SS} = GND, V_{CM} = $V_{DD}/2$ - 1.4V, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

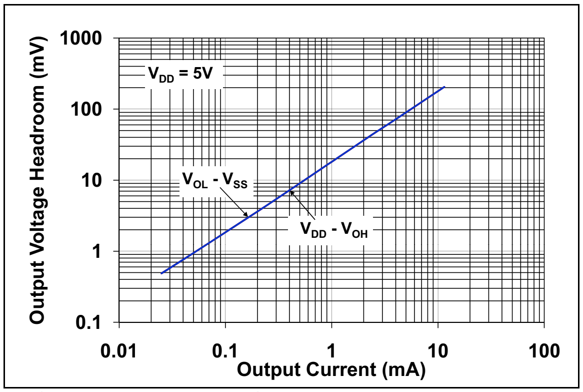


FIGURE 2-25: *Output Voltage Headroom vs. Output Current.*

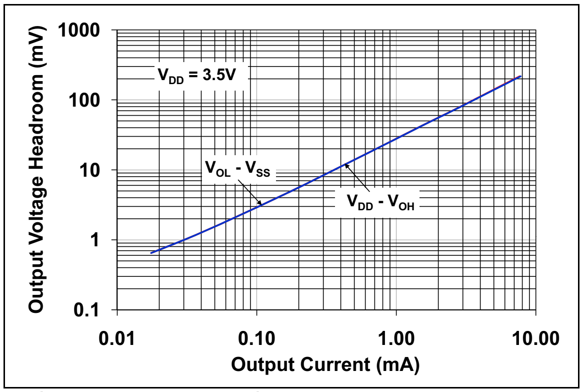


FIGURE 2-26: *Output Voltage Headroom vs. Output Current.*

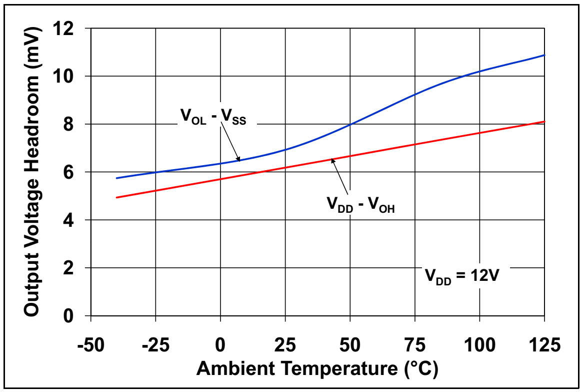


FIGURE 2-27: *Output Voltage Headroom vs. Ambient Temperature.*

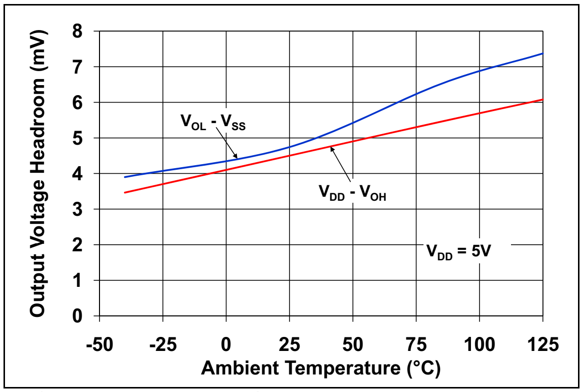


FIGURE 2-28: *Output Voltage Headroom vs. Ambient Temperature.*

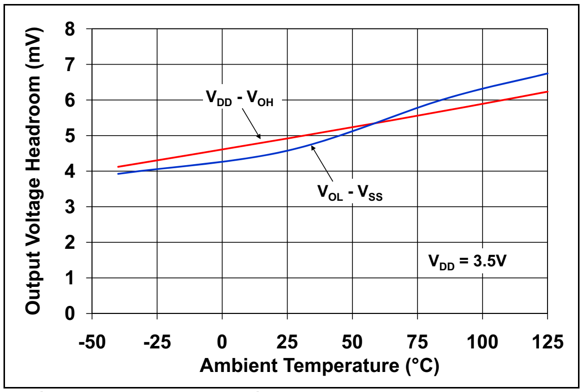


FIGURE 2-29: *Output Voltage Headroom vs. Ambient Temperature.*

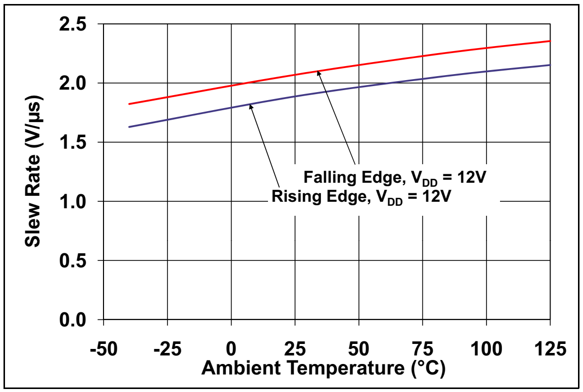


FIGURE 2-30: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5 V to +12 V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

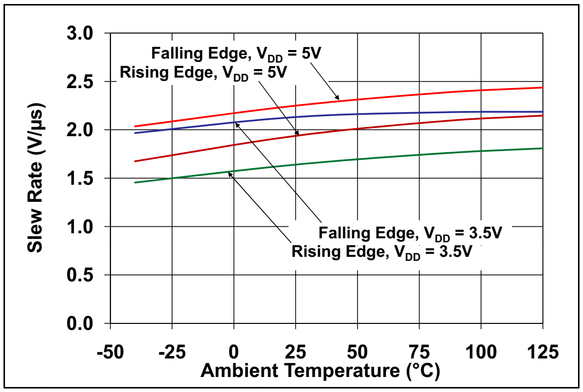


FIGURE 2-31: *Slew Rate vs. Ambient Temperature.*

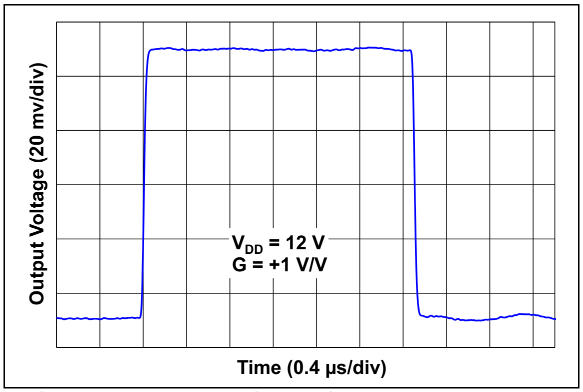


FIGURE 2-32: *Small Signal Non-Inverting Pulse Response.*

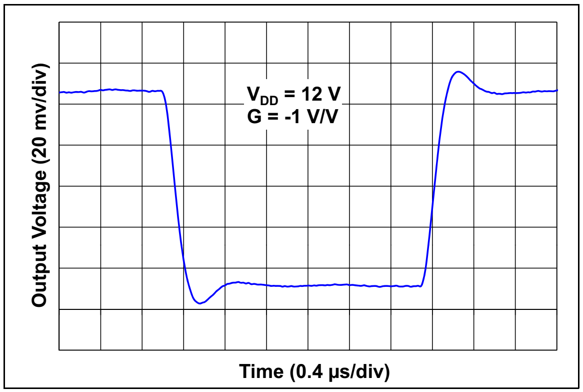


FIGURE 2-33: *Small Signal Inverting Pulse Response.*

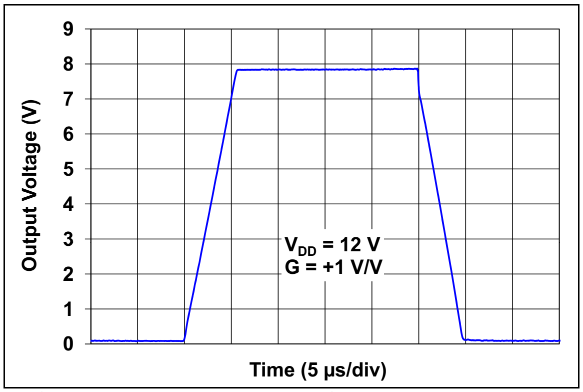


FIGURE 2-34: *Large Signal Non-Inverting Pulse Response.*

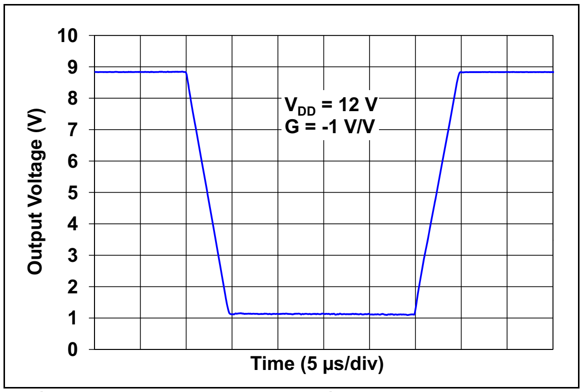


FIGURE 2-35: *Large Signal Inverting Pulse Response.*

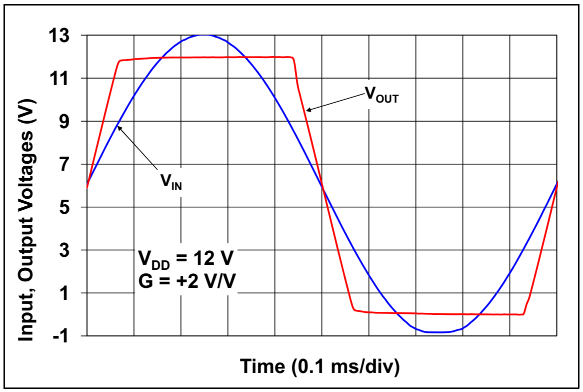


FIGURE 2-36: *The MCP6H71/2/4 Shows No Phase Reversal.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +3.5 V to +12 V, V_{SS} = GND, V_{CM} = V_{DD}/2 - 1.4V, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

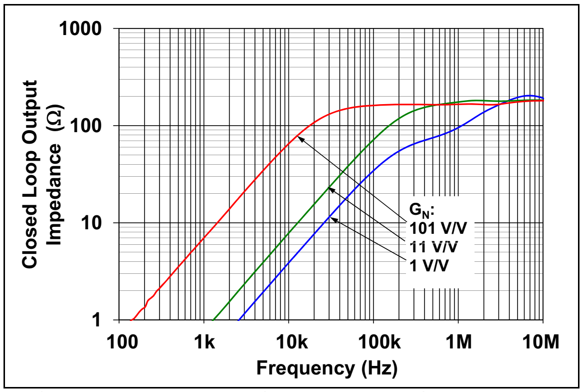


FIGURE 2-37: *Closed-Loop Output Impedance vs. Frequency.*

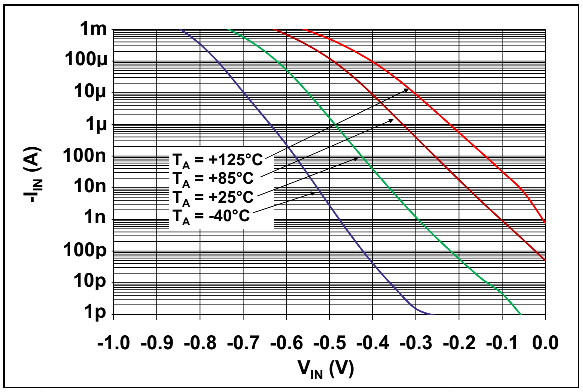


FIGURE 2-38: *Measured Input Current vs. Input Voltage (below V_{SS}).*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6H71		MCP6H72		MCP6H74	Symbol	Description
SOIC	2x3 TDFN	SOIC	2x3 TDFN	SOIC, TSSOP		
6	6	1	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
2	2	2	2	2	$V_{IN}–$, $V_{INA}–$	Inverting Input (op amp A)
3	3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
7	7	8	8	4	V_{DD}	Positive Power Supply
—	—	5	5	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	6	6	6	$V_{INB}–$	Inverting Input (op amp B)
—	—	7	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	9	$V_{INC}–$	Inverting Input (op amp C)
—	—	—	—	10	$V_{INC}+$	Non-Inverting Input (op amp C)
4	4	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	$V_{IND}+$	Non-Inverting Input (op amp D)
—	—	—	—	13	$V_{IND}–$	Inverting Input (op amp D)
—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
1, 5, 8	1, 5, 8	—	—	—	NC	No Internal Connection
—	9	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 3.5V to 12V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts can be used in single-supply operation or dual-supply operation. Also, V_{DD} will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

NOTES:

4.0 APPLICATION INFORMATION

The MCP6H71/2/4 family of op amps are manufactured using Microchip’s state-of-the-art CMOS process and are specifically designed for low-power, high-precision applications.

4.1 Inputs

4.1.1 PHASE REVERSAL

The MCP6H71/2/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-36 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1 “Absolute Maximum Ratings †”**).

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize the input bias current (I_B).

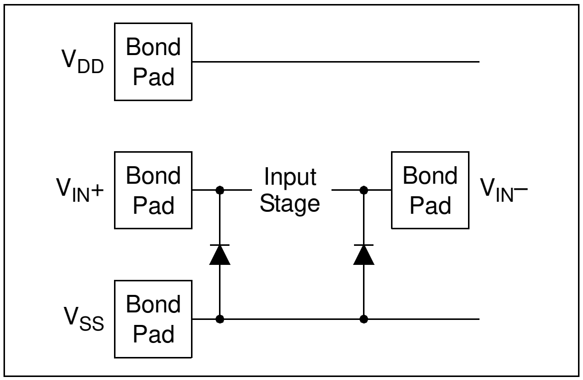


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}. Their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage (beyond V_{DD}) events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-2 shows one approach to protecting these inputs.

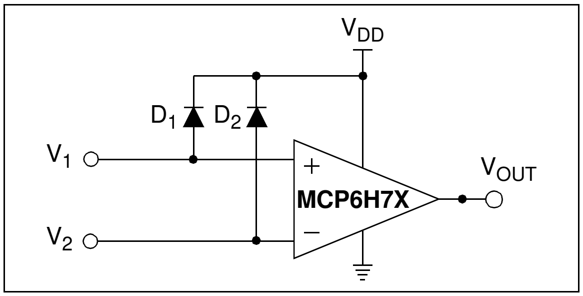


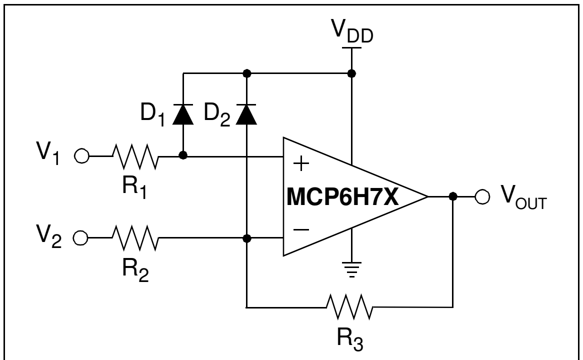
FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}), as shown in Figure 2-38.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1 “Absolute Maximum Ratings †”**).

Figure 4-3 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins (and the ESD diodes, D_1 and D_2). The diode currents will go through either V_{DD} or V_{SS}.



$$R_1 > \frac{V_{SS} - (\text{minimum expected } V_1)}{2\text{ mA}}$$

$$R_2 > \frac{V_{SS} - (\text{minimum expected } V_2)}{2\text{ mA}}$$

FIGURE 4-3: *Protecting the Analog Inputs.*

4.1.4 NORMAL OPERATION

The inputs of the MCP6H71/2/4 op amps connect to a differential PMOS input stage. It operates at a low common mode input voltage (V_{CM}), including ground. With this topology, the device operates with a V_{CM} up to $V_{DD} - 2.5V$ and 0.3V below V_{SS} (refer to Figures 2-3 through 2-5). The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and $V_{DD} - 2.5V$ to ensure proper operation.

For a unity gain buffer, V_{IN} must be maintained below $V_{DD} - 2.5V$ for correct operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6H71/2/4 op amps is 0.020V (typical) and 11.980V (typical) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 12V. Refer to Figures 2-24 through 2-29 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1V/V) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = + 1V/V), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will generally be lower than the bandwidth with no capacitance load.

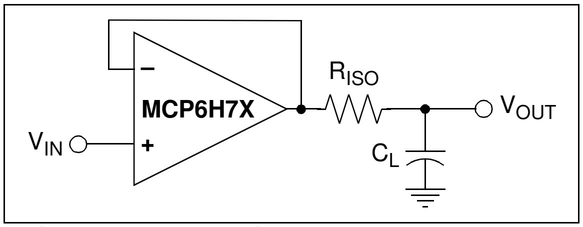


FIGURE 4-4: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-5 gives the recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1 + |Signal Gain| (e.g., -1V/V gives G_N = +2V/V).

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6H71/2/4 SPICE macro model are helpful.

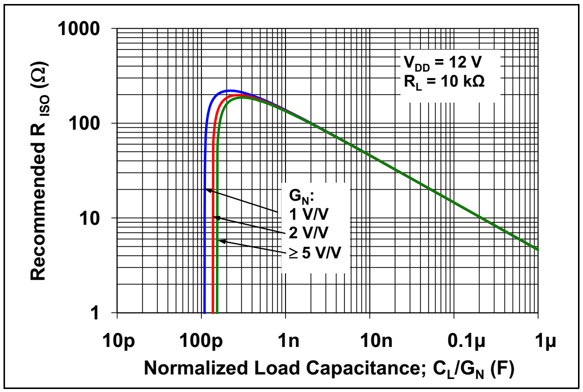


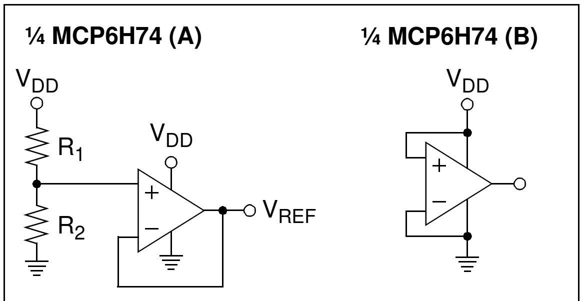
FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6H74) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp, and the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



$$V_{REF} = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

FIGURE 4-6: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low-input bias current is critical, PCB surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low-humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 15V difference would cause 15 pA of current to flow, which is greater than the MCP6H71/2/4 family's bias current at +25°C (10 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

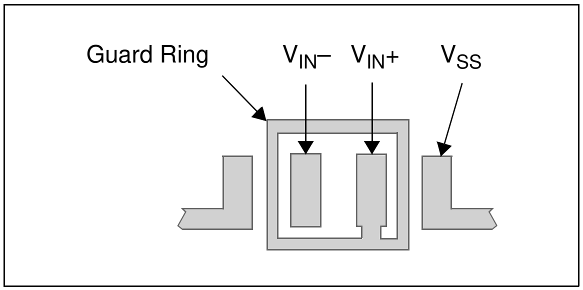


FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

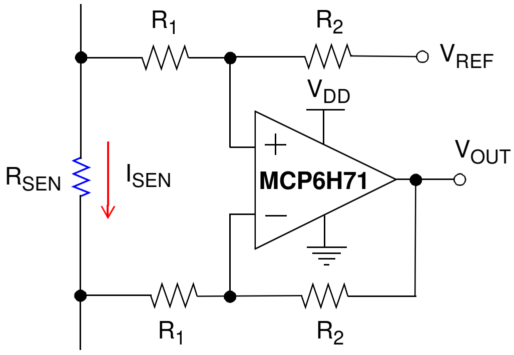
1. Non-Inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin ($V_{IN}-$). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b. Connect the inverting pin ($V_{IN}-$) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 DIFFERENCE AMPLIFIER

The MCP6H71/2/4 op amps can be used in current sensing applications. Figure 4-8 shows a resistor (R_{SEN}) that converts the sensor current (I_{SEN}) to voltage, as well as a difference amplifier that amplifies the voltage across the resistor while rejecting common mode noise. R_1 and R_2 must be well matched to obtain an acceptable Common Mode Rejection Ratio (CMRR). Moreover, R_{SEN} should be much smaller than R_1 and R_2 in order to minimize the resistive loading of the source.

To ensure proper operation, the op amp common mode input voltage must be kept within the allowed range. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single-supply applications, V_{REF} is typically $V_{DD}/2$.



$$R_{SEN} << R_1, R_2$$

$$V_{OUT} = (V_1 - V_2)\left(\frac{R_2}{R_1}\right) + V_{REF}$$

FIGURE 4-8: *High-Side Current Sensing Using Difference Amplifier.*

4.7.2 ACTIVE FULL-WAVE RECTIFIER

The MCP6H71/2/4 family of op amps can be used in applications such as an active full-wave rectifier, as shown in Figure 4-9. The amplifier and feedback loops in this active voltage rectifier circuit eliminate the diode drop problem that exists in a passive voltage rectifier. This circuit behaves as a voltage follower (the output follows the input) as long as the input signal is more positive than the reference voltage. If the input signal is more negative than the reference voltage, however, the circuit behaves as an inverting amplifier with a Gain = -1V/V. Therefore, the output voltage will always be above the reference voltage, regardless of the input signal. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single-supply applications, V_{REF} is typically $V_{DD}/2$.

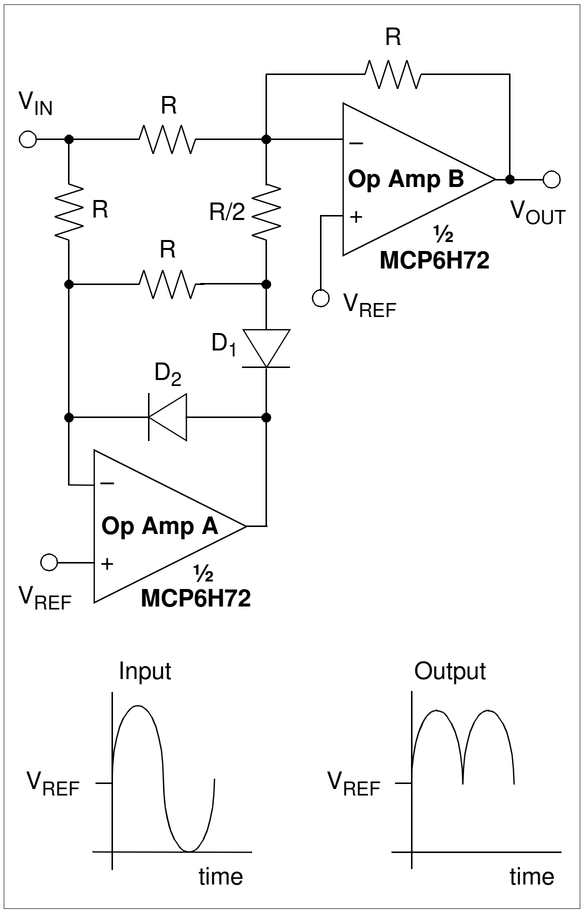


FIGURE 4-9: *Active Full-Wave Rectifier.*

4.7.3 TRIANGLE WAVES GENERATOR

The MCP6H71/2/4 family of op amps can be used in function generation applications, such as a triangle waves generator, as shown in Figure 4-10.

The triangle waves generator consists of an integrator and one comparator, connected in a positive feedback loop. This approach is based on the simple fact that integration of a constant voltage results in a linear ramp. The op amp is configured as an integrator using R_1 and C_1 to provide the triangular output, and the Schmitt triggers are designed with R_2 and R_3 to change the state corresponding to the desired peak voltages of the triangular wave output. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single-supply applications, V_{REF} is typically $V_{DD}/2$.

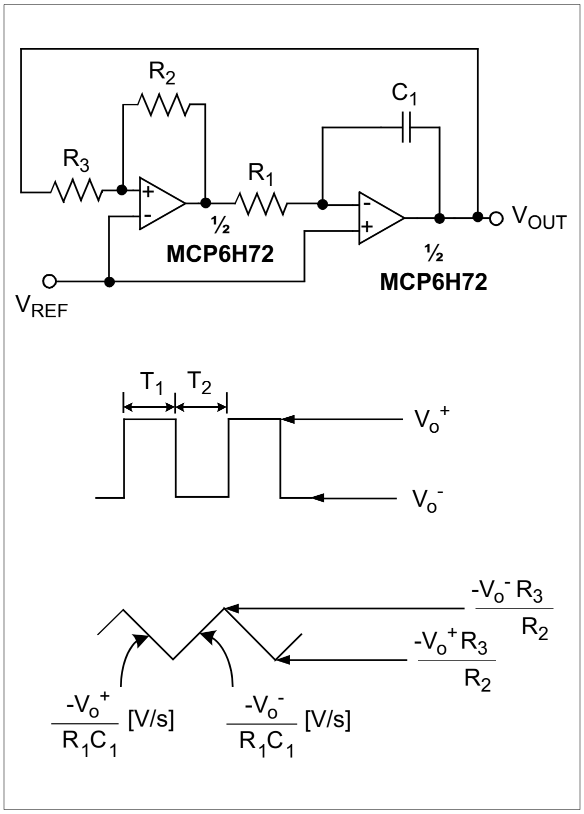


FIGURE 4-10: *Triangle Waves Generator.*

5.0 DESIGN AIDS

Microchip Technology Inc. provides the basic design tools needed for the MCP6H71/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6H71/2/4 op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in PSpice, owned by Orcad (Cadence®). For other simulators, translation may be required.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot be guaranteed to match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost on the Microchip web site at www.microchip.com/maps, MAPS is an overall selection tool for Microchip's product portfolio that includes analog, memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchases and sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site: www.microchip.com/analogtools.

Some boards that are especially useful include:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, part number VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, part number SOIC8EV

5.5 Application Notes

The following Microchip analog design note and application notes are available on the Microchip web site at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297:** *"Microchip's Op Amp SPICE Macro Models"'* DS01297
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals"'* DS01332

These application notes and others are listed in:

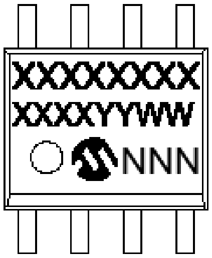
- *"Signal Chain Design Guide",* DS21825

NOTES:

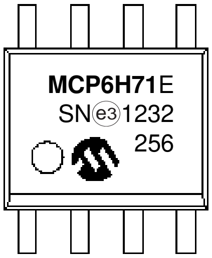
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

8-Lead SOIC (3.90 mm) **(MCP6H71, MCP6H72)**



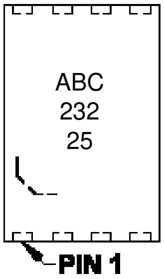
Example:



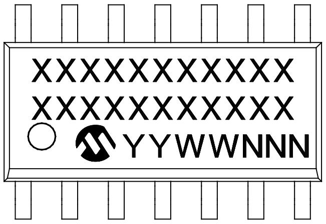
8-Lead TDFN (2x3x0.75 mm) **(MCP6H71, MCP6H72)**

Part Number	Code
MCP6H71T-E/MNY	ABC
MCP6H72T-E/MNY	ABD

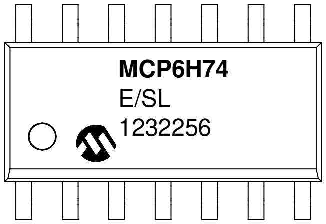
Example:



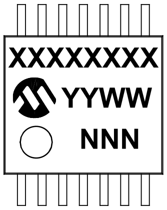
14-Lead SOIC (3.90 mm) (**MCP6H74**)



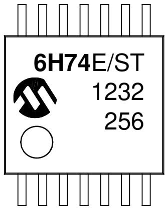
Example:



14-Lead TSSOP (4.4 mm) (**MCP6H74**)



Example:



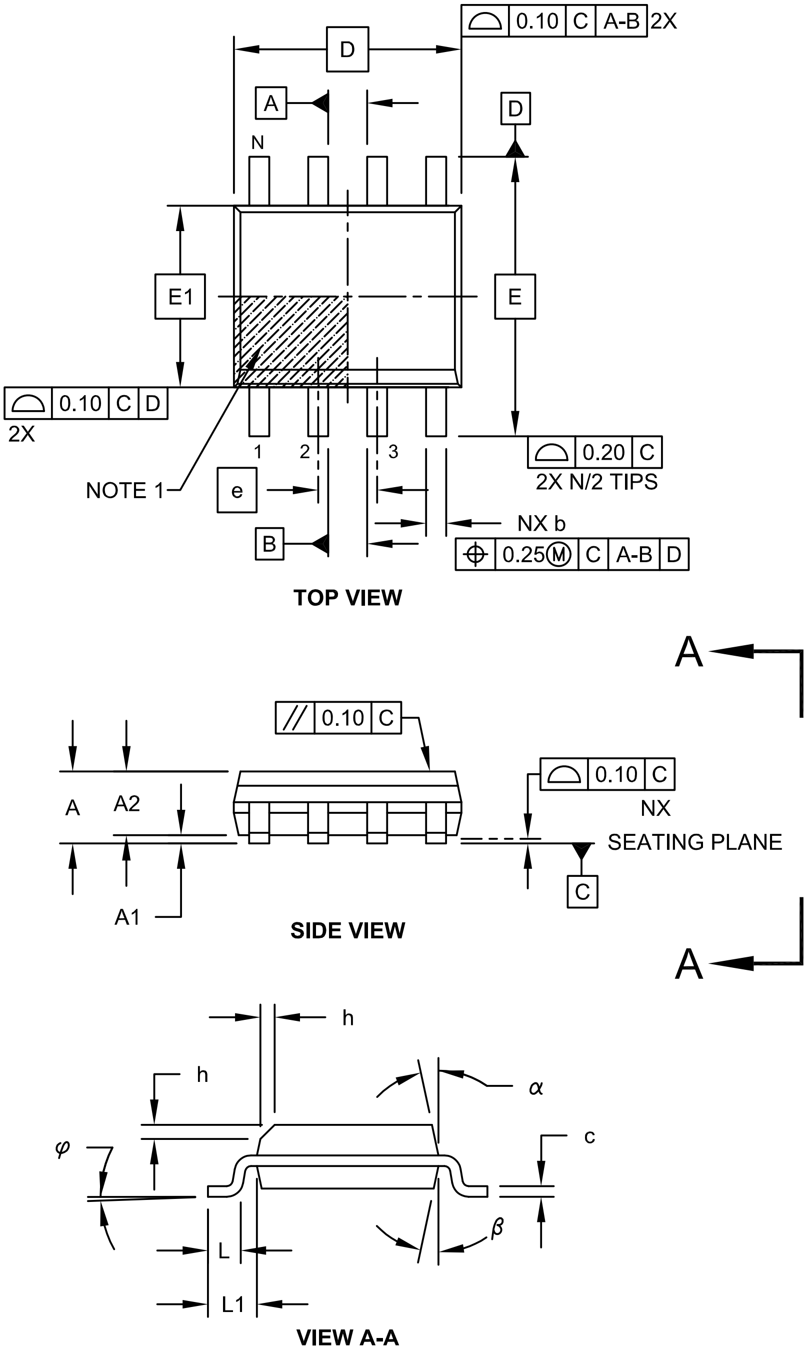
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

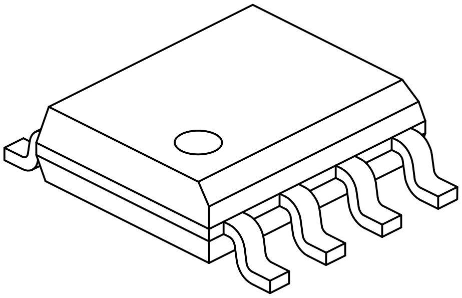
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2