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MCP6N11

500 kHz, 800 µA Instrumentation Amplifier

Features

- Rail-to-Rail Input and Output
- Gain Set by 2 External Resistors
- Minimum Gain (G_{MIN}) Options:
  1, 2, 5, 10 or 100 V/V
- Common Mode Rejection Ratio (CMRR): 115 dB (typical, G_{MIN} = 100)
- Power Supply Rejection Ratio (PSRR): 112 dB (typical, G_{MIN} = 100)
- Bandwidth: 500 kHz (typical, Gain = G_{MIN})
- Supply Current: 800 µA/channel (typical)
- Single Channel
- Enable/V_{OS} Calibration pin: (EN/$\overline{CAL}$)
- Power Supply: 1.8V to 5.5V
- Extended Temperature Range: -40°C to +125°C

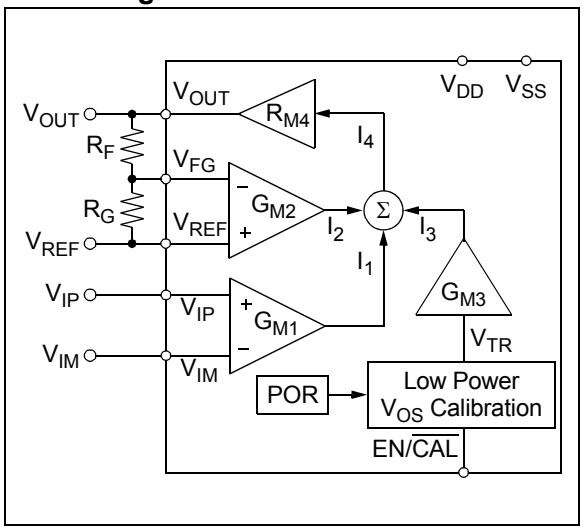
Typical Applications

- High Side Current Sensor
- Wheatstone Bridge Sensors
- Difference Amplifier with Level Shifting
- Power Control Loops

Design Aids

- Microchip Advanced Part Selector (MAPS)
- Demonstration Board
- Application Notes

Block Diagram



Description

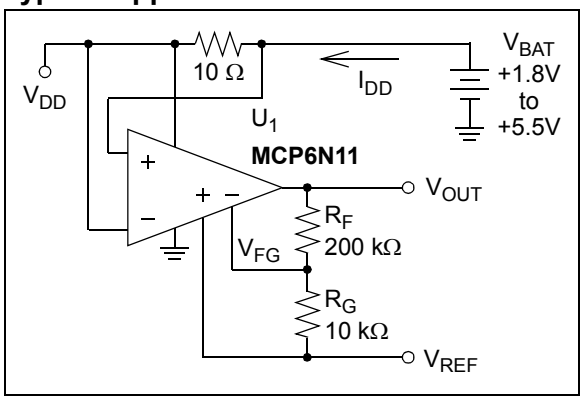
Microchip Technology Inc. offers the single MCP6N11 instrumentation amplifier (INA) with Enable/V_{OS} Calibration pin (EN/$\overline{CAL}$) and several minimum gain options. It is optimized for single-supply operation with rail-to-rail input (no common mode crossover distortion) and output performance.

Two external resistors set the gain, minimizing gain error and drift-over temperature. The reference voltage (V_{REF}) shifts the output voltage (V_{OUT}).

The supply voltage range (1.8V to 5.5V) is low enough to support many portable applications. All devices are fully specified from -40°C to +125°C.

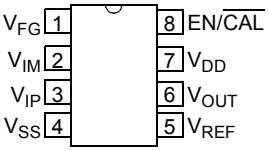
These parts have five minimum gain options (1, 2, 5, 10 and 100 V/V). This allows the user to optimize the input offset voltage and input noise for different applications.

Typical Application Circuit

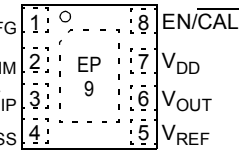


Package Types

MCP6N11
SOIC



MCP6N11
2×3 TDFN *



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Minimum Gain Options

Table 1 shows key specifications that differentiate between the different minimum gain (G_{MIN}) options. See **Section 1.0 "Electrical Characteristics"**, **Section 6.0 "Packaging Information"** and **Product Identification System** for further information on G_{MIN}.

TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS

Part No.	G_{MIN} (V/V) Nom.	V_{OS} (±mV) Max.	$\Delta V_{OS}/\Delta T_A$ (±µV/°C) Typ.	CMRR (dB) Min. V_{DD} = 5.5V	PSRR (dB) Min.	V_{DMH} (V) Max.	GBWP (MHz) Nom.	E_{ni} (μV_{P-P}) Nom. (f = 0.1 to 10 Hz)	e_{ni} (nV/√Hz) Nom. (f = 10 kHz)
MCP6N11-001	1	3.0	90	70	62	2.70	0.50	570	950
MCP6N11-002	2	2.0	45	78	68	1.35	1.0	285	475
MCP6N11-005	5	0.85	18	80	75	0.54	2.5	114	190
MCP6N11-010	10	0.50	9.0	81	81	0.27	5.0	57	95
MCP6N11-100	100	0.35	2.7	88	86	0.027	35	18	35

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins †† .....±2 mA
Analog Inputs (V_{IP} and V_{IM}) †† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, CDM, MM).≥ 2 kV, 1.5 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.1.2 "Input Voltage Limits"** and **Section 4.2.1.3 "Input Current Limits"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

Parameters	Sym	Min	Typ	Max	Units	G_{MIN}	Conditions
Input Offset							
Input Offset Voltage, Calibrated	V_{OS}	-3.0	—	+3.0	mV	1	**(Note 2)**
		-2.0	—	+2.0	mV	2	
		-0.85	—	+0.85	mV	5	
		-0.50	—	+0.50	mV	10	
		-0.35	—	+0.35	mV	100	
Input Offset Voltage Trim Step	V_{OSTRM}	—	0.36	—	mV	1	
		—	0.21	—	mV	2	
		—	0.077	—	mV	5	
		—	0.045	—	mV	10	
		—	0.014	—	mV	100	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	$\pm 90/G_{MIN}$	—	µV/°C	1 to 10	T_A= -40°C to +125°C **(Note 3)**
		—	±2.7	—	µV/°C	100	
Power Supply Rejection Ratio	PSRR	62	82	—	dB	1	
		68	88	—	dB	2	
		75	96	—	dB	5	
		81	102	—	dB	10	
		86	112	—	dB	100	

Note 1: $V_{CM} = (V_{IP} + V_{IM}) / 2$, $V_{DM} = (V_{IP} - V_{IM})$ and $G_{DM} = 1 + R_F/R_G$.
2: The V_{OS} spec limits include 1/f noise effects.
3: This is the input offset drift without V_{OS} re-calibration; toggle EN/$\overline{CAL}$ to minimize this effect.
4: These specs apply to both the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (V_{REF} takes V_{CM}'s place).
5: This spec applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.
6: Figure 2-11 and Figure 2-19 show the V_{IVR} and V_{DMR} variation over temperature.
7: See **Section 1.5 "Explanation of DC Error Specs"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = $V_{DD}/2$, V_{DM} = 0V, V_{REF} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

Parameters	Sym	Min	Typ	Max	Units	G_{MIN}	Conditions
Input Current and Impedance (Note 4)							
Input Bias Current	I_B	—	10	—	pA	all	
Across Temperature		—	80	—	pA		T_A= +85°C
Across Temperature		0	2	5	nA		T_A= +125°C
Input Offset Current	I_{OS}	—	±1	—	pA		
Across Temperature		—	±5	—	pA		T_A= +85°C
Across Temperature		-1	±0.05	+1	nA		T_A= +125°C
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF		
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF		
Input Common Mode Voltage (V_{CM} or V_{REF}) (Note 4)							
Input Voltage Range	V_{IVL}	—	—	V_{SS} – 0.2	V	all	**(Note 5, Note 6)**
	V_{IVH}	V_{DD} + 0.15	—	—	V		
Common Mode Rejection Ratio	CMRR	62	79	—	dB	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 1.8V
		69	87	—	dB	2	
		75	101	—	dB	5	
		79	107	—	dB	10	
		86	119	—	dB	100	
		70	94	—	dB	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 5.5V
		78	100	—	dB	2	
		80	108	—	dB	5	
		81	114	—	dB	10	
		88	115	—	dB	100	
Common Mode Non-Linearity	INL_{CM}	-1000	±115	+1000	ppm	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DM} = 0V, V_{DD} = 1.8V **(Note 7)**
		-570	±27	+570	ppm	2	
		-230	±11	+230	ppm	5	
		-125	±6	+125	ppm	10	
		-50	±2	+50	ppm	100	
		-400	±42	+400	ppm	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DM} = 0V, V_{DD} = 5.5V **(Note 7)**
		-220	±10	+220	ppm	2	
		-100	±4	+100	ppm	5	
		-50	±2	+50	ppm	10	
		-30	±1	+30	ppm	100	

Note 1: V_{CM} = (V_{IP} + V_{IM}) / 2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.
2: The V_{OS} spec limits include 1/f noise effects.
3: This is the input offset drift without V_{OS} re-calibration; toggle EN/$\overline{CAL}$ to minimize this effect.
4: These specs apply to both the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (V_{REF} takes V_{CM}'s place).
5: This spec applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.
6: Figure 2-11 and Figure 2-19 show the V_{IVR} and V_{DMR} variation over temperature.
7: See **Section 1.5 "Explanation of DC Error Specs"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

Parameters	Sym	Min	Typ	Max	Units	G_{MIN}	Conditions
Input Differential Mode Voltage (V_{DM}) (Note 4)							
Differential Input Voltage Range	V_{DML}	-2.7/G_{MIN}	—	—	V	all	V_{REF} = (V_{DD} – $G_{DM}V_{DM}$)/2 **(Note 6)**
	V_{DMH}	—	—	+2.7/G_{MIN}	V		
Differential Gain Error	g_E	-1	±0.13	+1	%		V_{DM} = V_{DML} to V_{DMH}, V_{REF} = (V_{DD} – $G_{DM}V_{DM}$)/2
Differential Gain Drift	$\Delta g_E/\Delta T_A$	—	±0.0006	—	%/°C		
Differential Non-Linearity	INL_{DM}	-500	±30	+500	ppm	1	**(Note 7)**
		-800	±40	+800	ppm	2, 5	
		-2000	±100	+2000	ppm	10, 100	
DC Open-Loop Gain	A_{OL}	61	84	—	dB	1	V_{DD} = 1.8V, V_{OUT} = 0.2V to 1.6V
		68	90	—	dB	2	
		76	98	—	dB	5	
		78	104	—	dB	10	
		86	116	—	dB	100	
		70	94	—	dB	1	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V
		77	100	—	dB	2	
		84	108	—	dB	5	
		90	114	—	dB	10	
		97	125	—	dB	100	
Output							
Minimum Output Voltage Swing	V_{OL}	—	—	V_{SS} + 15	mV	all	V_{DM} = -V_{DD}/(2G_{DM}), V_{DD} = 1.8V, V_{REF} = V_{DD}/2 – 1V
		—	—	V_{SS} + 25	mV		V_{DM} = -V_{DD}/(2G_{DM}), V_{DD} = 5.5V, V_{REF} = V_{DD}/2 – 1V
Maximum Output Voltage Swing	V_{OH}	V_{DD} – 15	—	—	mV		V_{DM} = V_{DD}/(2G_{DM}), V_{DD} = 1.8V, V_{REF} = V_{DD}/2 + 1V
		V_{DD} – 25	—	—	mV		V_{DM} = V_{DD}/(2G_{DM}), V_{DD} = 5.5V, V_{REF} = V_{DD}/2 + 1V
Output Short Circuit Current	I_{SC}	—	±8	—	mA		V_{DD} = 1.8V
		—	±30	—	mA		V_{DD} = 5.5V
Power Supply							
Supply Voltage	V_{DD}	1.8	—	5.5	V	all	
Quiescent Current per Amplifier	I_Q	0.5	0.8	1.1	mA		I_O = 0
POR Trip Voltage	V_{PRL}	1.1	1.4	—	V		
	V_{PRH}	—	1.4	1.7	V		

Note 1: V_{CM} = (V_{IP} + V_{IM}) / 2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.
2: The V_{OS} spec limits include 1/f noise effects.
3: This is the input offset drift without V_{OS} re-calibration; toggle EN/$\overline{CAL}$ to minimize this effect.
4: These specs apply to both the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (V_{REF} takes V_{CM}'s place).
5: This spec applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.
6: Figure 2-11 and Figure 2-19 show the V_{IVR} and V_{DMR} variation over temperature.
7: See **Section 1.5 "Explanation of DC Error Specs"**.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

Parameters	Sym	Min	Typ	Max	Units	G_{MIN}	Conditions
AC Response							
Gain Bandwidth Product	GBWP	—	0.50 G_{MIN}	—	MHz	1 to 10	
		—	35	—	MHz	100	
Phase Margin	PM	—	70	—	°	all	
Open-Loop Output Impedance	R_{OL}	—	0.9	—	kΩ	1 to 10	
		—	0.6	—	kΩ	100	
Power Supply Rejection Ratio	PSRR	—	94	—	dB	all	f < 10 kHz
Common Mode Rejection Ratio	CMRR	—	104	—	dB	1 to 10	f < 10 kHz
		—	94	—	dB	100	f < 10 kHz
Step Response							
Slew Rate	SR	—	3	—	V/µs	1 to 10	V_{DD} = 1.8V
		—	9	—	V/µs		V_{DD} = 5.5V
		—	2	—	V/µs	100	V_{DD} = 1.8V
		—	6	—	V/µs		V_{DD} = 5.5V
Overdrive Recovery, Input Common Mode	t_{IRC}	—	10	—	µs	all	V_{CM} = V_{SS} – 1V (or V_{DD} + 1V) to V_{DD}/2, $G_{DM}V_{DM}$ = ±0.1V, 90% of V_{OUT} change
Overdrive Recovery, Input Differential Mode	t_{IRD}	—	5	—	µs		V_{DM} = V_{DML} – (0.5V)/G_{MIN} (or V_{DMH} + (0.5V)/G_{MIN}) to 0V, V_{REF} = (V_{DD} – $G_{DM}V_{DM}$)/2, 90% of V_{OUT} change
Overdrive Recovery, Output	t_{OR}	—	8	—	µs		G_{DM} = 2G_{MIN}, $G_{DM}V_{DM}$ = 0.5V_{DD} to 0V, V_{REF} = 0.75V_{DD} (or 0.25V_{DD}), 90% of V_{OUT} change
Noise							
Input Noise Voltage	E_{ni}	—	570/G_{MIN}	—	μV_{P-P}	1 to 10	f = 0.1 Hz to 10 Hz
		—	18	—	μV_{P-P}	100	
Input Noise Voltage Density	e_{ni}	—	950/G_{MIN}	—	nV/√Hz	1 to 10	f = 100 kHz
		—	35	—	nV/√Hz	100	
Input Current Noise Density	i_{ni}	—	1	—	fA/√Hz	all	f = 1 kHz

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = 25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

Parameters	Sym	Min	Typ	Max	Units	G_{MIN}	Conditions
EN/$\overline{CAL}$ Low Specifications							
EN/$\overline{CAL}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	all	
EN/$\overline{CAL}$ Input Current, Low	I_{ENL}	—	-0.1	—	nA		EN/$\overline{CAL}$ = 0V
GND Current	I_{SS}	-7	-2.5	—	µA		EN/$\overline{CAL}$ = 0V, V_{DD} = 5.5V
Amplifier Output Leakage	$I_{O(LEAK)}$	—	10	—	nA		EN/$\overline{CAL}$ = 0V
EN/$\overline{CAL}$ High Specifications							
EN/$\overline{CAL}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}		V_{DD}	V	all	
EN/$\overline{CAL}$ Input Current, High	I_{ENH}	—	-0.01	—	nA		EN/$\overline{CAL}$ = V_{DD}
EN/$\overline{CAL}$ Dynamic Specifications							
EN/$\overline{CAL}$ Input Hysteresis	V_{HYST}	—	0.2	—	V	all	
EN/$\overline{CAL}$ Low to Amplifier Output High-Z Turn-off Time	t_{OFF}	—	3	10	µs		EN/$\overline{CAL}$ = 0.2V_{DD} to V_{OUT} = 0.1(V_{DD}/2), $V_{DM}G_{DM}$ = 1 V, V_L = 0V
EN/$\overline{CAL}$ High to Amplifier Output On Time	t_{ON}	12	20	28	ms		EN/$\overline{CAL}$ = 0.8V_{DD} to V_{OUT} = 0.9(V_{DD}/2), $V_{DM}G_{DM}$ = 1 V, V_L = 0V
EN/$\overline{CAL}$ Low to EN/$\overline{CAL}$ High low time	t_{ENLH}	100	—	—	µs		Minimum time before externally releasing EN/$\overline{CAL}$ (**Note 1**)
Amplifier On to EN/$\overline{CAL}$ Low Setup Time	t_{ENOL}	—	100	—	µs		
POR Dynamic Specifications							
V_{DD} ↓ to Output Off	t_{PHL}	—	10	—	µs	all	V_L = 0V, V_{DD} = 1.8V to V_{PRL} – 0.1V step, 90% of V_{OUT} change
V_{DD} ↑ to Output On	t_{PLH}	140	250	360	ms		V_L = 0V, V_{DD} = 0V to V_{PRH} + 0.1V step, 90% of V_{OUT} change

Note 1: For design guidance only; not tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = 1.8V to 5.5V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 8L-TDFN (2×3)	θ_{JA}	—	53	—	°C/W	

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature specification (+150°C).

1.3 Timing Diagrams

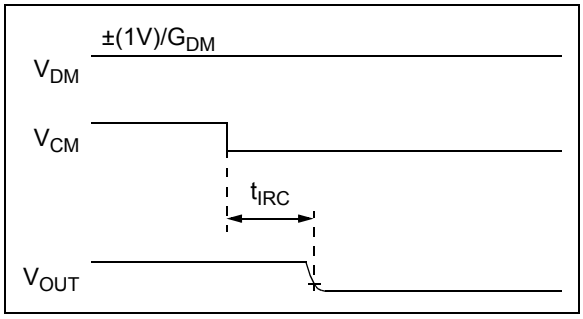


FIGURE 1-1: *Common Mode Input Overdrive Recovery Timing Diagram.*

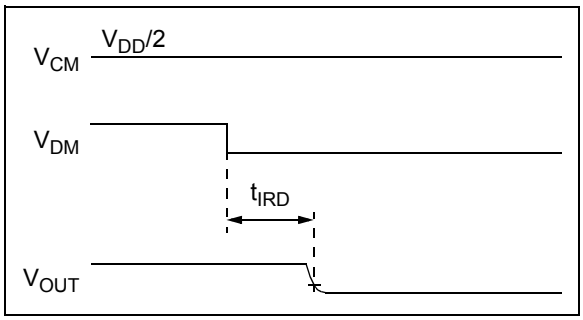


FIGURE 1-2: *Differential Mode Input Overdrive Recovery Timing Diagram.*

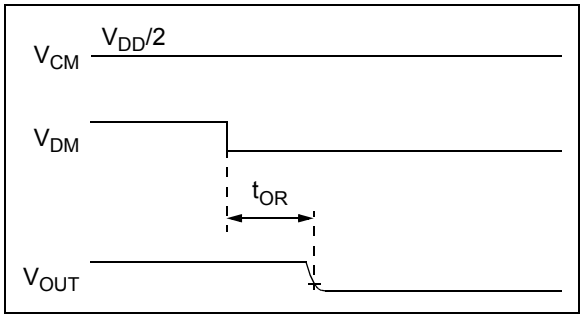


FIGURE 1-3: *Output Overdrive Recovery Timing Diagram.*

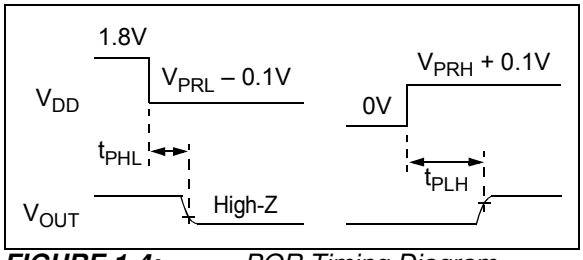


FIGURE 1-4: *POR Timing Diagram.*

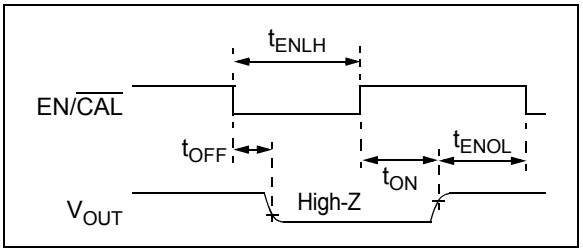


FIGURE 1-5: *EN/$\overline{CAL}$ Timing Diagram.*

1.4 DC Test Circuits

1.4.1 INPUT OFFSET TEST CIRCUIT

Figure 1-6 is used for testing the INA's input offset errors and input voltage range (V_E, V_{IVL} and V_{IVH}; see **Section 1.5.1 "Input Offset Related Errors"** and **Section 1.5.2 "Input Offset Common Mode Non-linearity"**). U_2 is part of a control loop that forces V_{OUT} to equal V_{CNT}; U_1 can be set to any bias point.

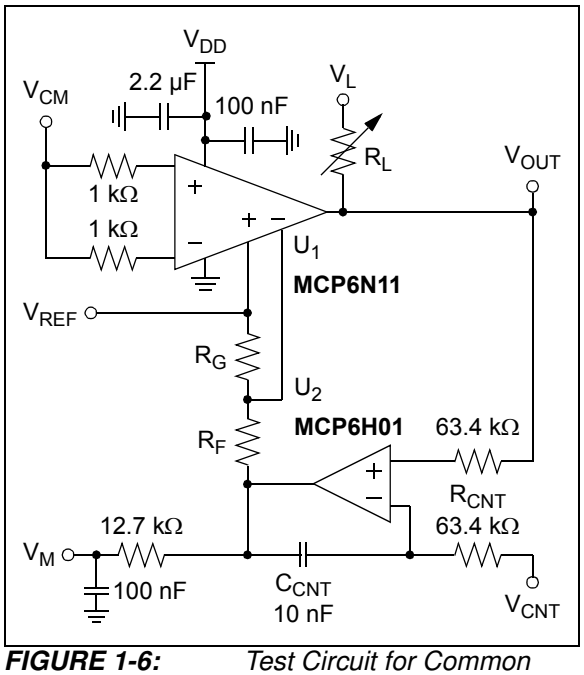


FIGURE 1-6: *Test Circuit for Common Mode (Input Offset).*

When MCP6N11 is in its normal range of operation, the DC output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-1:

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{CNT} \\ V_M &= V_{REF} + G_{DM}(1 + g_E)V_E \end{aligned}$$

Table 1-5 gives the recommended R_F and R_G values for different G_{MIN} options.

TABLE 1-5: SELECTING R_F AND R_G

G_{MIN} (V/V) Nom.	R_F (Ω) Nom.	R_G (Ω) Nom.	G_{DM} (V/V) Nom.	$G_{DM}V_{OS}$ (±V) Max.	BW (kHz) Nom.
1	100k	499	201.4	0.60	2.5
2				0.40	5.0
5	100k	100	1001	0.85	2.5
10				0.50	5.0
100				0.35	35

1.4.2 DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-7 is used for testing the INA's differential gain error, non-linearity and input voltage range (g_E, INL_{DM}, V_{DML} and V_{DMH}; see **Section 1.5.3 "Differential Gain Error and Non-linearity"**). R_F and R_G are 0.01% for accurate gain error measurements.

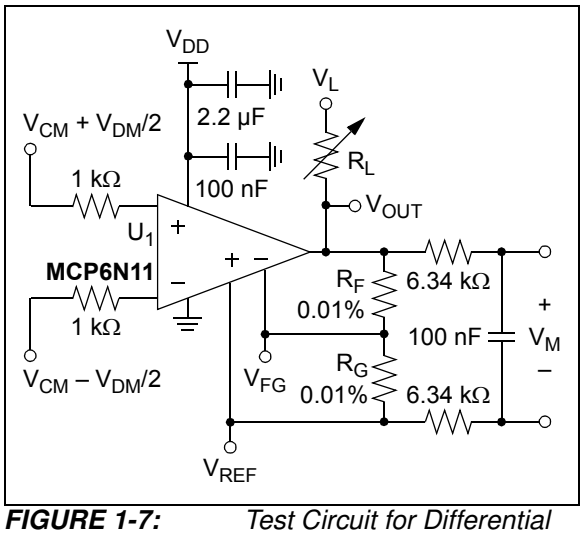


FIGURE 1-7: *Test Circuit for Differential Mode.*

The output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-2:

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E) \\ V_M &= V_{OUT} - V_{REF} \\ &= G_{DM}(1 + g_E)(V_{DM} + V_E) \end{aligned}$$

To keep V_{REF}, V_{FG} and V_{OUT} within their ranges, set:

EQUATION 1-3:

$$V_{REF} = (V_{DD} - G_{DM}V_{DM})/2$$

Table 1-6 shows the recommended R_F and R_G. They produce a 10 kΩ load; V_L can usually be left open.

TABLE 1-6: SELECTING R_F AND R_G

G_{MIN} (V/V) Nom.	R_F (Ω) Nom.	R_G (Ω) Nom.	G_{DM} (V/V) Nom.
1	0	Open	1.000
2	4.99k	4.99k	2.000
5	8.06k	2.00k	5.030
10	9.09k	1.00k	10.09
100	10.0k	100	101.0

1.5 Explanation of DC Error Specs

1.5.1 INPUT OFFSET RELATED ERRORS

The input offset error (V_E) is extracted from input offset measurements (see **Section 1.4.1 "Input Offset Test Circuit"**), based on Equation 1-1:

EQUATION 1-4:

$$V_E = \frac{V_M - V_{REF}}{G_{DM}(1 + g_E)}$$

V_E has several terms, which assume a linear response to changes in V_{DD}, V_{SS}, V_{CM}, V_{OUT} and T_A (all of which are in their specified ranges):

EQUATION 1-5:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR} + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot \frac{\Delta V_{OS}}{\Delta T_A}$$

Where:

PSRR, *CMRR* and A_{OL} are in units of V/V

ΔT_A is in units of °C

V_{DM} = 0

Equation 1-2 shows how V_E affects V_{OUT}.

1.5.2 INPUT OFFSET COMMON MODE NON-LINEARITY

The input offset error (V_E) changes non-linearly with V_{CM}. Figure 1-8 shows V_E vs. V_{CM}, as well as a linear fit line (V_{E_LIN}) based on V_{OS} and CMRR. The op amp is in standard conditions (ΔV_{OUT} = 0, V_{DM} = 0, etc.). V_{CM} is swept from V_{IVL} to V_{IVH}. The test circuit is in **Section 1.4.1 "Input Offset Test Circuit"** and V_E is calculated using Equation 1-4.

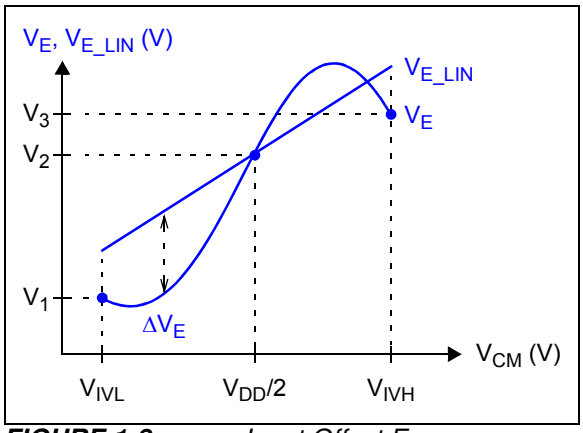


FIGURE 1-8: *Input Offset Error vs. Common Mode Input Voltage.*

Based on the measured V_E data, we obtain the following linear fit:

EQUATION 1-6:

$$V_{E\_LIN} = V_{OS} + \frac{V_{CM} - V_{DD}/2}{CMRR}$$

Where:

$$V_{OS} = V_2$$

$$\frac{1}{CMRR} = \frac{V_3 - V_1}{V_{IVH} - V_{IVL}}$$

The remaining error (ΔV_E) is described by the Common Mode Non-Linearity spec:

EQUATION 1-7:

$$INL_{CM} = \frac{max|\Delta V_E|}{V_{IVH} - V_{IVL}}$$

Where:

$$\Delta V_E = V_E - V_{E\_LIN}$$

The same common mode behavior applies to V_E when V_{REF} is swept, instead of V_{CM}, since both input stages are designed the same:

EQUATION 1-8:

$$V_{E\_LIN} = V_{OS} + \frac{V_{REF} - V_{DD}/2}{CMRR}$$

$$INL_{CM} = \frac{max|\Delta V_E|}{V_{IVH} - V_{IVL}}$$

1.5.3 DIFFERENTIAL GAIN ERROR AND NON-LINEARITY

The differential errors are extracted from differential gain measurements (see **Section 1.4.2 "Differential Gain Test Circuit"**), based on Equation 1-2. These errors are the differential gain error (g_E) and the input offset error (V_E, which changes non-linearly with V_{DM}):

EQUATION 1-9:

$$G_{DM} = 1 + R_F/R_G$$

$$V_M = G_{DM}(1 + g_E)(V_{DM} + V_E)$$

These errors are adjusted for the expected output, then referred back to the input, giving the differential input error (V_{ED}) as a function of V_{DM}:

EQUATION 1-10:

$$V_{ED} = \frac{V_M}{G_{DM}} - V_{DM}$$

Figure 1-9 shows V_{ED} vs. V_{DM}, as well as a linear fit line (V_{ED_LIN}) based on V_E and g_E. The op amp is in standard conditions (ΔV_{OUT} = 0, etc.). V_{DM} is swept from V_{DML} to V_{DMH}.

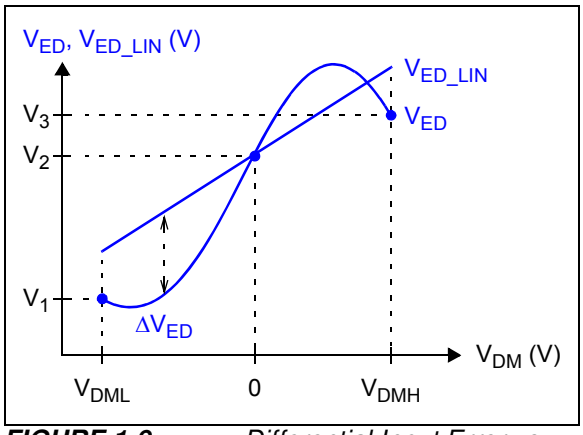


FIGURE 1-9: *Differential Input Error vs. Differential Input Voltage.*

Based on the measured V_{ED} data, we obtain the following linear fit:

EQUATION 1-11:

$$V_{ED\_LIN} = (1 + g_E)V_E + g_E V_{DM}$$

Where:

$$g_E = \frac{V_3 - V_1}{V_{DMH} - V_{DML}} - 1$$

$$V_E = \frac{V_2}{1 + g_E}$$

Note that the V_E value measured here is not as accurate as the one obtained in **Section 1.5.1 "Input Offset Related Errors"**.

The remaining error (ΔV_{ED}) is described by the Differential Mode Non-Linearity spec:

EQUATION 1-12:

$$INL_{DM} = \frac{max|\Delta V_{ED}|}{V_{DMH} - V_{DML}}$$

Where:

$$\Delta V_{ED} = V_{ED} - V_{ED\_LIN}$$

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

2.1 DC Voltages and Currents

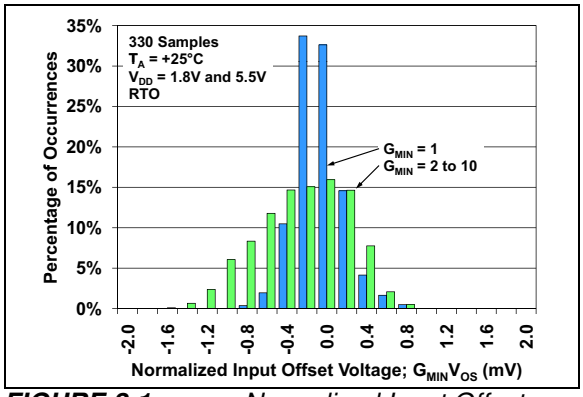


FIGURE 2-1: *Normalized Input Offset Voltage, with G_{MIN} = 1 to 10.*

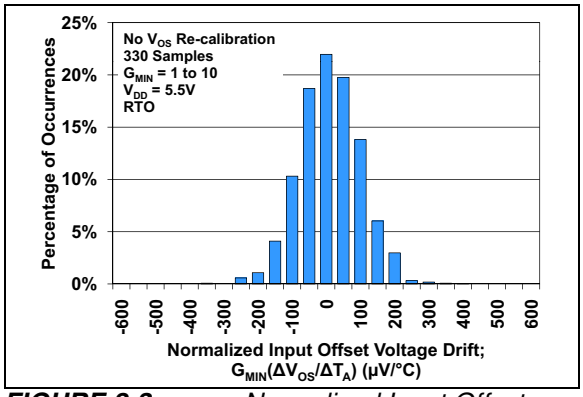


FIGURE 2-3: *Normalized Input Offset Voltage Drift, with G_{MIN} = 1 to 10.*

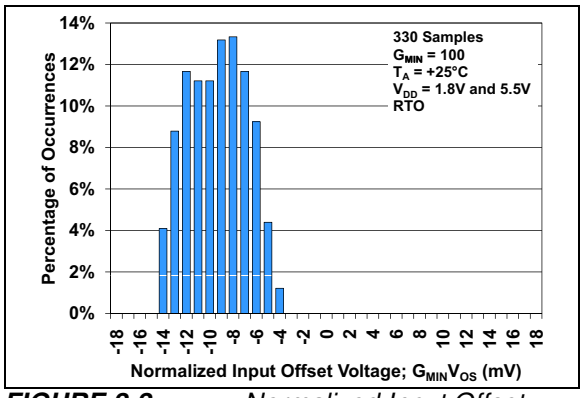


FIGURE 2-2: *Normalized Input Offset Voltage, with G_{MIN} = 100.*

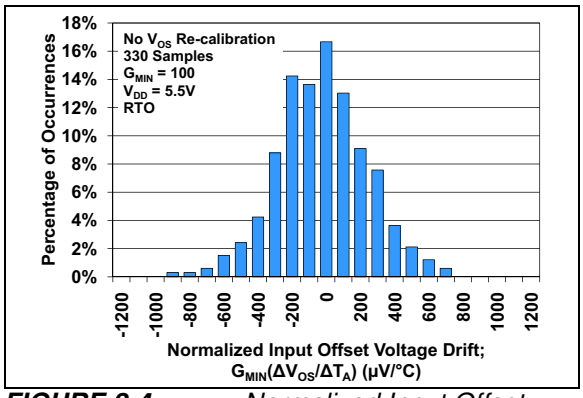


FIGURE 2-4: *Normalized Input Offset Voltage Drift, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = $V_{DD}/2$, V_{DM} = 0V, V_{REF} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

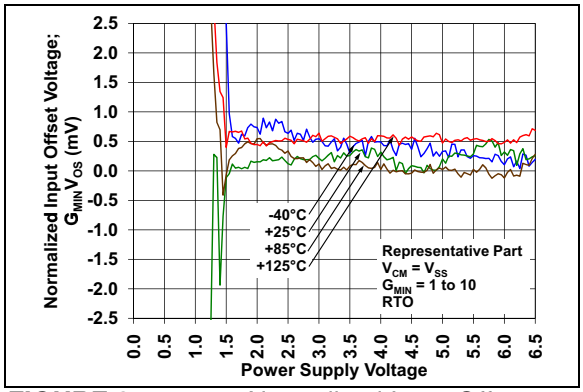


FIGURE 2-5: *Normalized Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 1 to 10.*

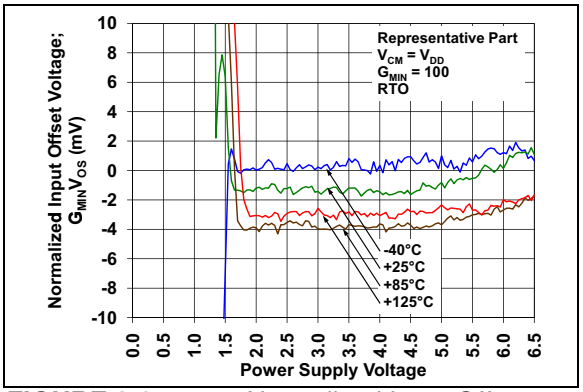


FIGURE 2-8: *Normalized Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 100.*

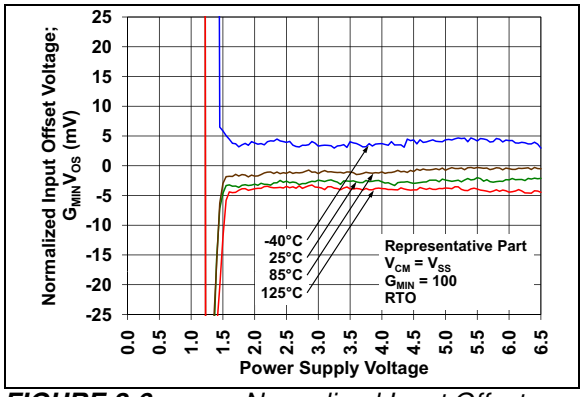


FIGURE 2-6: *Normalized Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 100.*

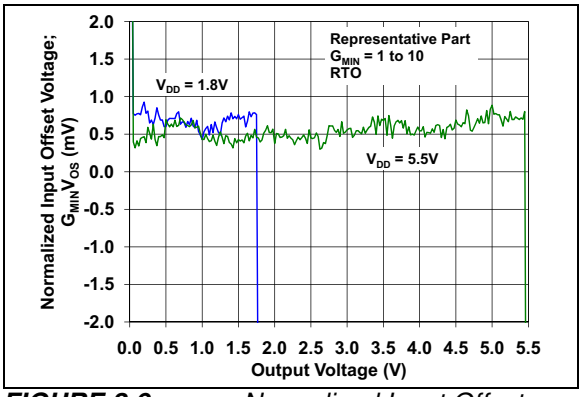


FIGURE 2-9: *Normalized Input Offset Voltage vs. Output Voltage, with G_{MIN} = 1 to 10.*

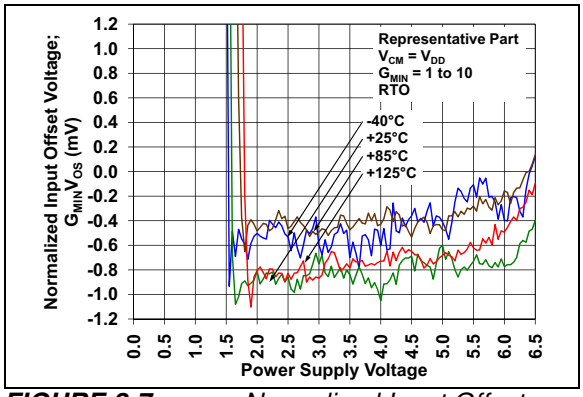


FIGURE 2-7: *Normalized Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 1 to 10.*

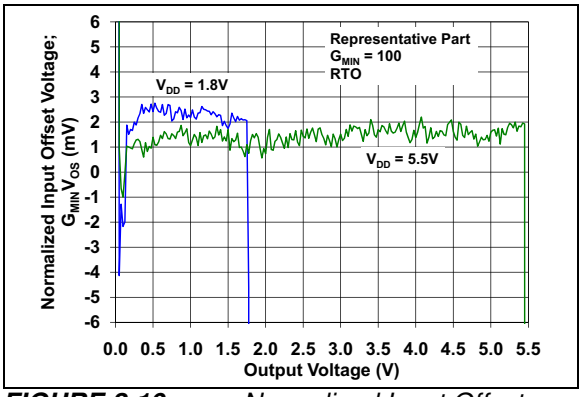


FIGURE 2-10: *Normalized Input Offset Voltage vs. Output Voltage, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

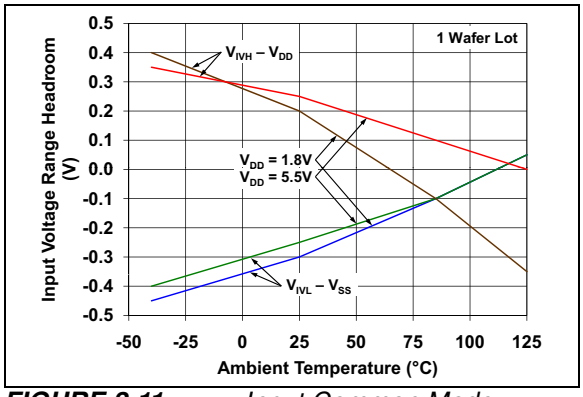


FIGURE 2-11: *Input Common Mode Voltage Headroom vs. Ambient Temperature.*

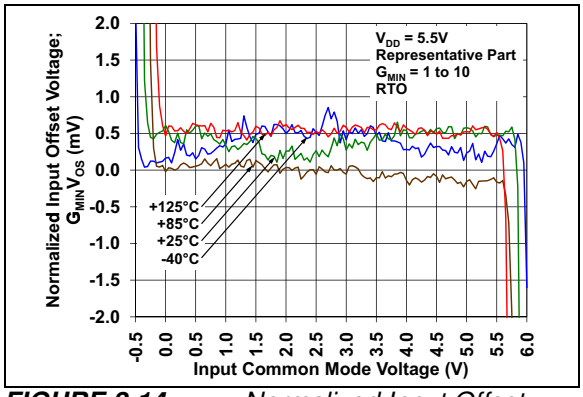


FIGURE 2-14: *Normalized Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 1 to 10.*

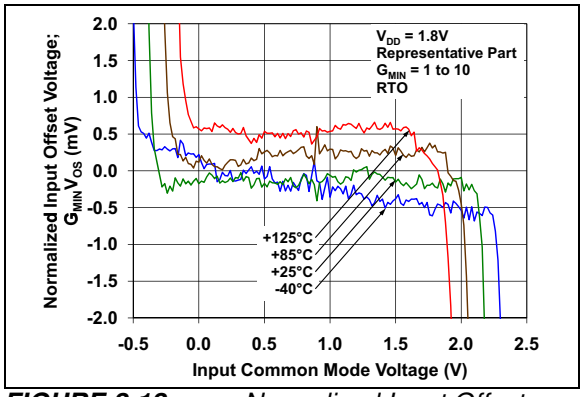


FIGURE 2-12: *Normalized Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 1 to 10.*

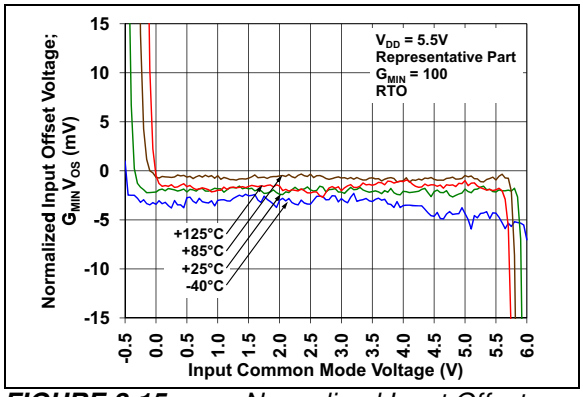


FIGURE 2-15: *Normalized Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 100.*

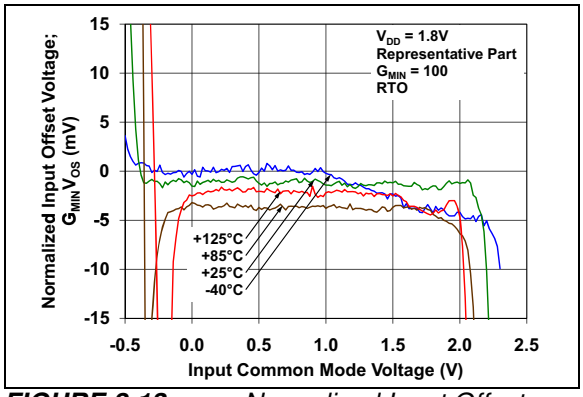


FIGURE 2-13: *Normalized Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 100.*

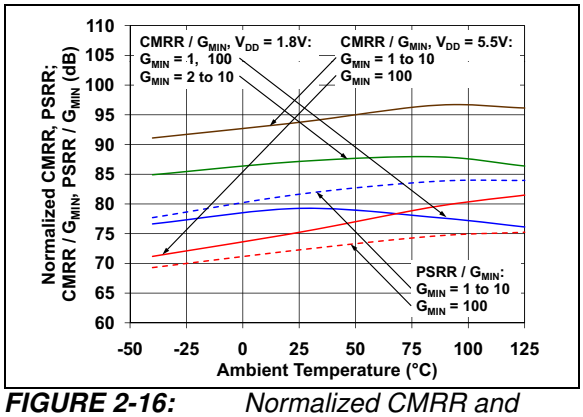


FIGURE 2-16: *Normalized CMRR and PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

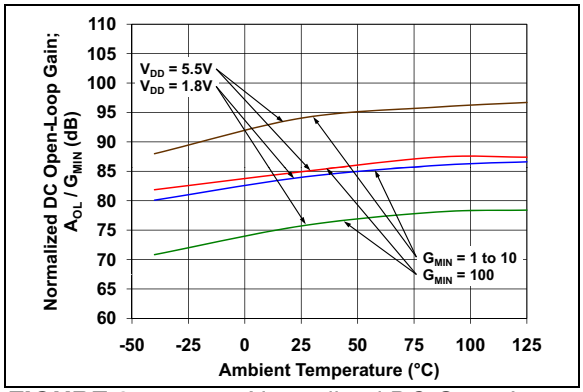


FIGURE 2-17: *Normalized DC Open-Loop Gain vs. Ambient Temperature.*

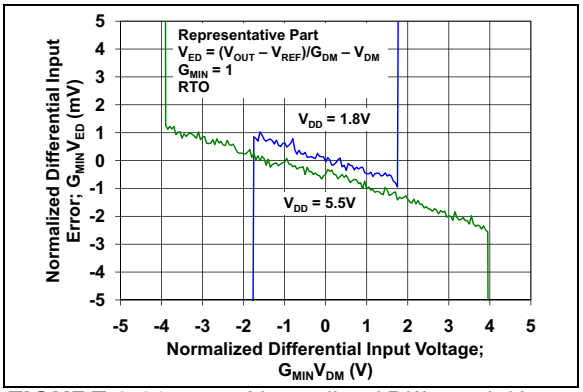


FIGURE 2-20: *Normalized Differential Input Error vs. Differential Voltage, with G_{MIN} = 1.*

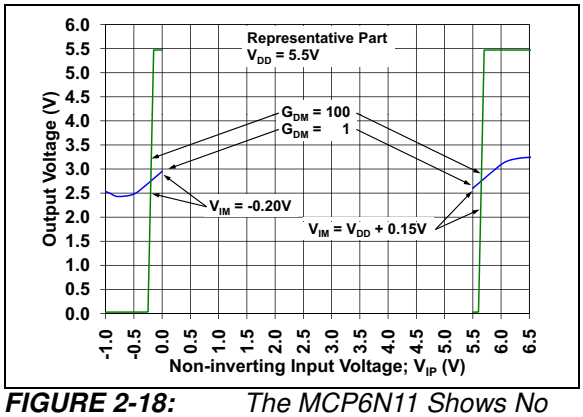


FIGURE 2-18: *The MCP6N11 Shows No Phase Reversal vs. Common Mode Voltage.*

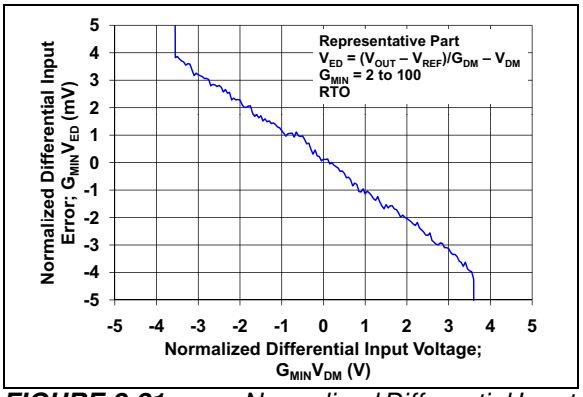


FIGURE 2-21: *Normalized Differential Input Error vs. Differential Voltage, with G_{MIN} = 2 to 100.*

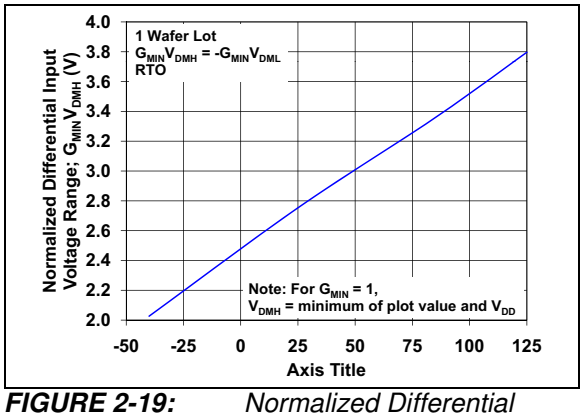


FIGURE 2-19: *Normalized Differential Mode Voltage Range vs. Ambient Temperature.*

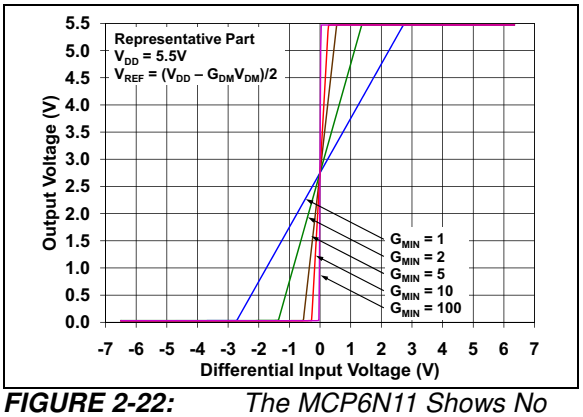


FIGURE 2-22: *The MCP6N11 Shows No Phase Reversal vs. Differential Voltage, with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

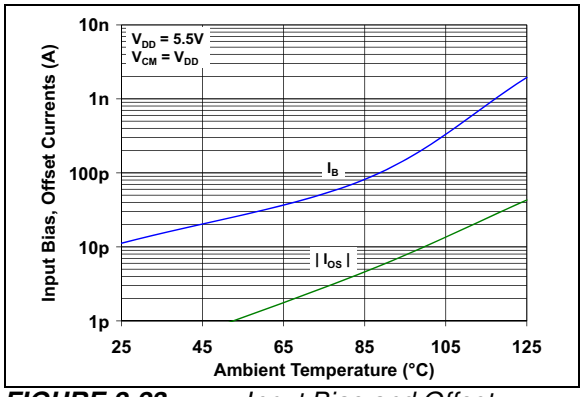


FIGURE 2-23: *Input Bias and Offset Currents vs. Ambient Temperature, with V_{DD} = +5.5V.*

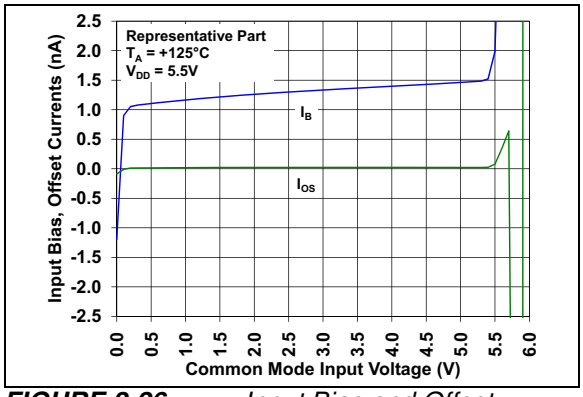


FIGURE 2-26: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +125°C.*

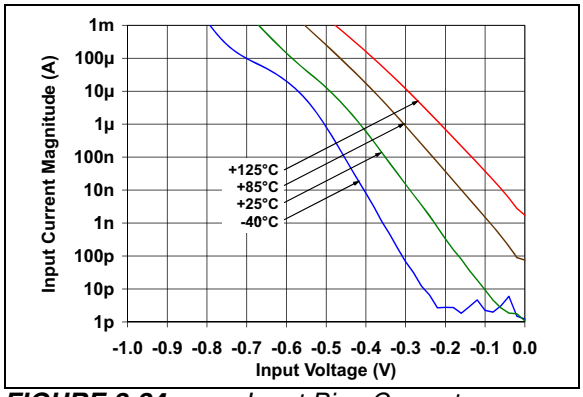


FIGURE 2-24: *Input Bias Current vs. Input Voltage (below V_{SS}).*

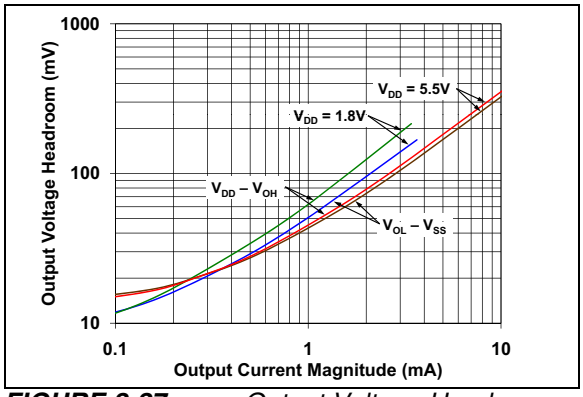


FIGURE 2-27: *Output Voltage Headroom vs. Output Current.*

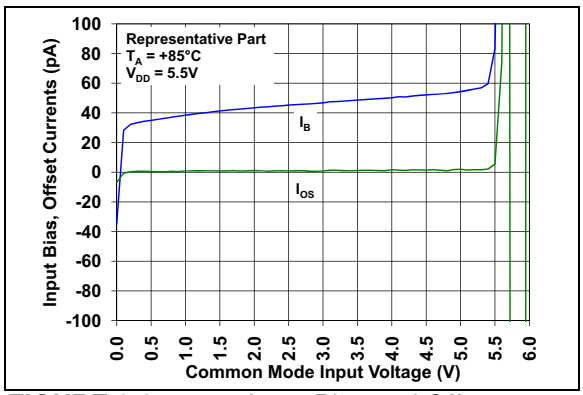


FIGURE 2-25: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +85°C.*

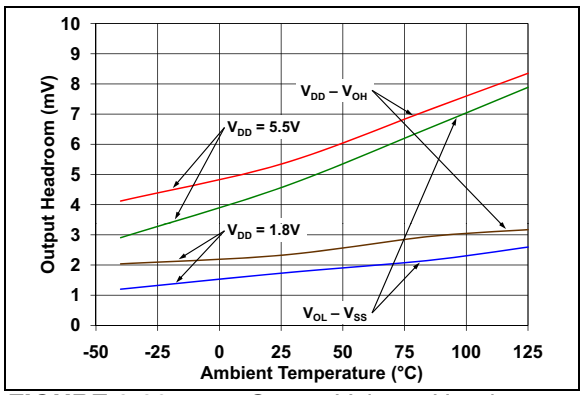


FIGURE 2-28: *Output Voltage Headroom vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

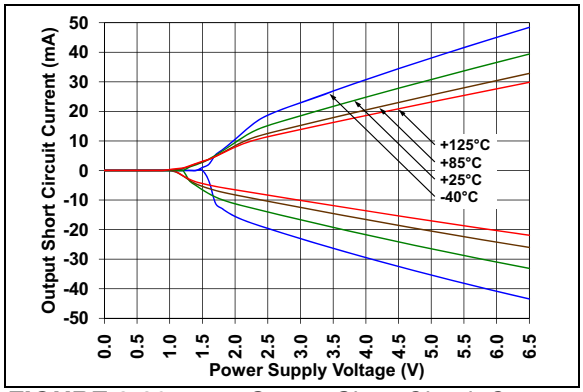


FIGURE 2-29: *Output Short Circuit Current vs. Power Supply Voltage.*

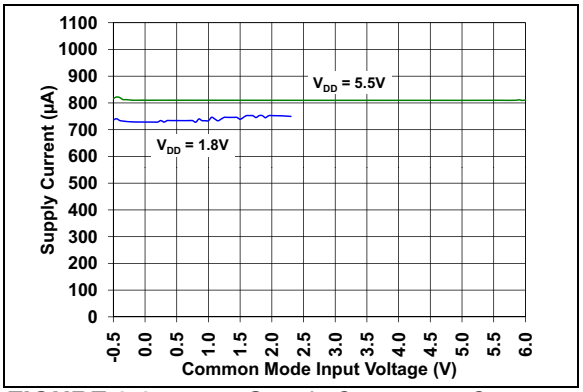


FIGURE 2-31: *Supply Current vs. Common Mode Input Voltage.*

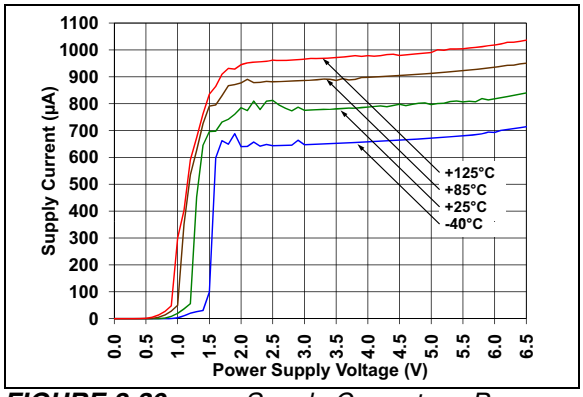


FIGURE 2-30: *Supply Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

2.2 Frequency Response

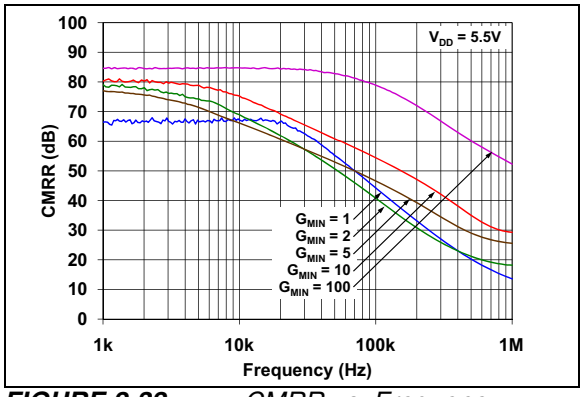


FIGURE 2-32: *CMRR vs. Frequency.*

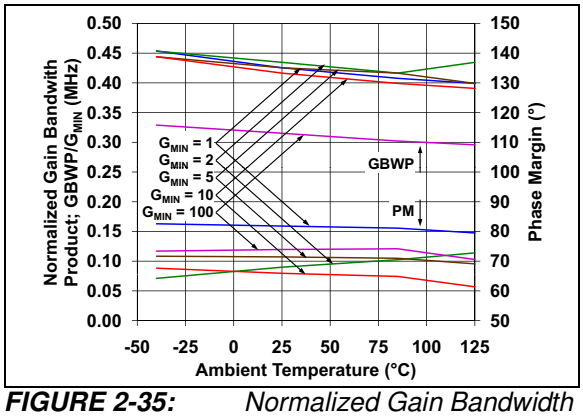


FIGURE 2-35: *Normalized Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.*

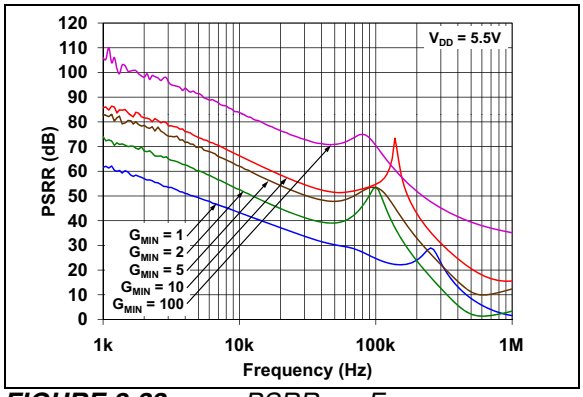


FIGURE 2-33: *PSRR vs. Frequency.*

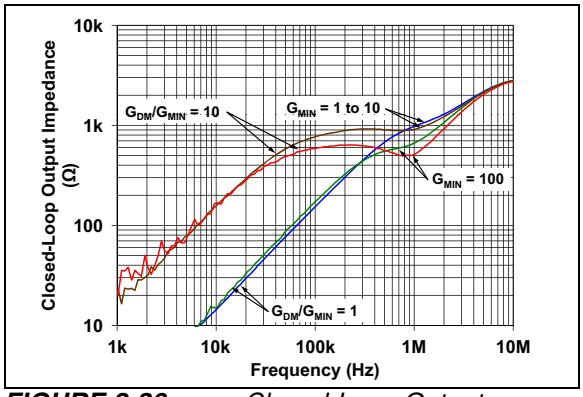


FIGURE 2-36: *Closed-Loop Output Impedance vs. Frequency.*

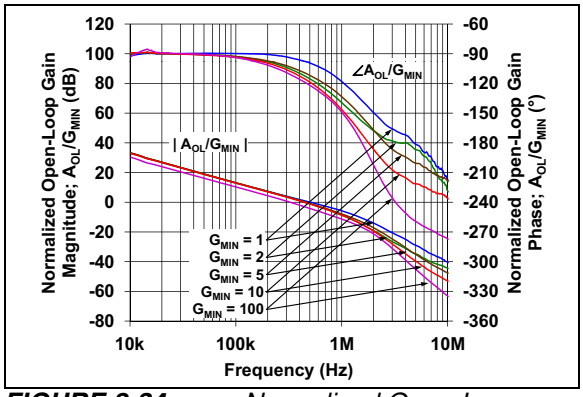


FIGURE 2-34: *Normalized Open-Loop Gain vs. Frequency.*

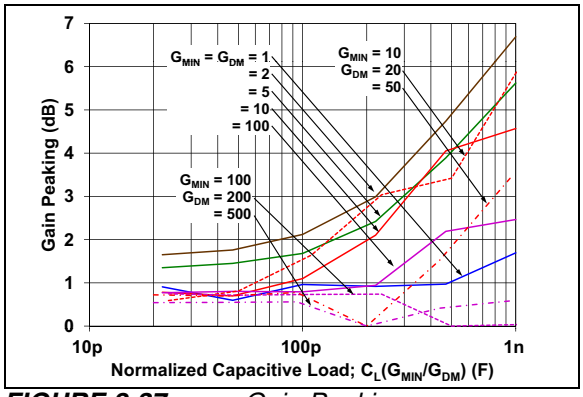


FIGURE 2-37: *Gain Peaking vs. Normalized Capacitive Load.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = $V_{DD}/2$, V_{DM} = 0V, V_{REF} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

2.3 Noise

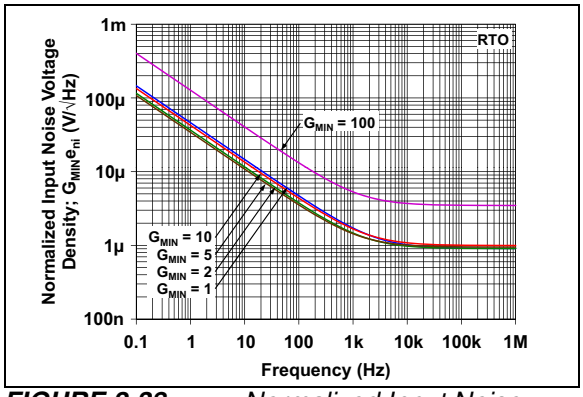


FIGURE 2-38: *Normalized Input Noise Voltage Density vs. Frequency.*

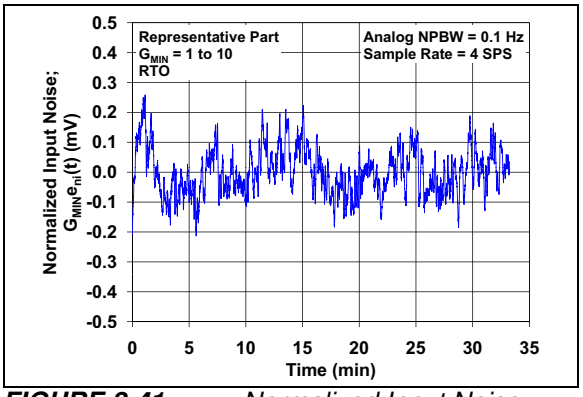


FIGURE 2-41: *Normalized Input Noise Voltage vs. Time, with G_{MIN} = 1 to 10.*

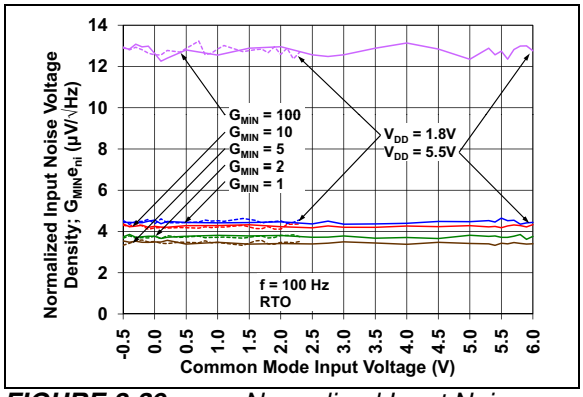


FIGURE 2-39: *Normalized Input Noise Voltage Density vs. Input Common Mode Voltage, with f = 100 Hz.*

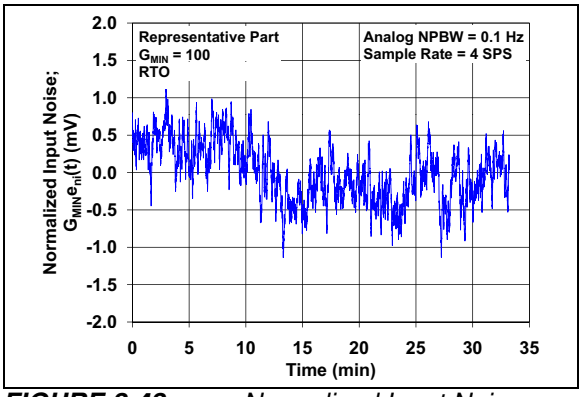


FIGURE 2-42: *Normalized Input Noise Voltage vs. Time, with G_{MIN} = 100.*

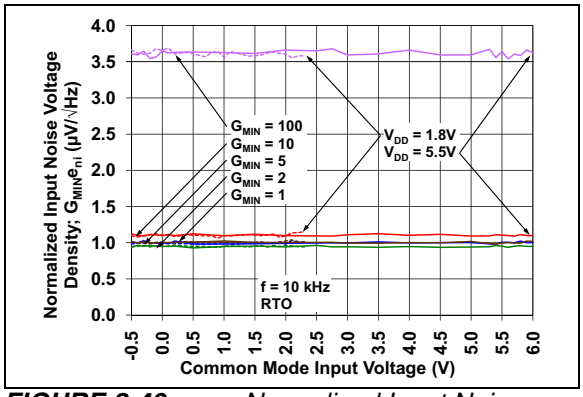


FIGURE 2-40: *Normalized Input Noise Voltage Density vs. Input Common Mode Voltage, with f = 10 kHz.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

2.4 Time Response

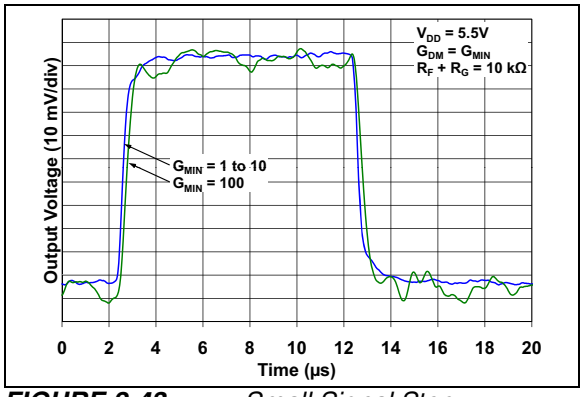


FIGURE 2-43: *Small Signal Step Response.*

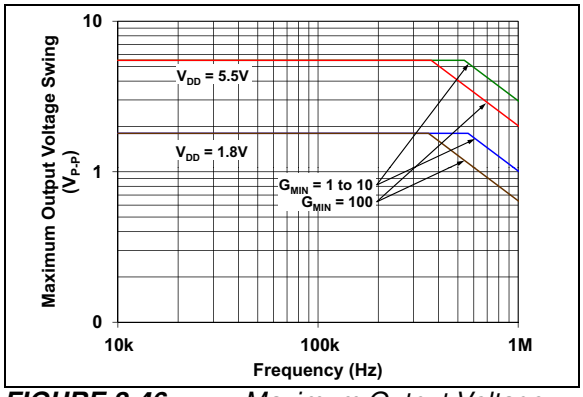


FIGURE 2-46: *Maximum Output Voltage Swing vs. Frequency.*

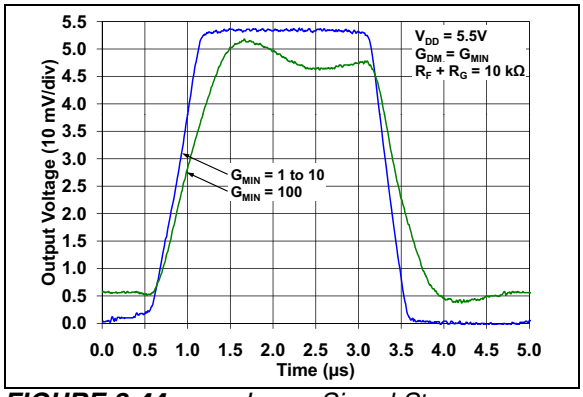


FIGURE 2-44: *Large Signal Step Response.*

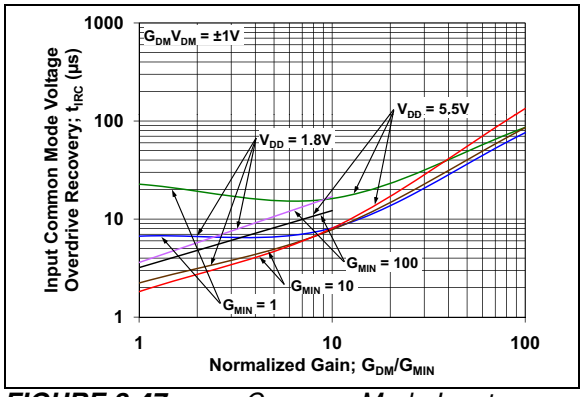


FIGURE 2-47: *Common Mode Input Overdrive Recovery Time vs. Normalized Gain.*

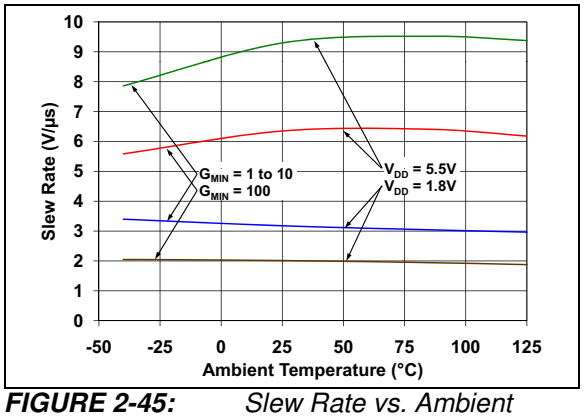


FIGURE 2-45: *Slew Rate vs. Ambient Temperature.*

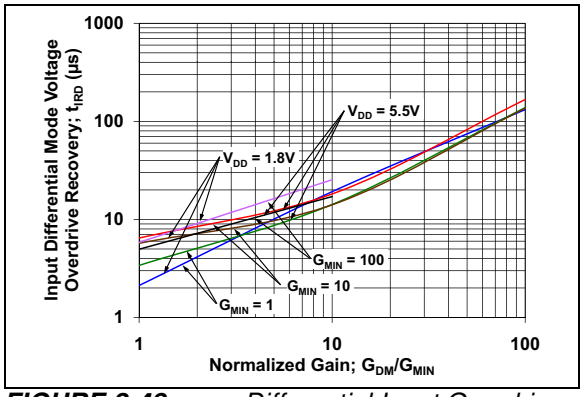


FIGURE 2-48: *Differential Input Overdrive Recovery Time vs. Normalized Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

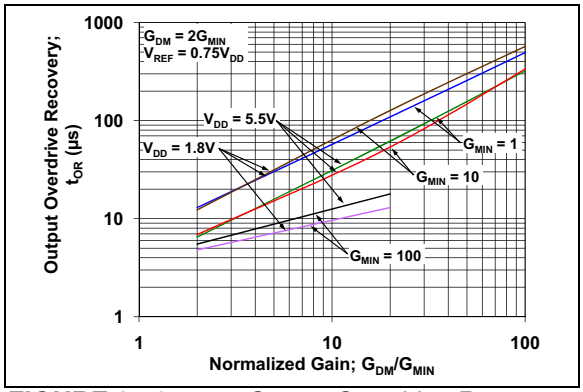


FIGURE 2-49: *Output Overdrive Recovery Time vs. Normalized Gain.*

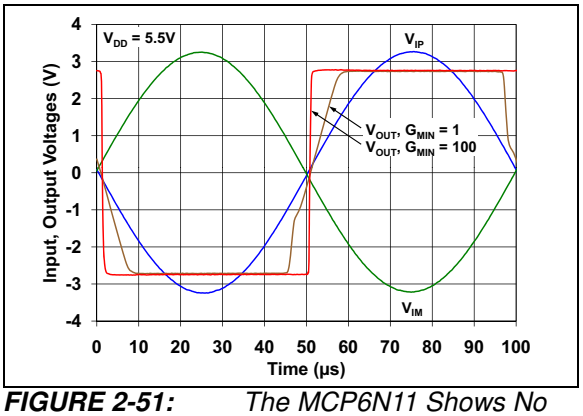


FIGURE 2-51: *The MCP6N11 Shows No Phase Reversal vs. Differential Input Overdrive, with V_{DD} = 5.5V.*

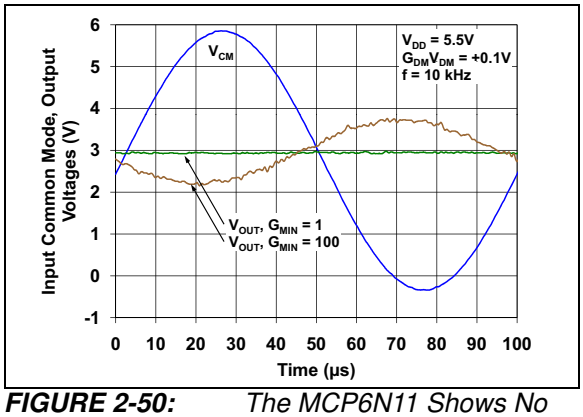


FIGURE 2-50: *The MCP6N11 Shows No Phase Reversal vs. Common Mode Input Overdrive, with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

2.5 Enable/Calibration and POR Responses

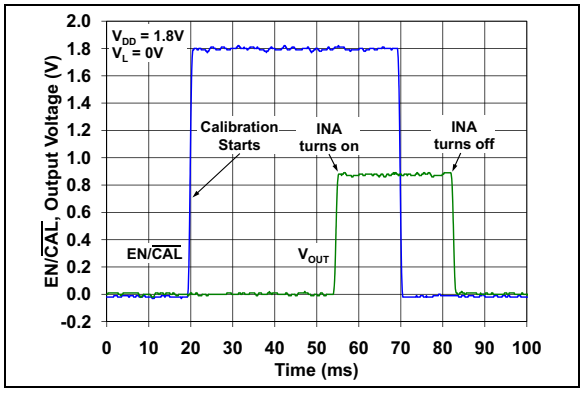


FIGURE 2-52: *EN/$\overline{CAL}$ and Output Voltage vs. Time, with V_{DD} = 1.8V.*

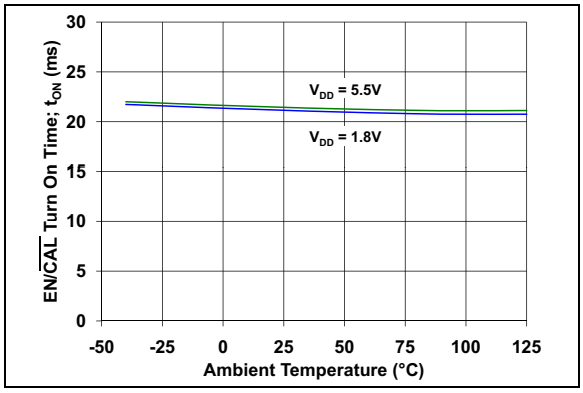


FIGURE 2-55: *EN/$\overline{CAL}$ Turn On Time vs. Ambient Temperature.*

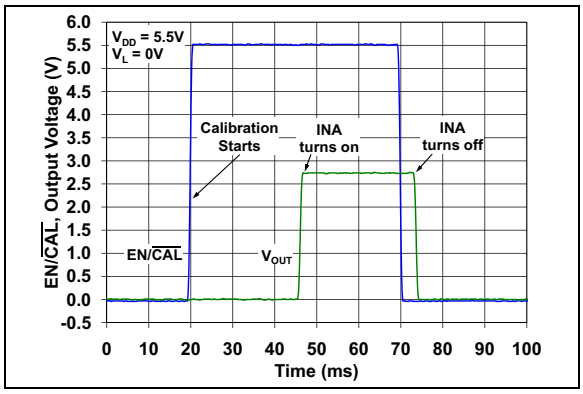


FIGURE 2-53: *EN/$\overline{CAL}$ and Output Voltage vs. Time, with V_{DD} = 5.5V*

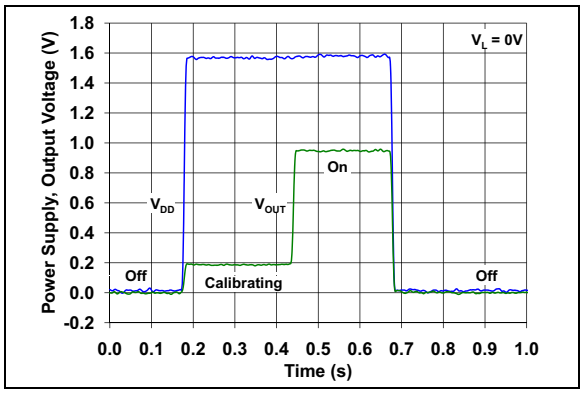


FIGURE 2-56: *Power Supply On and Off and Output Voltage vs. Time.*

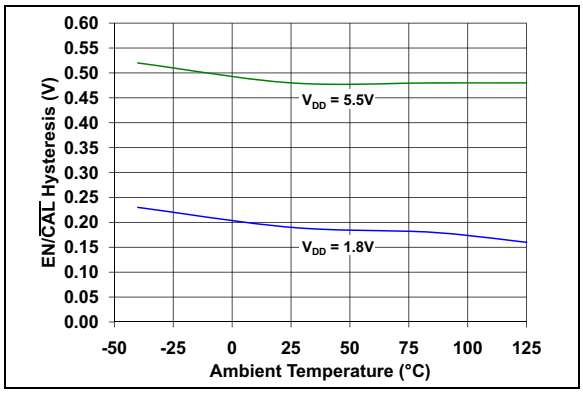


FIGURE 2-54: *EN/$\overline{CAL}$ Hysteresis vs. Ambient Temperature.*

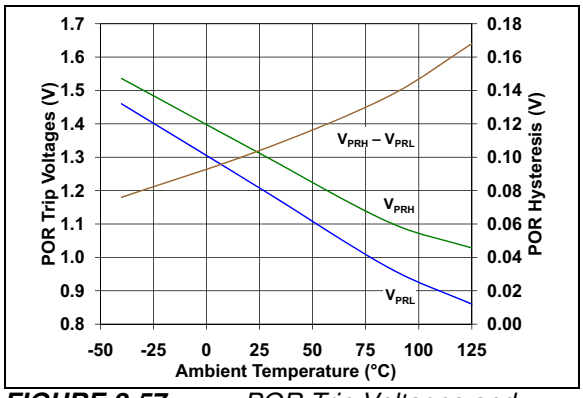


FIGURE 2-57: *POR Trip Voltages and Hysteresis vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, EN/$\overline{CAL}$ = V_{DD}, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and G_{DM} = G_{MIN}; see Figure 1-6 and Figure 1-7.

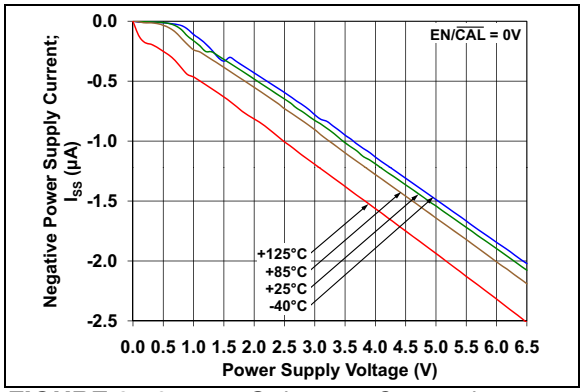


FIGURE 2-58: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

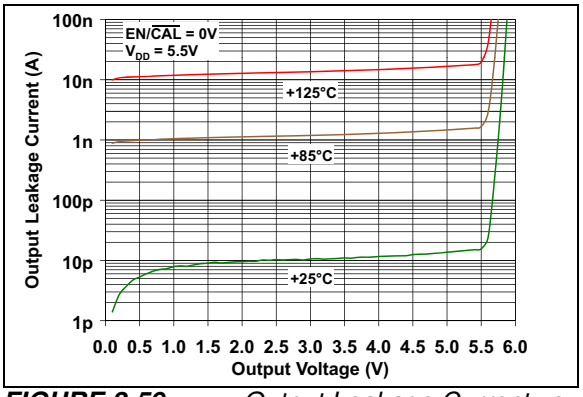


FIGURE 2-59: *Output Leakage Current vs. Output Voltage.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6N11		Symbol	Description
SOIC	TDFN		
1	1	V_{FG}	Feedback Input
2	2	V_{IM}	Inverting Input
3	3	V_{IP}	Non-inverting Input
4	4	V_{SS}	Negative Power Supply
5	5	V_{REF}	Reference Input
6	6	V_{OUT}	Output
7	7	V_{DD}	Positive Power Supply
8	8	EN/$\overline{CAL}$	Enable/V_{OS} Calibrate Digital Input
—	9	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}

3.1 Analog Signal Inputs

The non-inverting and inverting inputs (V_{IP}, and V_{IM}) are high-impedance CMOS inputs with low bias currents.

3.2 Analog Feedback Input

The analog feedback input (V_{FG}) is the inverting input of the second input stage. The external feedback components (R_F and R_G) are connected to this pin. It is a high-impedance CMOS input with low bias current.

3.3 Analog Reference Input

The analog reference input (V_{REF}) is the non-inverting input of the second input stage; it shifts V_{OUT} to its desired range. The external gain resistor (R_G) is connected to this pin. It is a high-impedance CMOS input with low bias current.

3.4 Analog Output

The analog output (V_{OUT}) is a low-impedance voltage output. It represents the differential input voltage ($V_{DM} = V_{IP} – V_{IM}$), with gain G_{DM} and is shifted by V_{REF}. The external feedback resistor (R_F) is connected to this pin.

3.5 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply; V_{DD} will need bypass capacitors.

3.6 Digital Enable and V_{OS} Calibration Input

This input (EN/$\overline{CAL}$) is a CMOS, Schmitt-triggered input that controls the active, low power and V_{OS} calibration modes of operation. When this pin goes low, the part is placed into a low power mode and the output is high-Z. When this pin goes high, the amplifier's input offset voltage is corrected by the calibration circuitry, then the output is re-connected to the V_{OUT} pin, which becomes low impedance, and the part resumes normal operation.

3.7 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).