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MCP6N16

Zero-Drift Instrumentation Amplifier

Features:

- High DC Precision:
  - V_{OS}: ±17 µV (maximum, G_{MIN} = 100)
  - TC_1: ±60 nV/°C (maximum, G_{MIN} = 100)
  - CMRR: 112 dB (minimum, G_{MIN} = 100, V_{DD} = 5.5V)
  - PSRR: 110 dB (minimum, G_{MIN} = 100, V_{DD} = 5.5V)
  - g_E: ±0.15% (maximum, G_{MIN} = 10, 100)
- Flexible:
  - Minimum Gain (G_{MIN}) Options: 1, 10 and 100 V/V
  - Rail-to-Rail Input and Output
  - Gain Set by Two External Resistors
- Bandwidth: 500 kHz (typical, Gain = G_{MIN} = 1, 10)
- Power Supply:
  - V_{DD}: 1.8V to 5.5V
  - I_Q: 1.1 mA (typical)
  - Power Savings (Enable) Pin: EN
- Enhanced EMI Protection:
  - Electromagnetic Interference Rejection Ratio (EMIRR): 111 dB at 2.4 GHz
- Extended Temperature Range: -40°C to +125°C

Typical Applications:

- High-Side Current Sensor
- Wheatstone Bridge Sensors
- Difference Amplifier with Level Shifting
- Power Control Loops

Design Aids:

- SPICE Macro Model
- Microchip Advanced Part Selector (MAPS)
- Application Notes

Description:

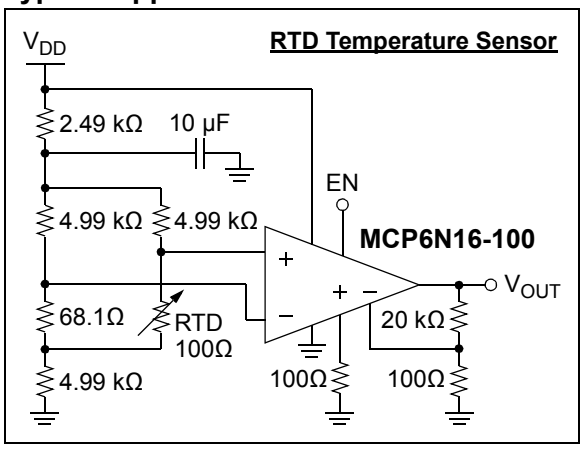
Microchip Technology Inc. offers the single Zero-Drift MCP6N16 instrumentation amplifier (INA) with Enable pin (EN) and three minimum gain options (G_{MIN}). The internal offset correction gives high DC precision: it has very low offset and offset drift, and negligible 1/f noise.

Two external resistors set the gain, minimizing gain error and drift over temperature. The reference voltage (V_{REF}) shifts the output voltage (V_{OUT}).

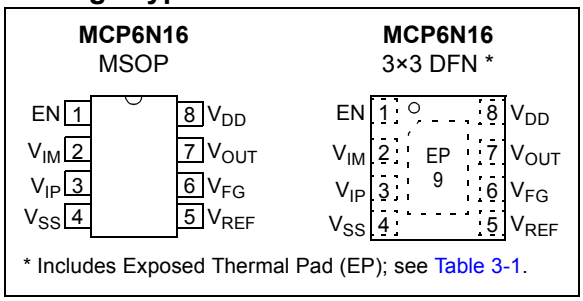
The MCP6N16 is designed for single-supply operation, with rail-to-rail input (no common mode crossover distortion) and output performance. The supply voltage range (1.8V to 5.5V) is low enough to support many portable applications. All devices are fully specified from -40°C to +125°C. Each part has EMI filters at the input pins, for good EMI rejection (EMIRR).

These parts have three minimum gain options (1, 10 and 100 V/V). This allows the user to optimize the input offset voltage and input noise for different applications.

Typical Application Circuit



Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Minimum Gain Options

Table 1 shows key specifications that differentiate between the different minimum gain (G_{MIN}) options. See **Section 1.0 "Electrical Characteristics"**, **Section 6.0 "Packaging Information"** and Product Identification System for further information on G_{MIN}.

TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS

Part No.	G_{MIN} (V/V) Nom.	V_{OS} (±µV) Max.	TC_1 (±nV/°C) Max. T_A = -40 to +125°C	CMRR (dB) Min. V_{DD} = 5.5V	PSRR (dB) Min.	V_{DMH} (V) Min.	GBWP (MHz) Typ.	E_{ni} (μV_{P-P}) Typ. f = 0.1 to 10 Hz	e_{ni} (nV/√Hz) Typ. f < 500 Hz
MCP6N16-001	1	85	1800	89	91	2.7	0.50	19	900
MCP6N16-010	10	22	180	103	104	0.27	5.0	2.2	105
MCP6N16-100	100	17	60	112	110	0.027	35	0.93	45

Note 1: G_{MIN} is the minimum stable gain (G_{DM}), for a given part option. In other words, $G_{DM} \geq G_{MIN}$.

Figures 1 to 3 show input offset voltage versus temperature for the three gain options (G_{MIN} = 1, 10, 100 V/V).

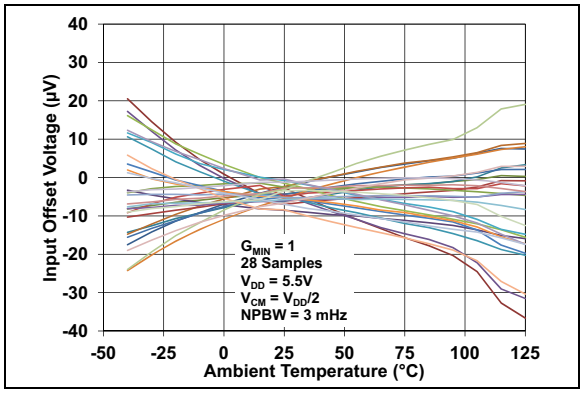


FIGURE 1: *Input Offset Voltage vs. Temperature, with G_{MIN} = 1.*

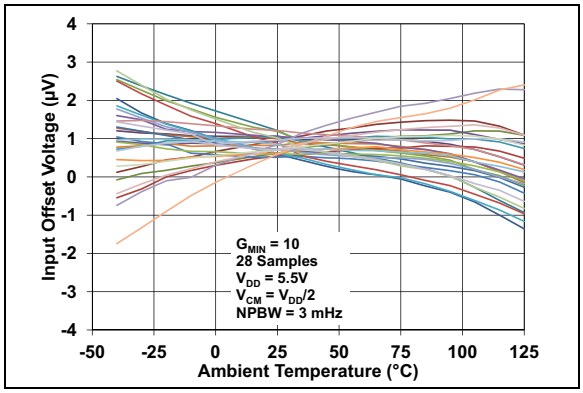


FIGURE 2: *Input Offset Voltage vs. Temperature, with G_{MIN} = 10.*

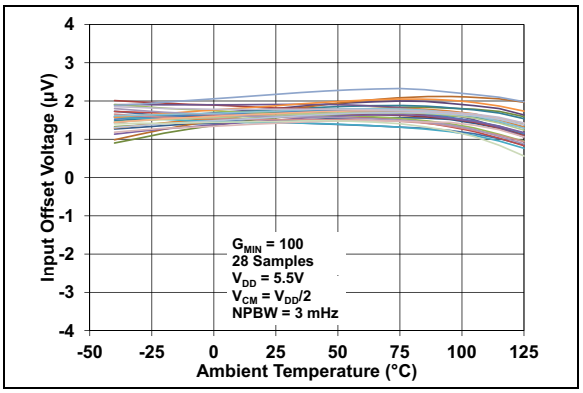


FIGURE 3: *Input Offset Voltage vs. Temperature, with G_{MIN} = 100.*

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 6.5V

Current at Input Pins **(Note 1)** ..... ±2 mA

Analog Inputs (V_{IP} and V_{IM}) **(Note 1)** ..... V_{SS} – 1.0V to V_{DD} + 1.0V

All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V

Difference Input Voltage ..... $|V_{DD} – V_{SS}|$

Output Short-Circuit Current ..... Continuous

Current at Output and Supply Pins ..... ±30 mA

Storage Temperature ..... -65°C to +150°C

Maximum Junction Temperature ..... +150°C

ESD protection on all pins (HBM, MM) ..... ≥ 4 kV, 400V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: See **Section 4.3.1.2 “Input Voltage Limits”** and **Section 4.3.1.3 “Input Current Limits”**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Input Offset							
Input Offset Voltage	V_{OS}	-85	—	+85	µV	1	T_A = +25°C
		-22	—	+22		10	
		-17	—	+17		100	
Input Offset Voltage Drift – Linear Temp. Co.	TC_1	-1800	—	+1800	nV/°C	1	T_A = -40°C to +125°C **(Note 2)**
		-180	—	+180		10	
		-60	—	+60		100	
Input Offset Voltage Drift – Quadratic Temp. Co.	TC_2	—	±560	—	pV/°C^2	1	T_A = -40°C to +125°C
		—	±63	—		10	
		—	±69	—		100	
Input Offset Aging	ΔV_{OS}	—	±1.0	—	µV	1	408 hr Life Test at +150°C, measured at +25°C
		—	±0.8	—		10	
		—	±0.7	—		100	
Power Supply Rejection Ratio	PSRR	91	109	—	dB	1	
		104	122	—		10	
		110	128	—		100	
Output Offset							
Output Offset Voltage	V_{OSO}		0		µV	all	
Input Current and Impedance (Note 3)							
Input Bias Current	I_B	-100	±2	+100	pA	all	
Across Temperature		—	20	—			T_A = +85°C
Across Temperature		0	250	2000			T_A = +125°C

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Input Offset Current	I_{OS}	-800	±300	+800	pA	all	
Across Temperature		—	±320	—			T_A = +85°C
Across Temperature		-1500	±350	+1500			T_A = +125°C
Common Mode Input Impedance	Z_{CM}	—	10^{13}||10	—	Ω||pF		
Differential Input Impedance	Z_{DIFF}	—	10^{13}||4	—			
Input Common Mode Voltage (V_{CM} or V_{REF}) (Note 3)							
Input Voltage Range **(Note 4, Note 5)**	V_{IVL}	—	V_{SS} – 0.25	V_{SS} – 0.15	V	all	
	V_{IVH}	V_{DD} + 0.15	V_{DD} + 0.30	—			
Common Mode Rejection Ratio	CMRR	80	98	—	dB	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 1.8V
		94	112	—		10	
		103	121	—		100	
		89	107	—		1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 5.5V
		103	121	—		10	
		112	130	—		100	
Common Mode Rejection Ratio at V_{REF}	CMRR2	83	101	—	dB	1	V_{REF} = 0.2V to V_{DD} – 0.2V, V_{DD} = 1.8V
		98	116	—		10	
		102	120	—		100	
		94	112	—		1	V_{REF} = 0.2V to V_{DD} – 0.2V, V_{DD} = 5.5V
		109	127	—		10	
		115	133	—		100	

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 (**Note 1**).

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Common Mode Nonlinearity (**Note 6**)	INL_{CM}	-550	—	+550	ppm	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 1.8V
		-75	—	+75		10	
		-20	—	+20		100	
		-310	—	+310		1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 5.5V
		-35	—	+35		10	
		-10	—	+10		100	
Input Differential Voltage (V_{DM}) (Note 3)							
Differential Input Voltage Range (**Note 5**)	V_{DML}	—	-3.4/G_{MIN}	-2.7/G_{MIN}	V	all	V_{DD} ≥ 2.9V, V_{REF} = V_{DD}, V_{OUT} within ±0.2%
	V_{DMH}	+2.7/G_{MIN}	+3.4/G_{MIN}	—			V_{DD} ≥ 2.9V, V_{REF} = 0V, V_{OUT} within ±0.2%
Differential Gain Error (**Note 6**)	g_E	—	±0.03	—	%	1	V_{DD} = 1.8V, V_{REF} = V_{DD}/2, V_{DM} = ±(0.7V)/G_{MIN}
		—	±0.02	—	%	10, 100	
		—	±0.03	—		1	V_{DD} = 5.5V, V_{REF} = V_{DD}/2, V_{DM} = ±(2.55V)/G_{MIN}
		—	±0.02	—		10, 100	
		-0.25	±0.04	+0.25	%	1	V_{DD} = 5.5V, V_{REF} = 0.2V, V_{DM} = 0 to (2.7V)/G_{MIN}
		-0.15	±0.02	+0.15	%	10, 100	
		-0.25	±0.04	+0.25	%	1	V_{DD} = 5.5V, V_{REF} = 5.3V, V_{DM} = 0 to (-2.7V)/G_{MIN}
		-0.15	±0.02	+0.15	%	10, 100	

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Differential Gain Drift **(Note 6)**	$\Delta g_E/\Delta T_A$	—	±3	—	ppm/°C	all	V_{DD} = 1.8V, V_{REF} = V_{DD}/2, V_{DM} = ±(0.7V)/G_{MIN}
		—	±4	—			V_{DD} = 5.5V, V_{REF} = V_{DD}/2, V_{DM} = ±(2.55V)/G_{MIN}
		—	±4	—			V_{DD} = 5.5V, V_{REF} = 0.2V, V_{DM} = 0 to (2.7V)/G_{MIN}
		—	±3	—			V_{DD} = 5.5V, V_{REF} = 5.3V, V_{DM} = 0 to (-2.7V)/G_{MIN}
Differential Nonlinearity **(Note 6)**	INL_{DM}	—	±300	—	ppm	all	V_{DD} = 1.8V, V_{REF} = V_{DD}/2, V_{DM} = ±(0.7V)/G_{MIN}
		—	±150	—			V_{DD} = 5.5V, V_{REF} = V_{DD}/2, V_{DM} = ±(2.55V)/G_{MIN}
		—	±300	—			V_{DD} = 5.5V, V_{REF} = 0.2V, V_{DM} = 0 to (2.7V)/G_{MIN}
		—	±300	—			V_{DD} = 5.5V, V_{REF} = 5.3V, V_{DM} = 0 to (-2.7V)/G_{MIN}
DC Open-Loop Gain	A_{OL}	84	102	—	dB	1	V_{DD} = 1.8V, V_{OUT} = 0.2V to 1.6V
		100	118	—		10	
		108	126	—		100	
		95	113	—		1	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V
		111	129	—		10	
		119	137	—		100	

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Output							
Minimum Output Voltage Swing	V_{OL}	—	V_{SS} + 3	—	mV	all	R_L = 10 kΩ, V_{DD} = 1.8V, V_{DM} = -V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 – 0.9V
		—	V_{SS} + 6	—			R_L = 10 kΩ, V_{DD} = 5.5V, V_{DM} = -V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 – 1V
		—	V_{SS} + 60	V_{SS} + 250			R_L = 1 kΩ, V_{DD} = 5.5V, V_{DM} = -V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 – 1V
Maximum Output Voltage Swing	V_{OH}	—	V_{DD} – 3	—	mV		R_L = 10 kΩ, V_{DD} = 1.8V, V_{DM} = V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 + 0.9V
		—	V_{DD} – 6	—			R_L = 10 kΩ, V_{DD} = 5.5V, V_{DM} = V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 + 1V
		V_{DD} – 250	V_{DD} – 60	—			R_L = 1 kΩ, V_{DD} = 5.5V, V_{DM} = V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 + 1V
Output Short-Circuit Current	I_{SC}	—	±10	—	mA		V_{DD} = 1.8V
		—	±35	—			V_{DD} = 5.5V
Power Supply							
Supply Voltage	V_{DD}	1.8	—	5.5	V	all	
Quiescent Current per Amplifier	I_Q	0.5	1.1	1.6	mA		I_O = 0
POR Trip Voltage	V_{PRL}	0.9	1.27	—	V		
	V_{PRH}	—	1.33	1.6	V		

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
AC Response							
Gain-Bandwidth Product	GBWP	—	0.5	—	MHz	1	
		—	5	—		10	
		—	35	—		100	
Phase Margin	PM	—	70	—	°	all	
Open-Loop Output Impedance	R_{OL}	—	1.6	—	kΩ		
Power Supply Rejection Ratio	PSRR	—	80	—	dB	1	f = 1 kHz
		—	98	—		10	
		—	123	—		100	
Common Mode Rejection Ratio at V_{CM} and V_{REF}	CMRR, CMRR2	—	83	—	dB	1	f = 10 kHz
		—	80	—		10	
		—	140	—		100	
Step Response (see **Section 4.1.4 "AC Performance"**)							
Slew Rate	SR	**Note 1**			V/µs	all	
Start-Up Time	t_{STR}	—	2	—	ms	1	G_{DM} = 1000, V_{DD} power up to 0.1% V_{OUT} settling **(Note 3, Note 4)**
		—	0.3	—		10	
		—	0.2	—		100	
Overdrive Recovery, Input Common Mode	t_{IRC}	—	1	—	µs	all	V_{IP} = V_{IM} = V_{IVH} + 0.5V to V_{DD} – 1V (or V_{IVL} – 0.5V to 1V), 90% of V_{OUT} change (I_B ≤ 2 mA) **(Note 4)**
Overdrive Recovery, Input Differential Mode	t_{IRD}	—	10	—			$G_{MIN}V_{DM}$ = $G_{MIN}V_{DMH}$ + 0.5V to 0V (or $G_{MIN}V_{DML}$ – 0.5V to 0V), V_{REF} = 1V (or V_{DD} – 1V), 90% of V_{OUT} change **(Note 4)**
Overdrive Recovery, Output	t_{OR}	—	180	—			$G_{DM}V_{DM}$ = 1.5V to 0V (or -1.5V to 0V), V_{REF} = V_{DD} – 1V (or 1V), 90% of V_{OUT} change **(Note 4)**

Note 1: The slew rate is limited by the GBWP; the large signal step response is dominated by the small signal bandwidth.

2: These parameters were characterized using the circuit in Figure 1-8. In Figures 2-75 and 2-76, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

3: High gains behave differently; see **Section 4.4.4 "Offset at Power-Up"**.

4: t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR} include some uncertainty due to clock edge timing.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Noise							
Input Noise Voltage Density	e_{ni}	—	900	—	nV/√Hz	1	f = 500 Hz
		—	105	—		10	
		—	45	—		100	
Input Noise Voltage	E_{ni}	—	19	—	μV_{P-P}	1	f = 0.1 Hz to 10 Hz
		—	2.2	—		10	
		—	0.93	—		100	
		—	5.9	—		1	f = 0.01 Hz to 1 Hz
		—	0.69	—		10	
		—	0.30	—		100	
Input Current Noise Density	i_{ni}	—	7	—	fA/√Hz	all	f = 1 kHz
Output Noise Voltage Density	e_{no}		0		nV/√Hz		
Output Noise Voltage	E_{no}		0		μV_{P-P}		
Amplifier Distortion (Note 2)							
Intermodulation Distortion (AC)	IMD	—	5	—	μV_{PK}	all	V_{CM} tone = 100 mV_{PK} at 100 Hz
EMI Protection							
EMI Rejection Ratio	EMIRR	—	103	—	dB	all	V_{IN} = 0.1 V_{PK}, f = 400 MHz
		—	106	—			V_{IN} = 0.1 V_{PK}, f = 900 MHz
		—	106	—			V_{IN} = 0.1 V_{PK}, f = 1800 MHz
		—	111	—			V_{IN} = 0.1 V_{PK}, f = 2400 MHz

Note 1: The slew rate is limited by the GBWP; the large signal step response is dominated by the small signal bandwidth.

2: These parameters were characterized using the circuit in Figure 1-8. In Figures 2-75 and 2-76, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

3: High gains behave differently; see **Section 4.4.4 "Offset at Power-Up"**.

4: t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR} include some uncertainty due to clock edge timing.

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
EN Low Specifications							
EN Logic Threshold, Low	V_{IL}	—	—	$0.2V_{DD}$	V	all	
EN Input Current, Low	I_{ENL}	—	-10	—	pA		EN = 0V
GND Current	I_{SS}	-8	-2	—	µA		EN = 0V, V_{DD} = 5.5V
Amplifier Output Leakage	$I_{O(LEAK)}$	—	-1	—	nA		EN = 0V
EN High Specifications							
EN Logic Threshold, High	V_{IH}	$0.8V_{DD}$	—	—	V	all	
EN Input Current, High	I_{ENH}	—	10	—	pA		EN = V_{DD}
EN Dynamic Specifications							
EN Input Hysteresis	V_{HYST}	—	$0.16V_{DD}$	—	V	all	
EN Input Resistance	R_{PD}	—	10^{13}	—	Ω		
EN Low to Amplifier Output High Z Turn-Off Time	t_{OFF}	—	0.1	2	µs		EN = $0.2V_{DD}$ to V_{OUT} = $0.1(V_{DD}/2)$, V_L = 0V
EN High to Amplifier Output On Time	t_{ON}	—	12	100			V_{DD} = 1.8V, EN = $0.8V_{DD}$ to V_{OUT} = $0.9(V_{DD}/2)$, V_L = 0V
		—	30	100			V_{DD} = 5.5V, EN = $0.8V_{DD}$ to V_{OUT} = $0.9(V_{DD}/2)$, V_L = 0V
EN Low to EN High hold time	t_{ENLH}	50	—	—			Minimum time before releasing EN (**Note 1**)
EN High to EN Low setup time	t_{ENHL}	50	—	—			Minimum time before exerting EN (**Note 1**)
POR Dynamic Specifications							
V_{DD} ↓ to Output Off	t_{PHL}	—	10	—	µs	all	V_L = 0V, V_{DD} = 1.8V to V_{PRL} – 0.1V step, 90% of V_{OUT} change
V_{DD} ↑ to Output On	t_{PLH}	—	100	—			V_L = 0V, V_{DD} = 0V to V_{PRH} + 0.1V step, 90% of V_{OUT} change

Note 1: For design guidance only; not tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = 1.8V to 5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125		**Note 1**
Storage Temperature Range	T_A	-65	—	+150		
Thermal Package Resistances						
Thermal Resistance, 8L-DFN (3×3)	θ_{JA}	—	57	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—		

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature specification (+150°C).

1.3 Timing Diagrams

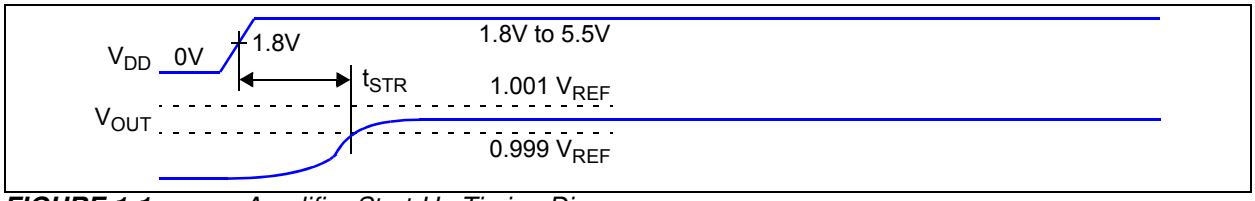


FIGURE 1-1: *Amplifier Start-Up Timing Diagram.*

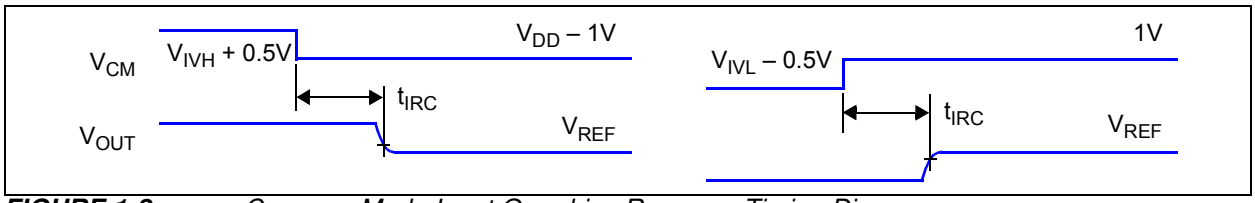


FIGURE 1-2: *Common Mode Input Overdrive Recovery Timing Diagram.*

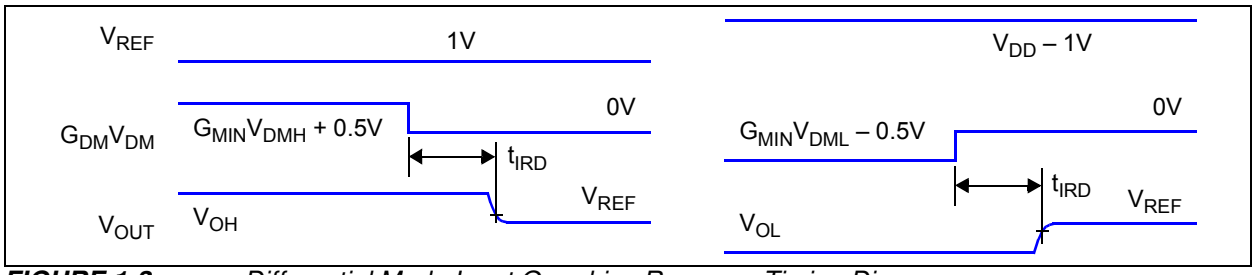


FIGURE 1-3: *Differential Mode Input Overdrive Recovery Timing Diagram.*

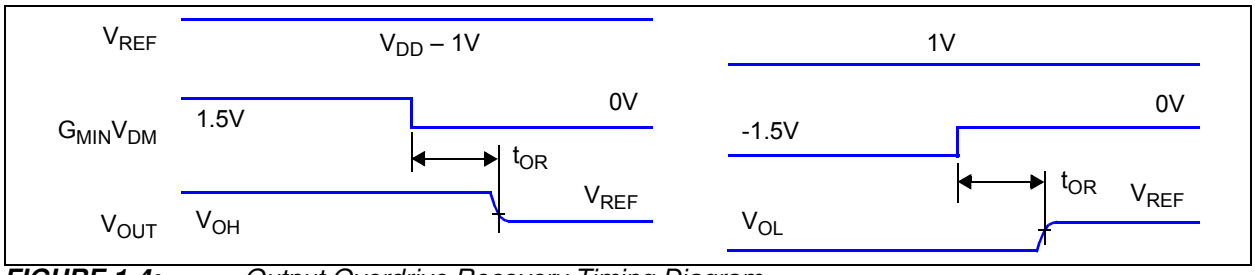


FIGURE 1-4: *Output Overdrive Recovery Timing Diagram.*

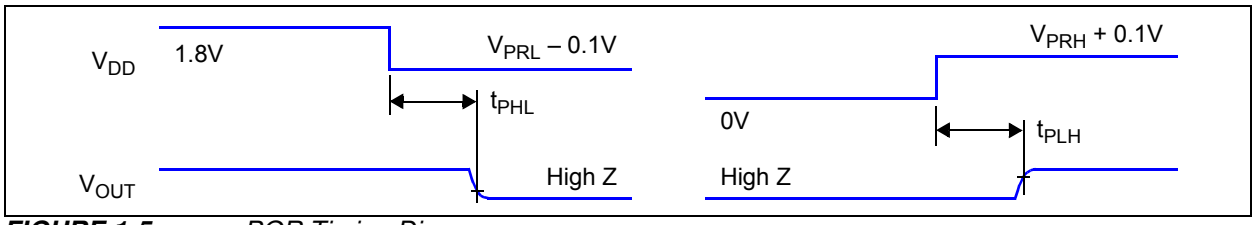


FIGURE 1-5: *POR Timing Diagram.*

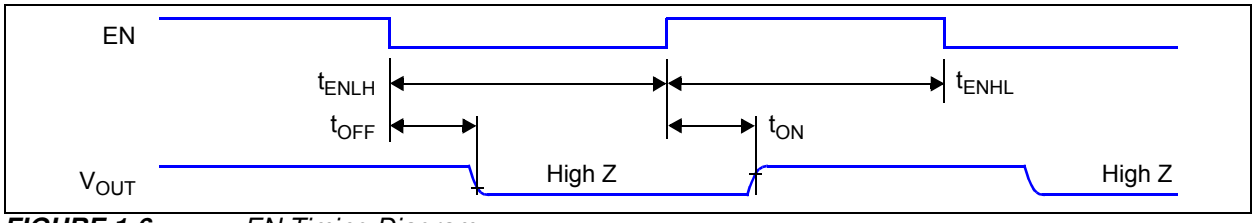


FIGURE 1-6: *EN Timing Diagram.*

1.4 DC Test Circuits

1.4.1 INPUT OFFSET TEST CIRCUIT

Figure 1-7 is a simple circuit that can test the INA's input offset errors and input voltage range (V_E, V_{IVL} and V_{IVH}; see **Section 1.5.1 "Input Offset Related Errors"** and **Section 1.5.2 "Input Offset Common Mode Nonlinearity"**). U_2 is part of a control loop that forces V_{OUT} to equal V_{CNT}; U_1 can be set to any bias point.

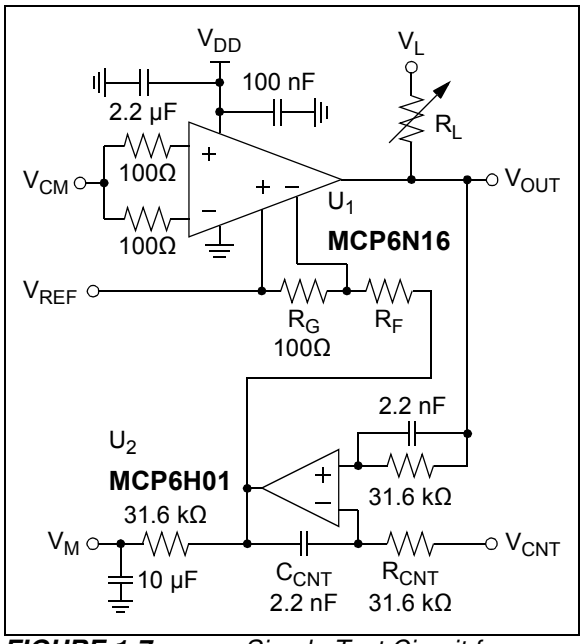


FIGURE 1-7: *Simple Test Circuit for Common Mode (Input Offset).*

When MCP6N16 is in its normal range of operation, the DC output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-1:

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{CNT} \\ V_M &= V_{REF} + G_{DM}(1 + g_E)V_E \end{aligned}$$

Table 1-5 shows the resulting behavior for different G_{MIN} options.

TABLE 1-5: RESULTS

G_{MIN} (V/V) Nom.	R_F (kΩ) Typ.	G_{DM} (kV/V) Typ.	$G_{DM}V_{OS}$ (±mV) Max.	BW (kHz) Typ. at V_{OUT}	BW (Hz) Typ. at V_M
1	100	1.00	85	0.50	0.50
10	402	4.02	88	1.2	
100			68	8.7	

1.4.2 DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-8 is a simple circuit that can test the INA's differential gain error, nonlinearity and input voltage range (g_E, INL_{DM}, V_{DML} and V_{DMH}; see **Section 1.5.3 "Differential Gain Error and Nonlinearity"**). R_F and R_G are 0.01% for accurate gain error measurements.

The output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-2:

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E) \\ V_M &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E) \end{aligned}$$

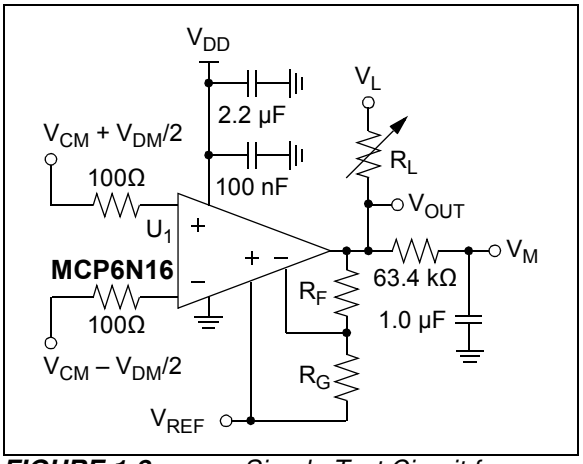


FIGURE 1-8: *Simple Test Circuit for Differential Mode.*

For different values of V_{REF}, V_{DM} sweeps over different ranges to keep V_{REF}, V_{FG} and V_{OUT} within their ranges.

Table 1-6 shows the recommended R_F and R_G; they produce a 10 kΩ load. V_L can usually be left open.

TABLE 1-6: SELECTING R_F AND R_G

G_{MIN} (V/V) Nom.	R_F (kΩ) Nom.	R_G (kΩ) Nom.	G_{DM} (V/V) Nom.
1	0	Open	1.0000
10	10.0 || 90.9	1.00	10.009
100	10.0 || 1000	100	100.01

1.4.3 DYNAMIC TESTING OF INPUT BEHAVIOR

The circuit in Figure 1-8 can test the input's dynamic behavior (i.e., IMD, t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR}); measure the output at V_{OUT}, instead of at V_M.

1.5 Explanation of DC Error Specifications

1.5.1 INPUT OFFSET RELATED ERRORS

The input offset error (V_E) is extracted from input offset measurements (see **Section 1.4.1 "Input Offset Test Circuit"**), based on Equation 1-1:

EQUATION 1-3:

$$V_E = (V_M - V_{REF}) / (G_{DM}(1 + g_E))$$

V_E has several terms, which assume a linear response to changes in V_{DD}, V_{SS}, V_{CM}, V_{OUT} and T_A (all of which are in their specified ranges):

EQUATION 1-4:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot TC_1$$

Where:

PSRR, *CMRR*, CMRR2 and A_{OL} are in units of V/V

ΔT_A is in units of °C

TC_1 is in units of V/°C

V_{DM} = 0

Equation 1-2 shows how V_E affects V_{OUT}.

1.5.2 INPUT OFFSET COMMON MODE NONLINEARITY

The input offset error (V_E) changes nonlinearly with V_{CM}. Figure 1-9 shows V_E vs. V_{CM}, as well as a linear fit line (V_{E_LIN}) based on V_{OS} and CMRR. The INA is in standard conditions (ΔV_{OUT} = 0, V_{DM} = 0, etc.). V_{CM} is swept from V_{IVL} to V_{IVH}. The test circuit is in **Section 1.4.1 "Input Offset Test Circuit"** and V_E is calculated using Equation 1-3.

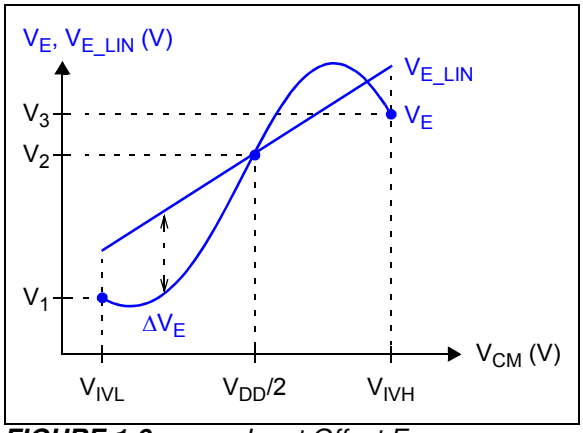


FIGURE 1-9: *Input Offset Error vs. Common Mode Input Voltage.*

Based on the measured V_E data, we obtain the following linear fit:

EQUATION 1-5:

$$V_{E\_LIN} = V_{OS} + (V_{CM} - V_{DD}/2) / CMRR$$

Where:

$$V_{OS} = V_2$$

$$1/CMRR = (V_3 - V_1) / (V_{IVH} - V_{IVL})$$

The remaining error (ΔV_E) is described by the Common Mode Nonlinearity spec:

EQUATION 1-6:

$$INL_{CMH} = max(\Delta V_E) / (V_{IVH} - V_{IVL})$$

$$INL_{CML} = min(\Delta V_E) / (V_{IVH} - V_{IVL})$$

$$INL_{CM} = INL_{CMH}, \quad |INL_{CMH}| \geq |INL_{CML}|$$

$$= INL_{CML}, \quad otherwise$$

Where:

$$\Delta V_E = V_E - V_{E\_LIN}$$

The same common mode behavior applies to V_E when V_{REF} is swept, instead of V_{CM}, since both input stages are designed the same:

EQUATION 1-7:

$$V_{E\_LIN2} = V_{OS} + (V_{REF} - V_{DD}/2) / CMRR2$$

$$INL_{CMH2} = max(\Delta V_{E2}) / (V_{IVH} - V_{IVL})$$

$$INL_{CML2} = min(\Delta V_{E2}) / (V_{IVH} - V_{IVL})$$

$$INL_{CM2} = INL_{CMH2}, \quad |INL_{CMH2}| \geq |INL_{CML2}|$$

$$= INL_{CML2}, \quad otherwise$$

Where:

$$\Delta V_{E2} = V_E - V_{E\_LIN2}$$

1.5.3 DIFFERENTIAL GAIN ERROR AND NONLINEARITY

The differential errors are extracted from differential gain measurements (see **Section 1.4.2 "Differential Gain Test Circuit"**), based on Equation 1-2. These errors are the differential gain error (g_E) and the input offset error (V_E, which changes nonlinearly with V_{DM}):

EQUATION 1-8:

$$G_{DM} = 1 + R_F/R_G$$
$$V_M = G_{DM}(1 + g_E)(V_{DM} + V_E)$$

These errors are adjusted for the expected output, then referred back to the input, giving the differential input error (V_{ED}) as a function of V_{DM}:

EQUATION 1-9:

$$V_{ED} = V_M/G_{DM} - V_{DM}$$

Figure 1-10 shows V_{ED} vs. V_{DM}, as well as a linear fit line (V_{ED_LIN}) based on V_{ED} and g_E. The INA is in standard conditions (ΔV_{OUT} = 0, etc.). V_{DM} is swept from V_{DML} to V_{DMH}.

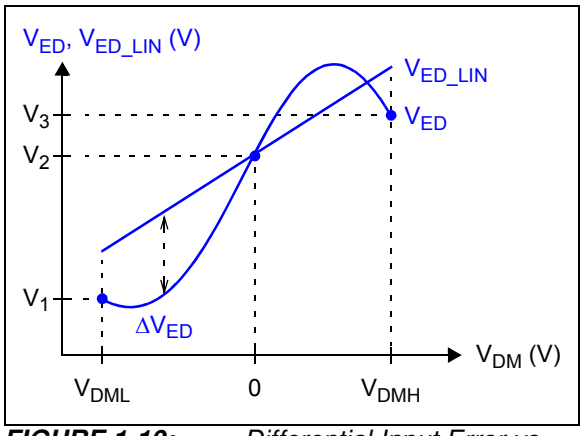


FIGURE 1-10: *Differential Input Error vs. Differential Input Voltage.*

Based on the measured V_{ED} data, we obtain the following linear fit:

EQUATION 1-10:

$$V_{ED\_LIN} = (1 + g_E)V_E + g_E V_{DM}$$
Where:
$$g_E = (V_3 - V_1)/(V_{DMH} - V_{DML}) - 1$$
$$V_E = V_2/(1 + g_E)$$

Note that the V_E value measured here is not as accurate as the one obtained in **Section 1.5.1 "Input Offset Related Errors"**.

The remaining error (ΔV_{ED}) is described by the Differential Nonlinearity spec:

EQUATION 1-11:

$$INL_{DMH} = max(\Delta V_{ED})/(V_{DMH} - V_{DML})$$
$$INL_{DML} = min(\Delta V_{ED})/(V_{DMH} - V_{DML})$$
$$INL_{DM} = INL_{DMH}, \quad |INL_{DMH}| \geq |INL_{DML}|$$
$$= INL_{DML}, \quad \text{otherwise}$$
Where:
$$\Delta V_{ED} = V_{ED} - V_{ED\_LIN}$$

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.1 DC Precision

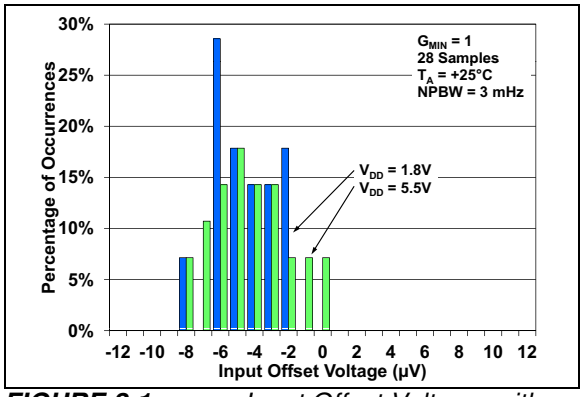


FIGURE 2-1: *Input Offset Voltage, with G_{MIN} = 1.*

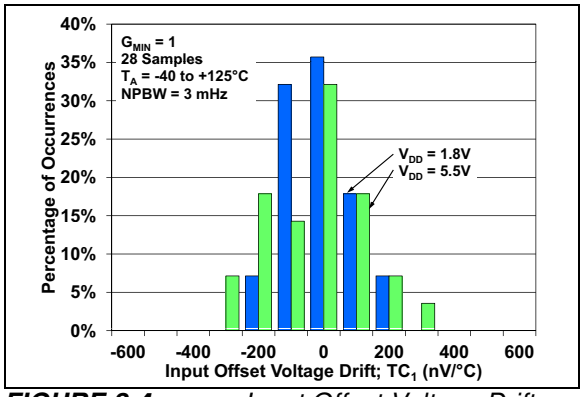


FIGURE 2-4: *Input Offset Voltage Drift, with G_{MIN} = 1.*

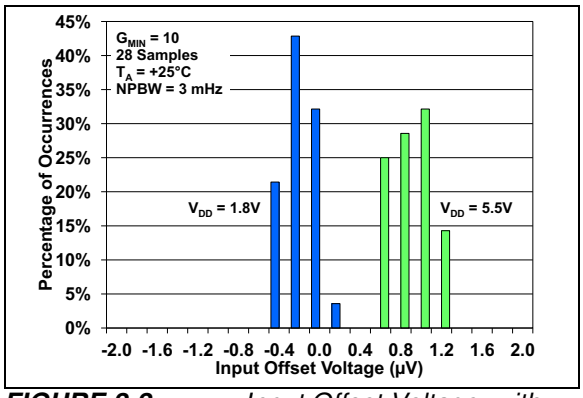


FIGURE 2-2: *Input Offset Voltage, with G_{MIN} = 10.*

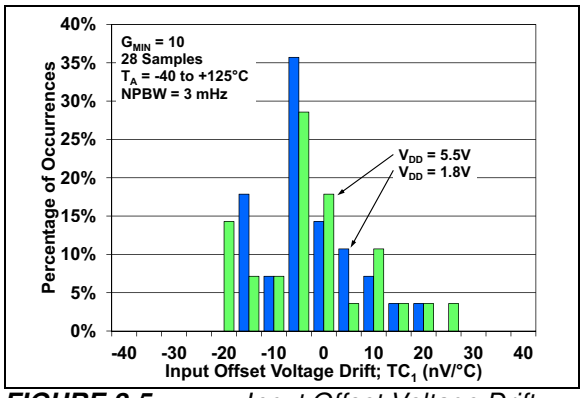


FIGURE 2-5: *Input Offset Voltage Drift, with G_{MIN} = 10.*

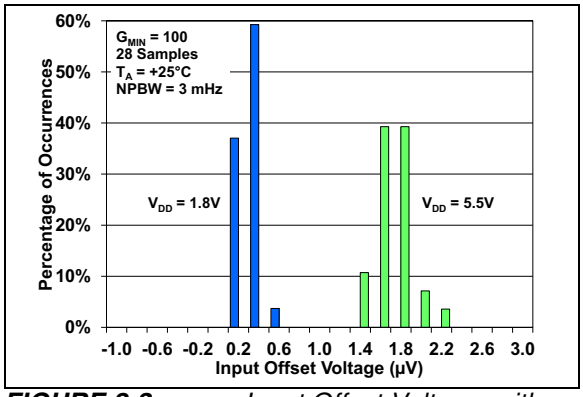


FIGURE 2-3: *Input Offset Voltage, with G_{MIN} = 100.*

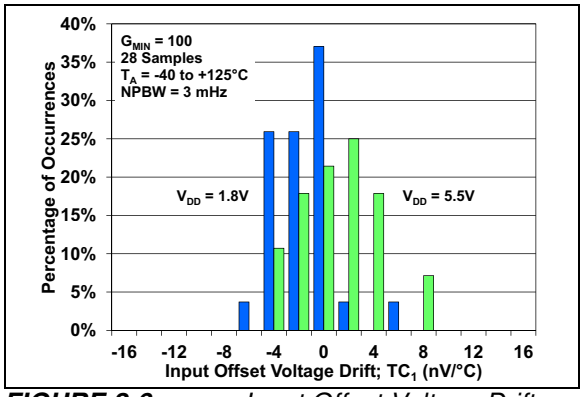


FIGURE 2-6: *Input Offset Voltage Drift, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

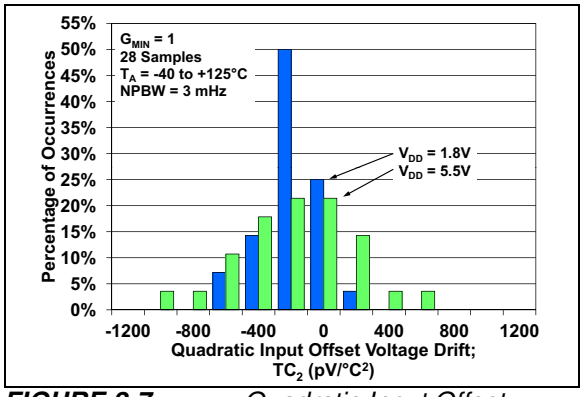


FIGURE 2-7: *Quadratic Input Offset Voltage Drift, with G_{MIN} = 1.*

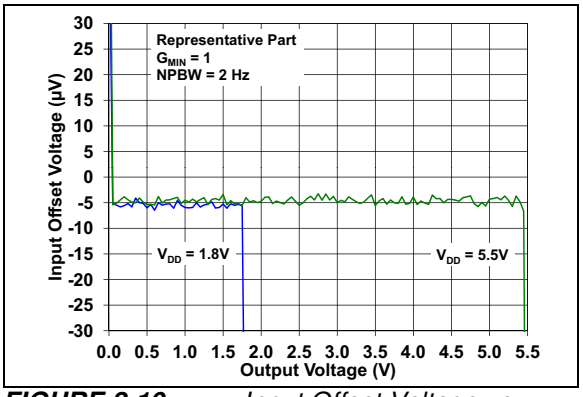


FIGURE 2-10: *Input Offset Voltage vs. Output Voltage, with G_{MIN} = 1.*

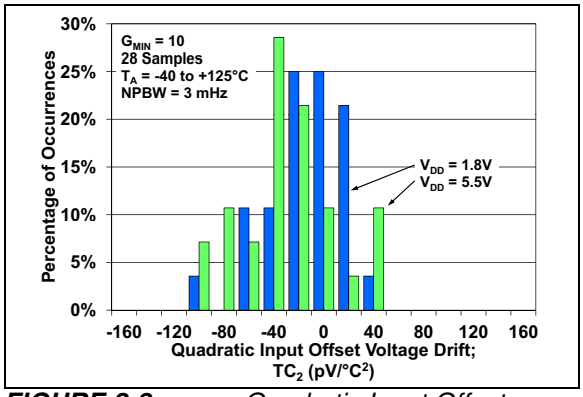


FIGURE 2-8: *Quadratic Input Offset Voltage Drift, with G_{MIN} = 10.*

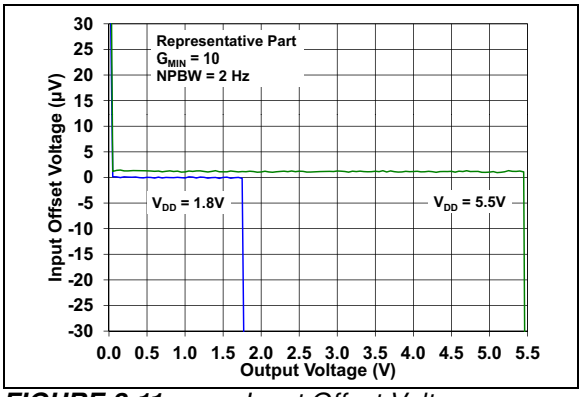


FIGURE 2-11: *Input Offset Voltage vs. Output Voltage, with G_{MIN} = 10.*

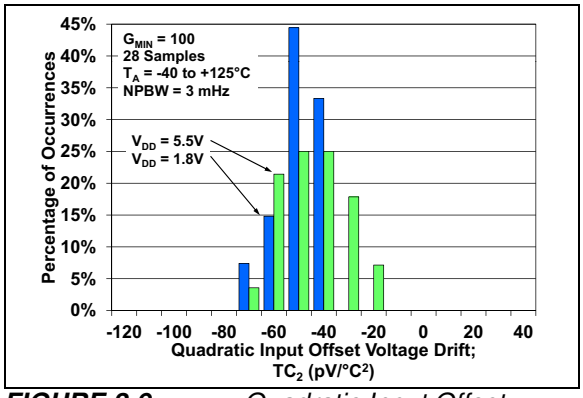


FIGURE 2-9: *Quadratic Input Offset Voltage Drift, with G_{MIN} = 100.*

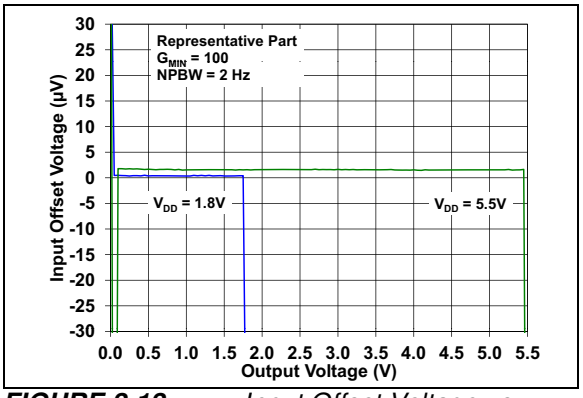


FIGURE 2-12: *Input Offset Voltage vs. Output Voltage, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

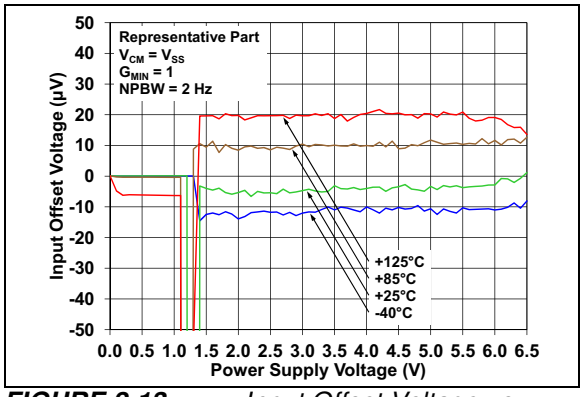


FIGURE 2-13: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 1.*

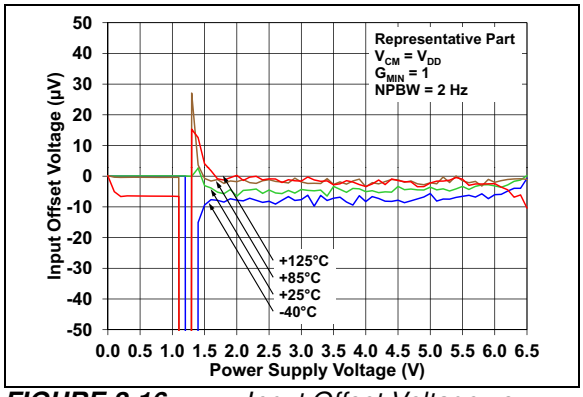


FIGURE 2-16: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 1.*

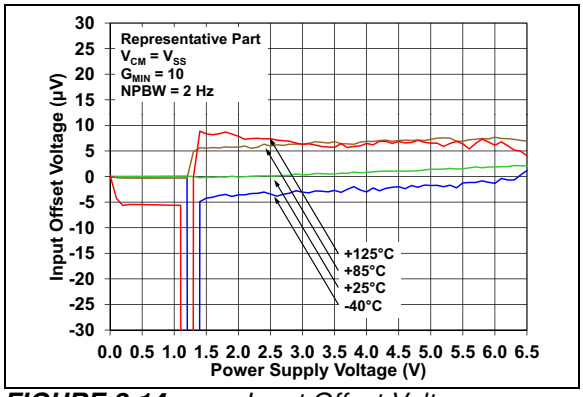


FIGURE 2-14: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 10.*

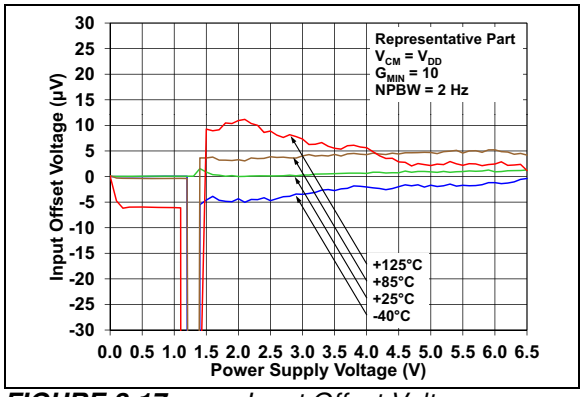


FIGURE 2-17: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 10.*

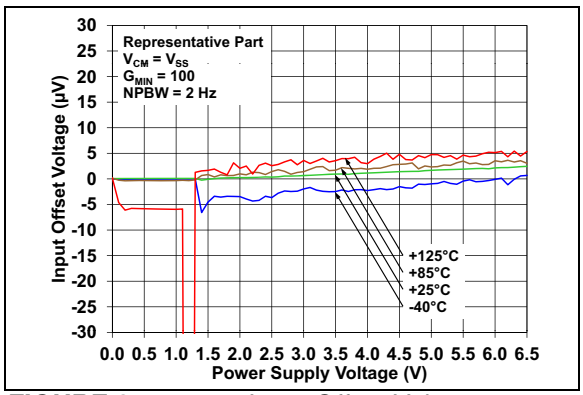


FIGURE 2-15: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 100.*

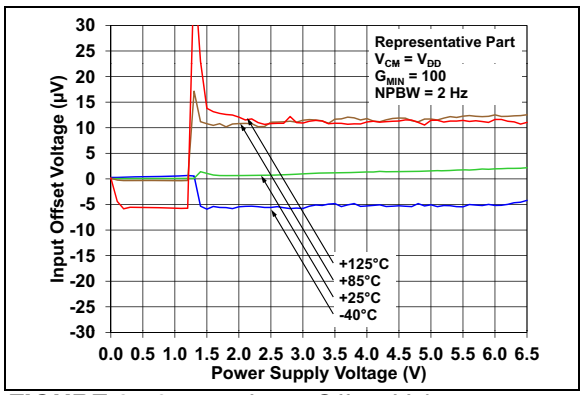


FIGURE 2-18: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

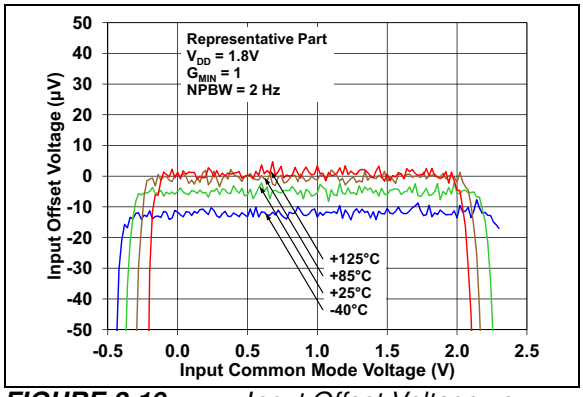


FIGURE 2-19: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 1.*

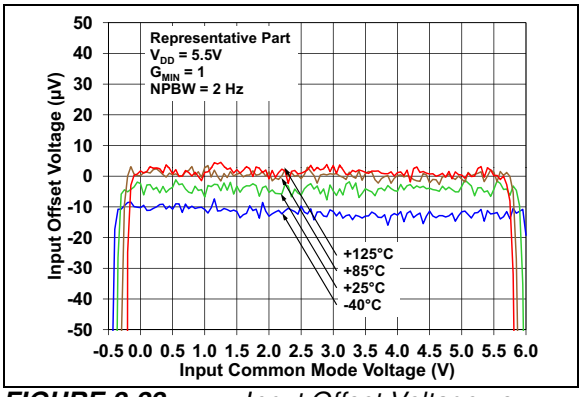


FIGURE 2-22: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 1.*

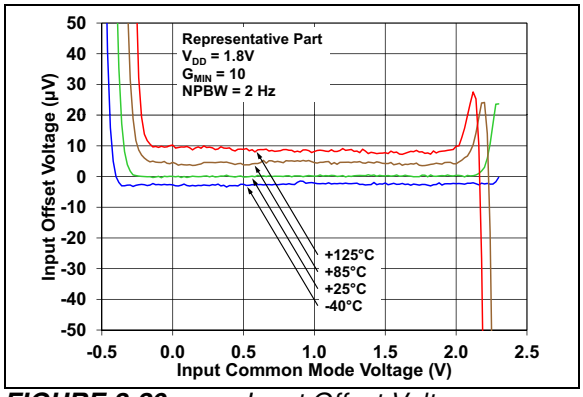


FIGURE 2-20: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 10.*

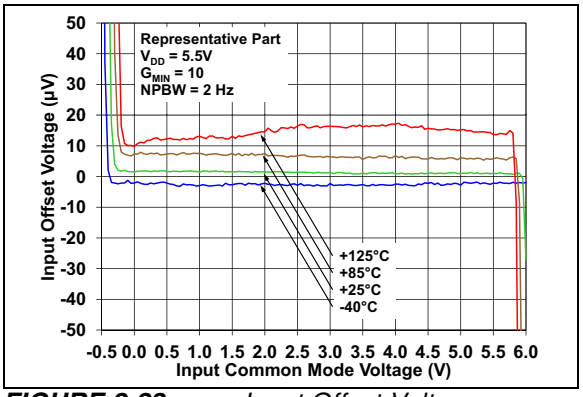


FIGURE 2-23: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 10.*

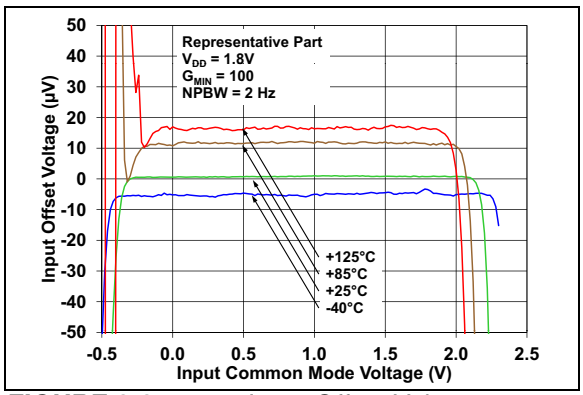


FIGURE 2-21: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 100.*

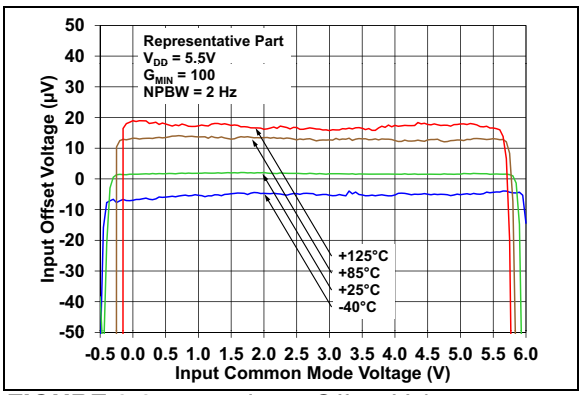


FIGURE 2-24: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

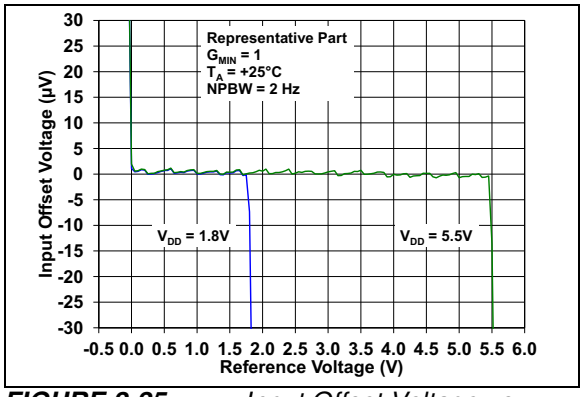


FIGURE 2-25: *Input Offset Voltage vs. Reference Voltage, with G_{MIN} = 1.*

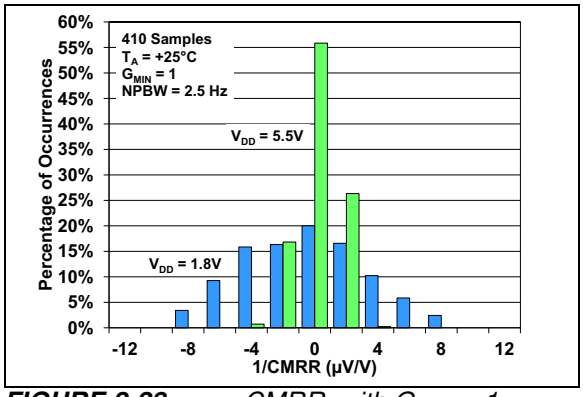


FIGURE 2-28: *CMRR, with G_{MIN} = 1.*

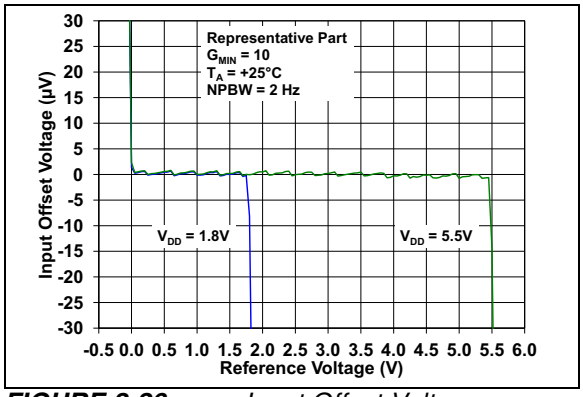


FIGURE 2-26: *Input Offset Voltage vs. Reference Voltage, with G_{MIN} = 10.*

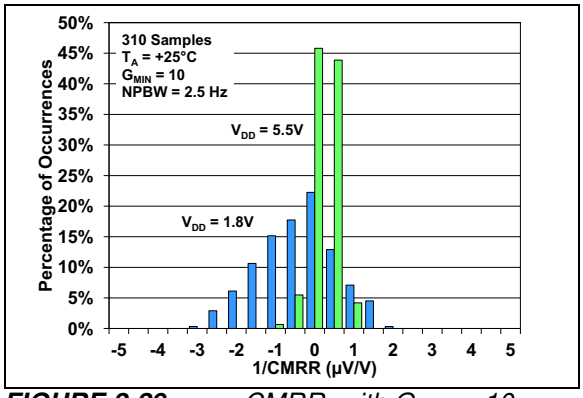


FIGURE 2-29: *CMRR, with G_{MIN} = 10.*

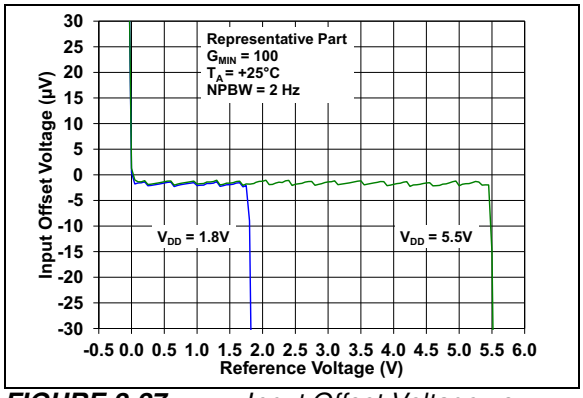


FIGURE 2-27: *Input Offset Voltage vs. Reference Voltage, with G_{MIN} = 100.*

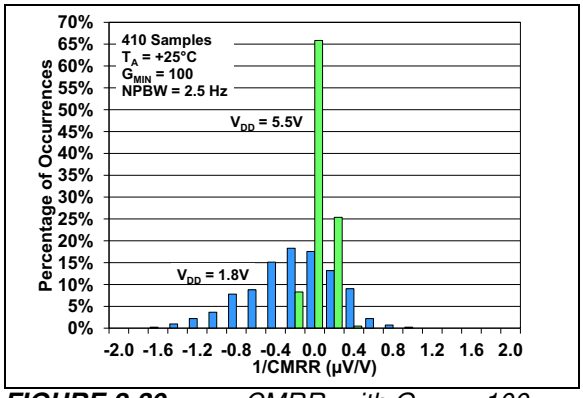


FIGURE 2-30: *CMRR, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

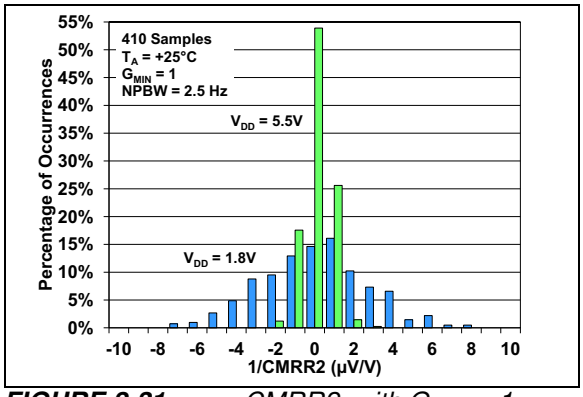


FIGURE 2-31: *CMRR2, with G_{MIN} = 1.*

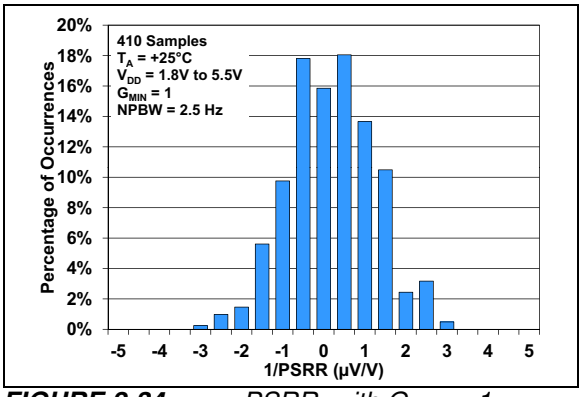


FIGURE 2-34: *PSRR, with G_{MIN} = 1.*

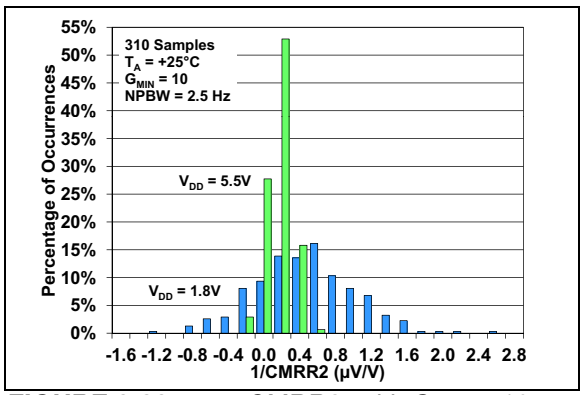


FIGURE 2-32: *CMRR2, with G_{MIN} = 10.*

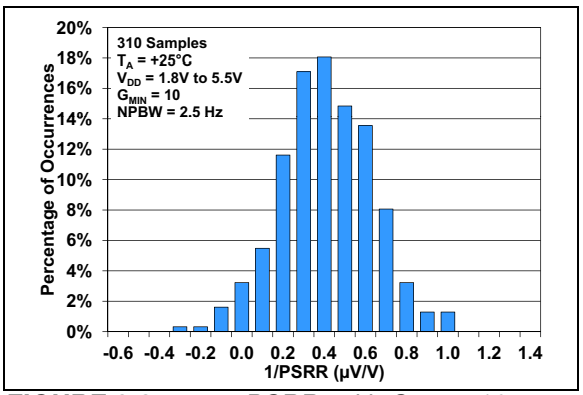


FIGURE 2-35: *PSRR, with G_{MIN} = 10.*

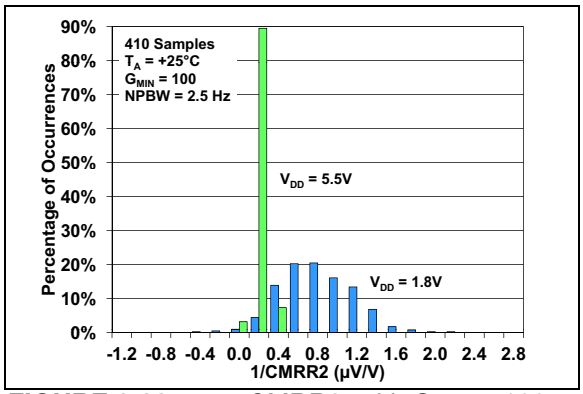


FIGURE 2-33: *CMRR2, with G_{MIN} = 100.*

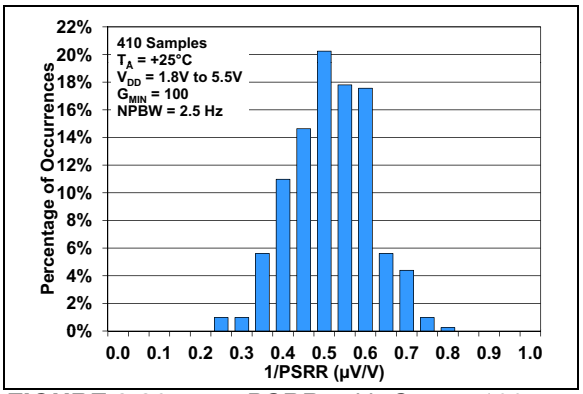


FIGURE 2-36: *PSRR, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

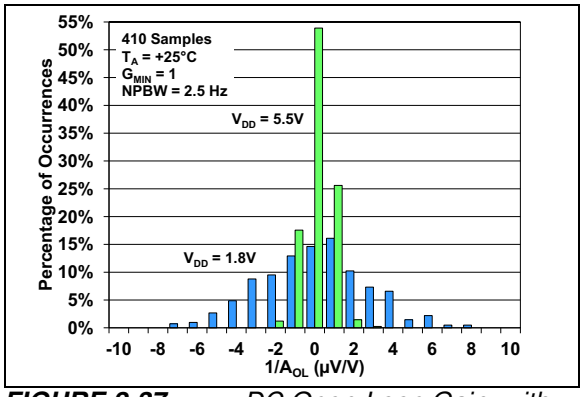


FIGURE 2-37: *DC Open-Loop Gain, with G_{MIN} = 1.*

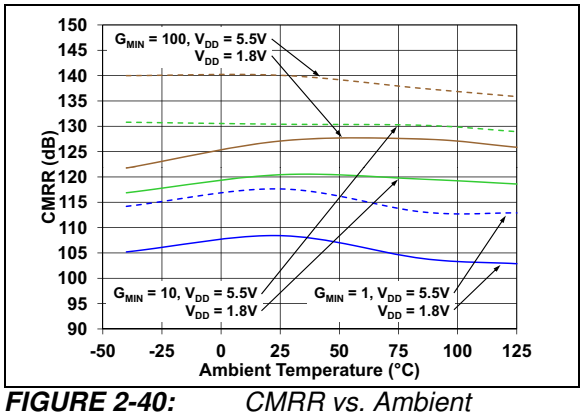


FIGURE 2-40: *CMRR vs. Ambient Temperature.*

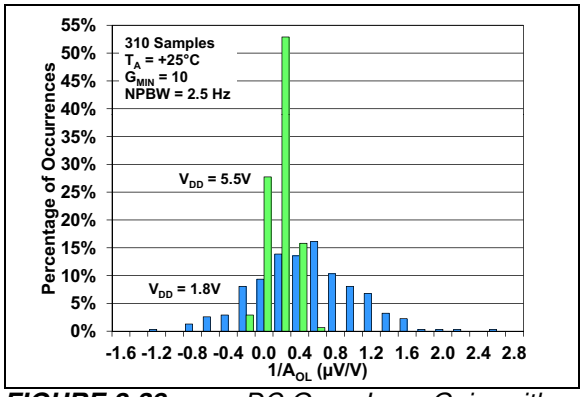


FIGURE 2-38: *DC Open-Loop Gain, with G_{MIN} = 10.*

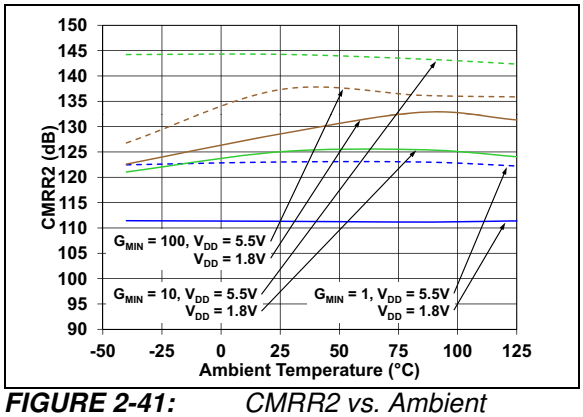


FIGURE 2-41: *CMRR2 vs. Ambient Temperature.*

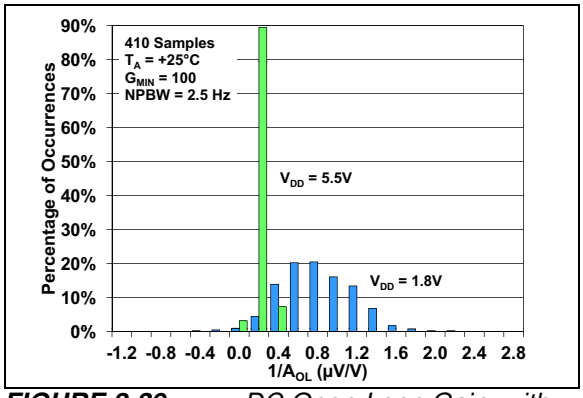


FIGURE 2-39: *DC Open-Loop Gain, with G_{MIN} = 100.*

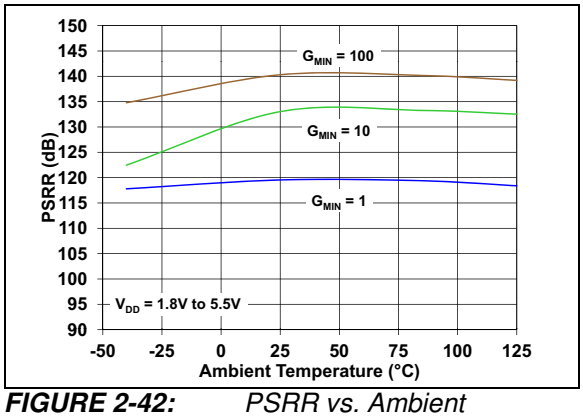


FIGURE 2-42: *PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

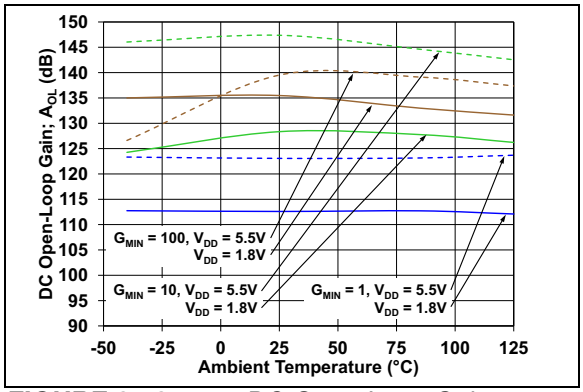


FIGURE 2-43: *DC Open-Loop Gain vs. Ambient Temperature.*

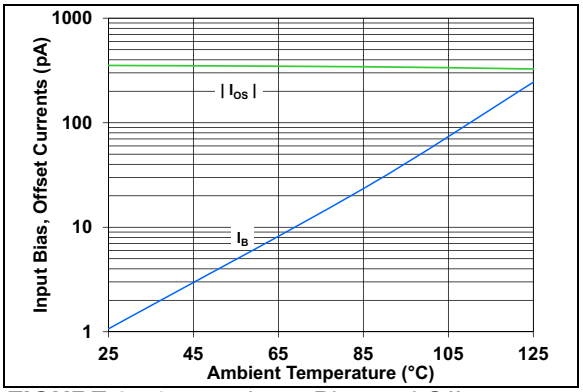


FIGURE 2-46: *Input Bias and Offset Currents vs. Ambient Temperature, with V_{DD} = 5.5V.*

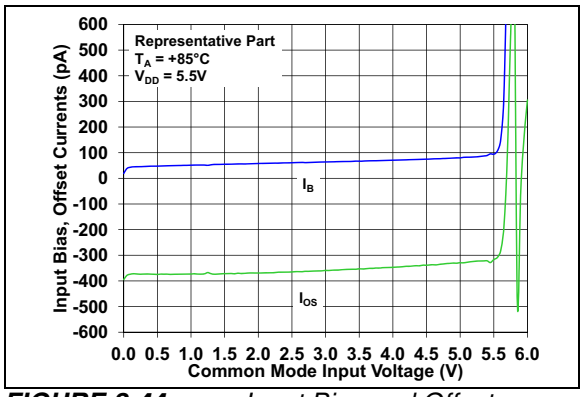


FIGURE 2-44: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +85°C.*

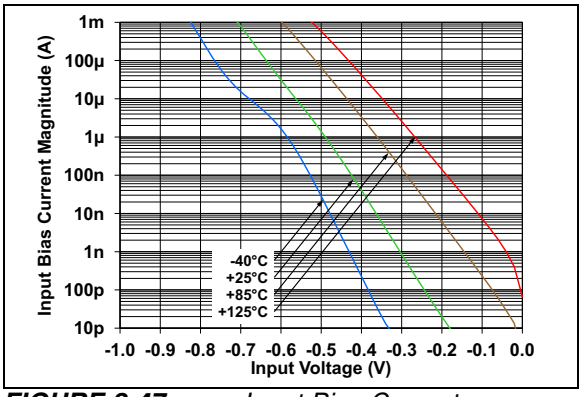


FIGURE 2-47: *Input Bias Current Magnitude vs. Input Voltage (below V_{SS}).*

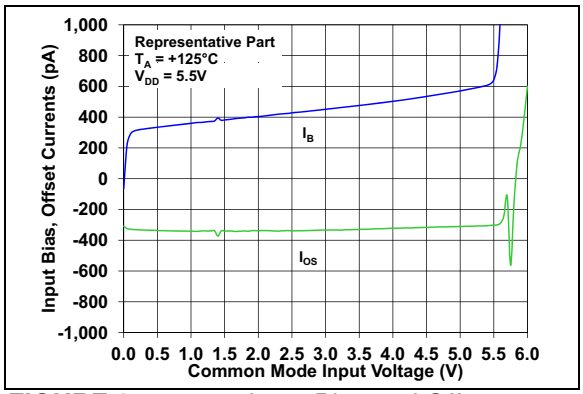


FIGURE 2-45: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +125°C.*

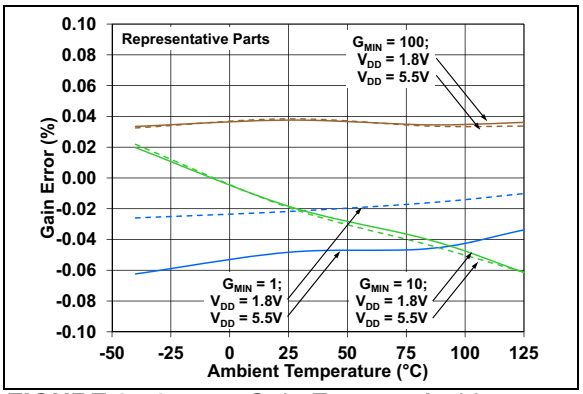


FIGURE 2-48: *Gain Error vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

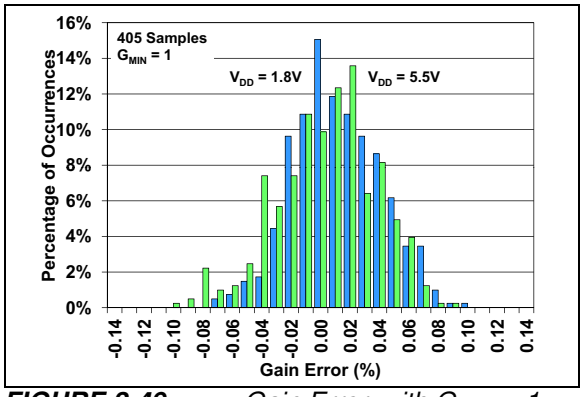


FIGURE 2-49: *Gain Error, with G_{MIN} = 1.*

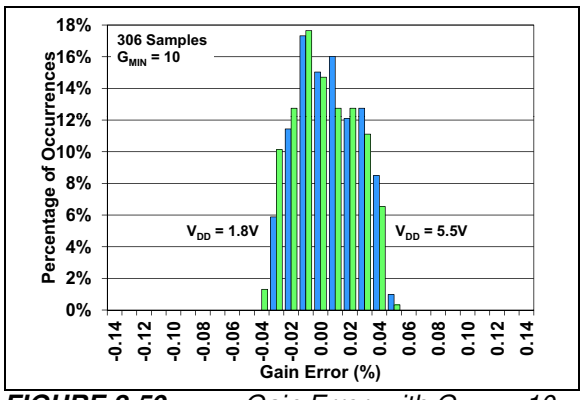


FIGURE 2-50: *Gain Error, with G_{MIN} = 10.*

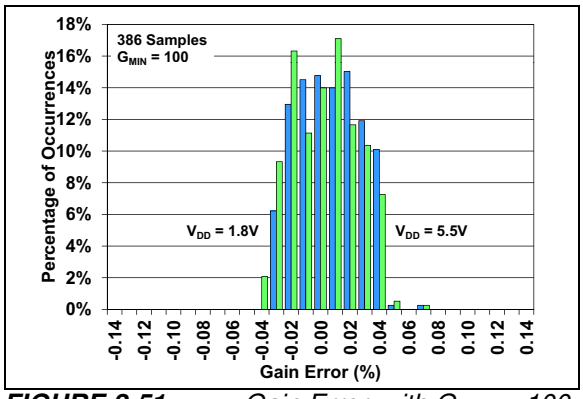


FIGURE 2-51: *Gain Error, with G_{MIN} = 100.*