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MCP6S21/2/6/8

Single-Ended, Rail-to-Rail I/O, Low Gain PGA

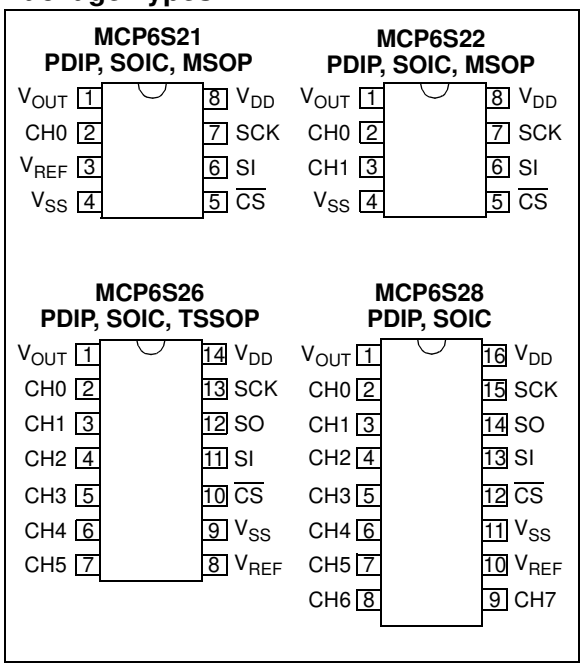
Features

- Multiplexed Inputs: 1, 2, 6 or 8 channels
- 8 Gain Selections:
  - +1, +2, +4, +5, +8, +10, +16 or +32 V/V
- Serial Peripheral Interface (SPI)
- Rail-to-Rail Input and Output
- Low Gain Error: ±1% (max)
- Low Offset: ±275 µV (max)
- High Bandwidth: 2 to 12 MHz (typ)
- Low Noise: 10 nV/√Hz @ 10 kHz (typ)
- Low Supply Current: 1.0 mA (typ)
- Single Supply: 2.5V to 5.5V

Typical Applications

- A/D Converter Driver
- Multiplexed Analog Applications
- Data Acquisition
- Industrial Instrumentation
- Test Equipment
- Medical Instrumentation

Package Types

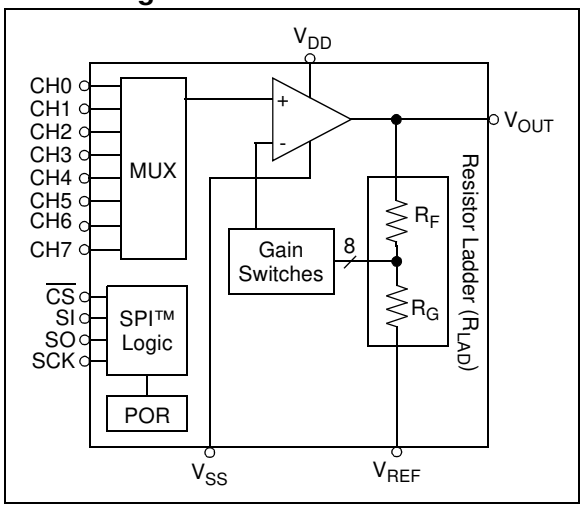


Description

The Microchip Technology Inc. MCP6S21/2/6/8 are analog Programmable Gain Amplifiers (PGA). They can be configured for gains from +1 V/V to +32 V/V and the input multiplexer can select one of up to eight channels through an SPI port. The serial interface can also put the PGA into shutdown to conserve power. These PGAs are optimized for high speed, low offset voltage and single-supply operation with rail-to-rail input and output capability. These specifications support single supply applications needing flexible performance or multiple inputs.

The one channel MCP6S21 and the two channel MCP6S22 are available in 8-pin PDIP, SOIC and MSOP packages. The six channel MCP6S26 is available in 14-pin PDIP, SOIC and TSSOP packages. The eight channel MCP6S28 is available in 16-pin PDIP and SOIC packages. All parts are fully specified from -40°C to +85°C.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V
All inputs and outputs..... V_{SS} - 0.3V to V_{DD} +0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current.....continuous
Current at Input Pin .....±2 mA
Current at Output and Supply Pins ..... ±30 mA
Storage temperature .....-65°C to +150°C
Junction temperature .....+150°C
ESD protection on all pins (HBM;MM)..... ≥ 2 kV; 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{OUT}	Analog Output
CH0-CH7	Analog Inputs
V_{SS}	Negative Power Supply
V_{DD}	Positive Power Supply
SCK	SPI Clock Input
SI	SPI Serial Data Input
SO	SPI Serial Data Output
$\overline{CS}$	SPI Chip Select
V_{REF}	External Reference Pin

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Amplifier Input						
Input Offset Voltage	V_{OS}	-275	—	+275	µV	G = +1, V_{DD} = 4.0V
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±4	—	µV/°C	T_A = -40 to +85°C
Power Supply Rejection Ratio	PSRR	70	85	—	dB	G = +1 **(Note 1)**
Input Bias Current	I_B	—	±1	—	pA	CHx = V_{DD}/2
Input Bias Current over Temperature	I_B	—	—	250	pA	T_A = -40 to +85°C, CHx = V_{DD}/2
Input Impedance	Z_{IN}	—	10^{13}||15	—	Ω||pF	
Input Voltage Range	V_{IVR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Amplifier Gain						
Nominal Gains	—	—	1 to 32	—	V/V	+1, +2, +4, +5, +8, +10, +16 or +32
DC Gain Error G = +1	g_E	-0.1	—	+0.1	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
G ≥ +2	g_E	-1.0	—	+1.0	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
DC Gain Drift G = +1	$\Delta G/\Delta T_A$	—	±0.0002	—	%/°C	T_A = -40 to +85°C
G ≥ +2	$\Delta G/\Delta T_A$	—	±0.0004	—	%/°C	T_A = -40 to +85°C
Internal Resistance	R_{LAD}	3.4	4.9	6.4	kΩ	**(Note 1)**
Internal Resistance over Temperature	$\Delta R_{LAD}/\Delta T_A$	—	+0.028	—	%/°C	**(Note 1)** T_A = -40 to +85°C
Amplifier Output						
DC Output Non-linearity G = +1	V_{ONL}	—	±0.003	—	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
G ≥ +2	V_{ONL}	—	±0.001	—	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
Maximum Output Voltage Swing	V_{OH}, V_{OL}	V_{SS}+20	—	V_{DD}-100	mV	G ≥ +2; 0.5V output overdrive
		V_{SS}+60	—	V_{DD}-60		G ≥ +2; 0.5V output overdrive, V_{REF} = V_{DD}/2
Short-Circuit Current	$I_{O(SC)}$	—	±30	—	mA	

Note 1: R_{LAD} (R_F + R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S22 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. We recommend the MCP6S22's V_{SS} pin be tied directly to ground to avoid noise problems.

2: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

3: The output goes Hi-Z and the registers reset to their defaults; see Section 5.4, "Power-On Reset".

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current	I_Q	0.5	1.0	1.35	mA	I_O = 0 **(Note 2)**
Quiescent Current, Shutdown mode	I_{Q_SHDN}	—	0.5	1.0	µA	I_O = 0 **(Note 2)**
Power-On Reset						
POR Trip Voltage	V_{POR}	1.2	1.7	2.2	V	**(Note 3)**
POR Trip Voltage Drift	$\Delta V_{POR}/\Delta T$	—	-3.0	—	mV/°C	T_A = -40°C to+85°C

Note 1: R_{LAD} (R_F + R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S22 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. We recommend the MCP6S22's V_{SS} pin be tied directly to ground to avoid noise problems.

2: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

3: The output goes Hi-Z and the registers reset to their defaults; see Section 5.4, "Power-On Reset".

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 =(0.3V)/G, CH1 to CH7=0.3V, R_L = 10 kΩ to V_{DD}/2, C_L = 60 pF, SI and SCK are tied low, and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
-3 dB Bandwidth	BW	—	2 to 12	—	MHz	All gains; V_{OUT} < 100 mV_{P-P} **(Note 1)**
Gain Peaking	GPK	—	0	—	dB	All gains; V_{OUT} < 100 mV_{P-P}
Total Harmonic Distortion plus Noise						
f = 1 kHz, G = +1 V/V	THD+N	—	0.0015	—	%	V_{OUT} = 1.5V ± 1.0V_{PK}, V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +4 V/V	THD+N	—	0.0058	—	%	V_{OUT} = 1.5V ± 1.0V_{PK}, V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +16 V/V	THD+N	—	0.023	—	%	V_{OUT} = 1.5V ± 1.0V_{PK}, V_{DD} = 5.0V, BW = 22 kHz
f = 20 kHz, G = +1 V/V	THD+N	—	0.0035	—	%	V_{OUT} = 1.5V ± 1.0V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +4 V/V	THD+N	—	0.0093	—	%	V_{OUT} = 1.5V ± 1.0V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +16 V/V	THD+N	—	0.036	—	%	V_{OUT} = 1.5V ± 1.0V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
Step Response						
Slew Rate	SR	—	4.0	—	V/µs	G = 1, 2
		—	11	—	V/µs	G = 4, 5, 8, 10
		—	22	—	V/µs	G = 16, 32
Noise						
Input Noise Voltage	E_{ni}	—	3.2	—	μV_{P-P}	f = 0.1 Hz to 10 kHz **(Note 2)**
		—	26	—		f = 0.1 Hz to 200 kHz **(Note 2)**
Input Noise Voltage Density	e_{ni}	—	10	—	nV/√Hz	f = 10 kHz **(Note 2)**
Input Noise Current Density	i_{ni}	—	4	—	fA/√Hz	f = 10 kHz

Note 1: See Table 4-1 for a list of typical numbers.

2: E_{ni} and e_{ni} include ladder resistance noise. See Figure 2-33 for e_{ni} vs. G data.

DIGITAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, C_L = 60 pF, SI and SCK are tied low, and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
SPI Inputs ($\overline{CS}$, SI, SCK)						
Logic Threshold, Low	V_{IL}	0	—	0.3V_{DD}	V	
Input Leakage Current	I_{IL}	-1.0	—	+1.0	µA	
Logic Threshold, High	V_{IH}	0.7V_{DD}	—	V_{DD}	V	
Amplifier Output Leakage Current	—	-1.0	—	+1.0	µA	In Shutdown mode
SPI Output (SO, for MCP6S26 and MCP6S28)						
Logic Threshold, Low	V_{OL}	V_{SS}	—	V_{SS}+0.4	V	I_{OL} = 2.1 mA, V_{DD} = 5V
Logic Threshold, High	V_{OH}	V_{DD}-0.5	—	V_{DD}	V	I_{OH} = -400 µA
SPI Timing						
Pin Capacitance	C_{PIN}	—	10	—	pF	All digital I/O pins
Input Rise/Fall Times ($\overline{CS}$, SI, SCK)	t_{RFI}	—	—	2	µs	**Note 1**
Output Rise/Fall Times (SO)	t_{RFO}	—	5	—	ns	MCP6S26 and MCP6S28
$\overline{CS}$ high time	t_{CSH}	40	—	—	ns	
SCK edge to $\overline{CS}$ fall setup time	t_{CS0}	10	—	—	ns	SCK edge when $\overline{CS}$ is high
$\overline{CS}$ fall to first SCK edge setup time	t_{CSSC}	40	—	—	ns	
SCK Frequency	f_{SCK}	—	—	10	MHz	V_{DD} = 5V **(Note 2)**
SCK high time	t_{HI}	40	—	—	ns	
SCK low time	t_{LO}	40	—	—	ns	
SCK last edge to $\overline{CS}$ rise setup time	t_{SCCS}	30	—	—	ns	
$\overline{CS}$ rise to SCK edge setup time	t_{CS1}	100	—	—	ns	SCK edge when $\overline{CS}$ is high
SI set-up time	t_{SU}	40	—	—	ns	
SI hold time	t_{HD}	10	—	—	ns	
SCK to SO valid propagation delay	t_{DO}	—	—	80	ns	MCP6S26 and MCP6S28
$\overline{CS}$ rise to SO forced to zero	t_{SOZ}	—	—	80	ns	MCP6S26 and MCP6S28
Channel and Gain Select Timing						
Channel Select Time	t_{CH}	—	1.5	—	µs	CHx = 0.6V, CHy =0.3V, G = 1, CHx to CHy select $\overline{CS}$ = 0.7V_{DD} to V_{OUT} 90% point
Gain Select Time	t_G	—	1	—	µs	CHx = 0.3V, G = 5 to G = 1 select, $\overline{CS}$ = 0.7V_{DD} to V_{OUT} 90% point
Shutdown Mode Timing						
Out of Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output Turn-on Time	t_{ON}	—	3.5	10	µs	$\overline{CS}$ = 0.7V_{DD} to V_{OUT} 90% point
Into Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output High-Z Turn-off Time	t_{OFF}	—	1.5	—	µs	$\overline{CS}$ = 0.7V_{DD} to V_{OUT} 90% point
POR Timing						
Power-On Reset power-up time	t_{RPU}	—	30	—	µs	V_{DD} = V_{POR} - 0.1V to V_{POR} + 0.1V, 50% V_{DD} to 90% V_{OUT} point
Power-On Reset power-down time	t_{RPD}	—	10	—	µs	V_{DD} = V_{POR} + 0.1V to V_{POR} - 0.1V, 50% V_{DD} to 90% V_{OUT} point

Note 1: Not tested in production. Set by design and characterization.

2: When using the device in the daisy chain configuration, maximum clock frequency is determined by a combination of propagation delay time ($t_{DO} \leq$ 80 ns), data input setup time ($t_{SU} \geq$ 40 ns), SCK high time ($t_{HI} \geq$ 40 ns), and SCK rise and fall times of 5 ns. Maximum f_{SCK} is, therefore, ≈ 5.8 MHz.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 16L-SOIC	θ_{JA}	—	90	—	°C/W	

Note 1: The MCP6S21/2/6/8 family of PGAs operates over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature (150°C).

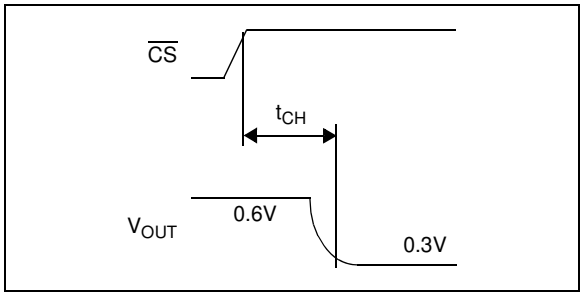


FIGURE 1-1: *Channel Select Timing Diagram.*

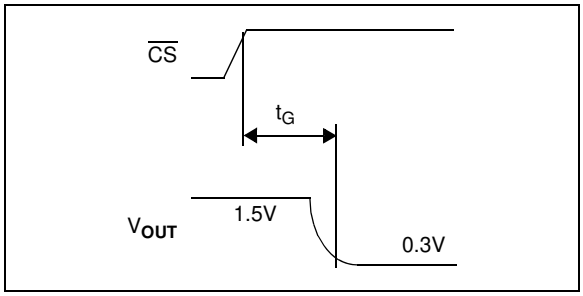


FIGURE 1-3: *Gain Select Timing Diagram.*

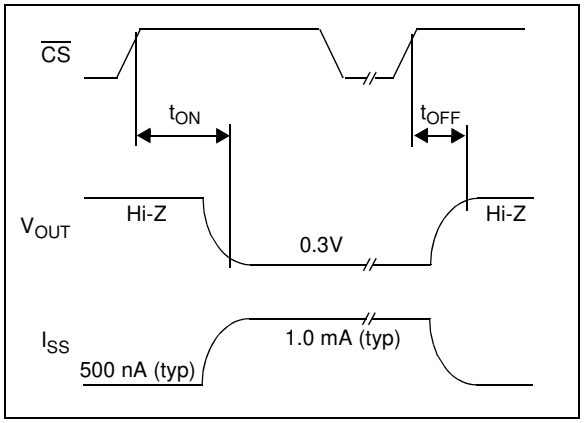


FIGURE 1-2: *PGA Shutdown timing diagram (must enter correct commands before CS goes high).*

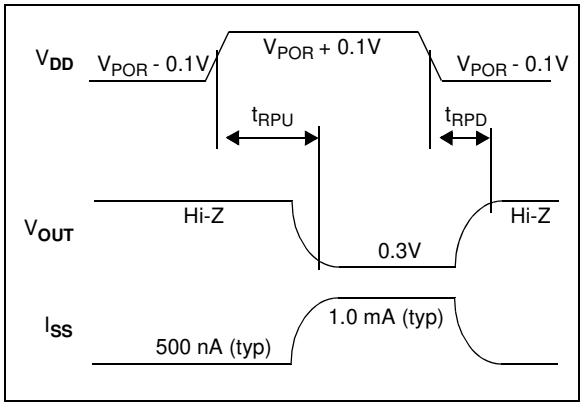


FIGURE 1-4: *POR power-up and power-down timing diagram.*

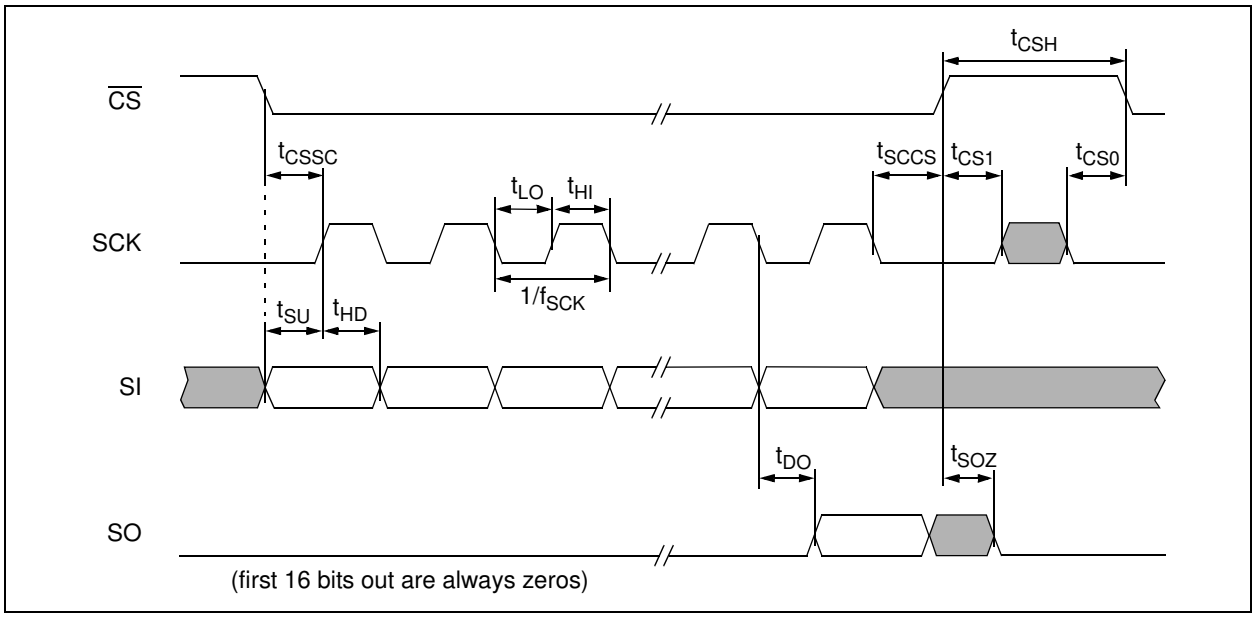


FIGURE 1-5: *Detailed SPI Serial Interface Timing, SPI 0,0 mode.*

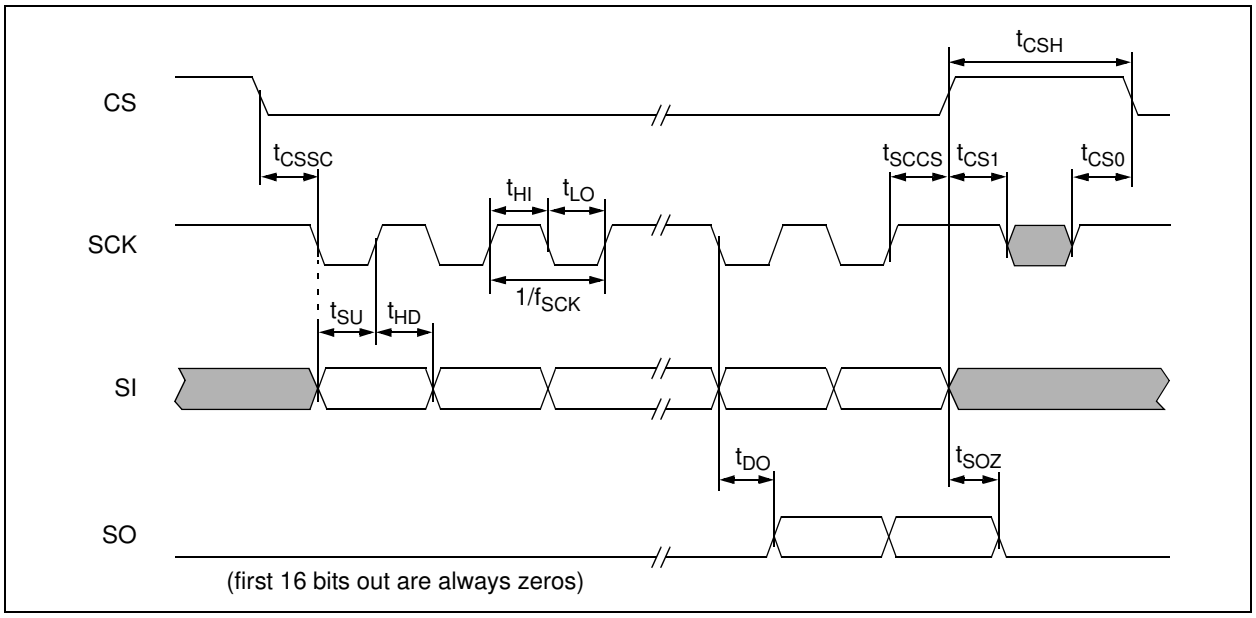


FIGURE 1-6: *Detailed SPI Serial Interface Timing, SPI 1,1 mode.*

1.1 DC Output Voltage Specs / Model

1.1.1 IDEAL MODEL

The ideal PGA output voltage (V_{OUT}) is:

EQUATION

$$V_{O\_ideal} = GV_{IN} \qquad V_{REF} = V_{SS} = 0V$$

where: G is the nominal gain

(see Figure 1-7). This equation holds when there are no gain or offset errors and when the V_{REF} pin is tied to a low impedance source (<< 0.1Ω) at ground potential (V_{SS} = 0V).

1.1.2 LINEAR MODEL

The PGA's linear region of operation, including offset and gain errors, is modeled by the line V_{O_linear}, shown in Figure 1-7.

EQUATION

$$V_{O\_linear} = G(1 + g_E)(V_{IN} - 0.3V + V_{OS}) + 0.3V$$
$$V_{REF} = V_{SS} = 0V$$

The endpoints of this line are at V_{O_ideal} = 0.3V and V_{DD}-0.3V. The gain and offset specifications referred to in the electrical specifications are related to Figure 1-7, as follows:

EQUATION

$$g_E = 100\% \frac{V_2 - V_1}{G(V_{DD} - 0.6V)}$$

$$V_{OS} = \frac{V_1}{G(1 + g_E)} \qquad G = +1$$

$$\Delta G / \Delta T_A = \frac{\Delta g_E}{\Delta T_A}$$

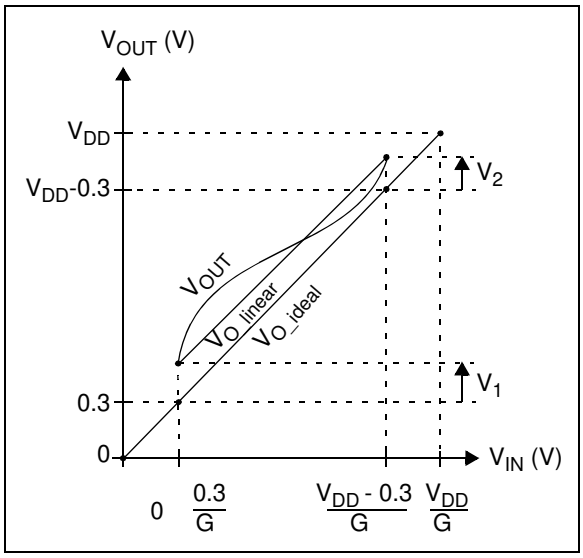


FIGURE 1-7: *Output Voltage Model with the standard condition $V_{REF} = V_{SS} = 0V$.*

1.1.3 OUTPUT NON-LINEARITY

Figure 1-8 shows the Integral Non-Linearity (INL) of the output voltage.

EQUATION

$$INL = V_{OUT} - V_{O\_linear}$$

The output non-linearity specification in the electrical specifications is related to Figure 1-8 by:

EQUATION

$$V_{ONL} = \frac{max\{V_4, V_3\}}{V_{DD} - 0.6V}$$

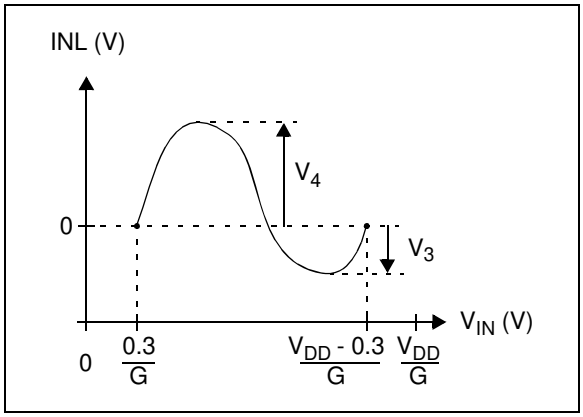


FIGURE 1-8: *Output Voltage INL with the standard condition $V_{REF} = V_{SS} = 0V$.*

1.1.4 DIFFERENT V_{REF} CONDITIONS

Some of the plots in Section 2.0, “Typical Performance Curves”, have the conditions $V_{REF} = V_{DD}/2$ or $V_{REF} = V_{DD}$. The equations and figures above are easily modified for these conditions. The ideal V_{OUT} becomes:

EQUATION

$$V_{O\_ideal} = V_{REF} + G(V_{IN} - V_{REF})$$

$$V_{DD} \geq V_{REF} > V_{SS} = 0V$$

The complete linear model is:

EQUATION

$$V_{O\_linear} = G(1 + g_E)(V_{IN} - V_{IN\_L} + V_{OS}) + 0.3V$$

where the new V_{IN} endpoints are:

EQUATION

$$V_{IN\_L} = \frac{0.3V - V_{REF}}{G + V_{REF}}$$

$$V_{IN\_R} = \frac{V_{DD} - 0.3V - V_{REF}}{G + V_{REF}}$$

The equations for extracting the specifications do not change.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{REF} = V_{SS}, G= +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

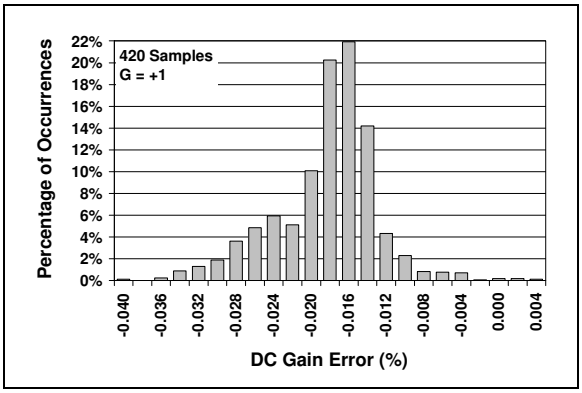


FIGURE 2-1: *DC Gain Error, G = +1.*

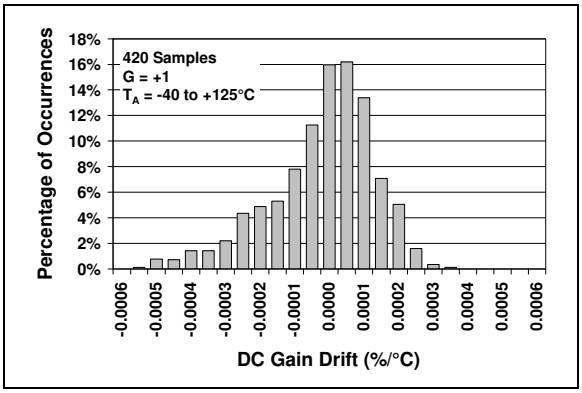


FIGURE 2-4: *DC Gain Drift, G = +1.*

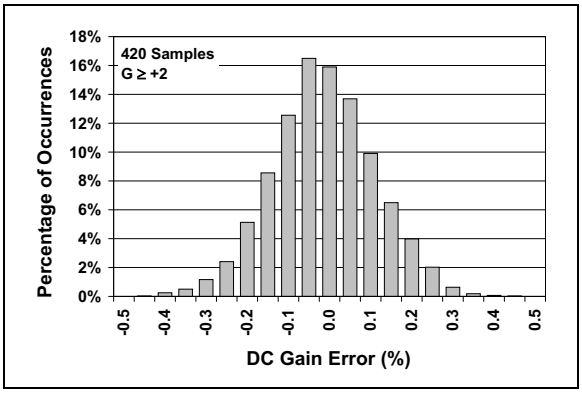


FIGURE 2-2: *DC Gain Error, G ≥+2.*

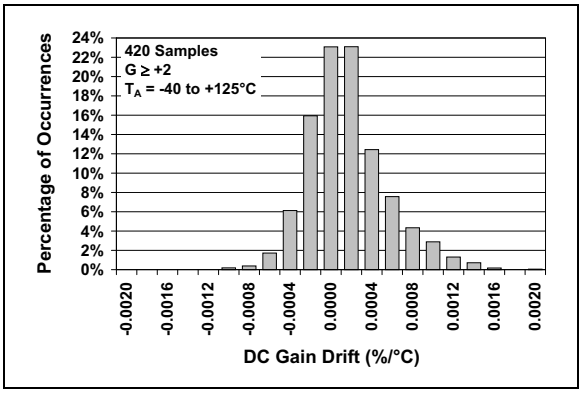


FIGURE 2-5: *DC Gain Drift, G ≥+2.*

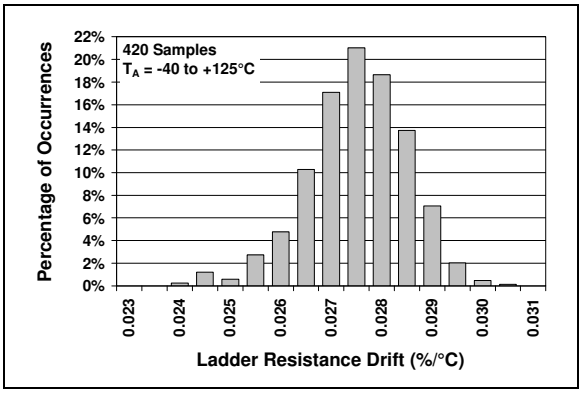


FIGURE 2-3: *Ladder Resistance Drift.*

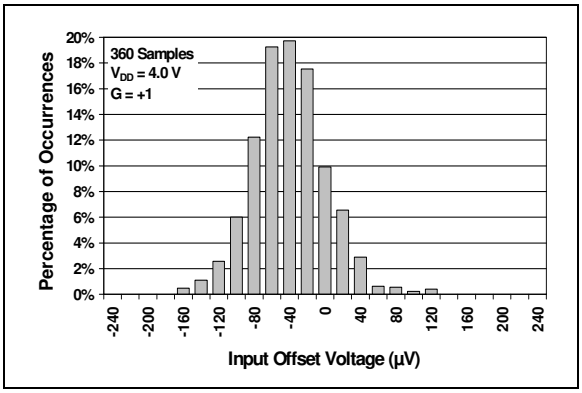


FIGURE 2-6: *Input Offset Voltage, V_{DD} = 4.0V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{REF} = V_{SS}, G= +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

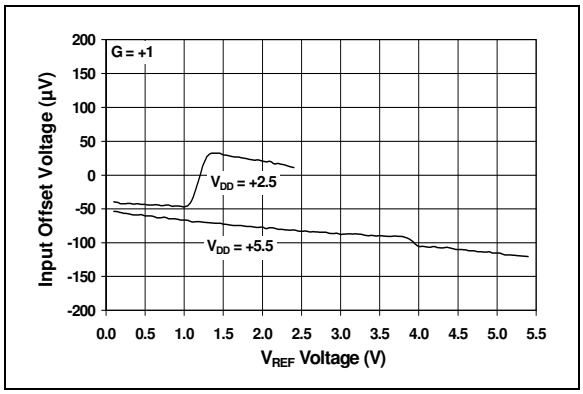


FIGURE 2-7: *Input Offset Voltage vs. V_{REF} Voltage.*

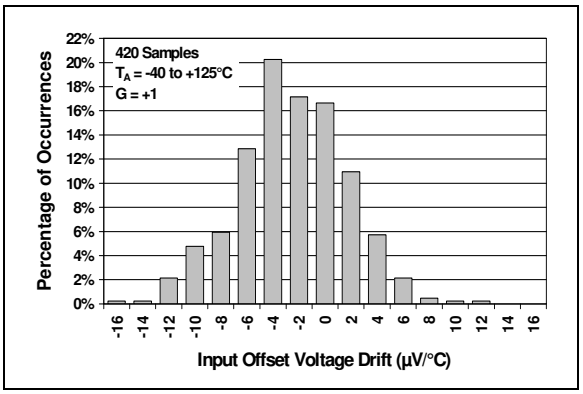


FIGURE 2-10: *Input Offset Voltage Drift.*

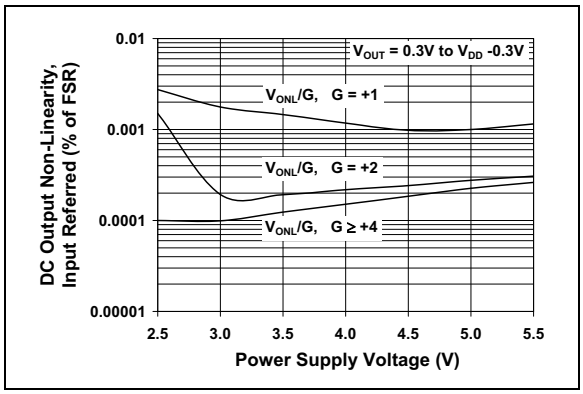


FIGURE 2-8: *DC Output Non-Linearity vs. Supply Voltage.*

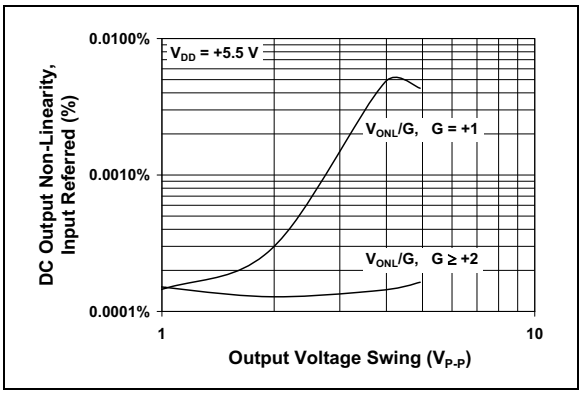


FIGURE 2-11: *DC Output Non-Linearity vs. Output Swing.*

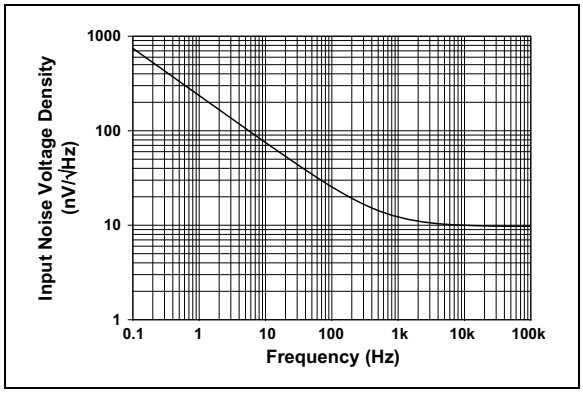


FIGURE 2-9: *Input Noise Voltage Density vs. Frequency.*

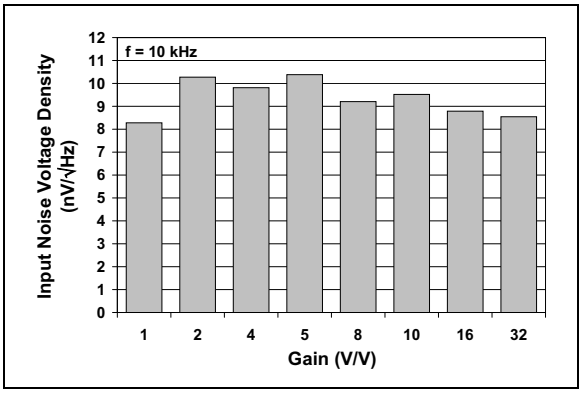


FIGURE 2-12: *Input Noise Voltage Density vs. Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{REF} = V_{SS}, G= +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

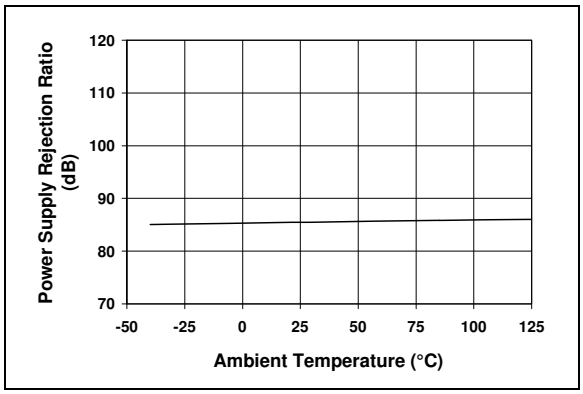


FIGURE 2-13: *PSRR vs. Ambient Temperature.*

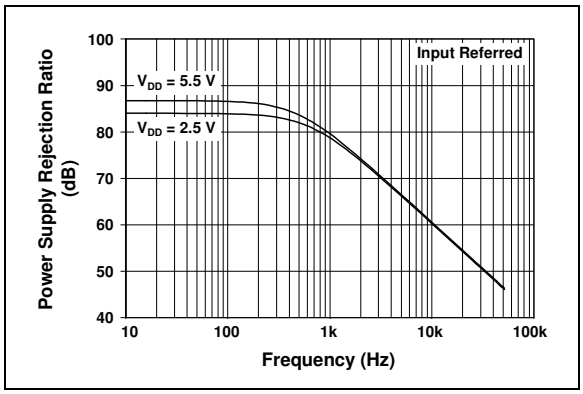


FIGURE 2-16: *PSRR vs. Frequency.*

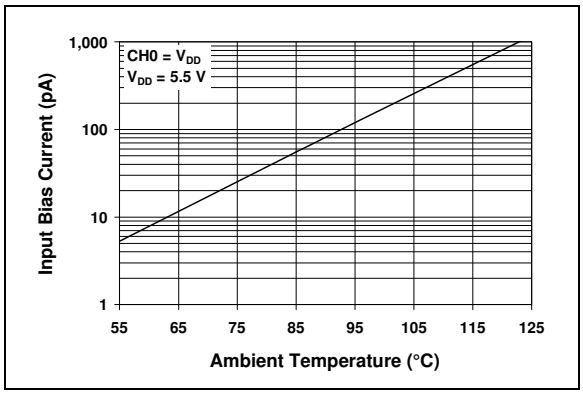


FIGURE 2-14: *Input Bias Current vs. Ambient Temperature.*

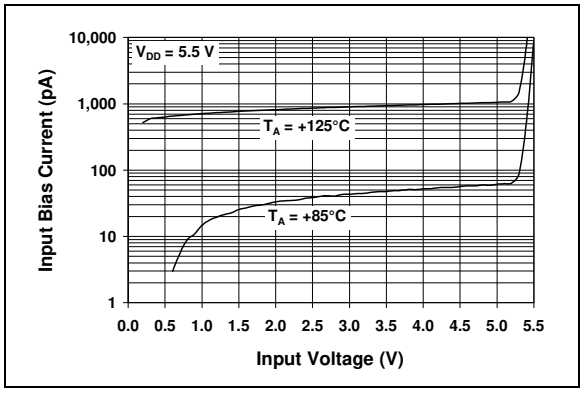


FIGURE 2-17: *Input Bias Current vs. Input Voltage.*

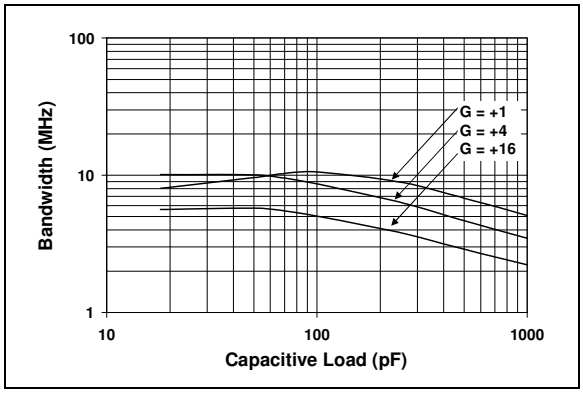


FIGURE 2-15: *Bandwidth vs. Capacitive Load.*

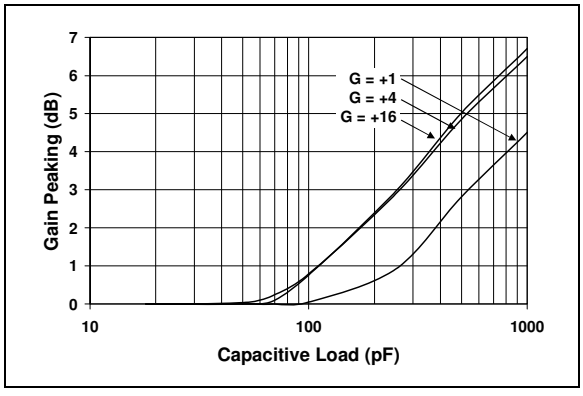


FIGURE 2-18: *Gain Peaking vs. Capacitive Load.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{REF} = V_{SS}, G= +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

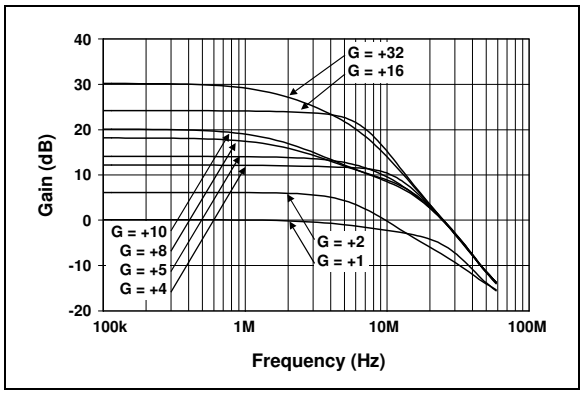


FIGURE 2-19: *Gain vs. Frequency.*

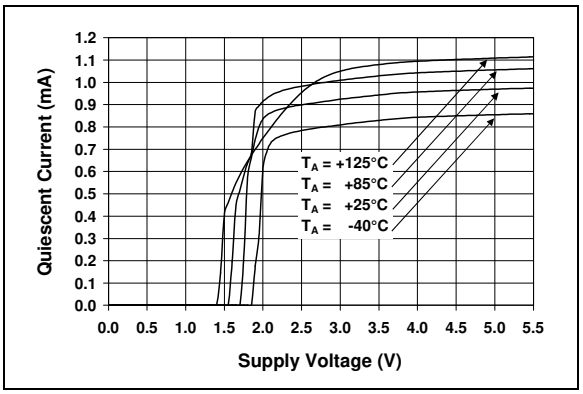


FIGURE 2-22: *Quiescent Current vs. Supply Voltage.*

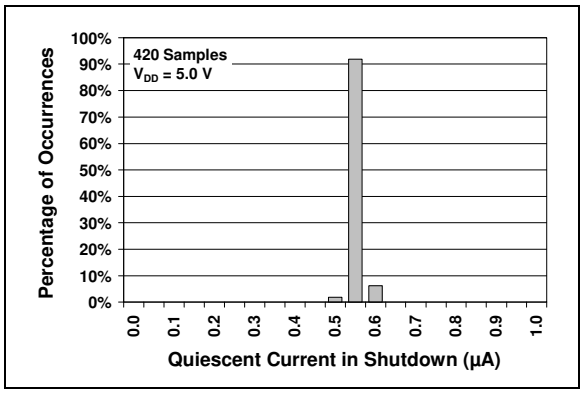


FIGURE 2-20: *Histogram of Quiescent Current in Shutdown Mode.*

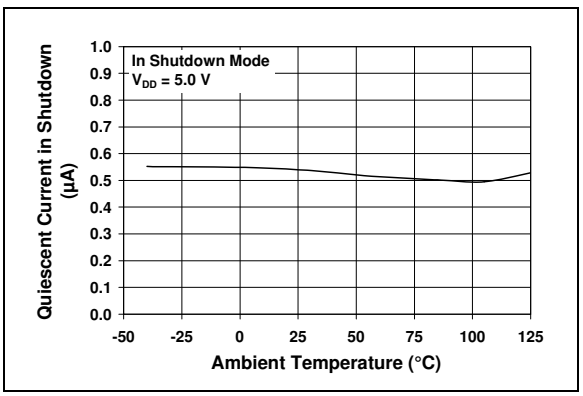


FIGURE 2-23: *Quiescent Current in Shutdown Mode vs. Ambient Temperature.*

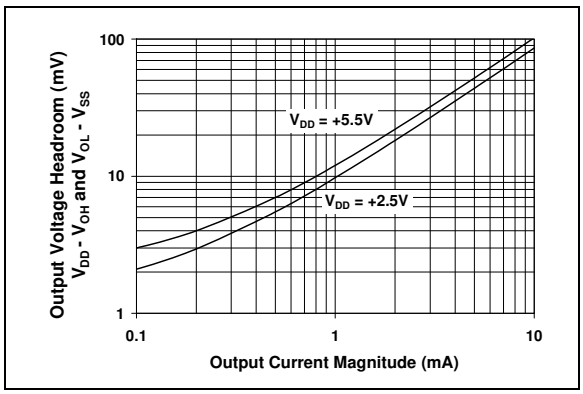


FIGURE 2-21: *Output Voltage Headroom vs. Output Current.*

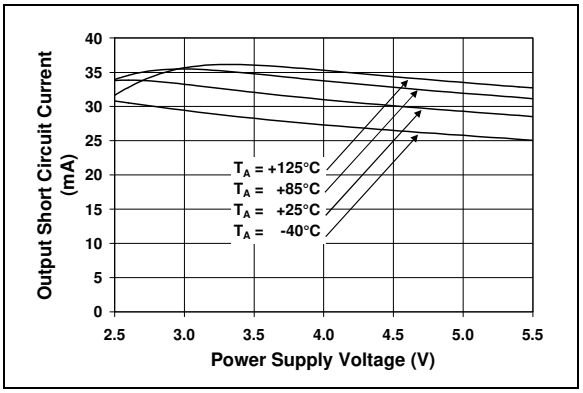


FIGURE 2-24: *Output Short Circuit Current vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{REF} = V_{SS}, G= +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

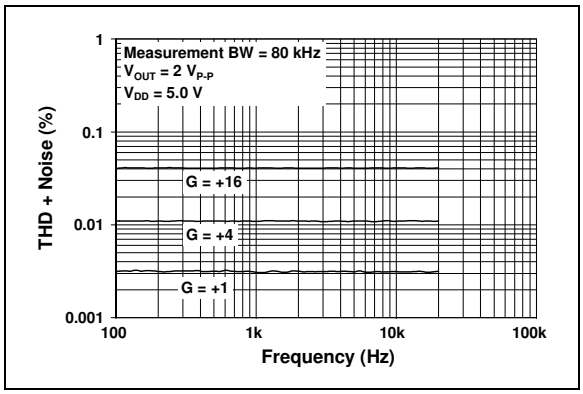


FIGURE 2-25: *THD plus Noise vs. Frequency, V_{OUT} = 2 V_{P-P}.*

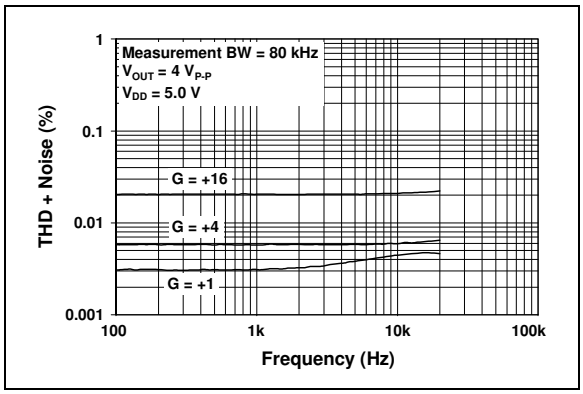


FIGURE 2-28: *THD plus Noise vs. Frequency, V_{OUT} = 4 V_{P-P}.*

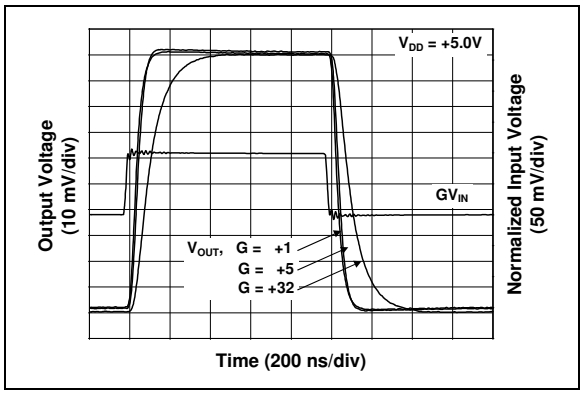


FIGURE 2-26: *Small Signal Pulse Response.*

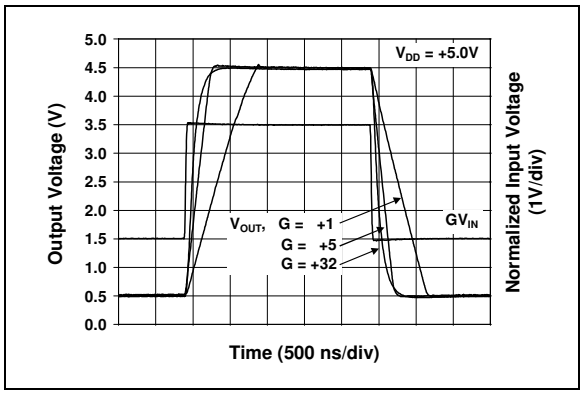


FIGURE 2-29: *Large Signal Pulse Response.*

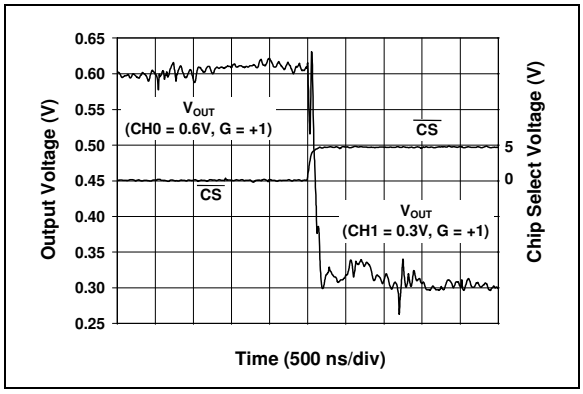


FIGURE 2-27: *Channel Select Timing.*

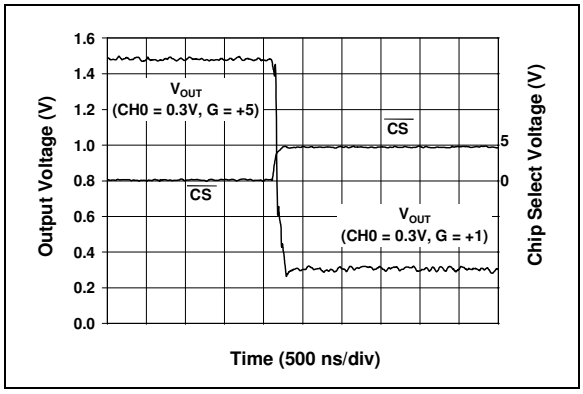


FIGURE 2-30: *Gain Select Timing.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{REF} = V_{SS}, G= +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

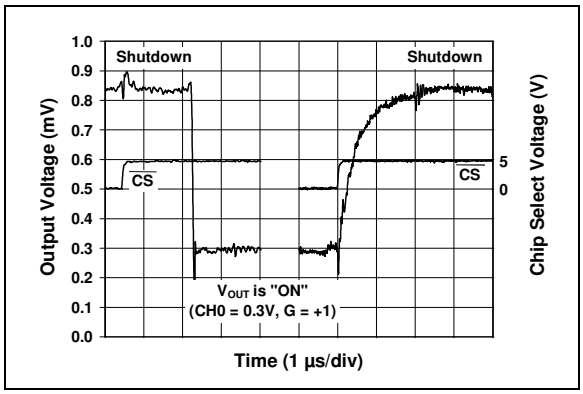


FIGURE 2-31: *Output Voltage vs. Shutdown Mode.*

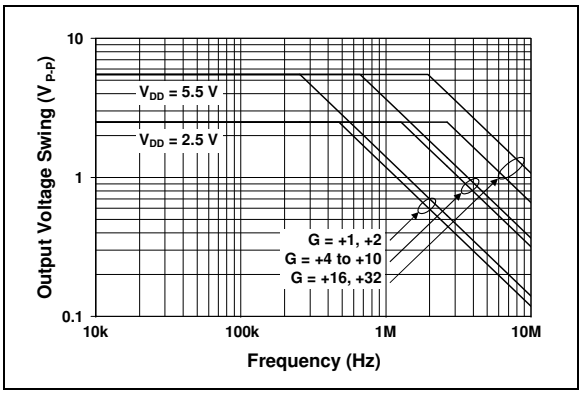


FIGURE 2-33: *Output Voltage Swing vs. Frequency.*

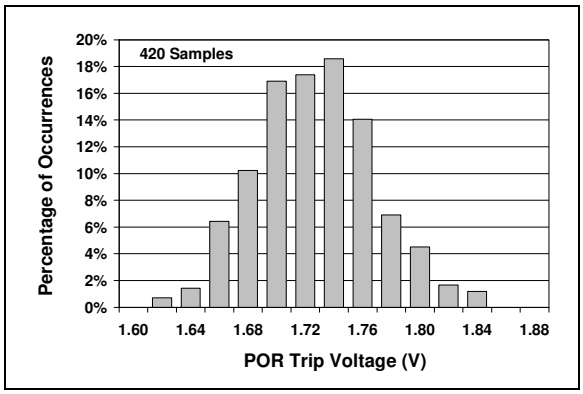


FIGURE 2-32: *POR Trip Voltage.*

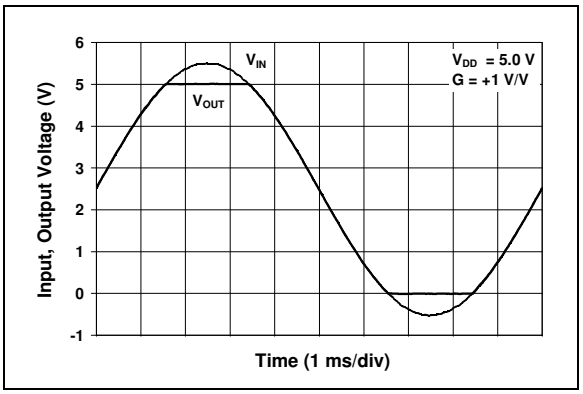


FIGURE 2-34: *The MCP6S21/2/6/8 family shows no phase reversal under overdrive.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6S21	MCP6S22	MCP6S26	MCP6S28	Symbol	Description
1	1	1	1	V_{OUT}	Analog Output
2	2	2	2	CH0	Analog Input
—	3	3	3	CH1	Analog Input
—	—	4	4	CH2	Analog Input
—	—	5	5	CH3	Analog Input
—	—	6	6	CH4	Analog Input
—	—	7	7	CH5	Analog Input
—	—	—	8	CH6	Analog Input
—	—	—	9	CH7	Analog Input
3	—	8	10	V_{REF}	External Reference Pin
4	4	9	11	V_{SS}	Negative Power Supply
5	5	10	12	$\overline{CS}$	SPI Chip Select
6	6	11	13	SI	SPI Serial Data Input
—	—	12	14	SO	SPI Serial Data Output
7	7	13	15	SCK	SPI Clock Input
8	8	14	16	V_{DD}	Positive Power Supply

3.1 Analog Output

The output pin (V_{OUT}) is a low-impedance voltage source. The selected gain (G), selected input (CH0-CH7) and voltage at V_{REF} determine its value.

3.2 Analog Inputs (CH0 thru CH7)

The inputs CH0 through CH7 connect to the signal sources. They are high-impedance CMOS inputs with low bias currents. The internal MUX selects which one is amplified to the output.

3.3 External Reference Voltage (V_{REF})

The V_{REF} pin should be at a voltage between V_{SS} and V_{DD} (the MCP6S22 has V_{REF} tied internally to V_{SS}). The voltage at this pin shifts the output voltage.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 2.5V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (0.1 µF) at the V_{DD} pin. It can share a bulk capacitor with nearby analog parts (typically 2.2 µF to 10 µF within 4 inches (100 mm) of the V_{DD} pin.

3.5 Digital Inputs

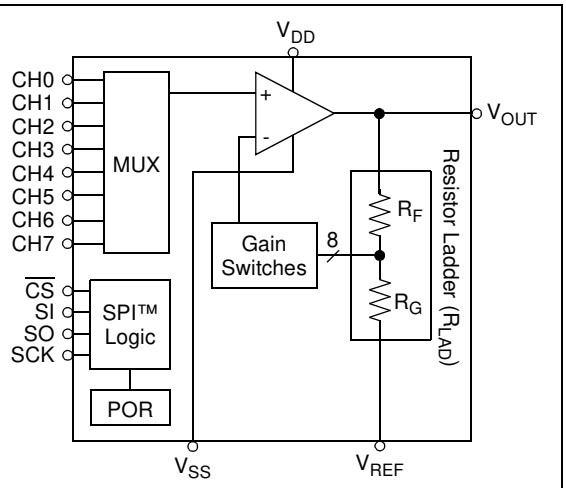
The SPI interface inputs are: Chip Select ($\overline{CS}$), Serial Input (SI) and Serial Clock (SCK). These are Schmitt-triggered, CMOS logic inputs.

3.6 Digital Output

The MCP6S26 and MCP6S28 devices have a SPI interface serial output (SO) pin. This is a CMOS push-pull output and does not ever go High-Z. Once the device is deselected ($\overline{CS}$ goes high), SO is forced low. This feature supports daisy chaining, as explained in Section 5.3, “Daisy Chain Configuration”.

4.0 ANALOG FUNCTIONS

The MCP6S21/2/6/8 family of Programmable Gain Amplifiers (PGA) are based on simple analog building blocks (see Figure 4-1). Each of these blocks will be explained in more detail in the following sub-sections.



MCP6S21–One input (CH0), no SO pin

MCP6S22–Two inputs (CH0, CH1), V_{REF} tied internally to V_{SS}, no SO pin

MCP6S26–Six inputs (CH0 to CH5)

MCP6S28–Eight inputs (CH0 to CH7)

FIGURE 4-1: *PGA Block Diagram.*

4.1 Input MUX

The MCP6S21 has one input, the MCP6S22 and MCP6S25 have two inputs, the MCP6S26 has six inputs and the MCP6S28 has eight inputs (see Figure 4-1).

For the lowest input current, float unused inputs. Tying these pins to a voltage near the used channels also works well. For simplicity, they can be tied to V_{SS} or V_{DD}, but the input current may increase.

The one channel MCP6S21 has the lowest input bias current, while the eight channel MCP6S28 has the highest. There is about a 2:1 ratio in I_B between these parts.

4.2 Internal Op Amp

The internal op amp provides the right combination of bandwidth, accuracy and flexibility.

4.2.1 COMPENSATION CAPACITORS

The internal op amp has three compensation capacitors connected to a switching network. They are selected to give good small signal bandwidth at high gains, and good slew rate (full power bandwidth) at low gains. The change in bandwidth as gain changes is between 2 MHz and 12 MHz. Refer to Table 4-1 for more information.

TABLE 4-1: GAIN VS. INTERNAL COMPENSATION CAPACITOR

Gain (V/V)	Internal Compensation Capacitor	Typical GBWP (MHz)	Typical SR (V/µs)	Typical FPBW (MHz)	Typical BW (MHz)
1	Large	12	4.0	0.30	12
2	Large	12	4.0	0.30	6
4	Medium	20	11	0.70	10
5	Medium	20	11	0.70	7
8	Medium	20	11	0.70	2.4
10	Medium	20	11	0.70	2.0
16	Small	64	22	1.6	5
32	Small	64	22	1.6	2.0

Note 1: FPBW is the Full Power Bandwidth. These numbers are based on V_{DD} = 5.0V.
2: No changes in DC performance (e.g., V_{OS}) accompany a change in compensation capacitor.
3: BW is the closed-loop, small signal -3 dB bandwidth.

4.2.2 RAIL-TO-RAIL INPUT

The input stage of the internal op amp uses two differential input stages in parallel; one operates at low V_{IN} (input voltage), while the other operates at high V_{IN}. With this topology, the internal inputs can operate to 0.3V past either supply rail. The input offset voltage is measured at both $V_{IN} = V_{SS}$ - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The transition between the two input stages occurs when $V_{IN} \approx V_{DD}$ - 1.5V. For the best distortion and gain linearity, avoid this region of operation.

4.2.3 RAIL-TO-RAIL OUTPUT

The Maximum Output Voltage Swing is the maximum swing possible under a particular output load. According to the specification table, the output can reach within 60 mV of either supply rail when R_L = 10 kΩ and $V_{REF} = V_{DD}/2$. See Figure 2-21 for typical performance under other conditions.

4.2.4 INPUT VOLTAGE AND PHASE REVERSAL

The amplifier family is designed with CMOS input devices. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-34 shows an input voltage exceeding both supplies with no resulting phase inversion.

The maximum voltage that can be applied to the input pins (CHX) is V_{SS} - 0.3V to V_{DD} + 0.3V. Voltages on the inputs that exceed this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor, as shown in Figure 4-2.

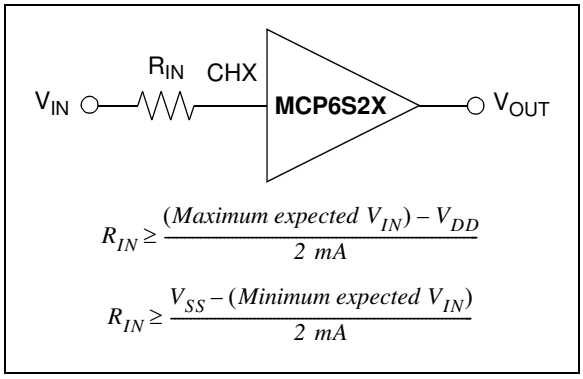


FIGURE 4-2: *R_{IN} limits the current flow into an input pin.*

4.3 Resistor Ladder

The resistor ladder shown in Figure 4-1 ($R_{LAD} = R_F + R_G$) sets the gain. Placing the gain switches in series with the inverting input reduces the parasitic capacitance, distortion and gain mismatch.

R_{LAD} is an additional load on the output of the PGA and causes additional current draw from the supplies.

In Shutdown mode, R_{LAD} is still attached to the OUT and V_{REF} pins. Thus, these pins and the internal amplifier's inverting input are all connected through R_{LAD} and the output is not high-Z (unlike the external op amp).

While R_{LAD} contributes to the output noise, its effect is small. Refer to Figure 2-12.

4.4 Shutdown Mode

These PGAs use a software shutdown command. When the SPI interface sends a shutdown command, the internal op amp is shut down and its output placed in a high-Z state.

The resistive ladder is always connected between V_{REF} and V_{OUT}; even in shutdown. This means that the output resistance will be on the order of 5 kΩ and there will be a path for output signals to appear at the input.

The Power-on Reset (POR) circuitry will temporarily place the part in shutdown when activated. See Section 5.4, "Power-On Reset", for details.

5.0 DIGITAL FUNCTIONS

The MCP6S21/2/6/8 PGAs use a standard SPI compatible serial interface to receive instructions from a controller. This interface is configured to allow daisy chaining with other SPI devices. There is an internal POR (Power On Reset) that resets the registers under low power conditions.

5.1 SPI Timing

Chip Select ($\overline{CS}$) toggles low to initiate communication with these devices. The first byte of each SI word (two bytes long) is the instruction byte, which goes into the Instruction Register. The Instruction Register points the second byte to its destination. In a typical application, $\overline{CS}$ is raised after one word (16 bits) to implement the desired changes. Section 5.3, "Registers", covers applications using multiple 16-bit words. SO goes low after $\overline{CS}$ goes high; it has a push-pull output that does not go into a high-Z state.

The MCP6S21/2/6/8 devices operate in SPI Modes 0,0 and 1,1. In 0,0 mode, the clock idles in the low state (Figure 5-1) and, in 1,1 mode, the clock idles in the high state (Figure 5-2). In both modes, SI data is loaded into the PGA on the rising edge of SCK and SO data is clocked out on the falling edge of SCK. In 0,0 mode, the falling edge of $\overline{CS}$ also acts as the first falling edge of SCK (see Figure 5-1). There must be multiples of 16 clocks (SCK) while $\overline{CS}$ is low or commands will abort (see Section 5.3, "Registers").

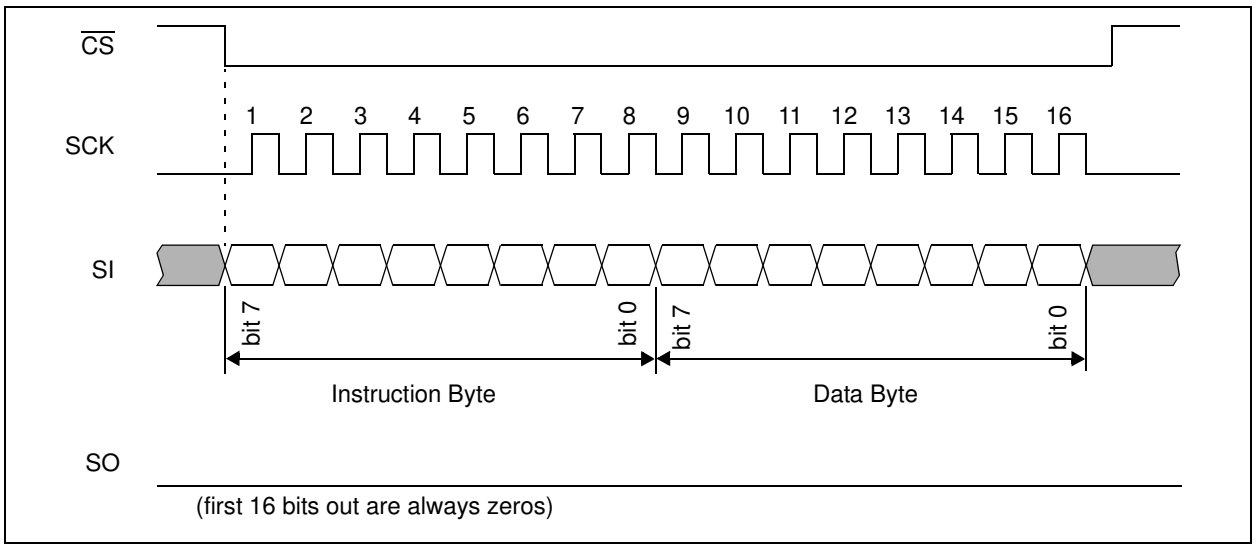


FIGURE 5-1: *Serial bus sequence for the PGA; SPI 0,0 mode (see Figure 1-5).*

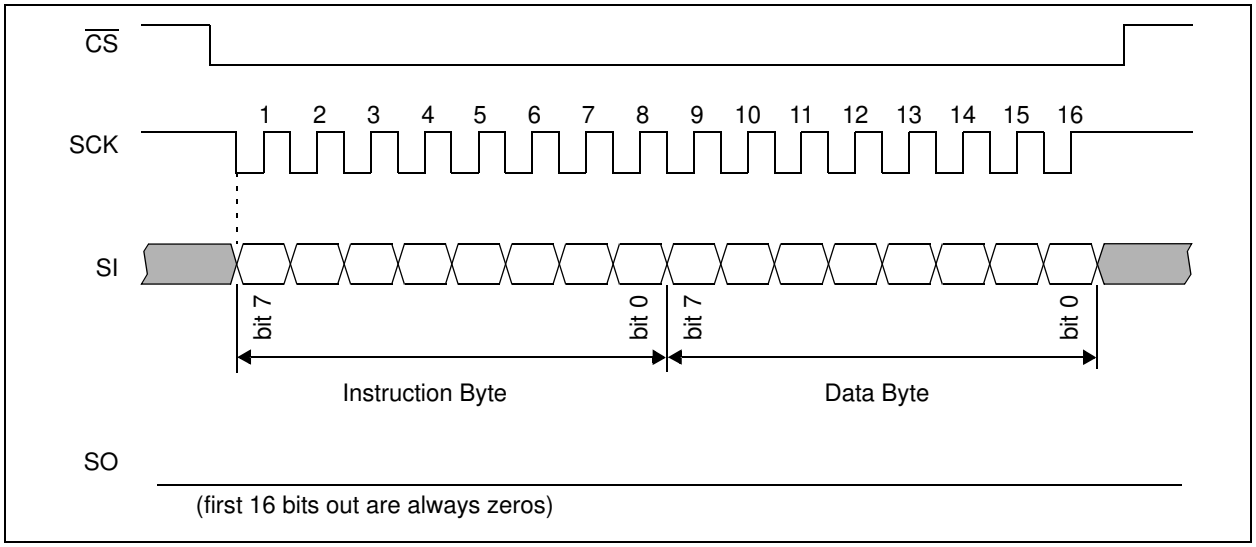


FIGURE 5-2: *Serial bus sequence for the PGA; SPI 1,1 mode (see Figure 1-6).*

5.2 Registers

The analog functions are programmed through the SPI interface using 16-bit words (see Figure 5-1 and Figure 5-2). This data is sent to two of three 8-bit registers: Instruction Register (Register 5-1), Gain Register (Register 5-2) and Channel Register (Register 5-3). The power-up defaults for these three registers are:

- Instruction Register: 000x xxx0
- Gain Register: xxxx x000
- Channel Register: xxxx x000

Thus, these devices are initially programmed with the Instruction Register set for NOP (no operation), a gain of +1 V/V and CH0 as the input channel.

5.2.1 INSTRUCTION REGISTER

The Instruction Register has 3 command bits and 1 indirect address bit; see Register 5-1. The command bits include a NOP (000) to support daisy chaining (see Section 5.3, "Registers"); the other NOP commands shown should not be used (they are reserved for future use). The device is brought out of Shutdown mode when a valid command, other than NOP or Shutdown, is sent and $\overline{CS}$ is raised.

REGISTER 5-1: INSTRUCTION REGISTER

W-0	W-0	W-0	U-x	U-x	U-x	U-x	W-0
M2	M1	M0	—	—	—	—	A0
bit 7							bit 0

bit 7-5 **M2-M0: Command Bits**

000 = NOP (Default) **(Note 1)**
001 = PGA enters Shutdown Mode as soon as a full 16-bit word is sent and $\overline{CS}$ is raised. **(Notes 1 and 2)**
010 = Write to register.
011 = NOP (reserved for future use) **(Note 1)**
1XX = NOP (reserved for future use) **(Note 1)**

bit 4-1 **Unimplemented:** Read as '0' (reserved for future use)

bit 0 **A0: Indirect Address Bit**

1 = Addresses the Channel Register
0 = Addresses the Gain Register (Default)

Note 1: All other bits in the 16-bit word (including A0) are "don't cares".

2: The device exits Shutdown mode when a valid command (other than NOP or Shutdown) is sent and $\overline{CS}$ is raised; that valid command will be executed. Shutdown does not toggle.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5.2.2 SETTING THE GAIN

The amplifier can be programmed to produce binary and decimal gain settings between +1 V/V and +32 V/V. Register 5-2 shows the details. At the same time, different compensation capacitors are selected to optimize the bandwidth vs. slew rate trade-off (see Table 4-1).

REGISTER 5-2: GAIN REGISTER

U-x	U-x	U-x	U-x	U-x	W-0	W-0	W-0
—	—	—	—	—	G2	G1	G0
bit 7							bit 0

bit 7-3 **Unimplemented:** Read as ‘0’ (reserved for future use)

bit 2-0 **G2-G0: Gain Select Bits**

000 = Gain of +1 (Default)
001 = Gain of +2
010 = Gain of +4
011 = Gain of +5
100 = Gain of +8
101 = Gain of +10
110 = Gain of +16
111 = Gain of +32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

5.2.3 CHANGING THE CHANNEL

If the instruction register is programmed to address the channel register, the multiplexed inputs of the MCP6S22, MCP6S26 and MCP6S28 can be changed per Register 5-3.

REGISTER 5-3: CHANNEL REGISTER

U-x	U-x	U-x	U-x	U-x	W-0	W-0	W-0
—	—	—	—	—	C2	C1	C0
bit 7							bit 0

bit 7-3 **Unimplemented:** Read as ‘0’ (reserved for future use)

bit 2-0 **C2-C0: Channel Select Bits**

	MCP6S21	**MCP6S22**	**MCP6S26**	**MCP6S28**
000 =	CH0 (Default)	CH0 (Default)	CH0 (Default)	CH0 (Default)
001 =	CH0	CH1	CH1	CH1
001 =	CH0	CH0	CH2	CH2
011 =	CH0	CH1	CH3	CH3
100 =	CH0	CH0	CH4	CH4
101 =	CH0	CH1	CH5	CH5
110 =	CH0	CH0	CH0	CH6
111 =	CH0	CH1	CH0	CH7

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

5.2.4 SHUTDOWN COMMAND

The software Shutdown command allows the user to put the amplifier into a low power mode (see Register 5-1). In this shutdown mode, most pins are high impedance (Section 4.4, “Shutdown Mode”, and Section 5.1, “SPI Timing”, cover the exceptions at pins V_{REF}, V_{OUT} and SO).

Once the PGA has entered shutdown mode, it will remain in this mode until either a valid command is sent to the device (other than NOP or Shutdown), or the device is powered down and back up again. The internal registers maintain their values while in shutdown.

Once brought out of shutdown mode, the part comes back to its previous state (see Section 5.4 for exceptions to this rule). This makes it possible to bring the device out of shutdown mode using one command; send a command to select the current channel (or gain) and the device will exit shutdown with the same state that existed before shutdown.

5.3 Daisy Chain Configuration

Multiple devices can be connected in a daisy chain configuration by connecting the SO pin from one device to the SI pin on the next device and using common SCK and $\overline{CS}$ lines (Figure 5-3). This approach reduces PCB layout complexity.

The example in Figure 5-3 shows a daisy chain configuration with two devices, although any number of devices can be configured this way. The MCP6S21 and MCP6S22 can only be used at the far end of the daisy chain because they do not have a serial data out (SO) pin. As shown in Figure 5-4 and Figure 5-5, both SI and SO data are sent in 16-bit (2 byte) words. These devices abort any command that is not a multiple of 16 bits.

When using the daisy chain configuration, the maximum clock speed possible is reduced to ≈ 5.8 MHz because of the SO pin’s propagation delay (see Electrical Specifications).

The internal SPI shift register is automatically loaded with zeros whenever $\overline{CS}$ goes high (a command is executed). Thus, the first 16-bits out of the SO pin once $\overline{CS}$ line goes low are always zeros. This means that the first command loaded into the next device in the daisy chain is a NOP. This feature makes it possible to send shorter command and data byte strings when the farthest devices do not need to change. For example, if there were three devices on the chain and only the middle device needed changing, only 32 bytes of data need to be transmitted (for the first and middle devices), and the last device on the chain would receive a NOP when the $\overline{CS}$ pin is raised to execute the command.

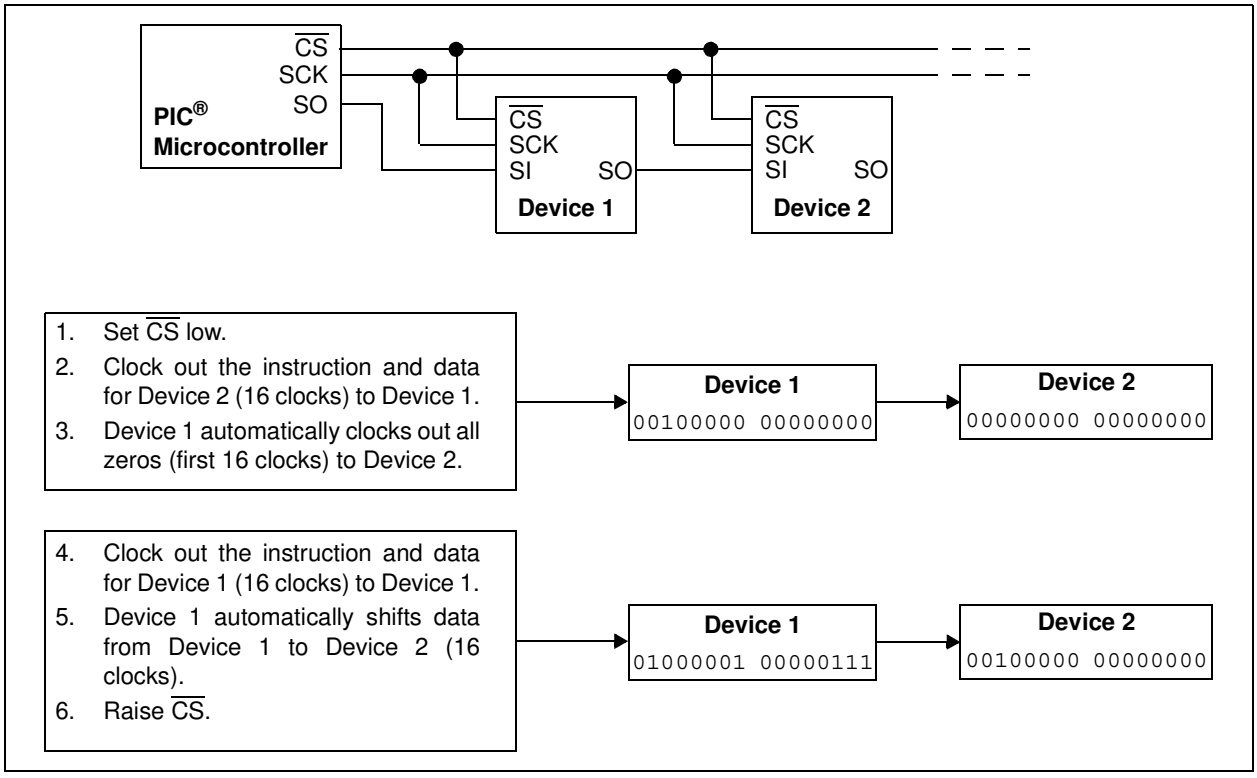


FIGURE 5-3: *Daisy Chain Configuration.*

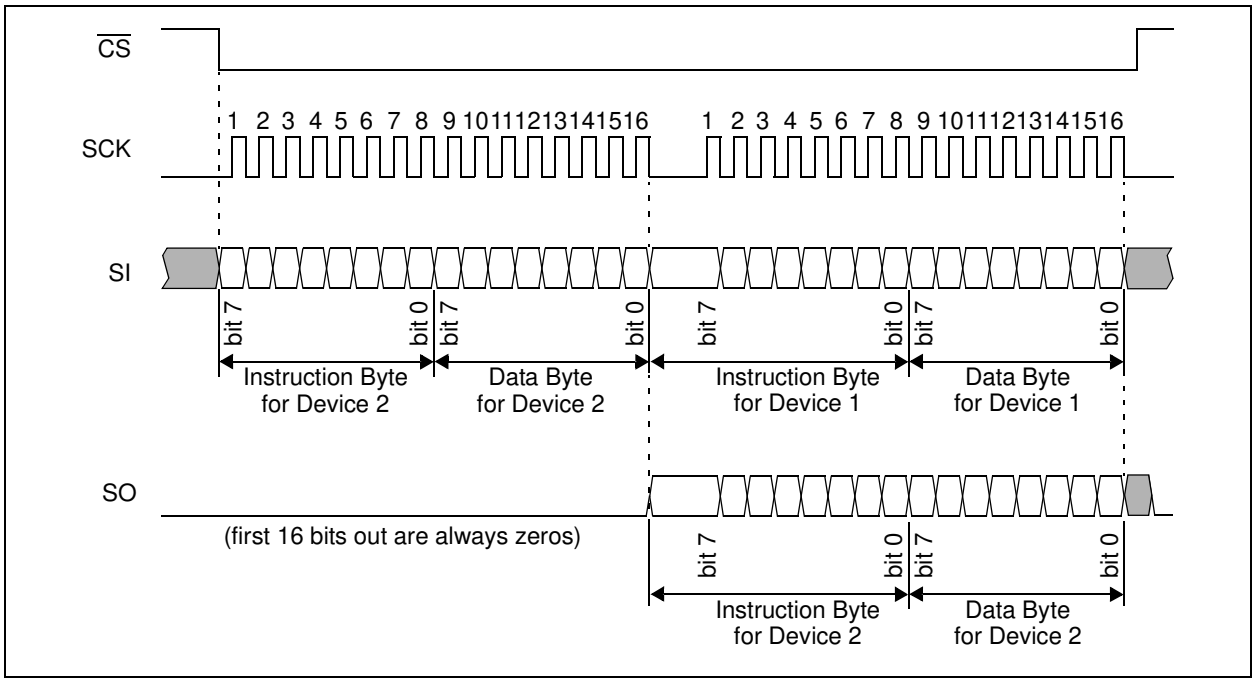


FIGURE 5-4: *Serial bus sequence for daisy-chain configuration; SPI 0,0 mode.*

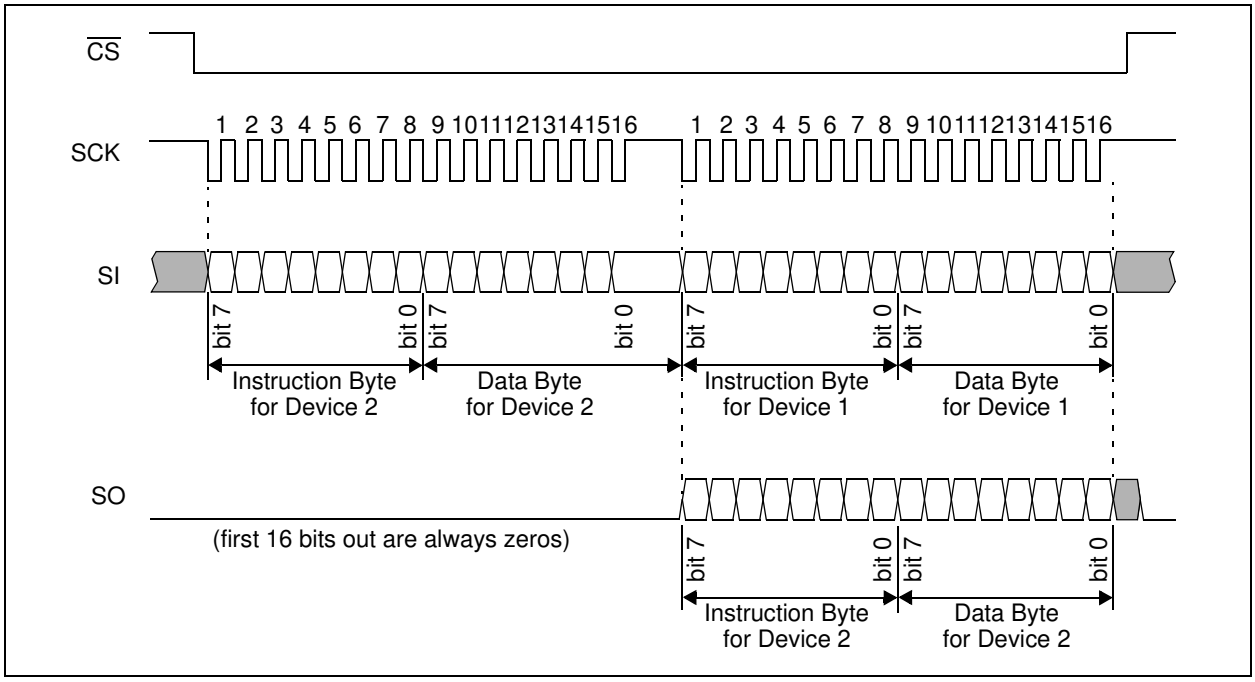


FIGURE 5-5: *Serial bus sequence for daisy-chain configuration; SPI 1,1 mode.*

5.4 Power-On Reset

If the power supply voltage goes below the POR trip voltage ($V_{DD} < V_{POR} \approx 1.7V$), the internal POR circuit will reset all of the internal registers to their power-up defaults (this is a protection against low power supply voltages). The POR circuit also holds the part in shutdown mode while it is activated. It temporarily overrides the software shutdown status. The POR releases the shutdown circuitry once it is released ($V_{DD} > V_{POR}$).

A 0.1 µF bypass capacitor mounted as close as possible to the V_{DD} pin provides additional transient immunity.

6.0 APPLICATIONS INFORMATION

6.1 Changing External Reference Voltage

Figure 6-1 shows a MCP6S21 with the V_{REF} pin at 2.5V and V_{DD} = 5.0V. This allows the PGA to amplify signals centered on 2.5V, instead of ground-referenced signals. The voltage reference MCP1525 is buffered by a MCP6021, which gives a low output impedance reference voltage from DC to high frequencies. The source driving the V_{REF} pin should have an output impedance of $\leq 0.1\Omega$ to maintain reasonable gain accuracy.

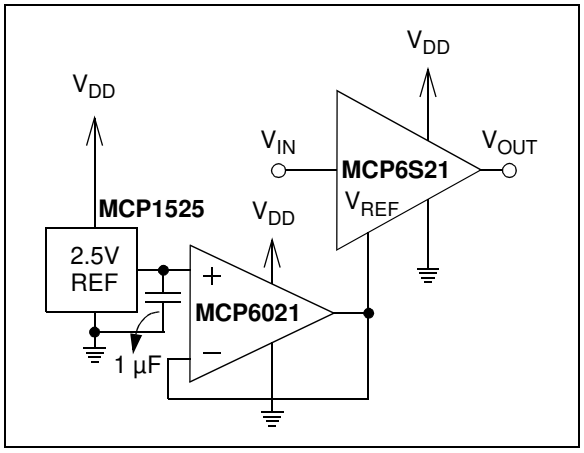


FIGURE 6-1: *PGA with Different External Reference Voltage.*

6.2 Capacitive Load and Stability

Large capacitive loads can cause both stability problems and reduced bandwidth for the MCP6S21/2/6/8 family of PGAs (Figure 2-17 and Figure 2-18). This happens because a large load capacitance decreases the internal amplifier's phase margin and bandwidth.

If the PGA drives a large capacitive load, the circuit in Figure 6-2 can be used. A small series resistor (R_{ISO}) at the V_{OUT} improves the phase margin by making the load resistive at high frequencies. It will not, however, improve the bandwidth.

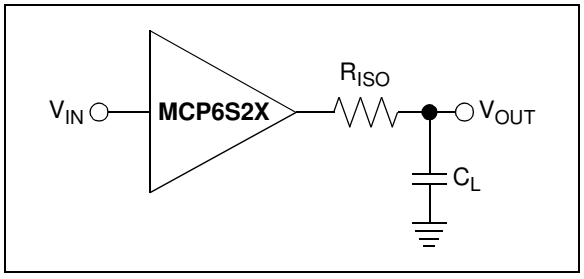


FIGURE 6-2: *PGA Circuit for Large Capacitive Loads.*

For $C_L \geq 100$ pF, a good estimate for R_{ISO} is 50Ω. This value can be fine-tuned on the bench. Adjust R_{ISO} so that the step response overshoot and frequency response peaking are acceptable at all gains.

6.3 Layout Considerations

Good PC board layout techniques will help achieve the performance shown in the Electrical Characteristics and Typical Performance Curves. It will also help minimize EMC (Electro-Magnetic Compatibility) issues.

6.3.1 COMPONENT PLACEMENT

Separate circuit functions; digital from analog, low speed from high speed, and low power from high power, as this will reduce crosstalk.

Keep sensitive traces short and straight, separating them from interfering components and traces. This is especially important for high frequency (low rise time) signals.

Use a 0.1 µF supply bypass capacitor within 0.1 inch (2.5 mm) of the V_{DD} pin. It must connect directly to the ground plane. A multi-layer ceramic chip capacitor, or high-frequency equivalent, works best.

6.3.2 SIGNAL COUPLING

The input pins of the MCP6S21/2/6/8 family of operational amplifiers (op amps) are high-impedance. This makes them especially susceptible to capacitively-coupled noise. Using a ground plane helps reduce this problem.

When noise is capacitively-coupled, the ground plane provides additional shunt capacitance to ground. When noise is magnetically coupled, the ground plane reduces the mutual inductance between traces. Increasing the separation between traces makes a significant difference.

Changing the direction of one of the traces can also reduce magnetic coupling. It may help to locate guard traces next to the victim trace. They should be on both sides of the victim trace and be as close as possible. Connect the guard traces to the ground plane at both ends, and in the middle, of long traces.

6.3.3 HIGH FREQUENCY ISSUES

Because the MCP6S21/2/6/8 PGAs reach unity gain near 64 MHz when G = 16 and 32, it is important to use good PCB layout techniques. Any parasitic coupling at high frequency might cause undesired peaking. Filtering high frequency signals (i.e., fast edge rates) can help. To minimize high frequency problems:

- Use complete ground and power planes
- Use HF, surface mount components
- Provide clean supply voltages and bypassing
- Keep traces short and straight
- Try a linear power supply (e.g., an LDO)