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MCP6S91/2/3

Single-Ended, Rail-to-Rail I/O, Low-Gain PGA

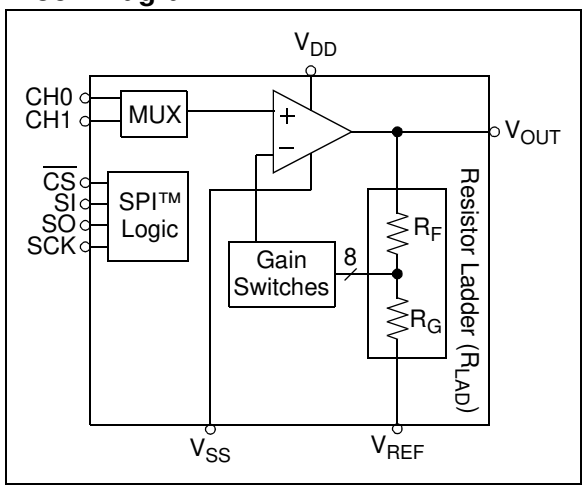
Features

- Multiplexed Inputs: 1 or 2 channels
- 8 Gain Selections:
  - +1, +2, +4, +5, +8, +10, +16 or +32 V/V
- Serial Peripheral Interface (SPI™)
- Rail-to-Rail Input and Output
- Low Gain Error: ±1% (max.)
- Offset Mismatch Between Channels: 0 µV
- High Bandwidth: 1 to 18 MHz (typ.)
- Low Noise: 10 nV/√Hz @ 10 kHz (typ.)
- Low Supply Current: 1.0 mA (typ.)
- Single Supply: 2.5V to 5.5V
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- A/D Converter Driver
- Multiplexed Analog Applications
- Data Acquisition
- Industrial Instrumentation
- Test Equipment
- Medical Instrumentation

Block Diagram

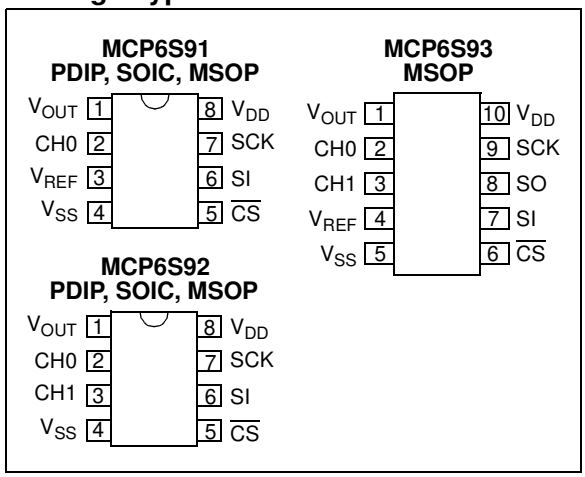


Description

The Microchip Technology Inc. MCP6S91/2/3 are analog Programmable Gain Amplifiers (PGAs). They can be configured for gains from +1 V/V to +32 V/V and the input multiplexer can select one of up to two channels through a SPI port. The serial interface can also put the PGA into shutdown to conserve power. These PGAs are optimized for high-speed, low offset voltage and single-supply operation with rail-to-rail input and output capability. These specifications support single-supply applications needing flexible performance or multiple inputs.

The one-channel MCP6S91 and the two-channel MCP6S92 are available in 8-pin PDIP, SOIC and MSOP packages. The two-channel MCP6S93 is available in a 10-pin MSOP package. All parts are fully specified from -40°C to +125°C.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
All inputs and outputs..... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pin .....±2 mA
Current at Output and Supply Pins..... ±30 mA
Storage temperature .....-65°C to +150°C
Junction temperature .....+150°C
ESD protection on all pins (HBM; MM) ..... ≥ 4 kV; 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{OUT}	Analog Output
CH0, CH1	Analog Inputs
V_{REF}	External Reference Pin
V_{SS}	Negative Power Supply
$\overline{CS}$	SPI Chip Select
SI	SPI Serial Data Input
SO	SPI Serial Data Output
SCK	SPI Clock Input
V_{DD}	Positive Power Supply

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, $V_{REF} = V_{SS}$, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters		Sym	Min	Typ	Max	Units	Conditions
Amplifier Inputs (CH0, CH1)							
Input Offset Voltage		V_{OS}	-4	—	+4	mV	G = +1
Input Offset Voltage Mismatch		ΔV_{OS}	—	0	—	µV	Between inputs (CH0, CH1)
Input Offset Voltage Drift		$\Delta V_{OS}/\Delta T_A$	—	±1.8	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection Ratio		PSRR	70	90	—	dB	G = +1 **(Note 1)**
Input Bias Current		I_B	—	±1	—	pA	CHx = $V_{DD}/2$
Input Bias Current at Temperature		I_B	—	30	—	pA	CHx = $V_{DD}/2$, T_A = +85°C
		I_B	—	600	—	pA	CHx = $V_{DD}/2$, T_A = +125°C
Input Impedance		Z_{IN}	—	$10^{13}\|\|7$	—	Ω||pF	
Input Voltage Range		V_{IVR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	**(Note 2)**
Reference Input (V_{REF})							
Input Impedance		Z_{IN_REF}	—	(5/G)||6	—	kΩ||pF	
Voltage Range		V_{IVR_REF}	V_{SS}	—	V_{DD}	V	**(Note 2)**
Amplifier Gain							
Nominal Gains		G	—	1 to 32	—	V/V	+1, +2, +4, +5, +8, +10, +16 or +32
DC Gain Error	G = +1	g_E	-0.2	—	+0.2	%	$V_{OUT} \approx 0.3V$ to $V_{DD} - 0.3V$
	G ≥ +2	g_E	-1.0	—	+1.0	%	$V_{OUT} \approx 0.3V$ to $V_{DD} - 0.3V$
DC Gain Drift	G = +1	$\Delta G/\Delta T_A$	—	±0.0002	—	%/°C	T_A = -40°C to +125°C
	G ≥ +2	$\Delta G/\Delta T_A$	—	±0.0004	—	%/°C	T_A = -40°C to +125°C

Note 1: R_{LAD} (R_F+R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S92 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. It is recommended that the MCP6S92's V_{SS} pin be tied directly to ground to avoid noise problems.

2: The MCP6S92's V_{IVR} and V_{IVR_REF} are not tested in production; they are set by design and characterization.

3: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Ladder Resistance						
Ladder Resistance	R_{LAD}	3.4	4.9	6.4	kΩ	**(Note 1)**
Ladder Resistance across Temperature	$\Delta R_{LAD}/\Delta T_A$	—	+0.028	—	%/°C	T_A = -40°C to +125°C **(Note 1)**
Amplifier Output						
DC Output Non-linearity G = +1	V_{ONL}	—	±0.18	—	% of FSR	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
G ≥ +2	V_{ONL}	—	±0.050	—	% of FSR	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
Maximum Output Voltage Swing	V_{OH_ANA}, V_{OL_ANA}	V_{SS} + 20	—	V_{DD} – 100	mV	G ≥ +2; 0.5V output overdrive
		V_{SS} + 60	—	V_{DD} – 60		G ≥ +2; 0.5V output overdrive, V_{REF} = V_{DD}/2
Short Circuit Current	I_{SC}	—	±25	—	mA	
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Minimum Valid Supply Voltage	V_{DD_VAL}	—	0.4	2.0	V	Register data still valid
Quiescent Current	I_Q	0.4	1.0	1.6	mA	I_O = 0 **(Note 3)**
Quiescent Current, Shutdown Mode	I_{Q_SHDN}	—	30	—	pA	I_O = 0 **(Note 3)**

Note 1: R_{LAD} (R_F+R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S92 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. It is recommended that the MCP6S92's V_{SS} pin be tied directly to ground to avoid noise problems.

2: The MCP6S92's V_{IVR} and V_{IVR_REF} are not tested in production; they are set by design and characterization.

3: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$, C_L = 60 pF, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
-3 dB Bandwidth	BW	—	1 to 18	—	MHz	All gains; V_{OUT} < 100 mV_{P-P} **(Note 1)**
Gain Peaking	GPK	—	0	—	dB	All gains; V_{OUT} < 100 mV_{P-P}
Total Harmonic Distortion plus Noise						
f = 20 kHz, G = +1 V/V	THD+N	—	0.0011	—	%	V_{OUT} = 1.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz, R_L = 10 kΩ to 1.5V
f = 20 kHz, G = +1 V/V	THD+N	—	0.0089	—	%	V_{OUT} = 2.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +4 V/V	THD+N	—	0.0045	—	%	V_{OUT} = 2.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +16 V/V	THD+N	—	0.028	—	%	V_{OUT} = 2.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
Step Response						
Slew Rate	SR	—	4.0	—	V/µs	G = 1, 2
		—	11	—	V/µs	G = 4, 5, 8, 10
		—	22	—	V/µs	G = 16, 32
Noise						
Input Noise Voltage	E_{ni}	—	4.5	—	μV_{P-P}	f = 0.1 Hz to 10 Hz **(Note 2)**
		—	30	—		f = 0.1 Hz to 200 kHz **(Note 2)**
Input Noise Voltage Density	e_{ni}	—	10	—	nV/√Hz	f = 10 kHz **(Note 2)**
Input Noise Current Density	i_{ni}	—	4	—	fA/√Hz	f = 10 kHz

Note 1: See Table 4-1 for a list of typical numbers and Figure 2-25 for the frequency response versus gain.

2: E_{ni} and e_{ni} include ladder resistance noise. See Figure 2-12 for e_{ni} versus G data.

DIGITAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2, C_L = 60 pF, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
SPI Inputs ($\overline{CS}$, SI, SCK)						
Logic Threshold, Low	V_{IL}	0	—	0.3V_{DD}	V	
Input Leakage Current	I_{IL}	-1.0	—	+1.0	µA	
Logic Threshold, High	V_{IH}	0.7 V_{DD}	—	V_{DD}	V	
Amplifier Output Leakage Current	—	-1.0	—	1.0	µA	In Shutdown mode
SPI Output (SO, for MCP6S93)						
Logic Threshold, Low	V_{OL_DIG}	V_{SS}	—	V_{SS}+0.4	V	I_{OL} = 2.1 mA, V_{DD} = 5V
Logic Threshold, High	V_{OH_DIG}	V_{DD} – 0.5	—	V_{DD}	V	I_{OH} = -400 µA
SPI Timing						
Pin Capacitance	C_{PIN}	—	10	—	pF	All digital I/O pins
Input Rise/Fall Times ($\overline{CS}$, SI, SCK)	t_{RFI}	—	—	2	µs	**(Note 1)**
Output Rise/Fall Times (SO)	t_{RFO}	—	5	—	ns	**MCP6S93**
$\overline{CS}$ High Time	t_{CSH}	40	—	—	ns	
SCK Edge to $\overline{CS}$ Fall Setup Time	t_{CS0}	10	—	—	ns	SCK edge when $\overline{CS}$ is high
$\overline{CS}$ Fall to First SCK Edge Setup Time	t_{CSSC}	40	—	—	ns	
SCK Frequency	f_{SCK}	—	—	10	MHz	V_{DD} = 5V **(Note 2)**
SCK High Time	t_{HI}	40	—	—	ns	
SCK Low Time	t_{LO}	40	—	—	ns	
SCK Last Edge to $\overline{CS}$ Rise Setup Time	t_{SCCS}	30	—	—	ns	
$\overline{CS}$ Rise to SCK Edge Setup Time	t_{CS1}	100	—	—	ns	SCK edge when $\overline{CS}$ is high
SI Setup Time	t_{SU}	40	—	—	ns	
SI Hold Time	t_{HD}	10	—	—	ns	
SCK to SO Valid Propagation Delay	t_{DO}	—	—	80	ns	**MCP6S93**
$\overline{CS}$ Rise to SO Forced to Zero	t_{SOZ}	—	—	80	ns	**MCP6S93**
Channel and Gain Select Timing						
Channel Select Time	t_{CH}	—	1.5	—	µs	CHx = 0.6V, CHy = 0.3V, G = 1, CHx to CHy select, $\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point
Gain Select Time	t_G	—	1	—	µs	CHx = CHy = 0.3V, G = 5 to G = 1 select, $\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point
Shutdown Mode Timing						
Out of Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output Turn-on Time	t_{ON}	—	3.5	10	µs	$\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point
Into Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output High-Z Turn-off Time	t_{OFF}	—	1.5	—	µs	$\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point

Note 1: Not tested in production. Set by design and characterization.

2: When using the device in the daisy-chain configuration, maximum clock frequency is determined by a combination of propagation delay time ($t_{DO} \leq$ 80 ns), data input set-up time ($t_{SU} \geq$ 40 ns), SCK high time ($t_{HI} \geq$ 40 ns) and SCK rise and fall times of 5 ns. Maximum f_{SCK} is therefore ≈ 5.8 MHz.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 10L-MSOP	θ_{JA}	—	143	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed Maximum Junction Temperature (+150°C).

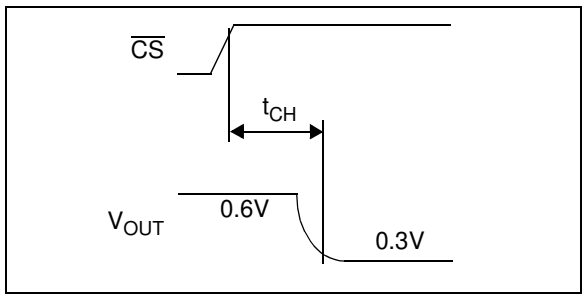


FIGURE 1-1: *Channel Select Timing Diagram.*

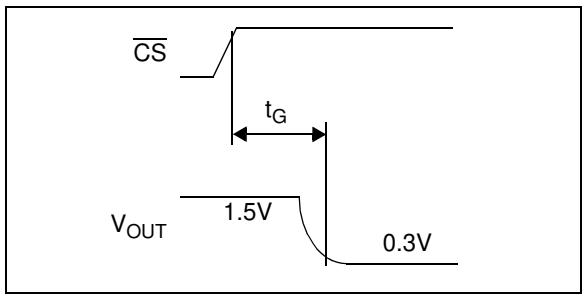


FIGURE 1-3: *Gain Select Timing Diagram.*

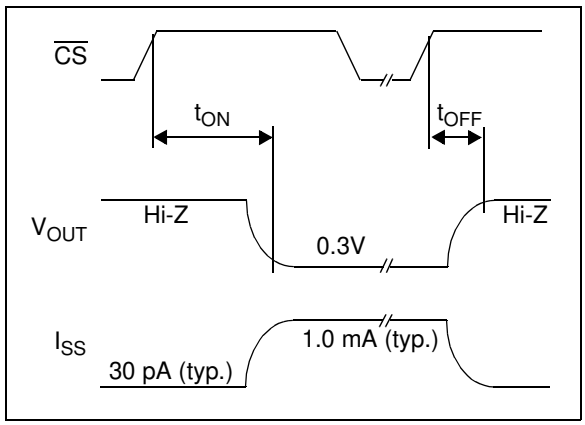


FIGURE 1-2: *PGA Shutdown Timing Diagram (must enter correct commands before CS goes high).*

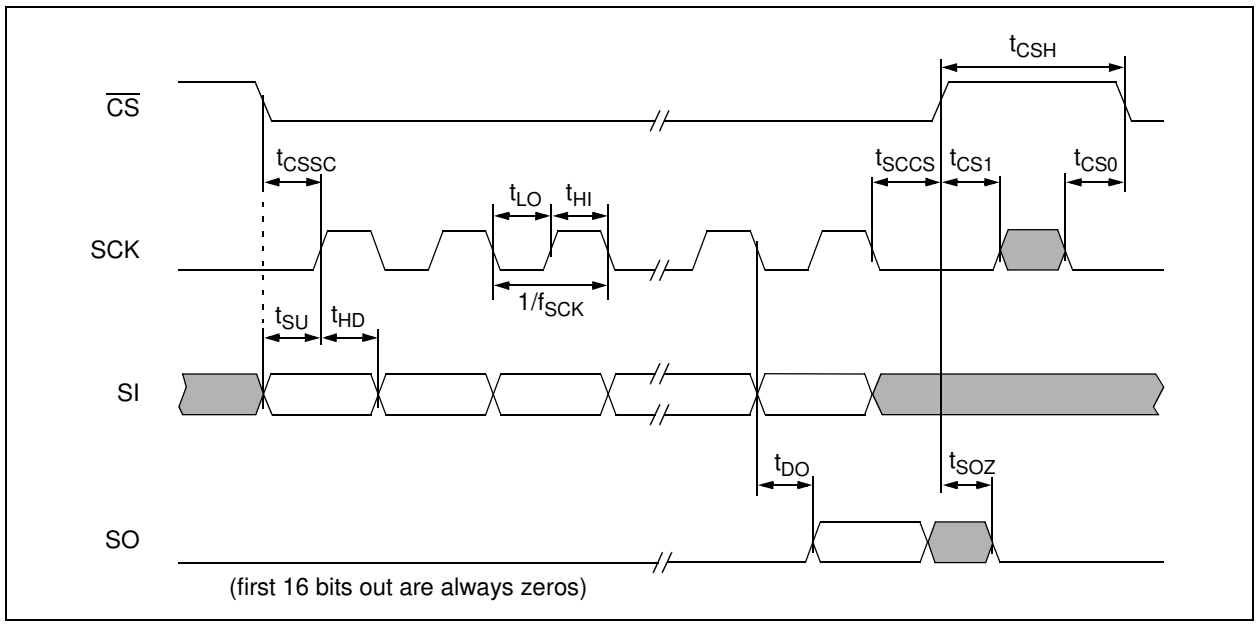


FIGURE 1-4: *Detailed SPI™ Serial Interface Timing; SPI 0,0 Mode.*

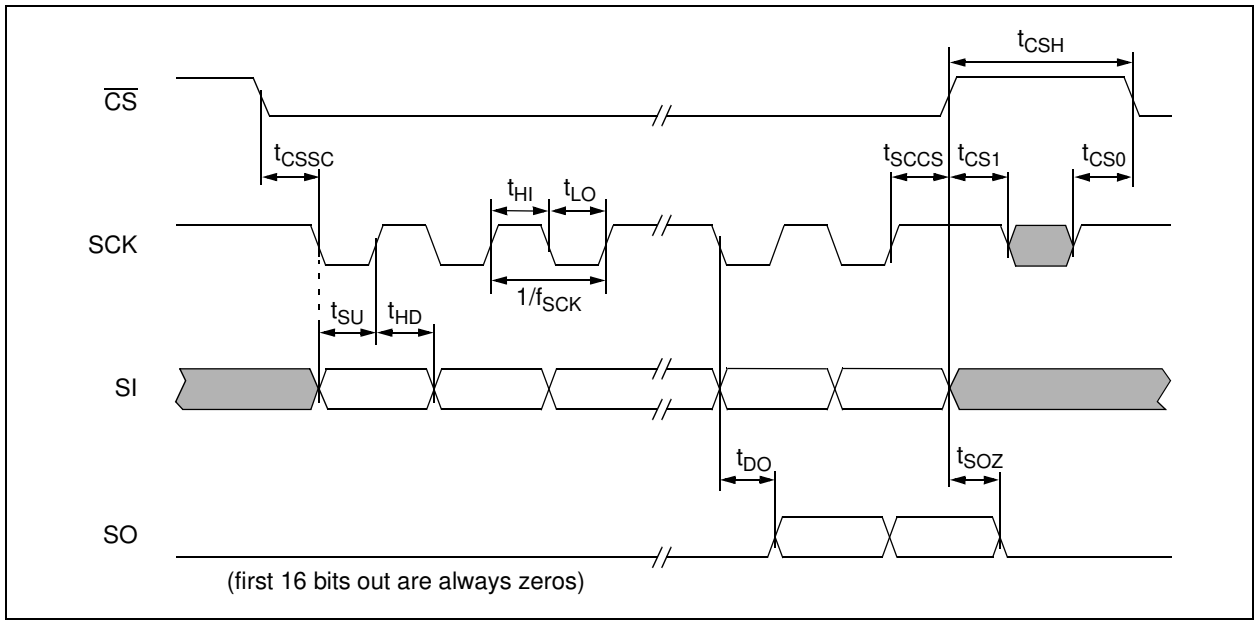


FIGURE 1-5: *Detailed SPI™ Serial Interface Timing; SPI 1,1 Mode.*

1.1 DC Output Voltage Specs / Model

1.1.1 IDEAL MODEL

The ideal PGA output voltage (V_{OUT}) is:

EQUATION 1-1:

$$V_{O\_ID} = G_{VIN} \qquad V_{REF} = V_{SS} = 0V$$

Where:

G is the nominal gain

(see Figure 1-6). This equation holds when there are no gain or offset errors and when the V_{REF} pin is tied to a low-impedance source (<< 0.1Ω) at ground potential (V_{SS} = 0V).

1.1.2 LINEAR MODEL

The PGA's linear region of operation, including offset and gain errors, is modeled by the line V_{O_LIN} shown in Figure 1-6.

EQUATION 1-2:

$$V_{O\_LIN} = G(1 + g_E)\left(V_{IN} - \frac{0.3V}{G} + V_{OS}\right) + 0.3V$$
$$V_{REF} = V_{SS} = 0V$$

The end points of this line are at V_{O_ID} = 0.3V and V_{DD} – 0.3V. Figure 1-6 shows the relationship between the gain and offset specifications referred to in the electrical specifications as follows:

EQUATION 1-3:

$$g_E = 100\% \frac{V_2 - V_1}{G(V_{DD} - 0.6V)}$$

$$V_{OS} = \frac{V_1}{G(1 + g_E)} \qquad G = +1$$

The DC Gain Drift ($\Delta G/\Delta T_A$) can be calculated from the change in g_E across temperature. This is shown in the following equation:

EQUATION 1-4:

$$\Delta G/\Delta T_A = \frac{\Delta g_E}{\Delta T_A}$$

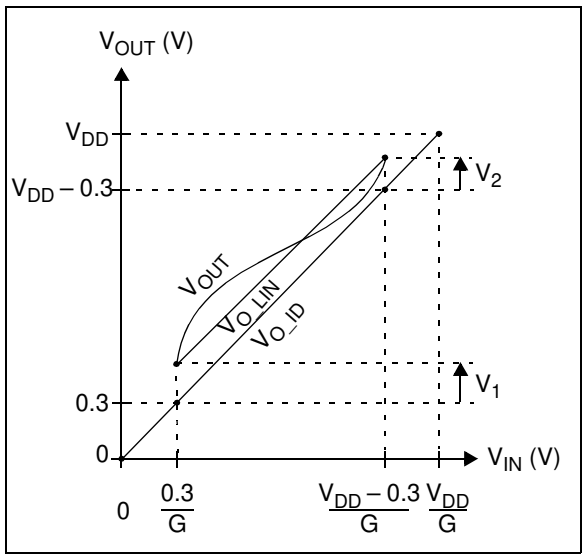


FIGURE 1-6: *Output Voltage Model with the standard condition $V_{REF} = V_{SS} = 0V$.*

1.1.3 OUTPUT NON-LINEARITY

Figure 1-7 shows the Integral Non-Linearity (INL) of the output voltage.

EQUATION 1-5:

$$INL = V_{OUT} - V_{O\_LIN}$$

The output non-linearity specification in the Electrical Specifications (with units of: % of FSR) is related to Figure 1-7 by:

EQUATION 1-6:

$$V_{ONL} = \frac{max(V_3, V_4)}{V_{DD} - 0.6V} \cdot 100\%$$

The Full-Scale Range (FSR) is V_{DD} – 0.6V (0.3V to V_{DD} – 0.3V).

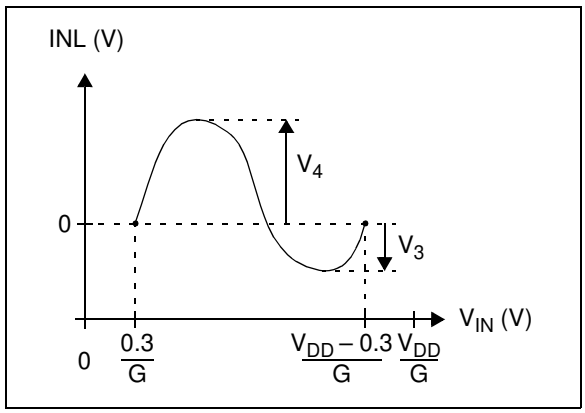


FIGURE 1-7: *Output Voltage INL with the standard condition $V_{REF} = V_{SS} = 0$ V.*

1.1.4 DIFFERENT V_{REF} CONDITIONS

Some of the plots in **Section 2.0 "Typical Performance Curves"**, have the conditions $V_{REF} = V_{DD}/2$ or $V_{REF} = V_{DD}$. The equations and figures above are easily modified for these conditions. The ideal V_{OUT} equation becomes:

EQUATION 1-7:

$$V_{O\_ID} = V_{REF} + G(V_{IN} - V_{REF})$$
$$V_{DD} \geq V_{REF} > V_{SS} = 0V$$

The complete linear model is:

EQUATION 1-8:

$$V_{ON\_LIN} = G(1 + g_E)(V_{IN} - V_{IN\_L} + V_{OS}) + 0.3V$$
$$V_{REF} = V_{SS} = 0V$$

where the new V_{IN} end points are:

EQUATION 1-9:

$$V_{IN\_L} = \frac{0.3V - V_{REF}}{G} + V_{REF}$$
$$V_{IN\_H} = \frac{V_{DD} - 0.3V - V_{REF}}{G} + V_{REF}$$

The equations for extracting the specifications do not change.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

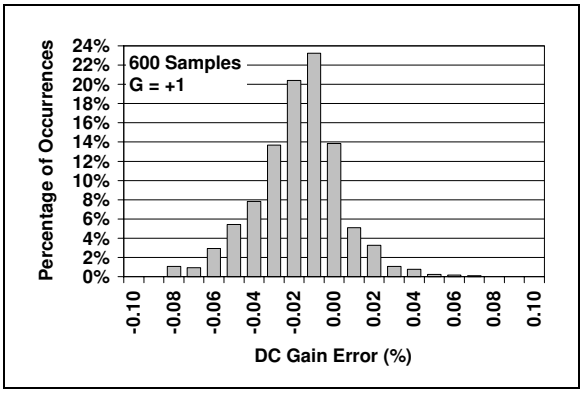


FIGURE 2-1: *DC Gain Error, G = +1.*

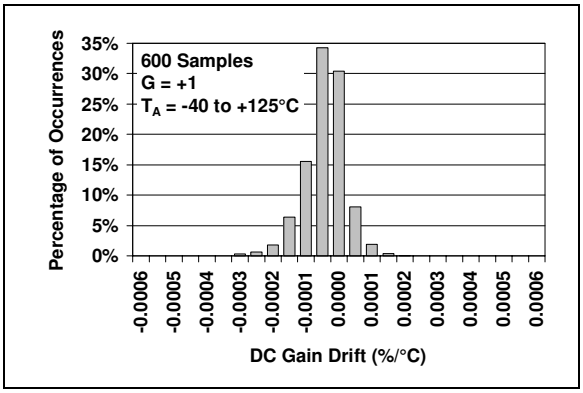


FIGURE 2-4: *DC Gain Drift, G = +1.*

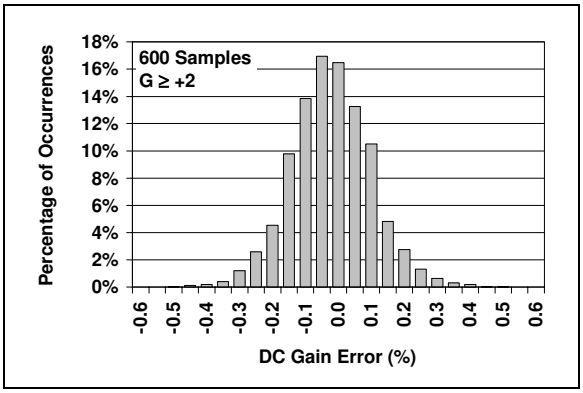


FIGURE 2-2: *DC Gain Error, G ≥ +2.*

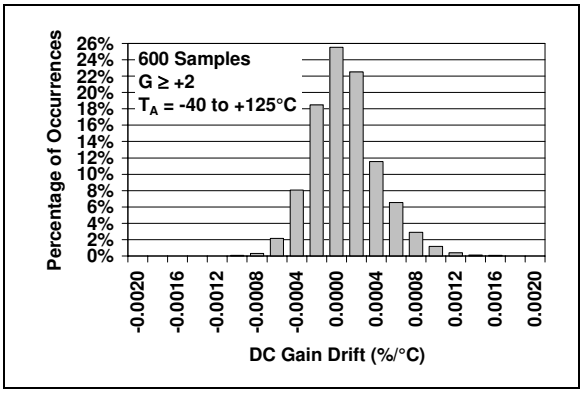


FIGURE 2-5: *DC Gain Drift, G ≥ +2.*

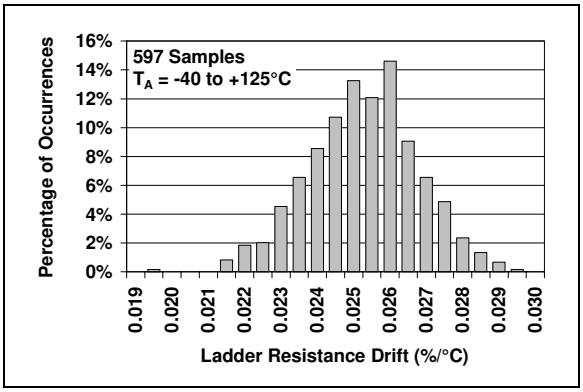


FIGURE 2-3: *Ladder Resistance Drift.*

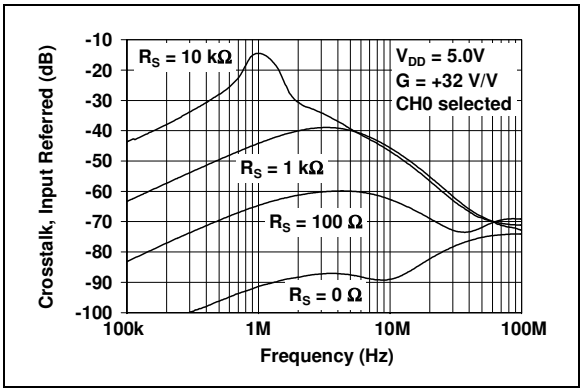


FIGURE 2-6: *Crosstalk vs. Frequency (circuit in Figure 6-4).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

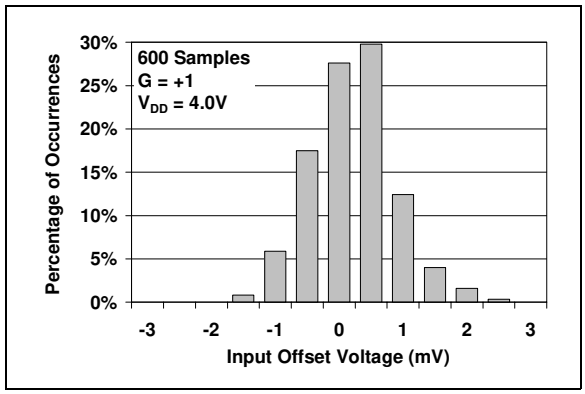


FIGURE 2-7: *Input Offset Voltage, V_{DD} = 4.0V.*

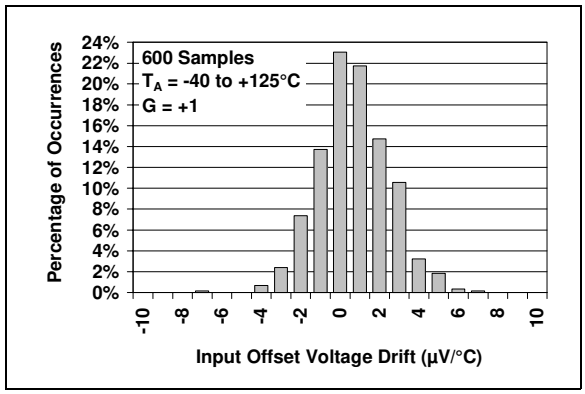


FIGURE 2-10: *Input Offset Voltage Drift.*

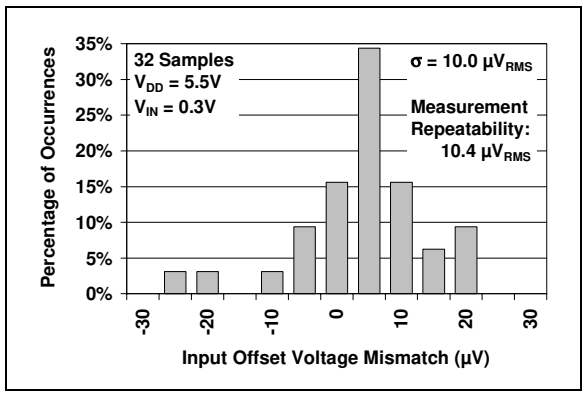


FIGURE 2-8: *Input Offset Voltage Mismatch.*

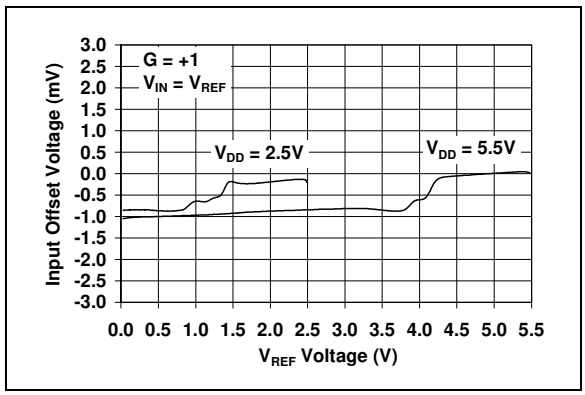


FIGURE 2-11: *Input Offset Voltage vs. V_{REF} Voltage.*

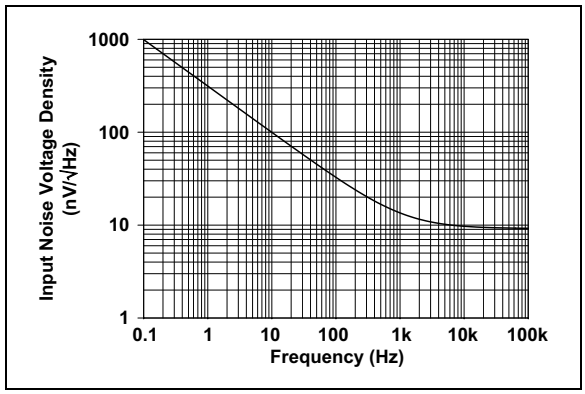


FIGURE 2-9: *Input Noise Voltage Density vs. Frequency.*

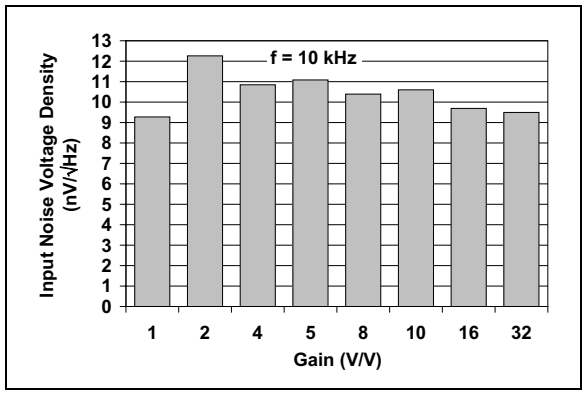


FIGURE 2-12: *Input Noise Voltage Density vs. Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

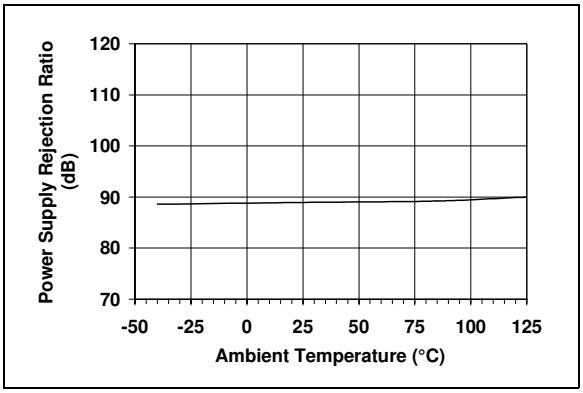


FIGURE 2-13: *PSRR vs. Ambient Temperature.*

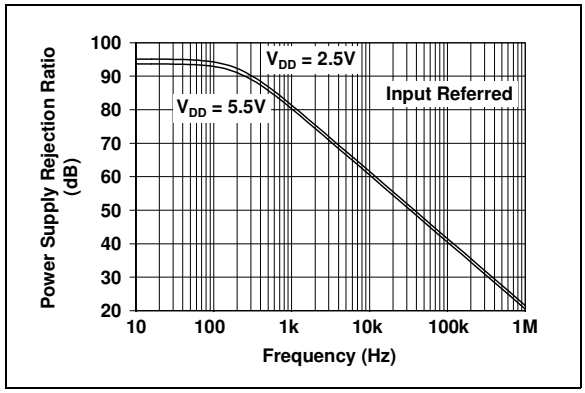


FIGURE 2-16: *PSRR vs. Frequency.*

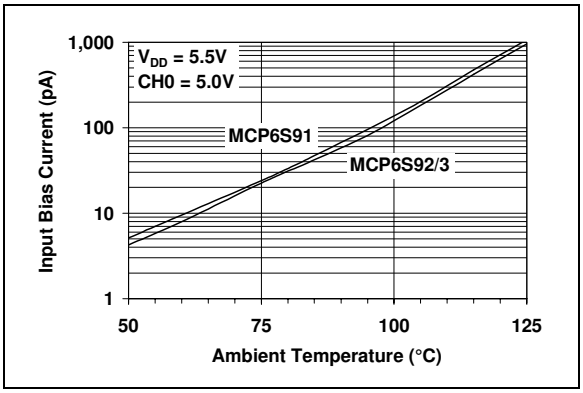


FIGURE 2-14: *Input Bias Current vs. Ambient Temperature.*

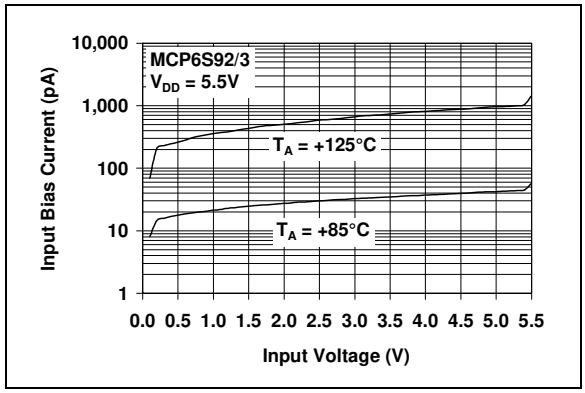


FIGURE 2-17: *Input Bias Current vs. Input Voltage.*

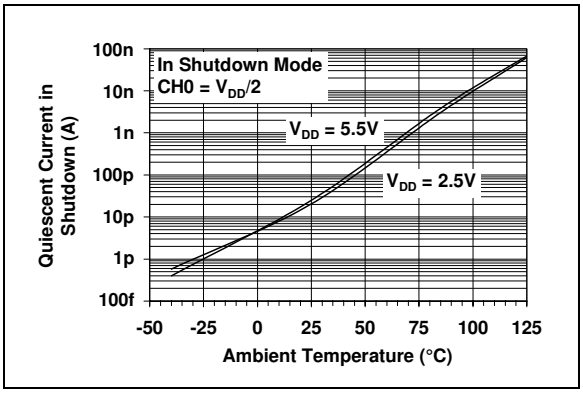


FIGURE 2-15: *Quiescent Current in Shutdown Mode vs. Ambient Temperature.*

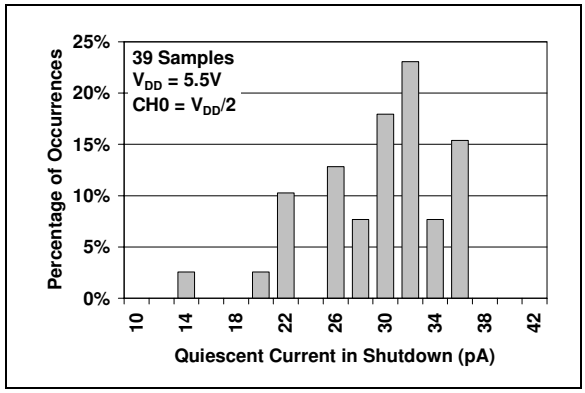


FIGURE 2-18: *Quiescent Current in Shutdown Mode.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

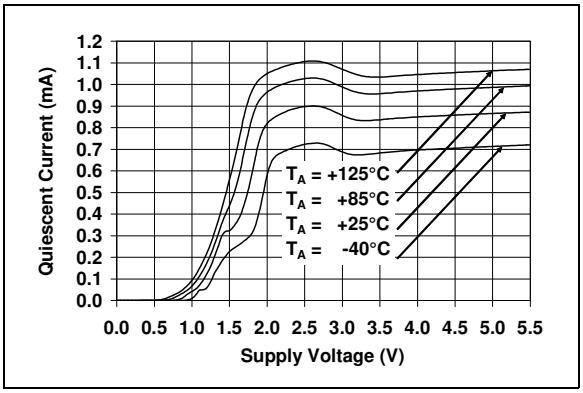


FIGURE 2-19: *Quiescent Current vs. Supply Voltage.*

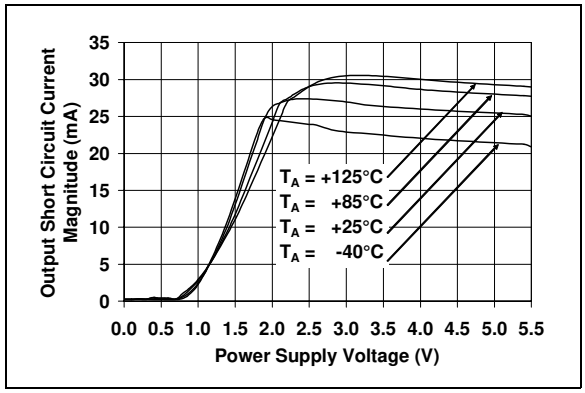


FIGURE 2-22: *Output Short Circuit Current vs. Supply Voltage.*

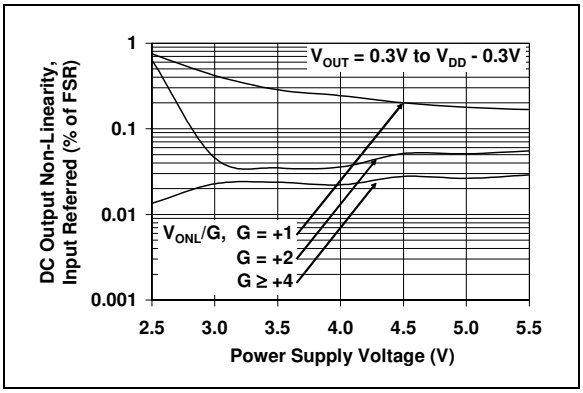


FIGURE 2-20: *DC Output Non-Linearity vs. Supply Voltage.*

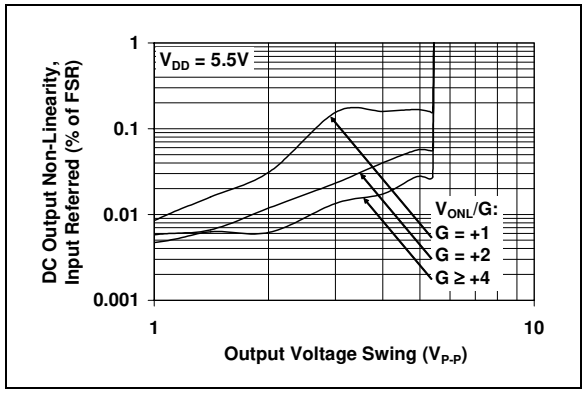


FIGURE 2-23: *DC Output Non-Linearity vs. Output Swing.*

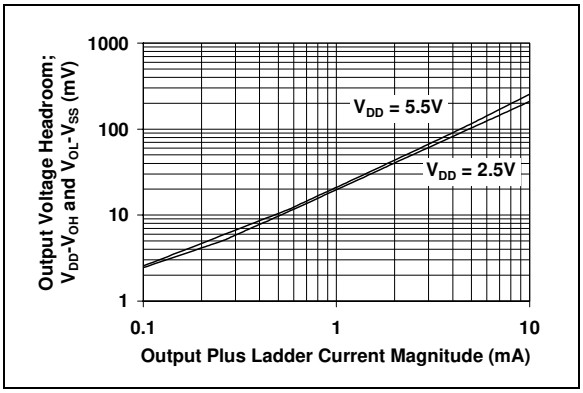


FIGURE 2-21: *Output Voltage Headroom vs. Output Plus Ladder Current (circuit in Figure 4-2).*

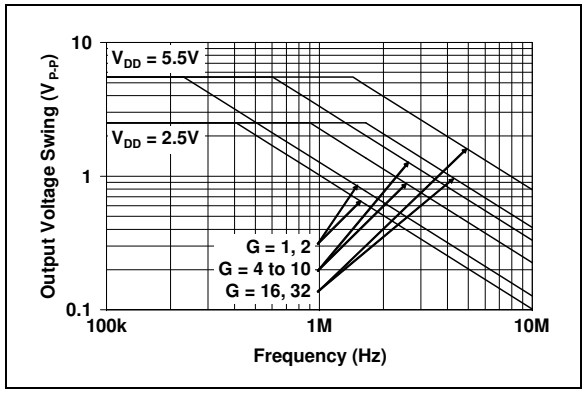


FIGURE 2-24: *Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

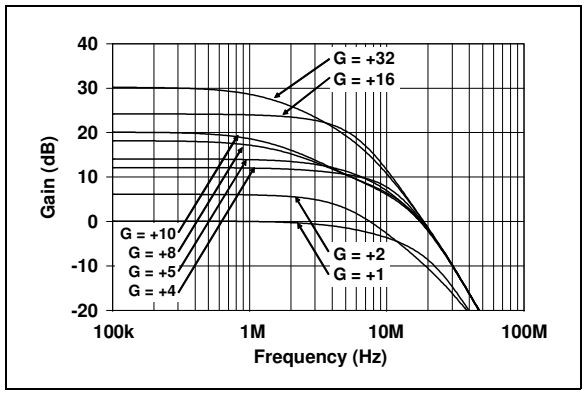


FIGURE 2-25: *Gain vs. Frequency.*

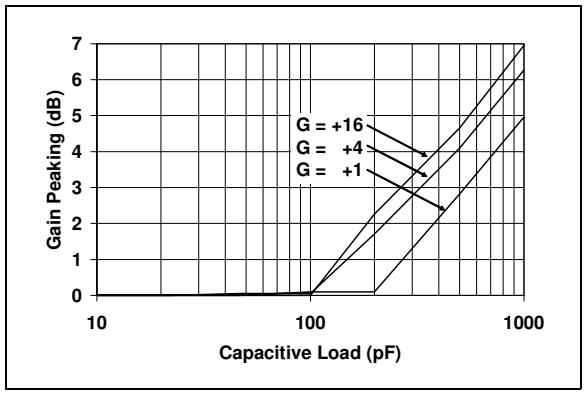


FIGURE 2-28: *Gain Peaking vs. Capacitive Load.*

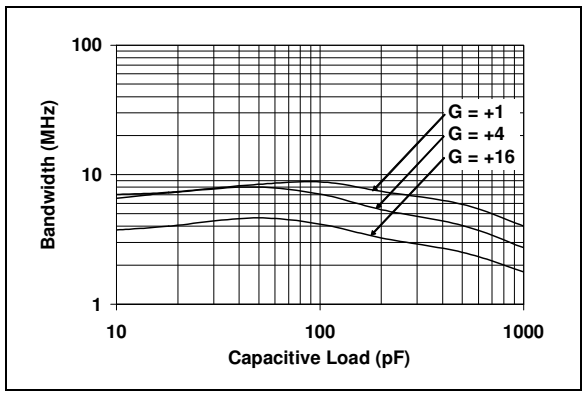


FIGURE 2-26: *Bandwidth vs. Capacitive Load.*

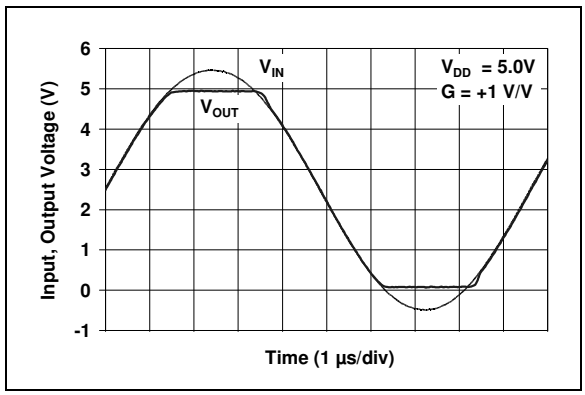


FIGURE 2-29: *The MCP6S91/2/3 family shows no phase reversal under overdrive.*

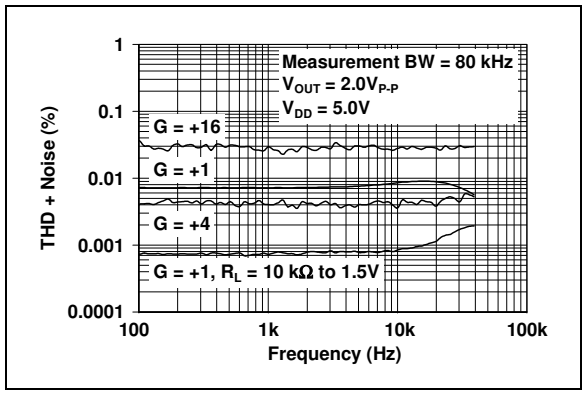


FIGURE 2-27: *THD plus Noise vs. Frequency, V_{OUT} = 2 V_{P-P}.*

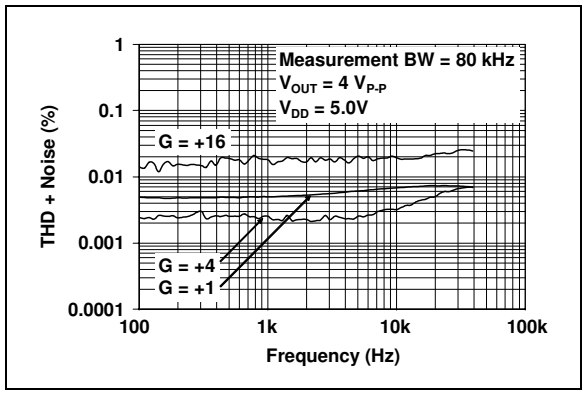


FIGURE 2-30: *THD plus Noise vs. Frequency, V_{OUT} = 4 V_{P-P}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

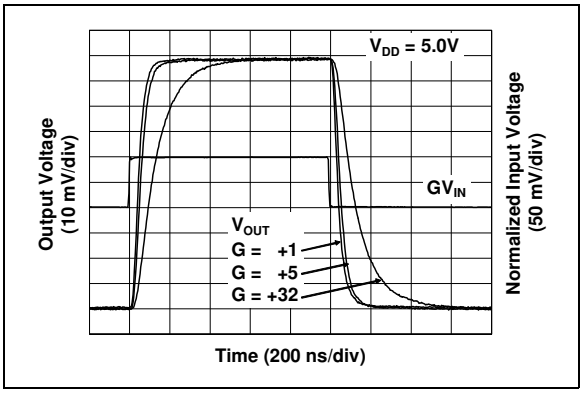


FIGURE 2-31: *Small-Signal Pulse Response.*

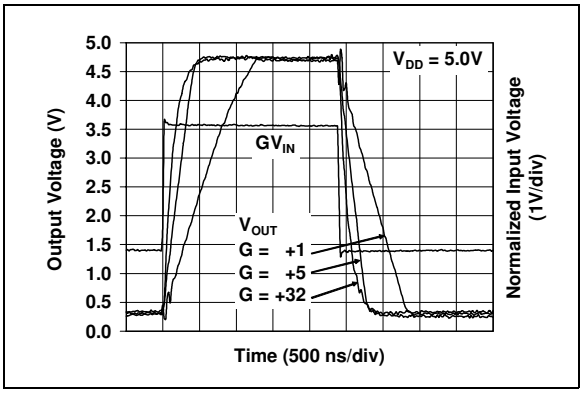


FIGURE 2-34: *Large-Signal Pulse Response.*

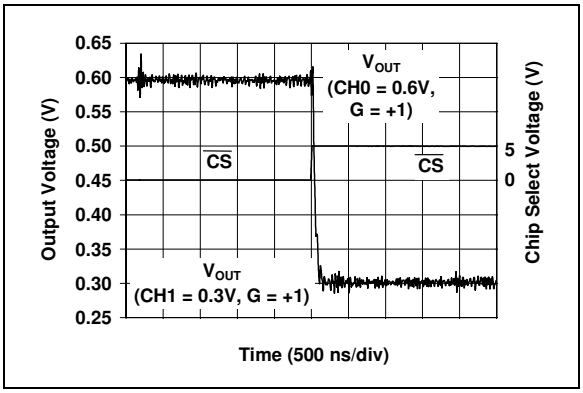


FIGURE 2-32: *Channel Select Timing.*

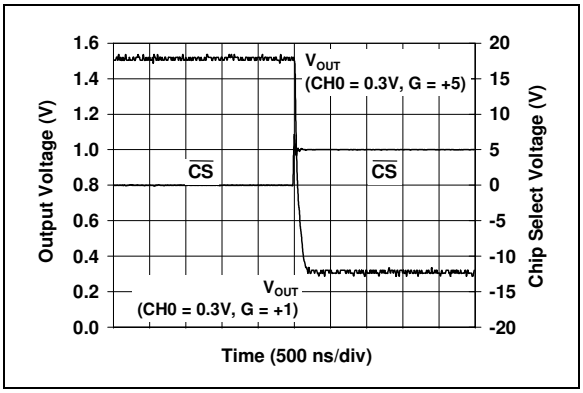


FIGURE 2-35: *Gain Select Timing.*

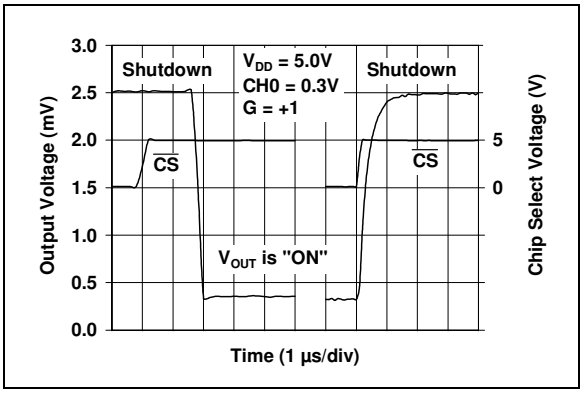


FIGURE 2-33: *Output Voltage vs. Shutdown Mode.*

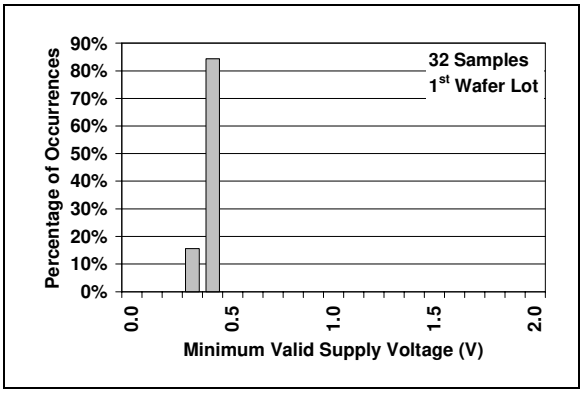


FIGURE 2-36: *Minimum Valid Supply Voltage (register data still valid).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

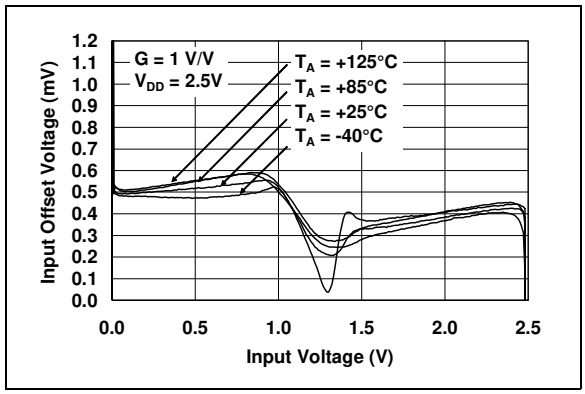


FIGURE 2-37: *Input Offset Voltage vs. Input Voltage, V_{DD} = 2.5V.*

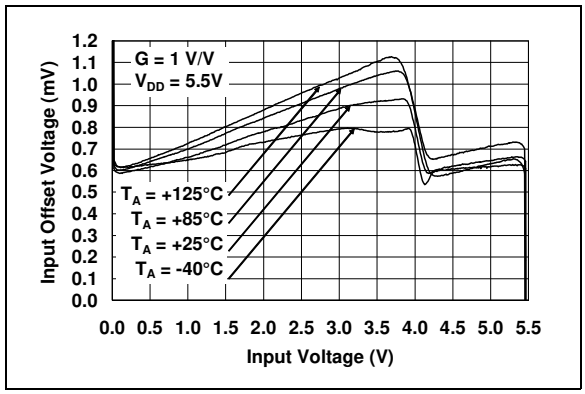


FIGURE 2-39: *Input Offset Voltage vs. Input Voltage, V_{DD} = 5.5V.*

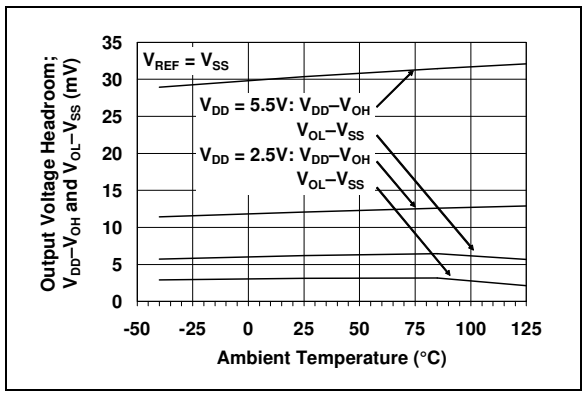


FIGURE 2-38: *Output Voltage Headroom vs. Ambient Temperature.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6S91	MCP6S92	MCP6S93	Symbol	Description
1	1	1	V_{OUT}	Analog Output
2	2	2	CH0	Analog Input
—	3	3	CH1	Analog Input
3	—	4	V_{REF}	External Reference Pin
4	4	5	V_{SS}	Negative Power Supply
5	5	6	$\overline{CS}$	SPI™ Chip Select
6	6	7	SI	SPI Serial Data Input
—	—	8	SO	SPI Serial Data Output
7	7	9	SCK	SPI Clock Input
8	8	10	V_{DD}	Positive Power Supply

3.1 Analog Output

The output pin (V_{OUT}) is a low-impedance voltage source. The selected gain (G), selected input (CH0, CH1) and voltage at V_{REF} determine its value.

3.2 Analog Inputs (CH0, CH1)

The inputs CH0 and CH1 connect to the signal sources. They are high-impedance CMOS inputs with low bias currents. The internal MUX selects which one is amplified to the output.

3.3 External Reference Voltage (V_{REF})

The V_{REF} pin, which is an analog input, should be at a voltage between V_{SS} and V_{DD} (the MCP6S92 has V_{REF} tied internally to V_{SS}). The voltage at this pin shifts the output voltage.

3.4 Power Supply (V_{SS} and V_{DD})

The Positive Power Supply Pin (V_{DD}) is 2.5V to 5.5V higher than the Negative Power Supply Pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These parts can share a bulk capacitor with analog parts (typically 2.2 µF to 10 µF) within 100 mm of the V_{DD} pin.

3.5 Digital Inputs

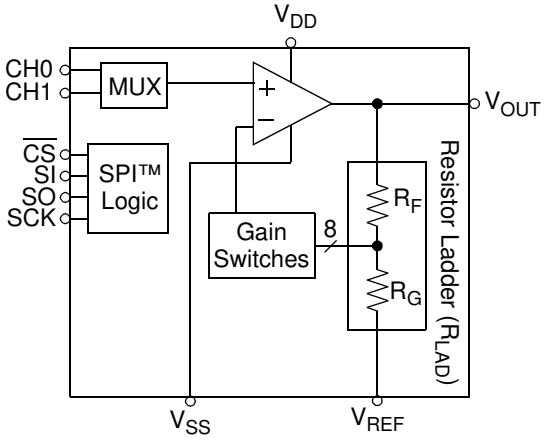
The SPI interface inputs are: Chip Select ($\overline{CS}$), Serial Input (SI) and Serial Clock (SCK). These are Schmitt-triggered, CMOS logic inputs.

3.6 Digital Output

The MCP6S93 device has a SPI interface Serial Output (SO) pin. This is a CMOS push-pull output and does not ever go High-Z. Once the device is deselected ($\overline{CS}$ goes high), SO is forced low. This feature supports daisy-chaining, as explained in **Section 5.3 "Daisy-Chain Configuration"**.

4.0 ANALOG FUNCTIONS

The MCP6S91/2/3 family of Programmable Gain Amplifiers (PGA) is based on simple analog building blocks (see Figure 4-1). Each of these blocks will be explained in more detail in the following subsections.



MCP6S91 – One input (CH0), no SO pin

MCP6S92 – Two inputs (CH0, CH1), V_{REF} tied internally to V_{SS}, no SO pin

MCP6S93 – Two inputs (CH0, CH1)

FIGURE 4-1: *PGA Block Diagram.*

4.1 Input MUX

The MCP6S91 has one input, while the MCP6S92 and MCP6S93 have two inputs (see Figure 4-1).

For the lowest input current, float unused inputs. Tying these pins to a voltage near the active channel's bias voltage also works well. For simplicity, they can be tied to V_{SS} or V_{DD}, but the input current may increase.

The one-channel MCP6S91 has approximately the same input bias current as the two-channel MCP6S92 and MCP6S93.

The input offset voltage mismatch between channels (ΔV_{OS}) is, ideally, 0 µV. The input MUX uses CMOS transmission gates that have drain-source (channel) resistance, but no offset voltage. The histogram in Figure 2-8 reflects the measurement repeatability (i.e., noise power bandwidth) rather than the actual mismatch. Reducing the measurement bandwidth will produce a more narrow histogram and give an average closer to 0 µV.

4.2 Internal Op Amp

The internal op amp gives the right combination of bandwidth, accuracy and flexibility.

4.2.1 COMPENSATION CAPACITORS

The internal op amp has three compensation capacitors (comp. caps.) connected to a switching network. They are selected to give good small-signal bandwidth at high gains and good slew rates (full-power bandwidth) at low gains. The change in bandwidth as gain changes is between 2 and 12 MHz. Refer to Table 4-1 for more information.

TABLE 4-1: GAIN VS. INTERNAL COMPENSATION CAPACITOR

Gain (V/V)	Internal Comp. Cap.	GBWP (MHz) Typ.	SR (V/µs) Typ.	FPBW (MHz) Typ.	BW (MHz) Typ.
1	Large	12	4.0	0.30	12
2	Large	12	4.0	0.30	6
4	Medium	20	11	0.70	10
5	Medium	20	11	0.70	7
8	Medium	20	11	0.70	2.4
10	Medium	20	11	0.70	2.0
16	Small	64	22	1.6	5
32	Small	64	22	1.6	2.0

Note 1: FPBW is the Full-Power Bandwidth. These numbers are based on V_{DD} = 5.0V.

2: No changes in DC performance (e.g., V_{OS}) accompany a change in compensation capacitor.

3: BW is the closed-loop, small signal -3 dB bandwidth.

4.2.2 RAIL-TO-RAIL CHANNEL INPUTS

The input stage of the internal op amp uses two differential input stages in parallel; one operates at low V_{IN} (input voltage), while the other operates at high V_{IN}. With this topology, the internal inputs can operate to 0.3V past either supply rail. The input offset voltage is measured at both $V_{IN} = V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ to ensure proper operation.

The transition between the two input stages occurs when $V_{IN} \approx V_{DD} - 1.5V$. For the best distortion and gain linearity, avoid this region of operation.

4.2.3 RAIL-TO-RAIL OUTPUT

The maximum output voltage swing is the maximum swing possible under a particular amplifier load current. The amplifier load current is the sum of the external load current (I_{OUT}) and the current through the ladder resistance (I_{LAD}); see Figure 4-2.

EQUATION 4-1:

$$Amplifier\ Load\ Current = I_{OUT} + I_{LAD}$$

Where:

$$I_{LAD} = \frac{(V_{OUT} - V_{REF})}{R_{LAD}}$$

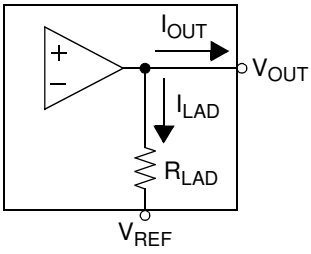


FIGURE 4-2: *Amplifier Load Current.*

See Figure 2-21 for the typical output headroom ($V_{DD} - V_{OH}$ or $V_{OL} - V_{SS}$) as a function of amplifier load current.

The specification table states the output can reach within 60 mV of either supply rail when R_L = 10 kΩ and $V_{REF} = V_{DD}/2$.

4.2.4 INPUT VOLTAGE AND PHASE REVERSAL

The MCP6S91/2/3 amplifier family is designed with CMOS input devices. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-29 shows an input voltage exceeding both supplies with no resulting phase inversion.

The maximum voltage that can be applied to the input pins (CHx) is $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$. Voltages on the inputs that exceed this absolute maximum rating can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor, as shown in Figure 4-3.

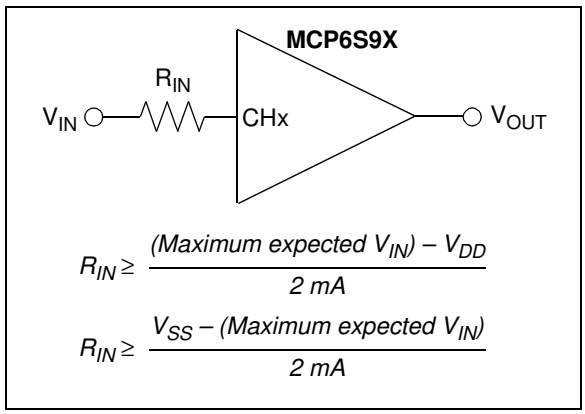


FIGURE 4-3: *R_{IN} limits the current flow into an input pin.*

4.3 Resistor Ladder

The resistor ladder shown in Figure 4-1 ($R_{LAD} = R_F + R_G$) sets the gain. Placing the gain switches in series with the inverting input reduces the parasitic capacitance, distortion and gain mismatch.

R_{LAD} is an additional load on the output of the PGA and causes additional current draw from the supplies. It is also a load (Z_{IN_REF}) on the external circuitry driving the V_{REF} pin.

In Shutdown mode, R_{LAD} is still attached to the V_{OUT} and V_{REF} pins. Thus, these pins and the internal amplifier's inverting input are all connected through R_{LAD} and the output is not High-Z (unlike the internal op amp).

While R_{LAD} contributes to the output noise, its effect is small. Refer to Figure 2-12.

4.4 Rail-to-Rail V_{REF} Input

The V_{REF} input is intended to be driven by a low-impedance voltage source. The source driving the V_{REF} pin should have an output impedance less than 0.1Ω to maintain reasonable gain accuracy. The supply voltage V_{SS} and V_{DD} usually meet this requirement.

R_{LAD} presents a load at the V_{REF} pin to the external circuit ($Z_{IN\_REF} \approx (5\ k\Omega/G)||(6\ pF)$), which depends on the gain. Any source driving the V_{REF} pin must be capable of driving a load as heavy as 0.16 kΩ||6 pF (G = 32).

The absolute maximum voltages that can be applied to the reference input pin (V_{REF}) are V_{SS} – 0.3V and V_{DD} + 0.3V. Voltages on the inputs that exceed this absolute maximum rating can cause excessive current to flow into or out of this pin. Current beyond ±2 mA can cause possible reliability problems. Because an external series resistor cannot be used (for low gain error), the external circuit *must* ensure that V_{REF} is between V_{SS} – 0.3V and V_{DD} + 0.3V.

The V_{IVR_REF} spec shows the region of normal operation for the V_{REF} pin (V_{SS} to V_{DD}). Staying within this region ensures proper operation of the PGA and its surrounding circuitry.

4.5 Shutdown Mode

These PGAs use a software shutdown command. When the SPI interface sends a shutdown command, the internal op amp is shut down and its output placed in a High-Z state.

The resistive ladder is always connected between V_{REF} and V_{OUT}; even in shutdown. This means that the output resistance will be on the order of 5 kΩ, with a path for output signals to appear at the input.

5.0 DIGITAL FUNCTIONS

The MCP6S91/2/3 PGAs use a standard SPI compatible serial interface to receive instructions from a controller. This interface is configured to allow daisy-chaining with other SPI devices.

5.1 SPI Timing

Chip Select ($\overline{CS}$) toggles low to initiate communication with these devices. The first byte of each SI word (two bytes long) is the instruction byte, which goes into the Instruction register. The Instruction register points the second byte to its destination. In a typical application, $\overline{CS}$ is raised after one word (16 bits) to implement the desired changes. **Section 5.3 "Daisy-Chain Configuration"**, covers applications using multiple 16-bit words. SO goes low after $\overline{CS}$ goes high; it has a push-pull output that does not go into a high-Z state.

The MCP6S91/2/3 devices operate in SPI modes 0,0 and 1,1. In 0,0 mode, the clock idles in the low state (Figure 5-1). In 1,1 mode, the clock idles in the high state (Figure 5-2). In both modes, SI data is loaded into the PGA on the rising edge of SCK, while SO data is clocked out on the falling edge of SCK. In 0,0 mode, the falling edge of $\overline{CS}$ also acts as the first falling edge of SCK (see Figure 5-1). There must be multiples of 16 clocks (SCK) while $\overline{CS}$ is low or commands will abort (see **Section 5.3 "Daisy-Chain Configuration"**).

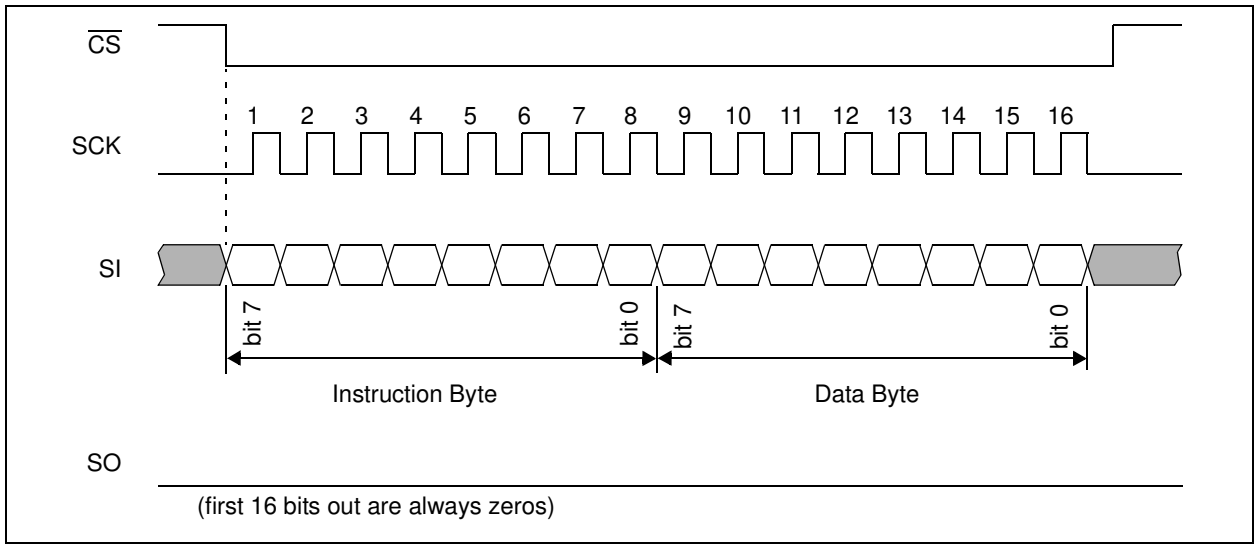


FIGURE 5-1: *Serial Bus Sequence for the PGA; SPI™ 0,0 Mode (see Figure 1-4).*

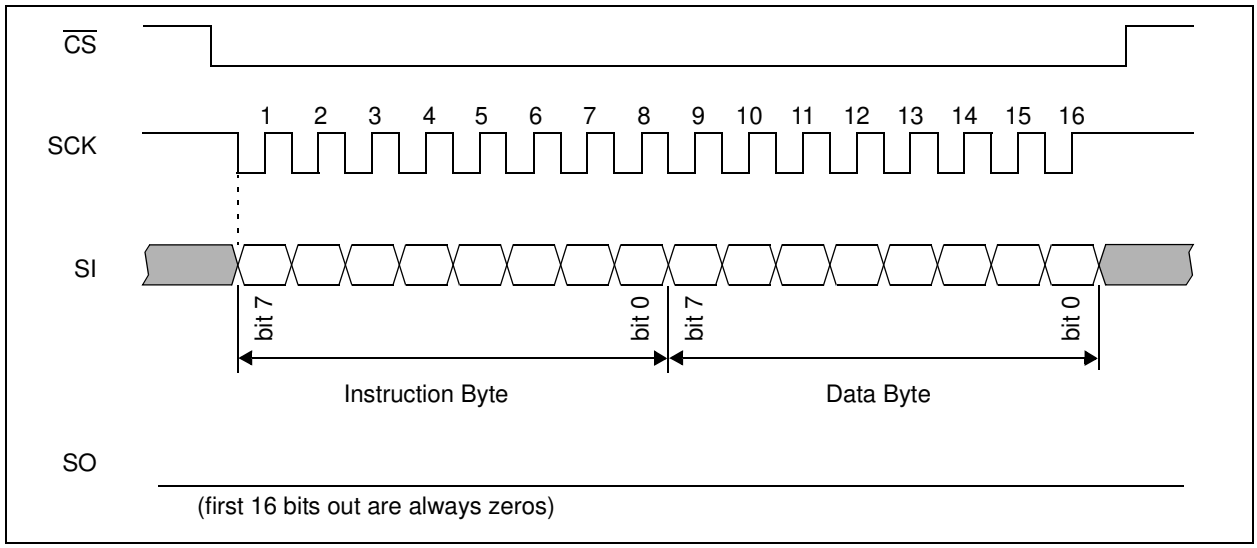


FIGURE 5-2: *Serial Bus Sequence for the PGA; SPI™ 1,1 Mode (see Figure 1-5).*

5.2 Registers

The analog functions are programmed through the SPI interface using 16-bit words (see Figure 5-1 and Figure 5-2). This data is sent to two of three 8-bit registers: Instruction register (Register 5-1), Gain register (Register 5-2) and Channel register (Register 5-3). There are no power-up defaults for these three registers.

5.2.1 ENSURING VALID DATA IN THE REGISTERS

After power up, the registers contain random data that must be initialized. Sending valid gain and channel selection commands to the internal registers puts valid data into those registers. Also, the internal state machine starts in an arbitrary state. Toggling the Chip Select pin ($\overline{CS}$) from high to low, then back to high again, puts the internal state machine in a known, valid condition (this can be done by entering any valid command).

After power-up, and when the power supply voltage dips below the minimum valid V_{DD} (V_{DD_VAL}), the internal register data and state machine may need to be reset. This is accomplished as described before. Use an external system supervisor to detect these events so that the microcontroller will reset the PGA state and registers.

A 0.1 µF bypass capacitor mounted as close as possible to the V_{DD} pin provides additional transient immunity.

5.2.2 INSTRUCTION REGISTER

The Instruction register has 3 command bits and 1 indirect address bit; see Register 5-1. The command bits include a `NOP` (`000`) to support daisy-chaining (see **Section 5.3 "Daisy-Chain Configuration"**); the other `NOP` commands shown should not be used (they are reserved for future use). The device is brought out of Shutdown mode when a valid command, other than `NOP` or Shutdown, is sent and $\overline{CS}$ is raised.

REGISTER 5-1: INSTRUCTION REGISTER

W-0	W-0	W-0	U-x	U-x	U-x	U-x	W-0
M2	M1	M0	—	—	—	—	A0
bit 7							bit 0

bit 7-5 **M2-M0:** Command bits
- `000` = `NOP` **(Note 1)**
- `001` = PGA enters Shutdown mode as soon as a full 16-bit word is sent and $\overline{CS}$ is raised. **(Notes 1 and 2)**
- `010` = Write to register.
- `011` = `NOP` (reserved for future use) **(Note 1)**
- `1XX` = `NOP` (reserved for future use) **(Note 1)**

bit 4-1 **Unimplemented:** Read as '0' (reserved for future use)

bit 0 **A0:** Indirect Address bit
- `1` = Addresses the Channel register
- `0` = Addresses the Gain register

Note 1: All other bits in the 16-bit word (including A0) are "don't cares."

2: The device exits Shutdown mode when a valid command (other than `NOP` or Shutdown) is sent and $\overline{CS}$ is raised; that valid command will be executed. Shutdown does not toggle.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5.2.3 SETTING THE GAIN

The amplifier can be programmed to produce binary and decimal gain settings between +1 V/V and +32 V/V. Register 5-2 shows the details. At the same time, different compensation capacitors are selected to optimize the bandwidth vs. slew rate trade-off (see Table 4-1).

REGISTER 5-2: GAIN REGISTER

U-x	U-x	U-x	U-x	U-x	W-0	W-0	W-0
—	—	—	—	—	G2	G1	G0
bit 7							bit 0

bit 7-3 **Unimplemented:** Read as ‘0’ (reserved for future use)

bit 2-0 **G2-G0:** Gain Select bits

000 = Gain of +1
001 = Gain of +2
010 = Gain of +4
011 = Gain of +5
100 = Gain of +8
101 = Gain of +10
110 = Gain of +16
111 = Gain of +32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

5.2.4 CHANGING THE CHANNEL

If the Instruction register is programmed to address the Channel register, the multiplexed inputs of the MCP6S92 and MCP6S93 can be changed using Register 5-3.

REGISTER 5-3: CHANNEL REGISTER

U-x	U-x	U-x	U-x	U-x	U-x	U-x	W-0
—	—	—	—	—	—	—	C0
bit 7							bit 0

bit 7-1 **Unimplemented:** Read as '0' (reserved for future use)

bit 0 **C0:** Channel Select bit

	MCP6S91	MCP6S92	MCP6S93
0 =	CH0	CH0	CH0
1 =	CH0	CH1	CH1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5.2.5 SHUTDOWN COMMAND

The software shutdown command allows the user to put the amplifier into a low-power mode (see Register 5-1). In this Shutdown mode, most pins are high-impedance (**Section 4.5 "Shutdown Mode"** and **Section 5.1 "SPI Timing"** cover the exceptions at pins V_{REF}, V_{OUT} and SO).

Once the PGA has entered Shutdown mode, it will remain in this mode until either a valid command is sent to the device (other than NOP or Shutdown) or the device is powered down and back up again. The internal registers maintain their values while in shutdown.

Once brought out of Shutdown mode, the part returns to its previous state (see **Section 5.2.1 "Ensuring Valid Data in the Registers"** for exceptions to this rule). This makes it possible to bring the device out of shutdown mode using one command; send a command to select the current channel (or gain) and the device will exit shutdown with the same state that existed before shutdown.

5.3 Daisy-Chain Configuration

Multiple MCP6S91/2/3 devices can be connected in a daisy-chain configuration by connecting the SO pin from one device to the SI pin on the next device and using common SCK and $\overline{CS}$ lines (Figure 5-3). This approach reduces PCB layout complexity and uses fewer PICmicro® microcontroller I/O pins.

The example in Figure 5-3 shows a daisy-chain configuration with two devices, although any number of devices can be configured this way. The MCP6S91 and MCP6S92 can only be used at the far end of the daisy-chain, because they do not have a serial data out (SO) pin. As shown in Figure 5-4 and Figure 5-5, both SI and SO data are sent in 16-bit (2 byte) words. These devices abort any command that is not a multiple of 16 bits.

When using the daisy-chain configuration, the maximum clock speed possible is reduced to ≈ 5.8 MHz due to the SO pin's propagation delay (see Electrical Specifications).

The internal SPI shift register is automatically loaded with zeros whenever $\overline{CS}$ goes high (a command is executed). Thus, the first 16-bits out of the SO pin after the $\overline{CS}$ line goes low are always zeros. This means that the first command loaded into the next device in the daisy-chain is a NOP. This feature makes it possible to send shorter command and data byte strings when the farthest devices do not need to change. For example, if there were three devices on the chain, and only the middle device needed changing, then only 32 bytes of data need to be transmitted (for the first and middle devices). The last device on the chain would receive a NOP when the $\overline{CS}$ pin is raised to execute the command.

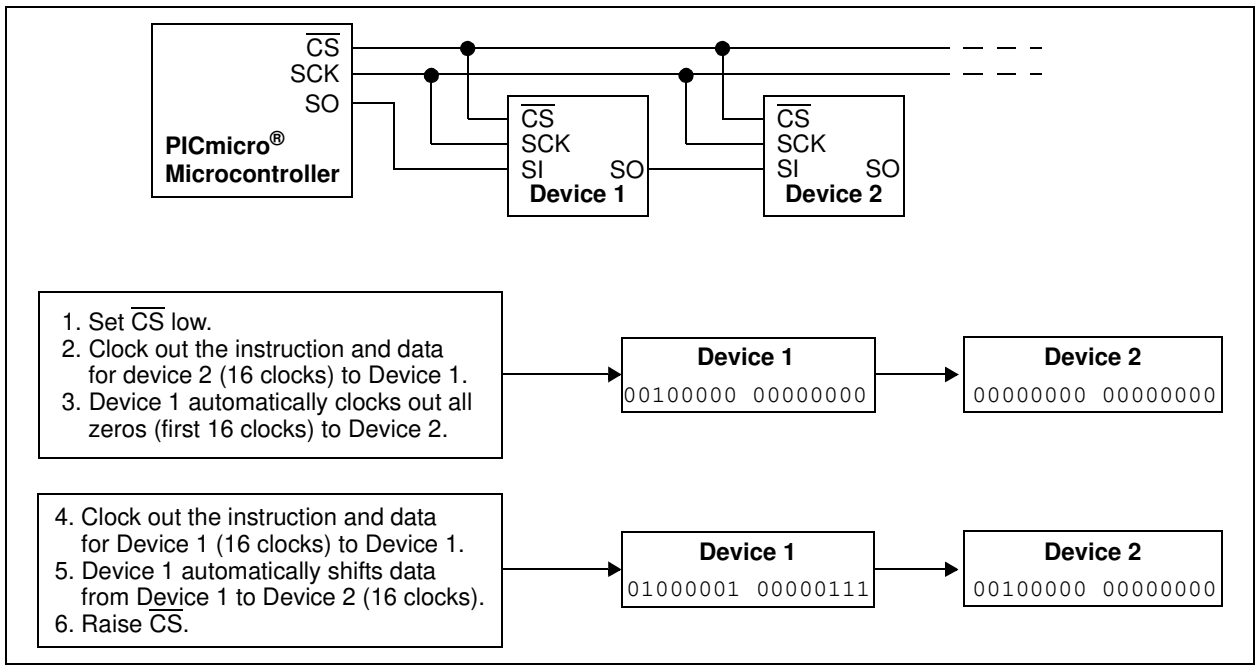


FIGURE 5-3: *Daisy-Chain Configuration.*