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MCP6V26/7/8

620 µA, 2 MHz Auto-Zeroed Op Amps

Features

- High DC Precision:
  - V_{OS} Drift: ±50 nV/°C (maximum)
  - V_{OS}: ±2 µV (maximum)
  - A_{OL}: 125 dB (minimum)
  - PSRR: 125 dB (minimum)
  - CMRR: 120 dB (minimum)
  - E_{ni}: 1.0 μV_{P-P} (typical), f = 0.1 Hz to 10 Hz
  - E_{ni}: 0.32 μV_{P-P} (typical), f = 0.01 Hz to 1 Hz
- Low Power and Supply Voltages:
  - I_Q: 620 µA/amplifier (typical)
  - Wide Supply Voltage Range: 2.3V to 5.5V
- Easy to Use:
  - Rail-to-Rail Input/Output
  - Gain Bandwidth Product: 2 MHz (typical)
  - Unity Gain Stable
  - Available in Single and Dual
  - Single with Chip Select ($\overline{CS}$): MCP6V28
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Portable Instrumentation
- Sensor Conditioning
- Temperature Measurement
- DC Offset Correction
- Medical Instrumentation

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Parts

Parts with lower power, lower bandwidth and higher noise:

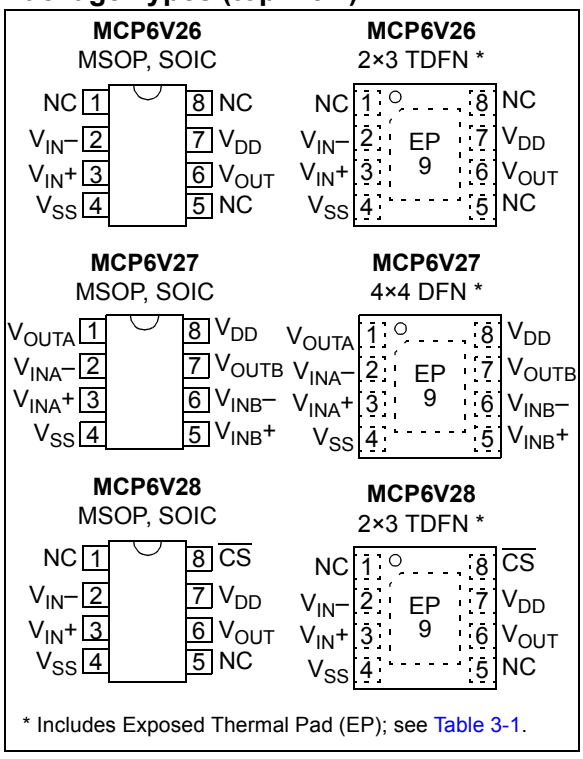
- MCP6V01/2/3: Spread clock
- MCP6V06/7/8: Non-spread clock

Description

The Microchip Technology Inc. MCP6V26/7/8 family of operational amplifiers provides input offset voltage correction for very low offset and offset drift. These devices have a wide gain bandwidth product (2 MHz, typical) and strongly reject switching noise. They are unity gain stable, have no 1/f noise, and have good power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). These products operate with a single supply voltage as low as 2.3V, while drawing 620 µA/amplifier (typical) of quiescent current.

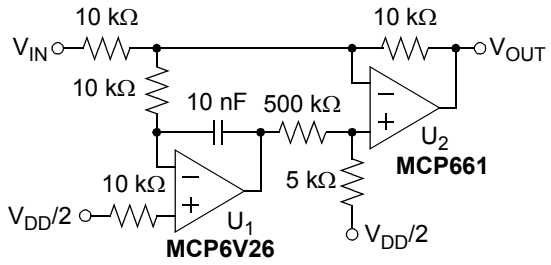
The Microchip Technology Inc. MCP6V26/7/8 op amps are offered as a single (MCP6V26), single with Chip Select ($\overline{CS}$) (MCP6V28) and dual (MCP6V27). They were designed using an advanced CMOS process.

Package Types (top view)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Application Circuit



Offset Voltage Correction for Power Driver

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins †† .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† ..... V_{SS} – 1.0V to V_{DD}+1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD}+0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, CDM, MM) ≥ 4 kV,1.5 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.1, Rail-to-Rail Inputs**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2	—	+2	µV	T_A = +25°C **(Note 1)**
Input Offset Voltage Drift with Temperature (linear Temp. Co.)	TC_1	-50	—	+50	nV/°C	T_A = -40 to +125°C **(Note 1)**
Input Offset Voltage Quadratic Temperature Coefficient	TC_2	—	±0.2	—	nV/°C^2	T_A = -40 to +125°C
Power Supply Rejection	PSRR	125	142	—	dB	**(Note 1)**
Input Bias Current and Impedance						
Input Bias Current	I_B	—	+7	—	pA	
Input Bias Current across Temperature	I_B	—	+110	—	pA	T_A = +85°C
	I_B	—	+1.2	+5	nA	T_A = +125°C
Input Offset Current	I_{OS}	—	±70	—	pA	
Input Offset Current across Temperature	I_{OS}	—	±50	—	pA	T_A = +85°C
	I_{OS}	—	±60	—	pA	T_A = +125°C
Common Mode Input Impedance	Z_{CM}	—	10^{13}||12	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||12	—	Ω||pF	

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC_1; see **Appendix B: "Offset Related Test Screens"**).

2: Figure 2-18 shows how V_{CML} and V_{CMH} changed across temperature for the first production lot.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Common Mode						
Common-Mode Input Voltage Range Low	V_{CML}	—	—	$V_{SS} - 0.15$	V	**(Note 2)**
Common-Mode Input Voltage Range High	V_{CMH}	$V_{DD} + 0.2$	—	—	V	**(Note 2)**
Common-Mode Rejection	CMRR	120	136	—	dB	V_{DD} = 2.3V, V_{CM} = -0.15V to 2.5V **(Note 1, Note 2)**
	CMRR	125	142	—	dB	V_{DD} = 5.5V, V_{CM} = -0.15V to 5.7V **(Note 1, Note 2)**
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	125	147	—	dB	V_{DD} = 2.3V, V_{OUT} = 0.2V to 2.1V **(Note 1)**
	A_{OL}	133	155	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V **(Note 1)**
Output						
Minimum Output Voltage Swing	V_{OL}	—	V_{SS} + 5	$V_{SS} + 15$	mV	G = +2, 0.5V input overdrive
Maximum Output Voltage Swing	V_{OH}	$V_{DD} - 15$	$V_{DD} - 5$	—	mV	G = +2, 0.5V input overdrive
Output Short Circuit Current	I_{SC}	—	±12	—	mA	V_{DD} = 2.3V
	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	2.3	—	5.5	V	
Quiescent Current per amplifier	I_Q	450	620	800	µA	I_O = 0
POR Trip Voltage	V_{POR}	1.15	—	1.65	V	

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC_1; see **Appendix B: "Offset Related Test Screens"**).

2: Figure 2-18 shows how V_{CML} and V_{CMH} changed across temperature for the first production lot.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Amplifier AC Response						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Slew Rate	SR	—	1.0	—	V/µs	
Phase Margin	PM	—	65	—	°	G = +1
Amplifier Noise Response						
Input Noise Voltage	E_{ni}	—	0.32	—	μV_{P-P}	f = 0.01 Hz to 1 Hz
	E_{ni}	—	1.0	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	50	—	nV/√Hz	f < 5 kHz
	e_{ni}	—	29	—	nV/√Hz	f = 100 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	
Amplifier Distortion (Note 1)						
Intermodulation Distortion (AC)	IMD	—	40	—	μV_{PK}	V_{CM} tone = 50 mV_{PK} at 1 kHz, G_N = 1
Amplifier Step Response						
Start Up Time	t_{STR}	—	75	—	µs	G = +1, V_{OS} within 50 µV of its final value **(Note 2)**
Offset Correction Settling Time	t_{STL}	—	150	—	µs	G = +1, V_{IN} step of 2V, V_{OS} within 50 µV of its final value
Output Overdrive Recovery Time	t_{ODR}	—	45	—	µs	G = -100, ±0.5V input overdrive to V_{DD}/2, V_{IN} 50% point to V_{OUT} 90% point **(Note 3)**

Note 1: These parameters were characterized using the circuit in Figure 1-7. In Figure 2-37 and Figure 2-38, there is an IMD tone at DC, a residual tone at 1 kHz, other IMD tones and clock tones.

2: High gains behave differently; see **Section 4.3.3, Offset at Power Up**.

3: t_{ODR} includes some uncertainty due to clock edge timing.

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/3$, V_{OUT} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kW to V_L, C_L = 60 pF, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Pull-Down Resistor (MCP6V28)						
$\overline{CS}$ Pull-Down Resistor	R_{PD}	3	5	—	MΩ	
$\overline{CS}$ Low Specifications (MCP6V28)						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.3V_{DD}$	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications (MCP6V28)						
$\overline{CS}$ Logic Threshold, High	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	V_{DD}/R_{PD}	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current per amplifier	I_{SS}	—	-0.4	—	µA	$\overline{CS}$ = V_{DD}, V_{DD} = 2.3V
	I_{SS}	—	-1	—	µA	$\overline{CS}$ = V_{DD}, V_{DD} = 5.5V
Amplifier Output Leakage, $\overline{CS}$ High	I_{O_LEAK}	—	20	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications (MCP6V28)						
$\overline{CS}$ Low to Amplifier Output On Turn-on Time	t_{ON}	—	4	50	µs	$\overline{CS}$ Low = V_{SS}+0.3 V, G = +1 V/V, V_{OUT} = 0.9 $V_{DD}/2$
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	1	—	µs	$\overline{CS}$ High = V_{DD} – 0.3 V, G = +1 V/V, V_{OUT} = 0.1 $V_{DD}/2$
Internal Hysteresis	V_{HYST}	—	0.2	—	V	

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +2.3V to +5.5V, V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-4x4 DFN	θ_{JA}	—	48	—	°C/W	**(Note 2)**
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	53	—	°C/W	**(Note 2)**

Note 1: Operation must not cause T_J to exceed Maximum Junction Temperature specification (+150°C).

2: Measured on a standard JC51-7, four layer printed circuit board with ground plane and vias.

1.3 Timing Diagrams

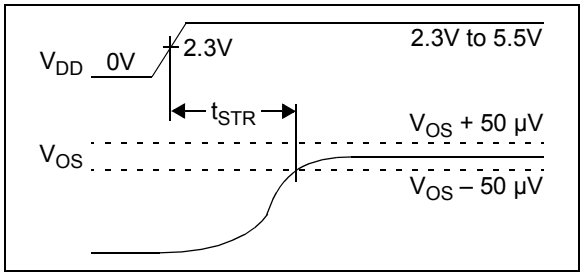


FIGURE 1-1: *Amplifier Start Up.*

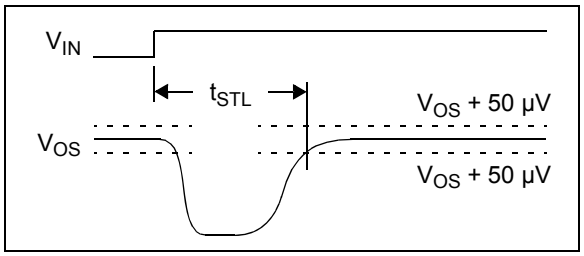


FIGURE 1-2: *Offset Correction Settling Time.*

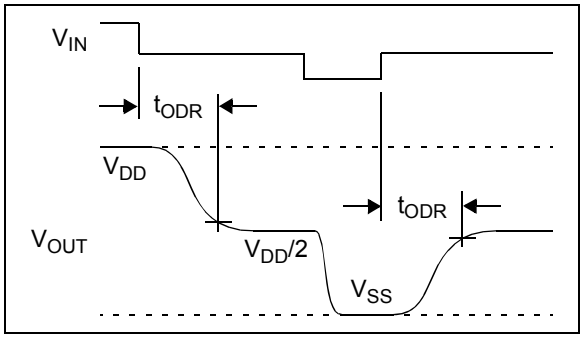


FIGURE 1-3: *Output Overdrive Recovery.*

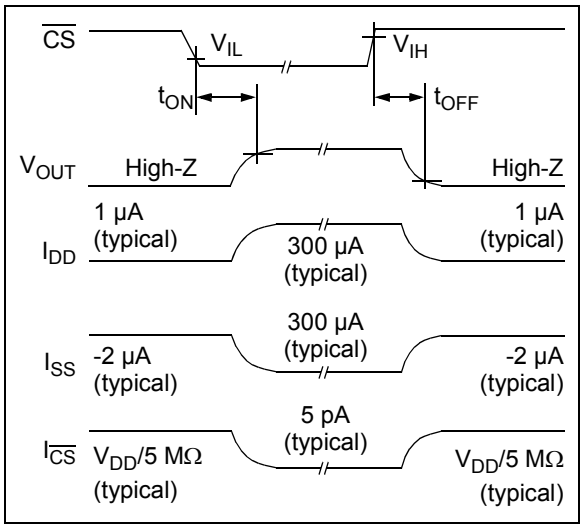


FIGURE 1-4: *Chip Select (MCP6V28).*

1.4 Test Circuits

The circuits used for the DC and AC tests are shown in Figure 1-5 and Figure 1-6. Lay the bypass capacitors out as discussed in **Section 4.3.10, Supply Bypassing and Filtering**. R_N is equal to the parallel combination of R_F and R_G to minimize bias current effects.

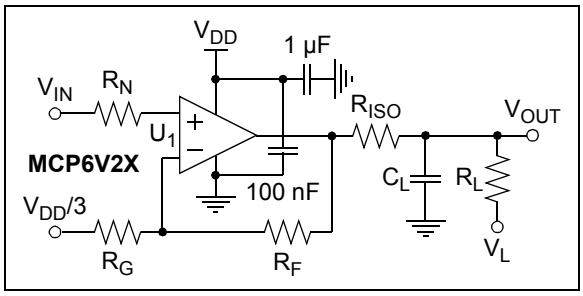


FIGURE 1-5: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

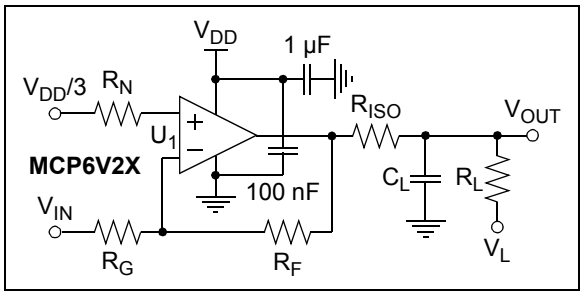


FIGURE 1-6: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

The circuit in Figure 1-7 tests the op amp input's dynamic behavior (i.e., IMD, t_{STR}, t_{STL} and t_{ODR}). The potentiometer balances the resistor network (V_{OUT} should equal V_{REF} at DC). The op amp's common mode input voltage is $V_{CM} = V_{IN}/2$. The error at the input (V_{ERR}) appears at V_{OUT} with a noise gain of 10 V/V.

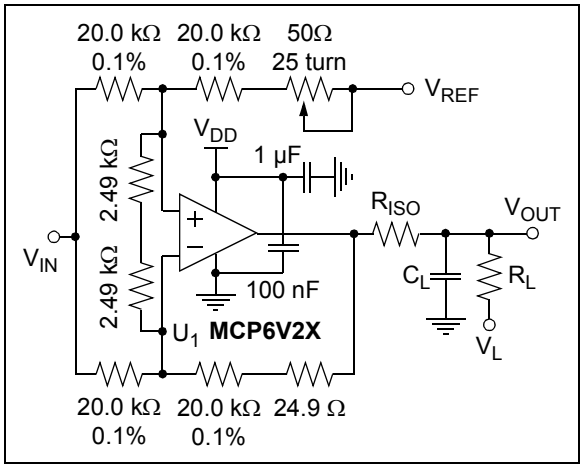


FIGURE 1-7: *Test Circuit for Dynamic Input Behavior.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

2.1 DC Input Precision

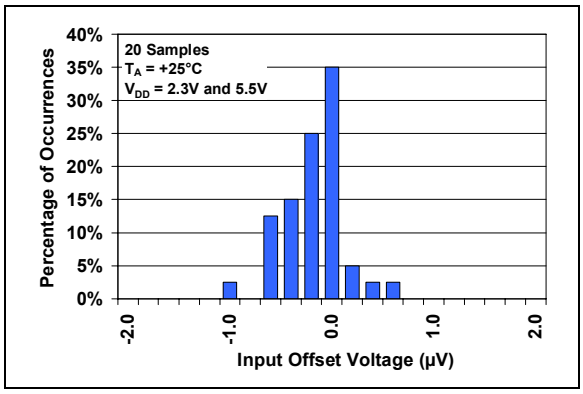


FIGURE 2-1: *Input Offset Voltage.*

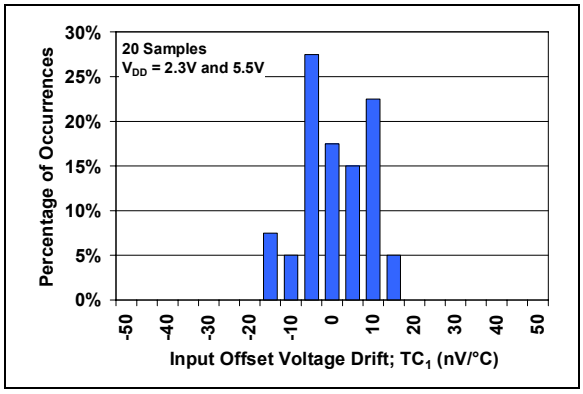


FIGURE 2-2: *Input Offset Voltage Drift.*

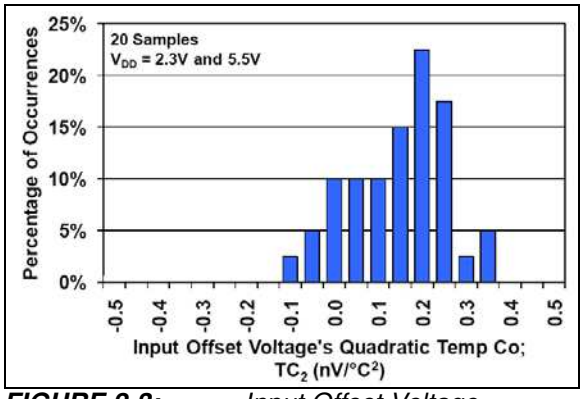


FIGURE 2-3: *Input Offset Voltage Quadratic Temperature Coefficient.*

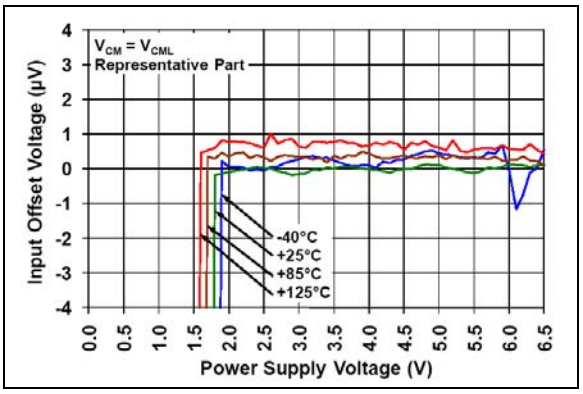


FIGURE 2-4: *Input Offset Voltage vs. Power Supply Voltage with V_{CM} = V_{CML}.*

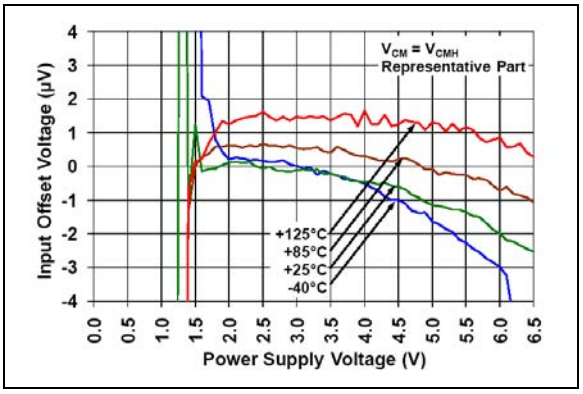


FIGURE 2-5: *Input Offset Voltage vs. Power Supply Voltage with V_{CM} = V_{CMH}.*

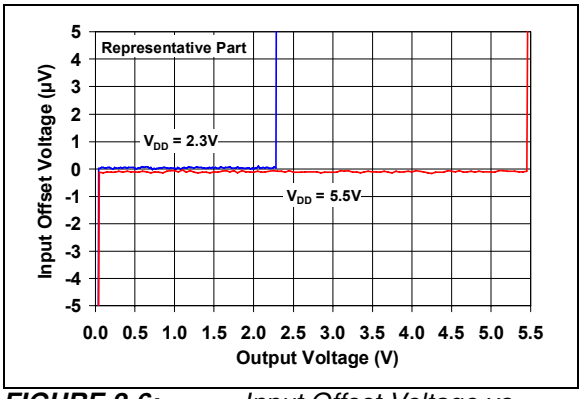


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

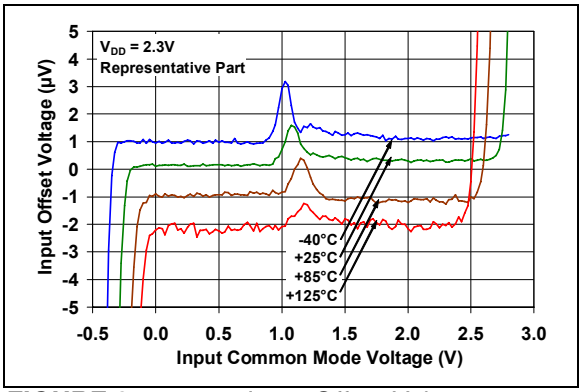


FIGURE 2-7: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 2.3V.*

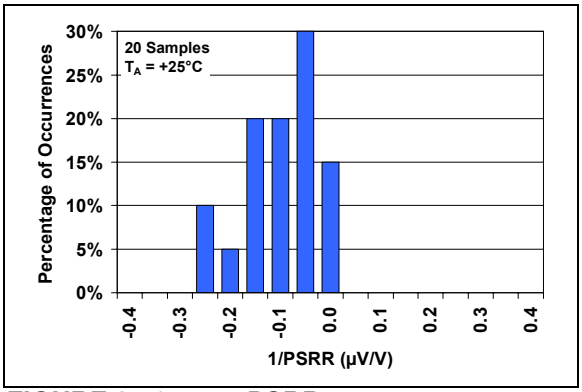


FIGURE 2-10: *PSRR.*

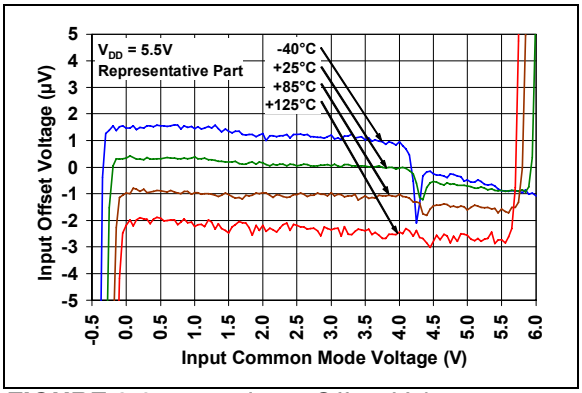


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Voltage with V_{DD} = 5.5V.*

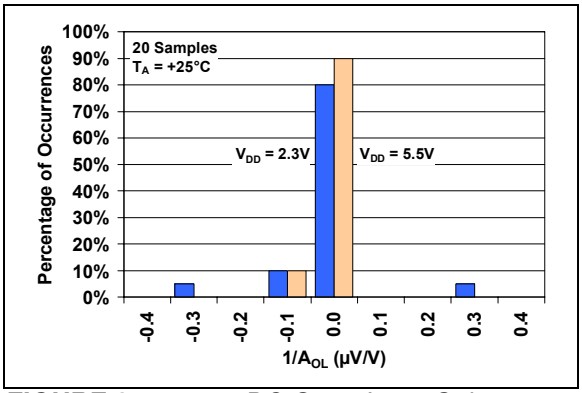


FIGURE 2-11: *DC Open-Loop Gain.*

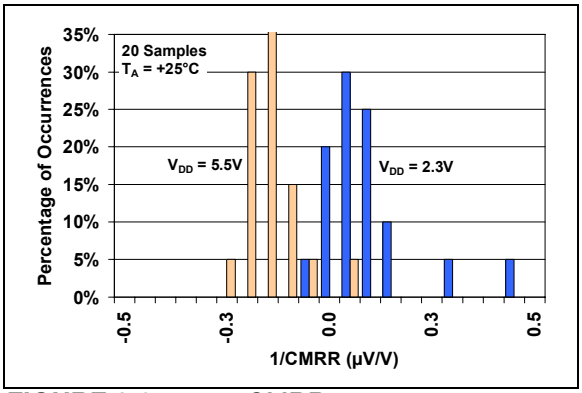


FIGURE 2-9: *CMRR.*

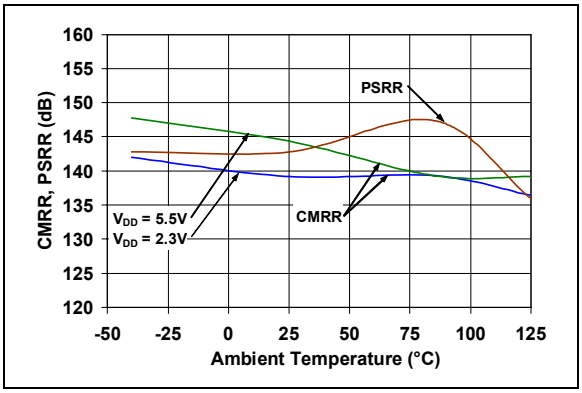


FIGURE 2-12: *CMRR and PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

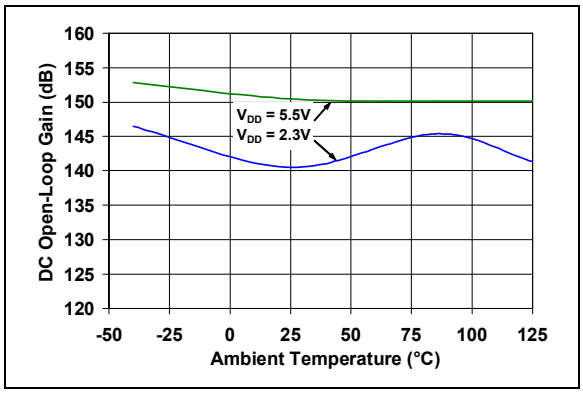


FIGURE 2-13: *DC Open-Loop Gain vs. Ambient Temperature.*

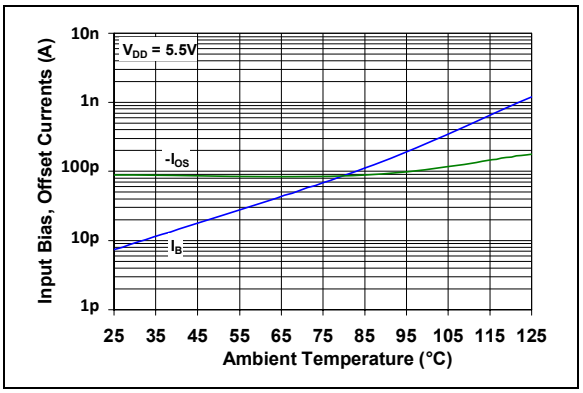


FIGURE 2-16: *Input Bias and Offset Currents vs. Ambient Temperature with V_{DD} = +5.5V.*

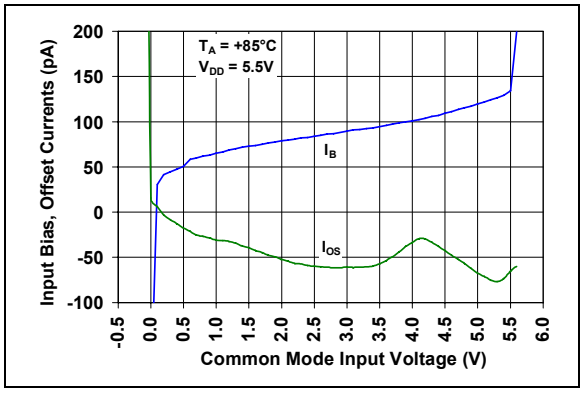


FIGURE 2-14: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +85°C.*

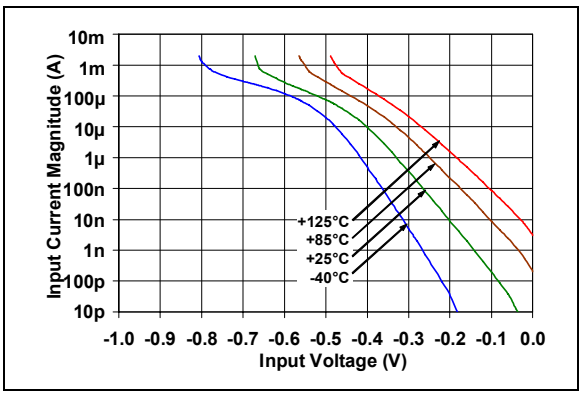


FIGURE 2-17: *Input Bias Current vs. Input Voltage (below V_{SS}).*

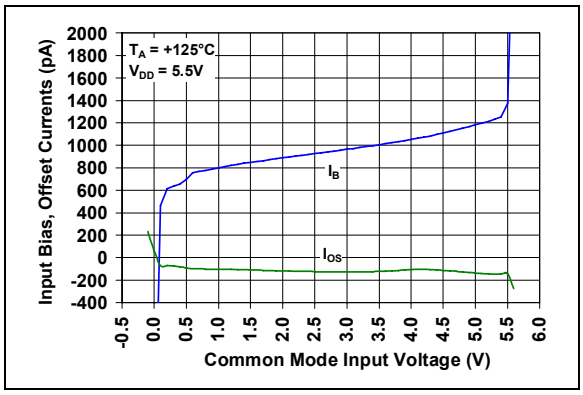


FIGURE 2-15: *Input Bias and Offset Currents vs. Common Mode Input Voltage with T_A = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

2.2 Other DC Voltages and Currents

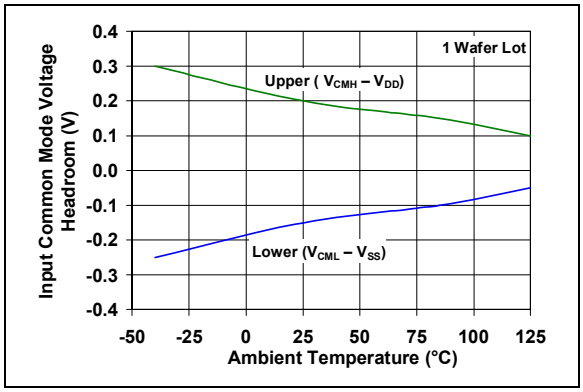


FIGURE 2-18: *Input Common Mode Voltage Headroom (Range) vs. Ambient Temperature.*

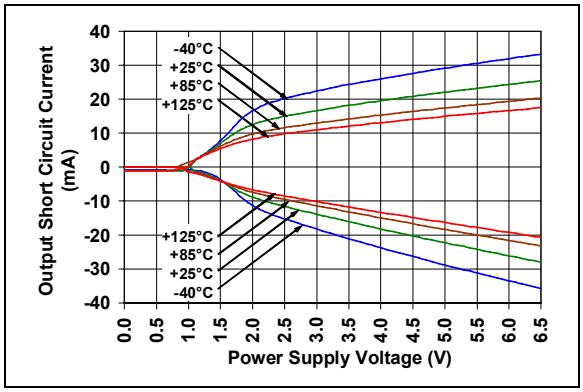


FIGURE 2-21: *Output Short Circuit Current vs. Power Supply Voltage.*

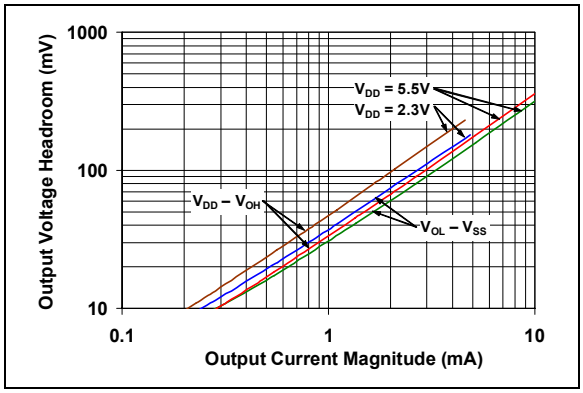


FIGURE 2-19: *Output Voltage Headroom vs. Output Current.*

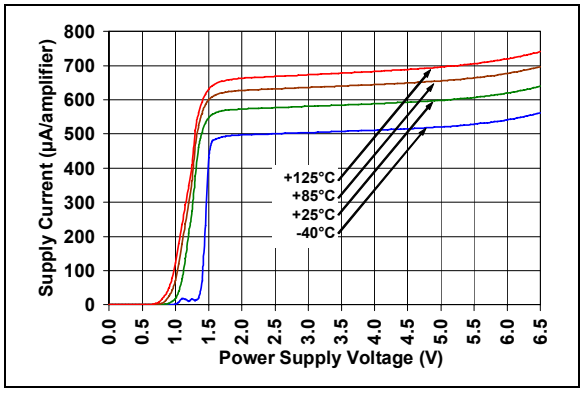


FIGURE 2-22: *Supply Current vs. Power Supply Voltage.*

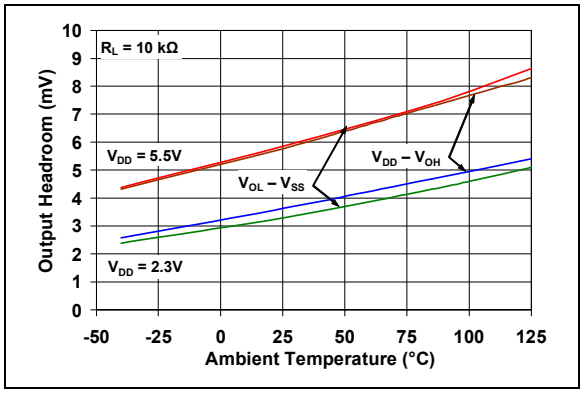


FIGURE 2-20: *Output Voltage Headroom vs. Ambient Temperature.*

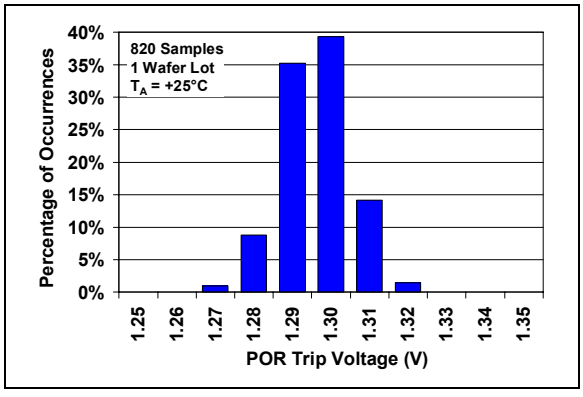


FIGURE 2-23: *Power On Reset Trip Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

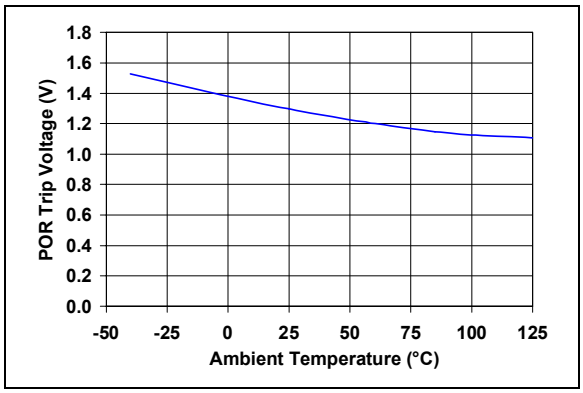


FIGURE 2-24: *Power On Reset Voltage vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

2.3 Frequency Response

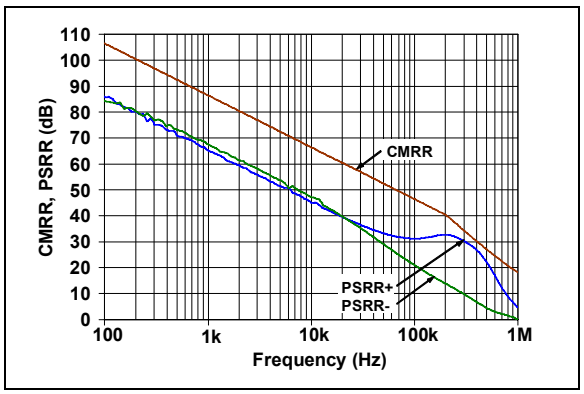


FIGURE 2-25: *CMRR and PSRR vs. Frequency.*

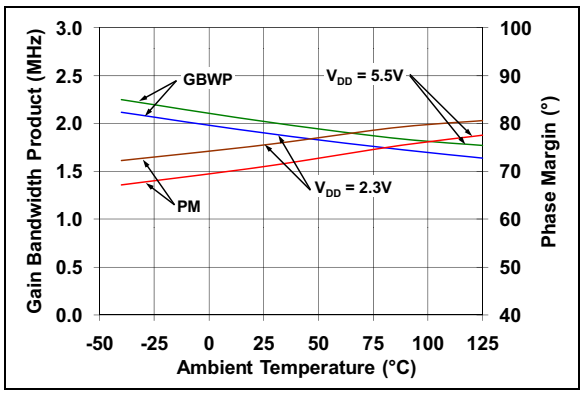


FIGURE 2-28: *Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.*

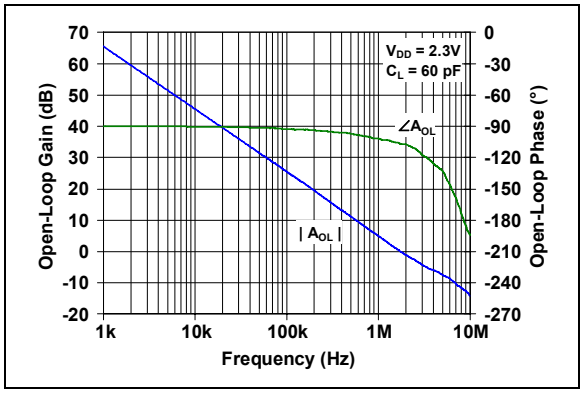


FIGURE 2-26: *Open-Loop Gain vs. Frequency with V_{DD} = 2.3V.*

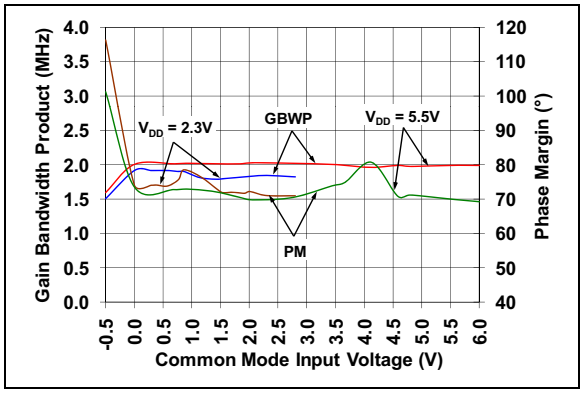


FIGURE 2-29: *Gain Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.*

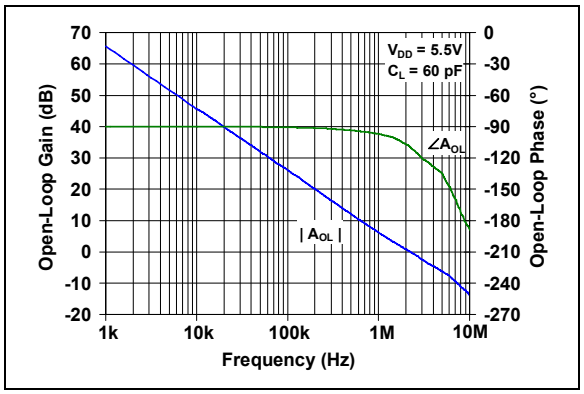


FIGURE 2-27: *Open-Loop Gain vs. Frequency with V_{DD} = 5.5V.*

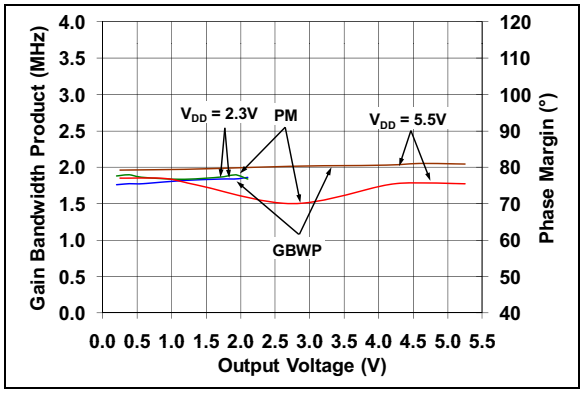


FIGURE 2-30: *Gain Bandwidth Product and Phase Margin vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

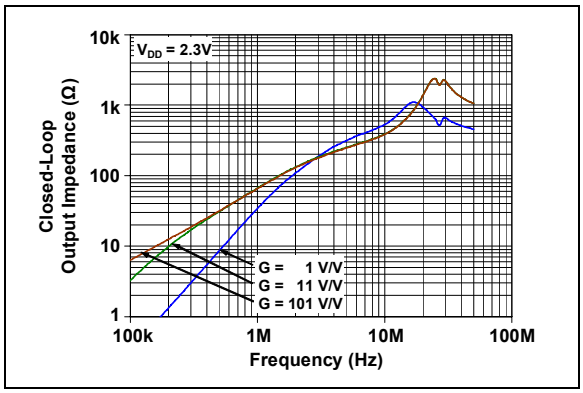


FIGURE 2-31: *Closed-Loop Output Impedance vs. Frequency with V_{DD} = 2.3V.*

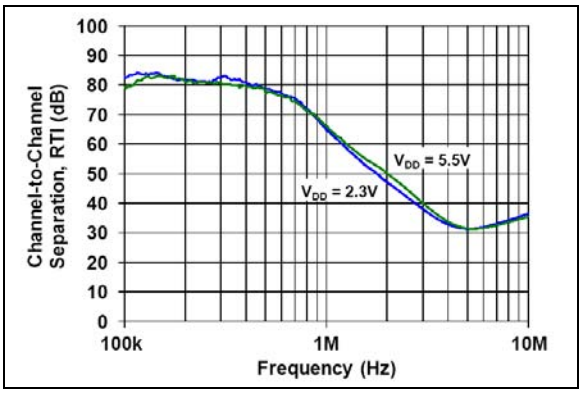


FIGURE 2-33: *Channel-to-Channel Separation vs. Frequency.*

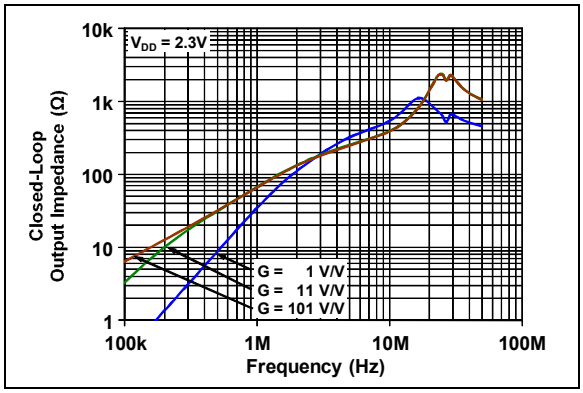


FIGURE 2-32: *Closed-Loop Output Impedance vs. Frequency with V_{DD} = 5.5V.*

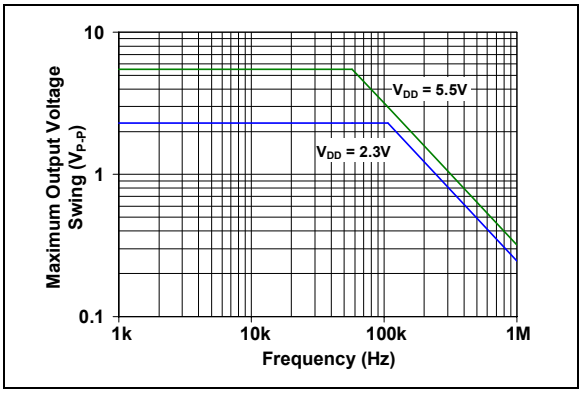


FIGURE 2-34: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

2.4 Input Noise and Distortion

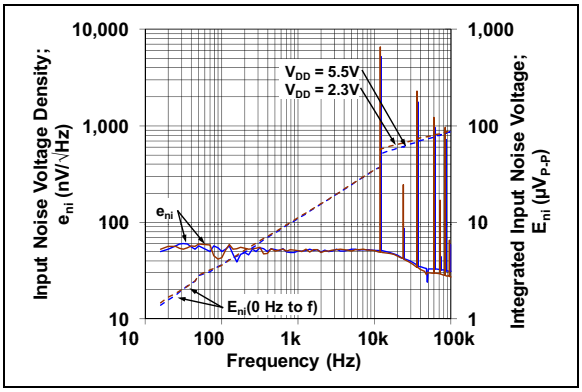


FIGURE 2-35: *Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.*

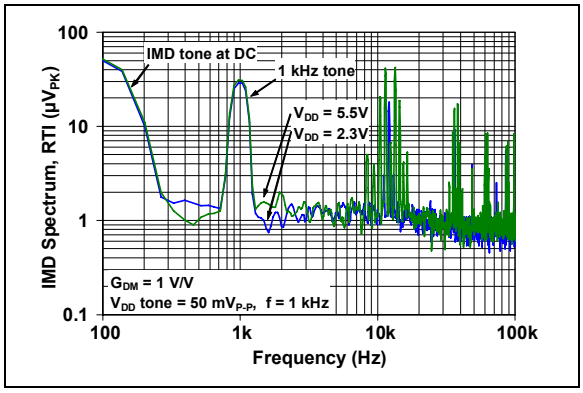


FIGURE 2-38: *Intermodulation Distortion vs. Frequency with V_{DD} Disturbance (see Figure 1-7).*

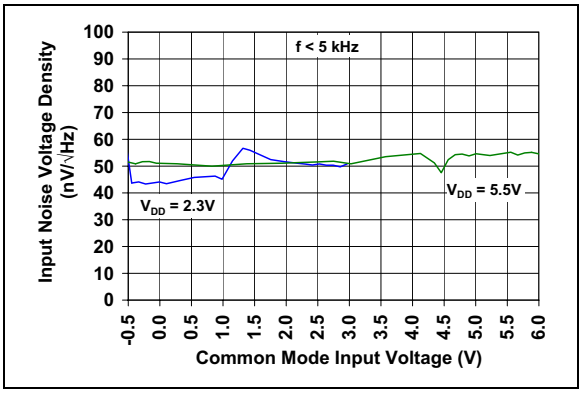


FIGURE 2-36: *Input Noise Voltage Density vs. Input Common Mode Voltage.*

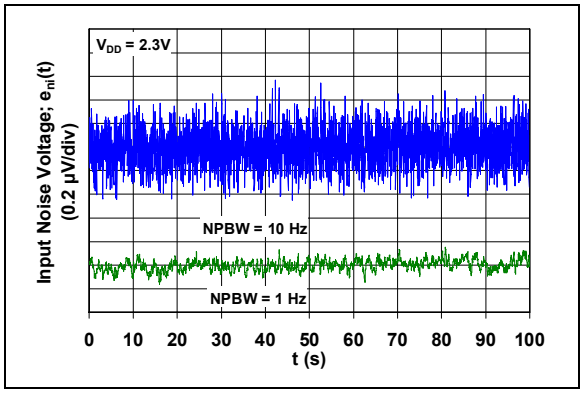


FIGURE 2-39: *Input Noise vs. Time with 1 Hz and 10 Hz Filters and V_{DD} =2.3V.*

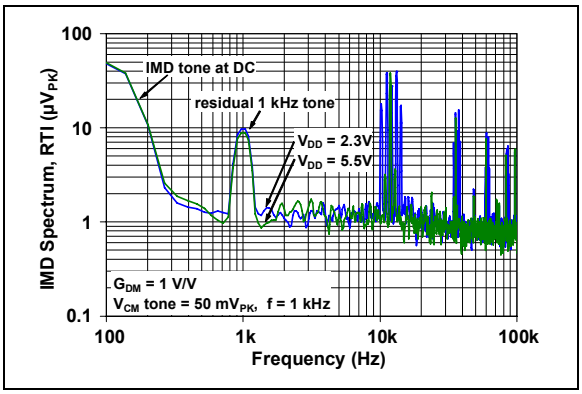


FIGURE 2-37: *Intermodulation Distortion vs. Frequency with V_{CM} Disturbance (see Figure 1-7).*

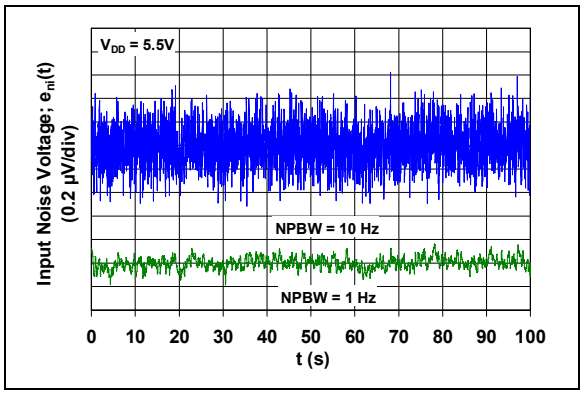


FIGURE 2-40: *Input Noise vs. Time with 1 Hz and 10 Hz Filters and V_{DD} =5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

2.5 Time Response

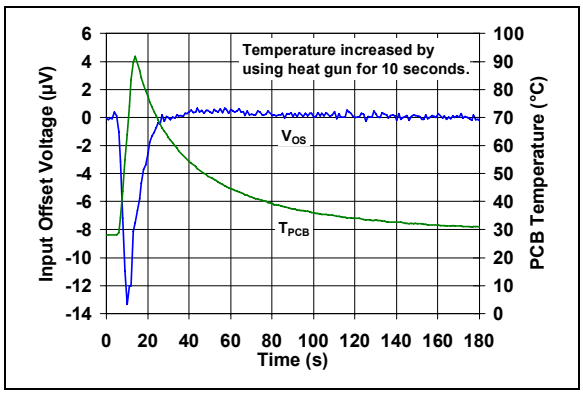


FIGURE 2-41: *Input Offset Voltage vs. Time with Temperature Change.*

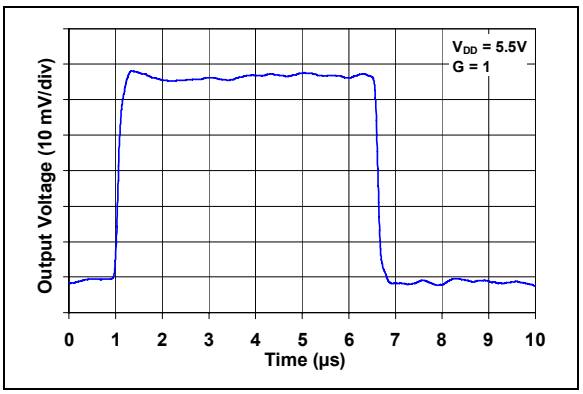


FIGURE 2-44: *Non-inverting Small Signal Step Response.*

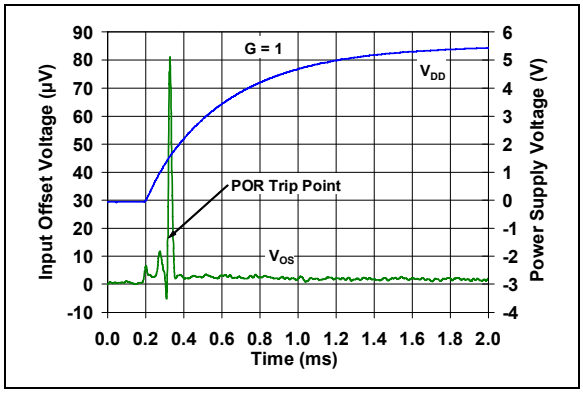


FIGURE 2-42: *Input Offset Voltage vs. Time at Power Up.*

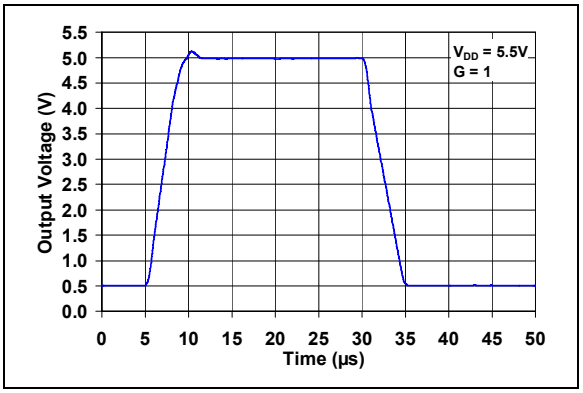


FIGURE 2-45: *Non-inverting Large Signal Step Response.*

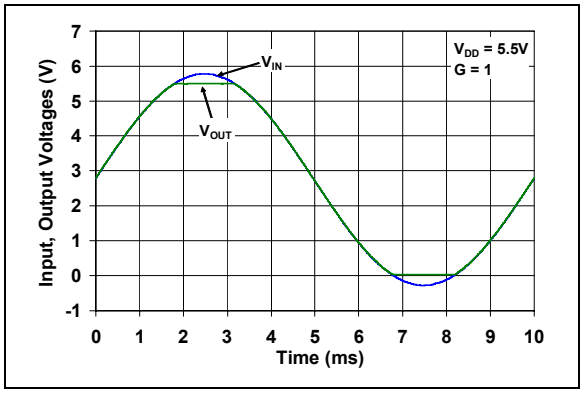


FIGURE 2-43: *The MCP6V26/7/8 Device Shows No Input Phase Reversal with Overdrive.*

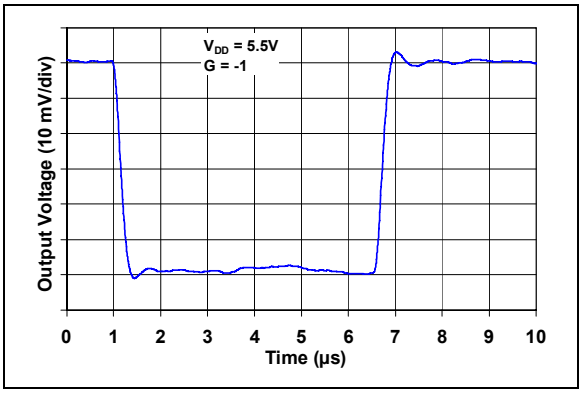


FIGURE 2-46: *Inverting Small Signal Step Response.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF and $\overline{CS}$ = GND.

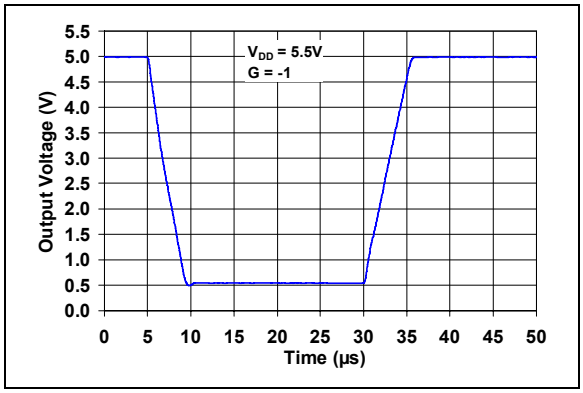


FIGURE 2-47: *Inverting Large Signal Step Response.*

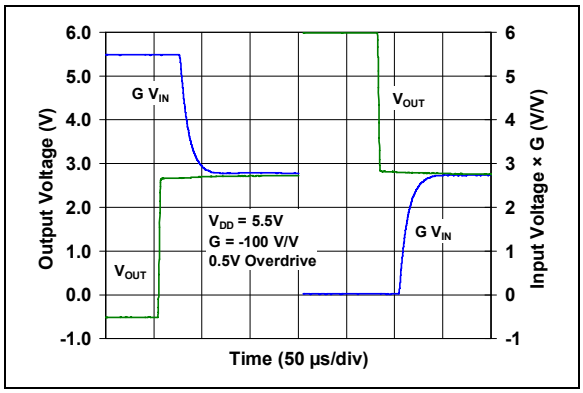


FIGURE 2-49: *Output Overdrive Recovery vs. Time with G = -100 V/V.*

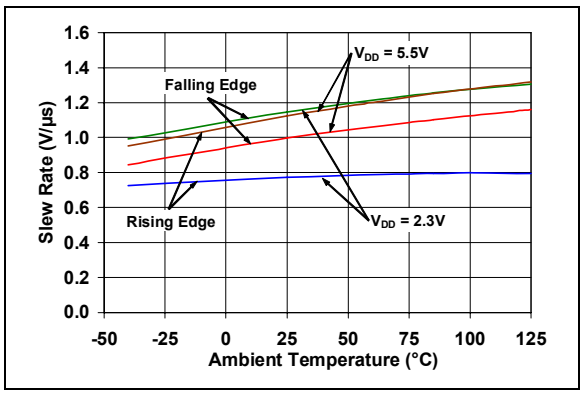


FIGURE 2-48: *Slew Rate vs. Ambient Temperature.*

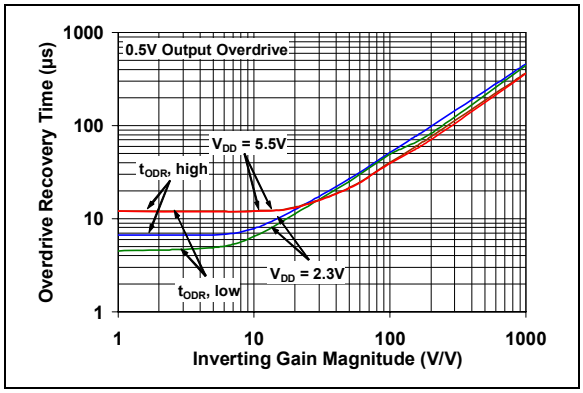


FIGURE 2-50: *Output Overdrive Recovery Time vs. Inverting Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

2.6 Chip Select Response (MCP6V28 only)

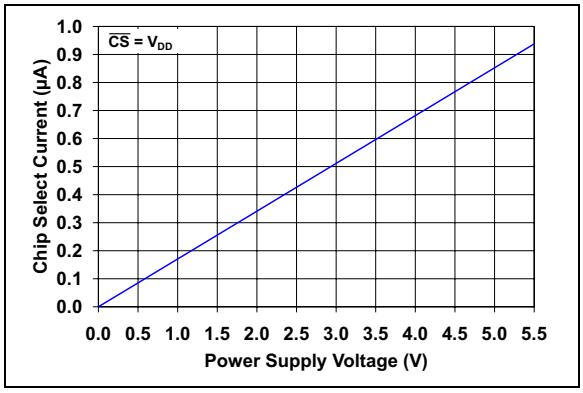


FIGURE 2-51: *Chip Select Current vs. Power Supply Voltage.*

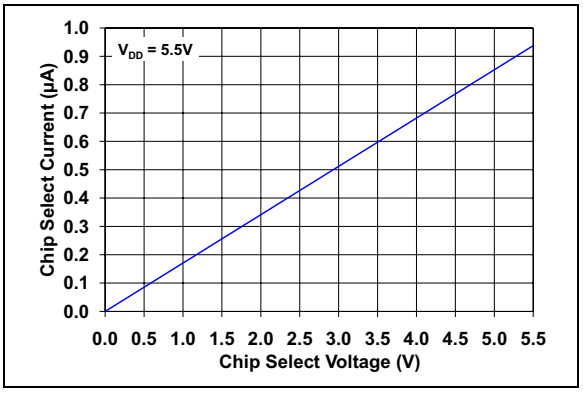


FIGURE 2-54: *Chip Select Current vs. Chip Select Voltage.*

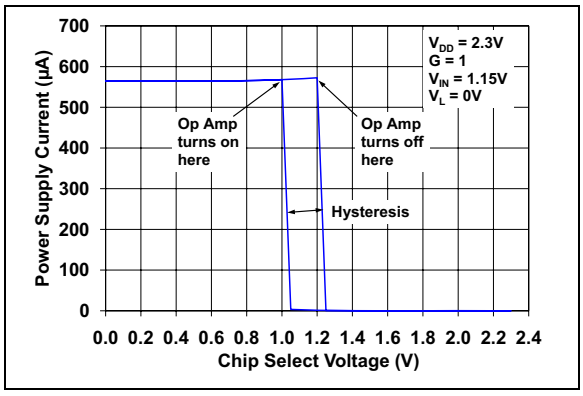


FIGURE 2-52: *Power Supply Current vs. Chip Select Voltage with V_{DD} = 2.3V.*

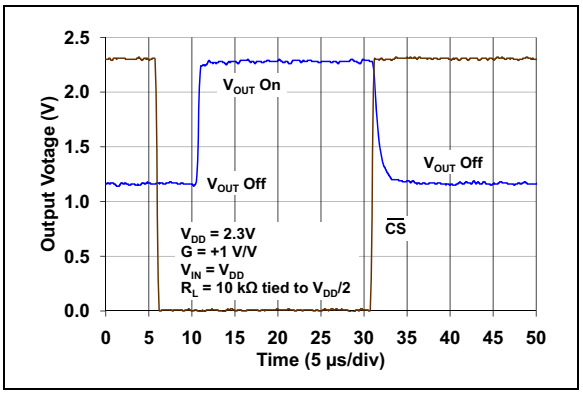


FIGURE 2-55: *Chip Select Voltage, Output Voltage vs. Time with V_{DD} = 2.3V.*

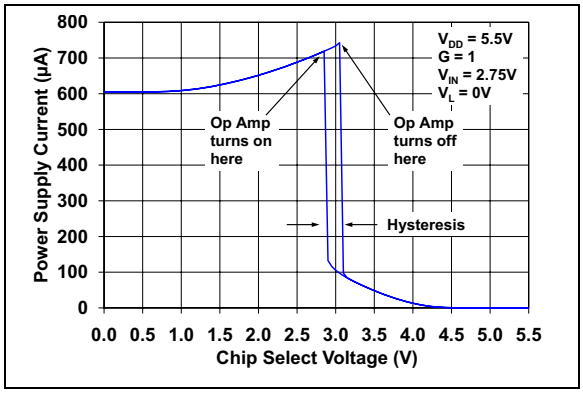


FIGURE 2-53: *Power Supply Current vs. Chip Select Voltage with V_{DD} = 5.5V.*

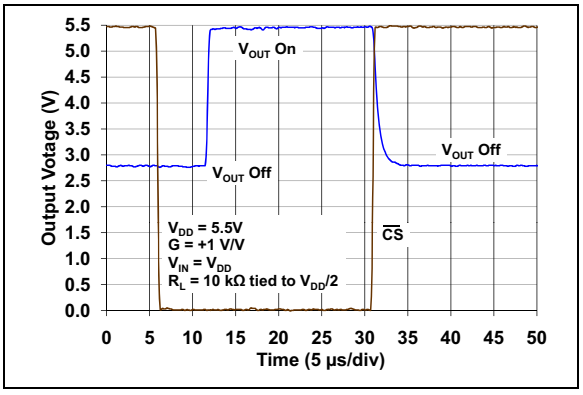


FIGURE 2-56: *Chip Select Voltage, Output Voltage vs. Time with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND.

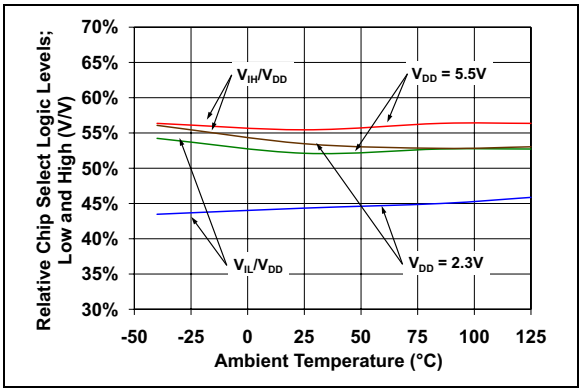


FIGURE 2-57: *Chip Select Relative Logic Thresholds vs. Ambient Temperature.*

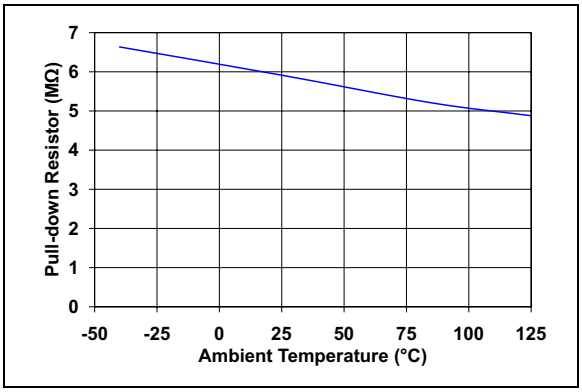


FIGURE 2-60: *Chip Select's Pull-down Resistor (R_{PD}) vs. Ambient Temperature.*

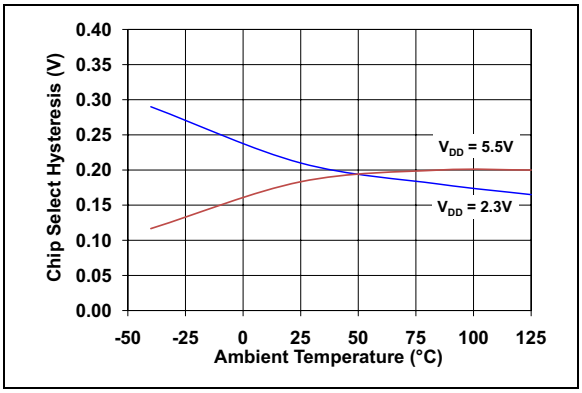


FIGURE 2-58: *Chip Select Hysteresis.*

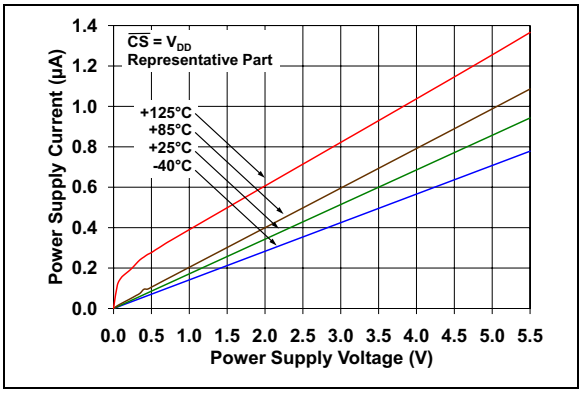


FIGURE 2-61: *Quiescent Current in Shutdown vs. Power Supply Voltage.*

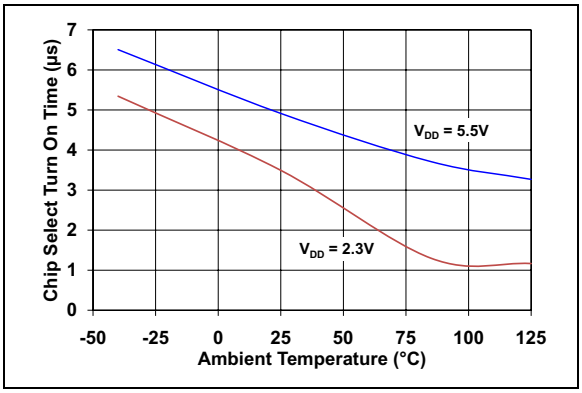


FIGURE 2-59: *Chip Select Turn On Time vs. Ambient Temperature.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6V26		MCP6V27		MCP6V28		Symbol	Description
TDFN	MSOP, SOIC	DFN	MSOP, SOIC	TDFN	MSOP, SOIC		
6	6	1	1	6	6	V_{OUT}, V_{OUTA}	Output (op amp A)
2	2	2	2	2	2	V_{IN}–, V_{INA}–	Inverting Input (op amp A)
3	3	3	3	3	3	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
4	4	4	4	4	4	V_{SS}	Negative Power Supply
—	—	5	5	—	—	V_{INB}+	Non-inverting Input (op amp B)
—	—	6	6	—	—	V_{INB}–	Inverting Input (op amp B)
—	—	7	7	—	—	V_{OUTB}	Output (op amp B)
7	7	8	8	7	7	V_{DD}	Positive Power Supply
—	—	—	—	8	8	$\overline{CS}$	Chip Select (op amp A)
1, 5, 8	1, 5, 8	—	—	1, 5	1, 5	NC	No Internal Connection
9	—	9	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs (V_{IN}+, V_{IN}–, …) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.3V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Chip Select ($\overline{CS}$) Digital Input

This pin ($\overline{CS}$) is a CMOS, Schmitt-triggered input that places the MCP6V28 op amp into a low power mode of operation.

3.5 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

4.0 APPLICATIONS

The MCP6V26/7/8 family of auto-zeroed op amps are manufactured using Microchip's state-of-the-art CMOS process. This family is designed for low cost, low power and high precision applications. Its low supply voltage, low quiescent current and wide bandwidth make the MCP6V26/7/8 devices ideal for battery-powered applications.

4.1 Overview of Auto-Zeroing Operation

Figure 4-1 shows a simplified diagram of the MCP6V26/7/8 auto-zeroed op amps. This will be used to explain how the DC voltage errors are reduced in this architecture.

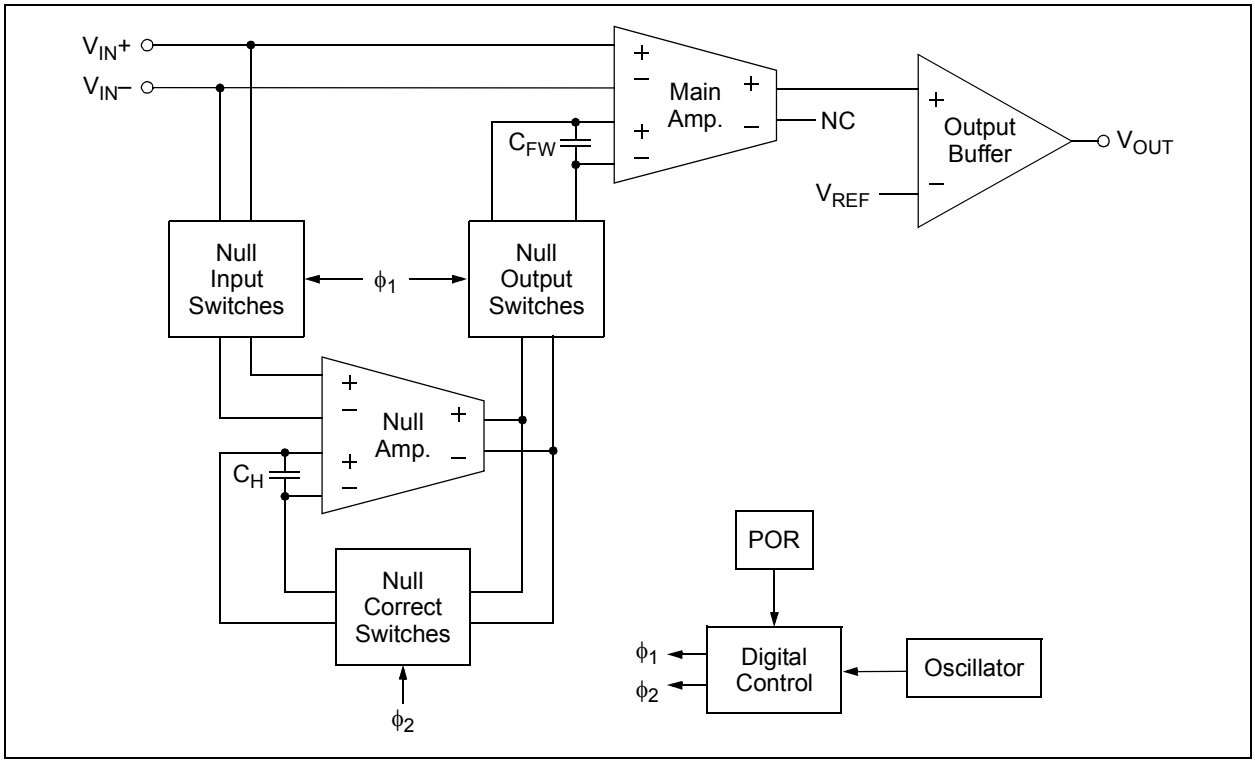


FIGURE 4-1: *Simplified Auto-Zeroed Op Amp Functional Diagram.*

4.1.1 BUILDING BLOCKS

The Null Amplifier and Main Amplifier are designed for high gain and accuracy using a differential topology. They have a main input pair (+ and - pins at their top left) used for the signal. They have an auxiliary input pair (+ and - pins at their bottom left) used for correcting the offset voltages. Both input pairs are added together internally. The capacitors at the auxiliary inputs (C_{FW} and C_H) hold the corrected values during normal operation.

The Output Buffer is designed to drive external loads at the V_{OUT} pin. It also produces a single-ended output voltage (V_{REF} is an internal reference voltage).

All of these switches are make-before-break in order to minimize glitch-induced errors. They are driven by two clock phases (ϕ_1 and ϕ_2) that select between normal mode and auto-zeroing mode.

The clock is derived from an internal R-C oscillator running at a rate of f_{OSC1} = 850 kHz. The oscillator's output is divided down to the desired rate.

The internal POR ensures the part starts up in a known good state. It also provides protection against power supply brown-out events.

The Digital Control circuitry takes care of all of the housekeeping details of the switching operation. It also takes care of POR events.

4.1.2 AUTO-ZEROING ACTION

Figure 4-2 shows the connections between amplifiers during the Normal Mode of operation (ϕ_1). The hold capacitor (C_H) corrects the Null Amplifier's input offset. Since the Null Amplifier has very high gain, it dominates the signal seen by the Main Amplifier. This greatly reduces the impact of the Main Amplifier's input offset voltage on overall performance. Essentially, the Null Amplifier and Main Amplifier behave as a regular op amp with very high gain (A_{OL}) and very low offset voltage (V_{OS}).

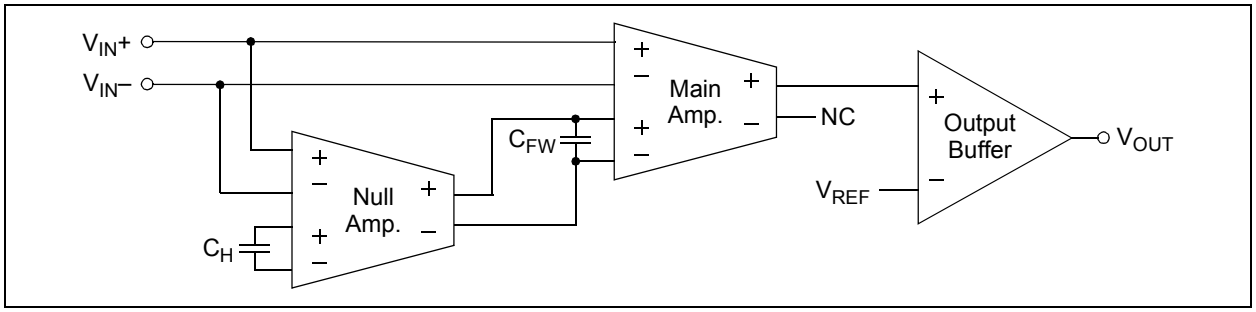


FIGURE 4-2: *Normal Mode of Operation (ϕ_1); Equivalent Amplifier Diagram.*

Figure 4-3 shows the connections between amplifiers during the Auto-zeroing Mode of operation (ϕ_2). The signal goes directly through the Main Amplifier, and the flywheel capacitor (C_{FW}) maintains a constant correction on the Main Amplifier's offset.

The Null Amplifier uses its own high open loop gain to drive the voltage across C_H to the point where its input offset voltage is almost zero. Because the signal input pair is connected to V_{IN}+, the auto-zeroing action corrects the offset at the current common mode input voltage (V_{CM}) and supply voltage (V_{DD}). This makes the DC CMRR and PSRR very high also.

Since these corrections happen every 40 µs, or so, we also minimize slow errors, including offset drift with temperature ($\Delta V_{OS}/\Delta T_A$), 1/f noise, and input offset aging.

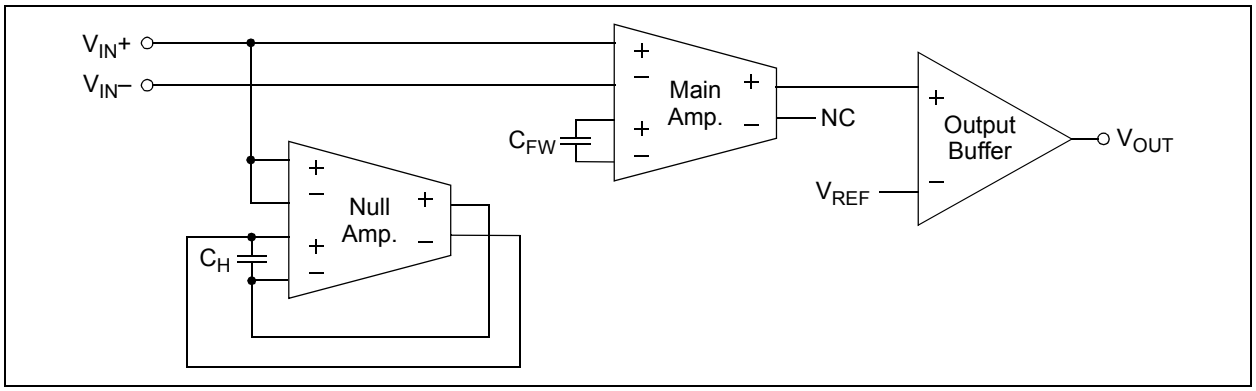


FIGURE 4-3: *Auto-zeroing Mode of Operation (ϕ_2); Equivalent Diagram.*

4.1.3 INTERMODULATION DISTORTION (IMD)

The MCP6V26/7/8 op amps will show intermodulation distortion (IMD), products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the auto-zeroing circuitry's non-linear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock's harmonics has a series of IMD tones centered on it. See Figure 2-37 and Figure 2-38.

4.2 Other Functional Blocks

4.2.1 RAIL-TO-RAIL INPUTS

The input stage of the MCP6V26/7/8 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}, which is approximately equal to $V_{IN}+$ and $V_{IN}–$ in normal operation) and the other at high V_{CM}. With this topology, the input operates with V_{CM} up to V_{DD} + 0.2V, and down to V_{SS} – 0.15V, at +25°C (see Figure 2-18). The input offset voltage (V_{OS}) is measured at $V_{CM} = V_{SS} – 0.15V$ and V_{DD} + 0.2V to ensure proper operation.

The transition between the input stages occurs when $V_{CM} \approx V_{DD} – 1.2V$ (see Figure 2-7 and Figure 2-8). For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-43 shows an input voltage exceeding both supplies with no phase inversion.

4.2.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings †**). This requirement is independent of the current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-4. This structure was chosen to protect the input transistors against many (but not all) over-voltage conditions, and to minimize input bias current (I_B).

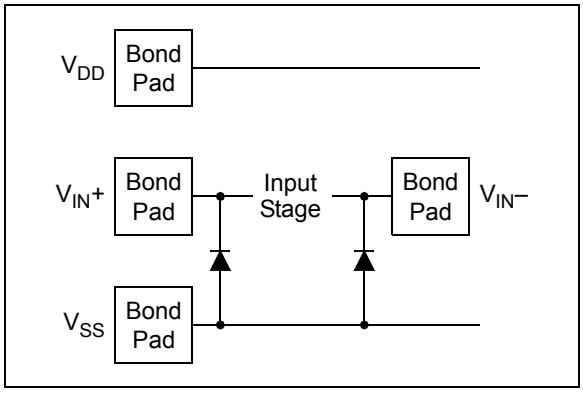


FIGURE 4-4: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that are well above V_{DD}; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V_{DD}) events. Very fast ESD events (that meet the spec) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-5 shows one approach to protecting these inputs. D_1 and D_2 may be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode-connected FETs for low leakage.

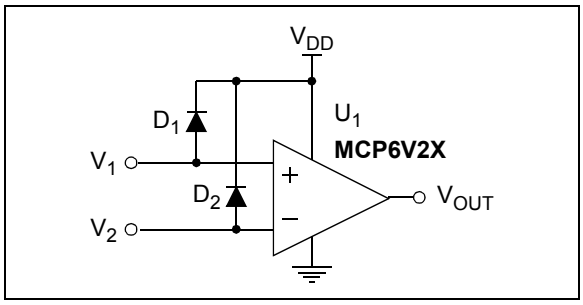


FIGURE 4-5: *Protecting the Analog Inputs Against High Voltages.*

4.2.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1, Absolute Maximum Ratings †**). This requirement is independent of the voltage limits previously discussed.

Figure 4-6 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible current in or out of the input pins (and into D_1 and D_2). The diode currents will dump onto V_{DD}.

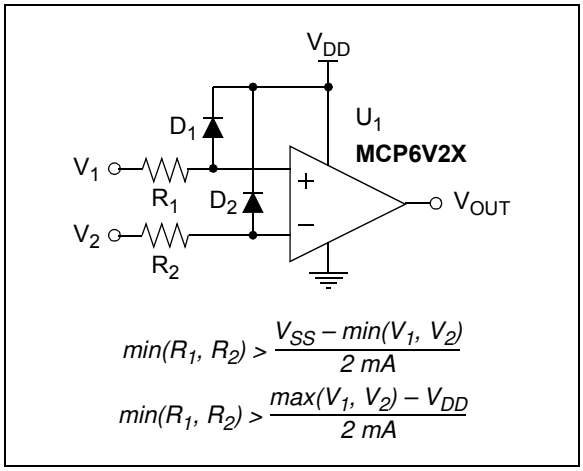


FIGURE 4-6: *Protecting the Analog Inputs Against High Currents.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, the currents through diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-17.

4.2.2 RAIL-TO-RAIL OUTPUT

The output voltage range of the MCP6V26/7/8 zero-drift op amps is V_{DD} – 15 mV (minimum) and V_{SS} + 15 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-19 and Figure 2-20.

This op amp is designed to drive light loads; use another amplifier to buffer the output from heavy loads.

4.2.3 CHIP SELECT ($\overline{CS}$)

The single MCP6V28 has a Chip Select ($\overline{CS}$) pin. When $\overline{CS}$ is pulled high, the supply current for the corresponding op amp drops to about 1 µA (typical), and is pulled through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the internal pull-down resistor (about 5 MΩ) will keep the part on. Figure 1-4 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.3 Application Tips

4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1-1 gives both the linear and quadratic temperature coefficients (TC_1 and TC_2) of input offset voltage. The input offset voltage, at any temperature in the specified range, can be calculated as follows:

EQUATION 4-1:

$$V_{OS}(T_A) = V_{OS} + TC_1\Delta T + TC_2\Delta T^2$$

Where:

ΔT	=	T_A – 25°C
$V_{OS}(T_A)$	=	input offset voltage at T_A
V_{OS}	=	input offset voltage at +25°C
TC_1	=	linear temperature coefficient
TC_2	=	quadratic temperature coefficient

4.3.2 DC GAIN PLOTS

Figure 2-9, Figure 2-10 and Figure 2-11 are histograms of the reciprocals (in units of µV/V) of CMRR, PSRR and A_{OL}, respectively. They represent the change in input offset voltage (V_{OS}) with a change in common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}).

The $1/A_{OL}$ histogram is centered near 0 µV/V because the measurements are dominated by the op amp's input noise. The negative values shown represent noise, *not* unstable behavior. We validate the op amps' stability by making multiple measurements of V_{OS}; an unstable part would fail, because it would show either greater variability in V_{OS}, or the output stuck at one of the rails.

4.3.3 OFFSET AT POWER UP

When these parts power up, the input offset (V_{OS}) starts at its uncorrected value (usually less than ±5 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an output overdrive time (like t_{ODR}), in addition to the startup time (like t_{STR}).

It can be simple to avoid this extra startup time. Reducing the gain is one method. Adding a capacitor across the feedback resistor (R_F) is another method.

4.3.4 SOURCE RESISTANCES

The input bias currents have two significant components; switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.

The inputs should see a resistance on the order of 10Ω to 1 kΩ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

Small input resistances are needed for high gains. Without them, parasitic capacitances can cause positive feedback and instability.

4.3.5 SOURCE CAPACITANCE

The capacitances seen by the two inputs should be small and matched. The internal switches connected to the inputs dump charges on these capacitors; an offset can be created if the capacitances do not match. Large input capacitances and source resistances, together with high gain, can lead to positive feedback and instability.

4.3.6 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. These auto-zeroed op amps have a different output impedance than most op amps, due to their unique topology.

When driving a capacitive load with these op amps, a series resistor at the output (R_{ISO} in Figure 4-7) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

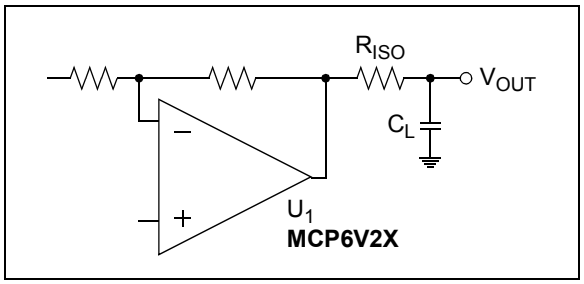


FIGURE 4-7: *Output Resistor, R_{ISO}, Stabilizes Capacitive Loads.*

Figure 4-8 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N^2). The y-axis is the normalized resistance ($G_N R_{ISO}$).

G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

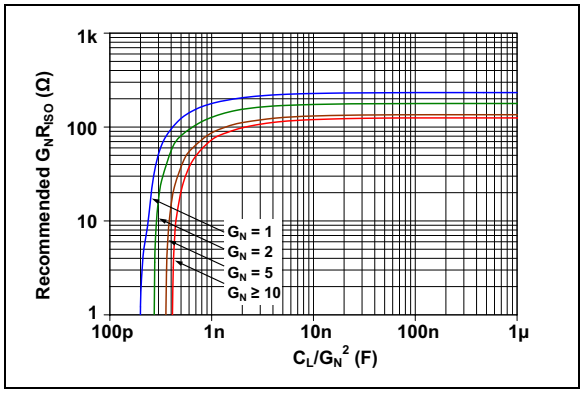


FIGURE 4-8: *Recommended R_{ISO} values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6V26/7/8 SPICE macro model are helpful.

4.3.7 STABILIZING OUTPUT LOADS

This family of auto-zeroed op amps has an output impedance (Figure 2-31 and Figure 2-32) that has a double zero when the gain is low. This can cause a large phase shift in feedback networks that have low resistance near the part's bandwidth. This large phase shift can cause stability problems.

Figure 4-9 shows that the load on the output is $(R_L + R_{ISO})||(R_F + R_G)$, where R_{ISO} is before the load (like Figure 4-7). This load needs to be large enough to maintain stability; it should be at least (2 kΩ)/G_N.

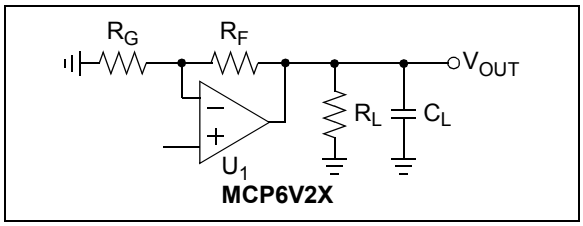


FIGURE 4-9: *Output Load.*

4.3.8 GAIN PEAKING

Figure 4-10 shows an op amp circuit that represents non-inverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp's common mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel. The capacitance C_{FP} represents the parasitic capacitance coupling the output and non-inverting input pins.

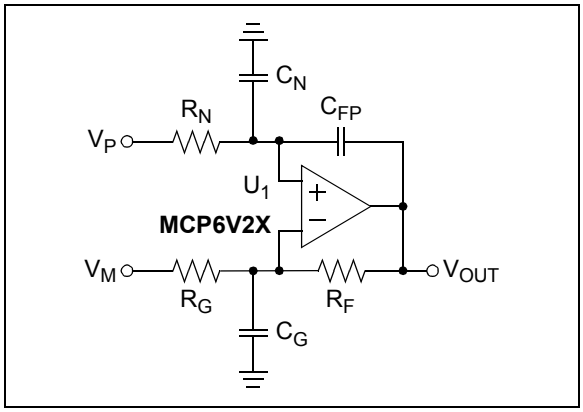


FIGURE 4-10: *Amplifier with Parasitic Capacitance.*

C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G or $R_F||R_G$.

C_N and R_N form a low-pass filter that affects the signal at V_P. This filter has a single real pole at $1/(2\pi R_N C_N)$.