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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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MCP79400/MCP79401/MCP79402

Battery-Backed I²C Real-Time Clock/Calendar with SRAM and Protected EEPROM

Device Selection Table

Part Number	Protected EEPROM
MCP79400	Unprogrammed
MCP79401	EUI-48™
MCP79402	EUI-64™

Timekeeping Features

- Real-Time Clock/Calendar (RTCC):
  - Hours, Minutes, Seconds, Day of Week, Day, Month, Year
  - Leap year compensated to 2399
  - 12/24-hour modes
- Oscillator for 32.768 kHz Crystals:
  - Optimized for 6-9 pF crystals
- On-Chip Digital Trimming/Calibration:
  - ±1 ppm resolution
  - ±129 ppm
- Dual Programmable Alarms
- Versatile Output Pin:
  - Clock output with selectable frequency
  - Alarm output
  - General purpose output
- Power-Fail Time-Stamp:
  - Time logged on switchover to and from Battery mode

Low-Power Features

- Wide Voltage Range:
  - Operating voltage range of 1.8V to 5.5V
  - Backup voltage range of 1.3V to 5.5V
- Low Typical Timekeeping Current:
  - Operating from VCC: 1.2 µA at 3.3V
  - Operating from battery backup: 925 nA at 3.0V
- Automatic Switchover to Battery Backup

User Memory

- 64-Byte Battery-Backed SRAM
- 64-Bit Protected EEPROM Area:
  - Robust write unlock sequence
  - EUI-48™ MAC address (MCP79401)
  - EUI-64™ MAC address (MCP79402)
  - Custom programming available

Operating Ranges

- 2-Wire Serial Interface, I²C Compatible:
  - I²C clock rate up to 400 kHz
- Temperature Range:
  - Industrial (I): -40°C to +85°C

Packages

- 8-Lead SOIC, MSOP, TSSOP and 2x3 TDFN

General Description

The MCP7940X Real-Time Clock/Calendar (RTCC) tracks time using internal counters for hours, minutes, seconds, days, months, years, and day of week. Alarms can be configured on all counters up to and including months. For usage and configuration, the MCP7940X supports I²C communications up to 400 kHz.

The open-drain, multi-functional output can be configured to assert on an alarm match, to output a selectable frequency square wave or as a general purpose output.

The MCP7940X is designed to operate using a 32.768 kHz tuning fork crystal with external crystal load capacitors. On-chip digital trimming can be used to adjust for frequency variance caused by crystal tolerance and temperature.

SRAM and timekeeping circuitry are powered from the back-up supply when main power is lost, allowing the device to maintain accurate time and the SRAM contents. The times when the device switches over to the back-up supply and when primary power returns are both logged by the power-fail time-stamp.

The MCP7940X features 64 bits of EEPROM which is only writable after an unlock sequence, making it ideal for storing a unique ID or other critical information. The MCP79401 and MCP79402 are pre-programmed with EUI-48 and EUI-64 addresses, respectively. Custom programming is also available.

Package Types

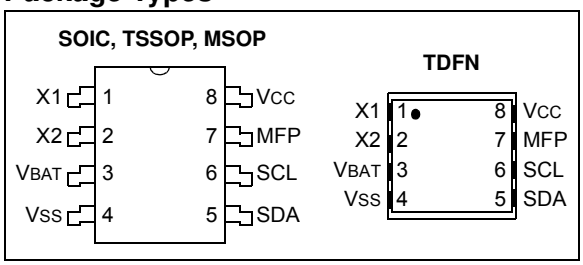


FIGURE 1-1: TYPICAL APPLICATION SCHEMATIC

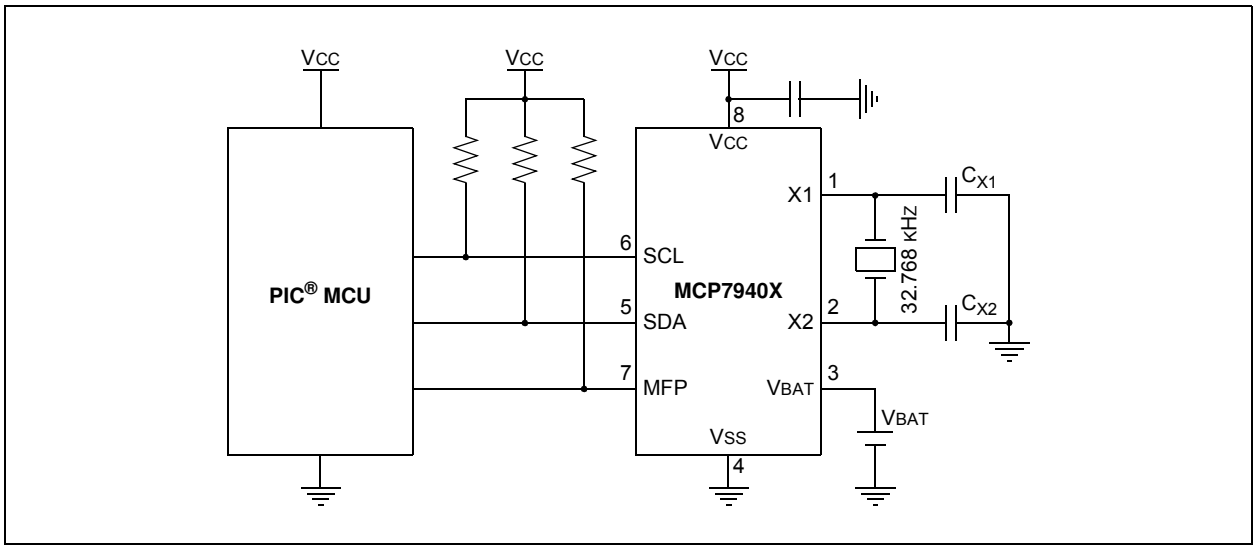
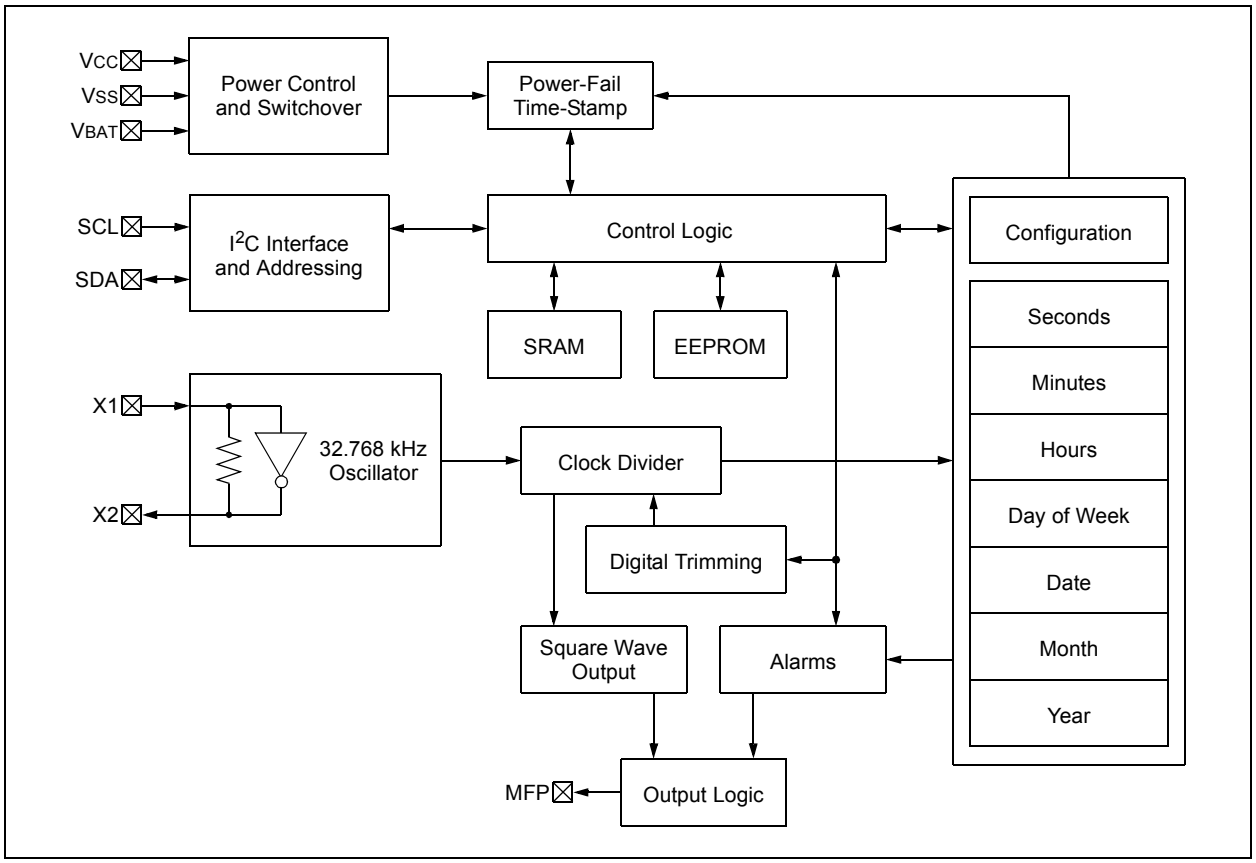


FIGURE 1-2: BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs (except SDA and SCL) w.r.t. VSS.....-0.6V to VCC +1.0V

SDA and SCL w.r.t. VSS.....-0.6V to 6.5V

Storage temperature.....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins.....≥4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	—	V	
D2	VIL	Low-Level Input Voltage	—	—	0.3 VCC	V	VCC ≥ 2.5V
			—	—	0.2 VCC	V	VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 VCC	—	—	V	**Note 1**
D4	VOL	Low-Level Output Voltage (MFP, SDA pins)	—	—	0.40	V	IOL = 3.0 mA; VCC = 4.5V IOL = 2.1 mA; VCC = 2.5V
D5	ILI	Input Leakage Current	—	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (SDA, SCL, MFP pins)	—	—	10	pF	VCC = 5.0V (**Note 1**) TA = 25°C, f = 1 MHz
D8	COSC	Oscillator Pin Capacitance (X1, X2 pins)	—	3	—	pF	**Note 1**
D9	ICCEERD	EEPROM Operating Current	—	—	400	µA	VCC = 5.5V, SCL = 400 kHz
	ICCEEWR		—	—	3	mA	VCC = 5.5V
D10	ICCREAD	SRAM/RTCC Register Operating Current	—	—	300	µA	VCC = 5.5V, SCL = 400 kHz
	ICCWRITE		—	—	400	µA	VCC = 5.5V, SCL = 400 kHz
D11	ICCDAT	VCC Data-Retention Current (oscillator off)	—	—	1	µA	SCL, SDA, VCC = 5.5V
D12	ICCT	Timekeeping Current	—	1.2	—	µA	VCC = 3.3V (**Note 1**)
D13	VTRIP	Power-Fail Switchover Voltage	1.3	1.5	1.7	V	
D14	VBAT	Backup Supply Voltage Range	1.3	—	5.5	V	**Note 1**

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): V_{CC} = +1.8V to 5.5V T_A = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
D15	I_{BATT}	Timekeeping Backup Current	—	—	850	nA	V_{BAT} = 1.3V, V_{CC} = V_{SS} **(Note 1)**
			—	925	1200	nA	V_{BAT} = 3.0V, V_{CC} = V_{SS} **(Note 1)**
			—	—	9000	nA	V_{BAT} = 5.5V, V_{CC} = V_{SS} **(Note 1)**
D16	I_{BATDAT}	V_{BAT} Data-Retention Current (oscillator off)	—	—	750	nA	V_{BAT} = 3.6V, V_{CC} = V_{SS}

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

TABLE 1-1: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	—	100	kHz	1.8V ≤ VCC < 2.5V
			—	—	400	kHz	2.5V ≤ VCC ≤ 5.5V
2	THIGH	Clock High Time	4000	—	—	ns	1.8V ≤ VCC < 2.5V
			600	—	—	ns	2.5V ≤ VCC ≤ 5.5V
3	TLOW	Clock Low Time	4700	—	—	ns	1.8V ≤ VCC < 2.5V
			1300	—	—	ns	2.5V ≤ VCC ≤ 5.5V
4	TR	SDA and SCL Rise Time (**Note 1**)	—	—	1000	ns	1.8V ≤ VCC < 2.5V
			—	—	300	ns	2.5V ≤ VCC ≤ 5.5V
5	TF	SDA and SCL Fall Time (**Note 1**)	—	—	1000	ns	1.8V ≤ VCC < 2.5V
			—	—	300	ns	2.5V ≤ VCC ≤ 5.5V
6	THD:STA	Start Condition Hold Time	4000	—	—	ns	1.8V ≤ VCC < 2.5V
			600	—	—	ns	2.5V ≤ VCC ≤ 5.5V
7	TSU:STA	Start Condition Setup Time	4700	—	—	ns	1.8V ≤ VCC < 2.5V
			600	—	—	ns	2.5V ≤ VCC ≤ 5.5V
8	THD:DAT	Data Input Hold Time	0	—	—	ns	**Note 2**
9	TSU:DAT	Data Input Setup Time	250	—	—	ns	1.8V ≤ VCC < 2.5V
			100	—	—	ns	2.5V ≤ VCC ≤ 5.5V
10	TSU:STO	Stop Condition Setup Time	4000	—	—	ns	1.8V ≤ VCC < 2.5V
			600	—	—	ns	2.5V ≤ VCC ≤ 5.5V
11	TAA	Output Valid from Clock	—	—	3500	ns	1.8V ≤ VCC < 2.5V
			—	—	900	ns	2.5V ≤ VCC ≤ 5.5V
12	TBUF	Bus Free Time: Bus time must be free before a new transmission can start	4700	—	—	ns	1.8V ≤ VCC < 2.5V
			1300	—	—	ns	2.5V ≤ VCC ≤ 5.5V
13	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	—	50	ns	**Note 1**
14	TWC	Write Cycle Time (byte or page)	—	—	5	ms	
15	TFVCC	VCC Fall Time	300	—	—	µs	**Note 1**
16	TRVCC	VCC Rise Time	0	—	—	µs	**Note 1**
17	FOSC	Oscillator Frequency	—	32.768	—	kHz	
18	TOSF	Oscillator Timeout Period	1	—	—	ms	**Note 1**
19		Endurance	1M	—	—	cycles	Page Mode, 25°C,VCC = 5.5V (**Note 3**)

Note 1: Not 100% tested.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: This parameter is not tested but ensured by characterization.

FIGURE 1-3: I²C BUS TIMING DATA

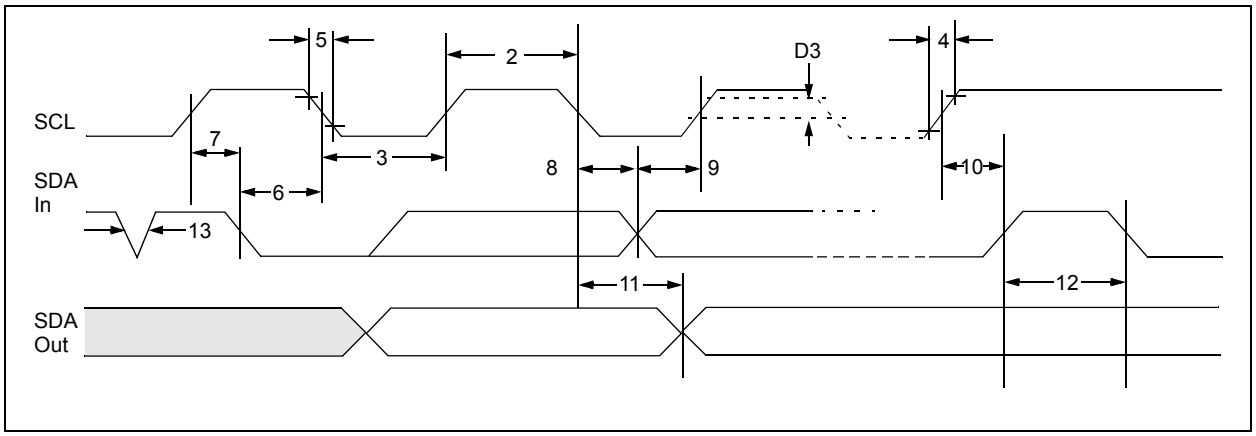
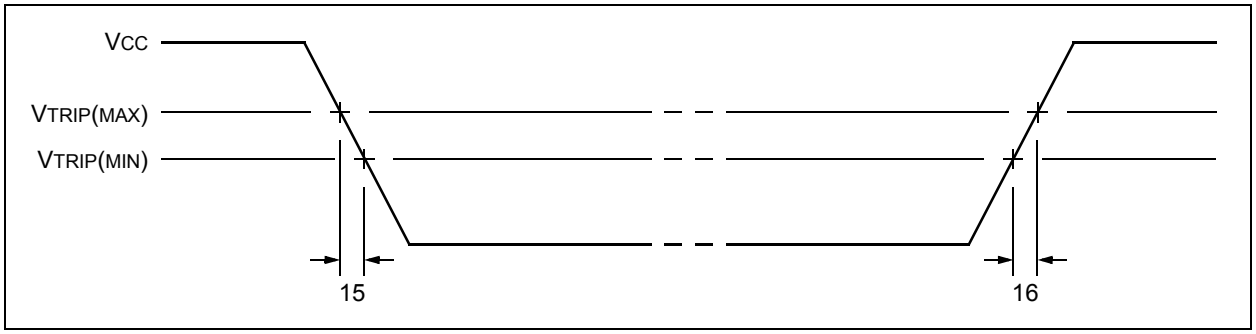


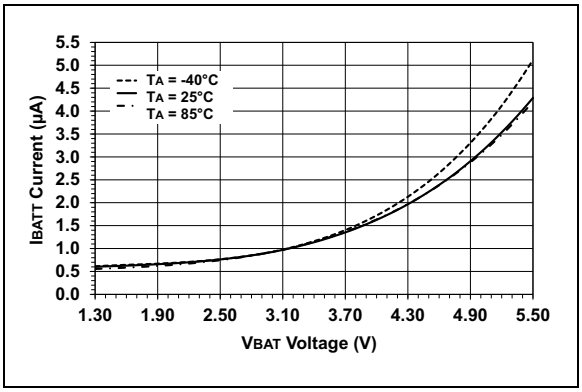
FIGURE 1-4: POWER SUPPLY TRANSITION TIMING



2.0 TYPICAL PERFORMANCE CURVE

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data represented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 2-1: TIMEKEEPING BACKUP CURRENT VS. BACKUP SUPPLY VOLTAGE



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	8-pin SOIC	8-pin MSOP	8-pin TSSOP	8-pin TDFN	Function
X1	1	1	1	1	Quartz Crystal Input, External Oscillator Input
X2	2	2	2	2	Quartz Crystal Output
VBAT	3	3	3	3	Battery Backup Supply Input
VSS	4	4	4	4	Ground
SDA	5	5	5	5	Bidirectional Serial Data (I^2C)
SCL	6	6	6	6	Serial Clock (I^2C)
MFP	7	7	7	7	Multifunction Pin
VCC	8	8	8	8	Primary Power Supply

Note: Exposed pad on TFDN can be connected to VSS or left floating.

3.1 Oscillator Input/Output (X1, X2)

These pins are used as the connections for an external 32.768 kHz quartz crystal and load capacitors. X1 is the crystal oscillator input and X2 is the output. The MCP7940X is designed to allow for the use of external load capacitors in order to provide additional flexibility when choosing external crystals. The MCP7940X is optimized for crystals with a specified load capacitance of 6-9 pF.

X1 also serves as the external clock input when the MCP7940X is configured to use an external oscillator.

3.2 Backup Supply (VBAT)

This is the input for a backup supply to maintain the RTCC and SRAM registers during the time when VCC is unavailable.

If the battery backup feature is not being used, the VBAT pin should be connected to VSS.

3.3 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typically 10 kΩ for 100 kHz, 2 kΩ for 400 kHz). For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

3.4 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

3.5 Multifunction Pin (MFP)

This is an output pin used for the alarm and square wave output functions. It can also serve as a general purpose output pin by controlling the OUT bit in the CONTROL register.

The MFP is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ). This pin may be left floating if not used.

4.0 I²C BUS CHARACTERISTICS

4.1 I²C Interface

The MCP7940X supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the MCP7940X works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.1.1 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1.1.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note 1:	The MCP7940X does not generate an Acknowledge bit in response to an EEPROM control byte if an internal EEPROM programming cycle is in progress, but the SRAM and RTCC registers can still be accessed.
2:	The I²C interface is disabled while operating from the backup power supply.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (MCP7940X) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

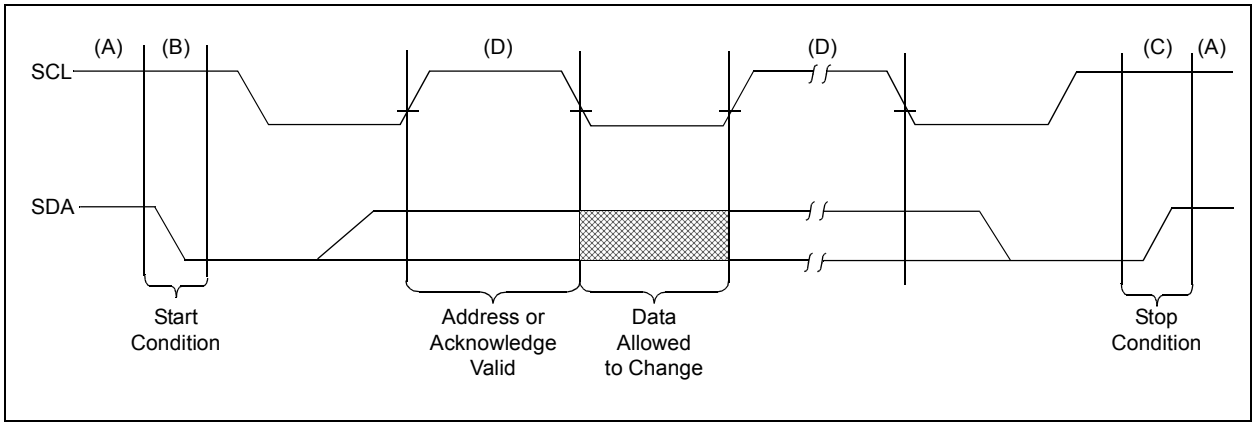
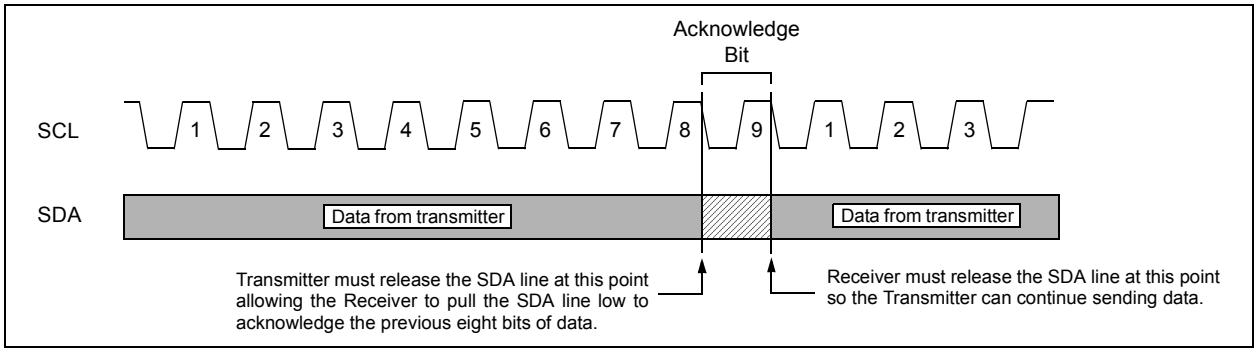


FIGURE 4-2: ACKNOWLEDGE TIMING



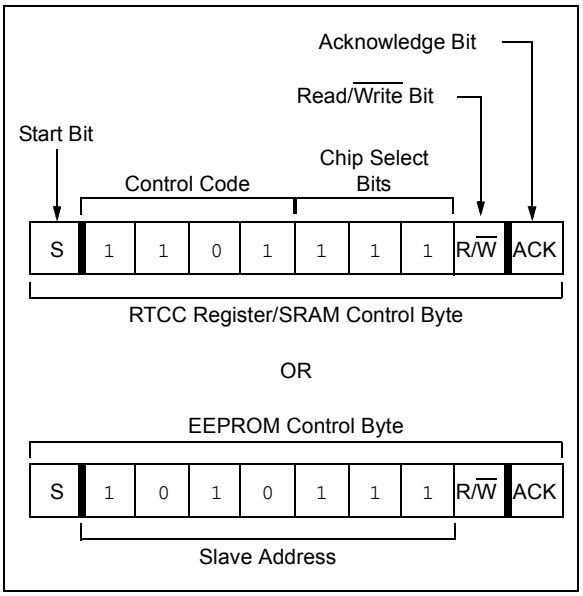
4.1.2 DEVICE ADDRESSING

The control byte is the first byte received following the Start condition from the master device (Figure 4-3). The control byte begins with a 4-bit control code. For the MCP7940X, this is set as '1010' for EEPROM read and write operations, and '1101' for SRAM/RTCC register read and write operations. The next three bits are non-configurable Chip Select bits that must always be set to '1'.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected.

The combination of the 4-bit control code and the three Chip Select bits is called the slave address. Upon receiving a valid slave address, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the MCP7940X will select a read or a write operation.

FIGURE 4-3: CONTROL BYTE FORMAT



5.0 FUNCTIONAL DESCRIPTION

The MCP7940X is a highly-integrated Real-Time Clock/Calendar (RTCC). Using an on-board, low-power oscillator, the current time is maintained in seconds, minutes, hours, day of week, date, month, and year. The MCP7940X also features 64 bytes of general purpose SRAM and eight bytes of protected EEPROM. Two alarm modules allow interrupts to be generated at specific times with flexible comparison options. Digital trimming can be used to compensate for inaccuracies inherent with crystals. Using the backup supply input and an integrated power switch, the MCP7940X will automatically switch to backup power when primary power is unavailable, allowing the current time and the SRAM contents to be maintained. The time-stamp module captures the time when primary power is lost and when it is restored.

The RTCC configuration and status registers are used to access all of the modules featured on the MCP7940X.

5.1 Memory Organization

The MCP7940X features three different blocks of memory: the RTCC registers, general purpose SRAM, and protected EEPROM. The RTCC registers and SRAM share the same address space, accessed through the '1101111X' control byte. The protected EEPROM is in a separate address space and is accessed using the '1010111X' control byte (Figure 5-1). Unused locations are not accessible. The MCP7940X will not acknowledge if the address is out of range, as shown in the shaded region of the memory map in Figure 5-1.

The RTCC registers are contained in addresses 0x00-0x1F. Table 5-1 shows the detailed RTCC register map. There are 64 bytes of user-accessible SRAM, located in the address range 0x20-0x5F. The SRAM is a separate block from the RTCC registers. All RTCC registers and SRAM locations are maintained while operating from backup power.

The protected EEPROM section is located in addresses 0xF0-0xF7.

FIGURE 5-1: MEMORY MAP

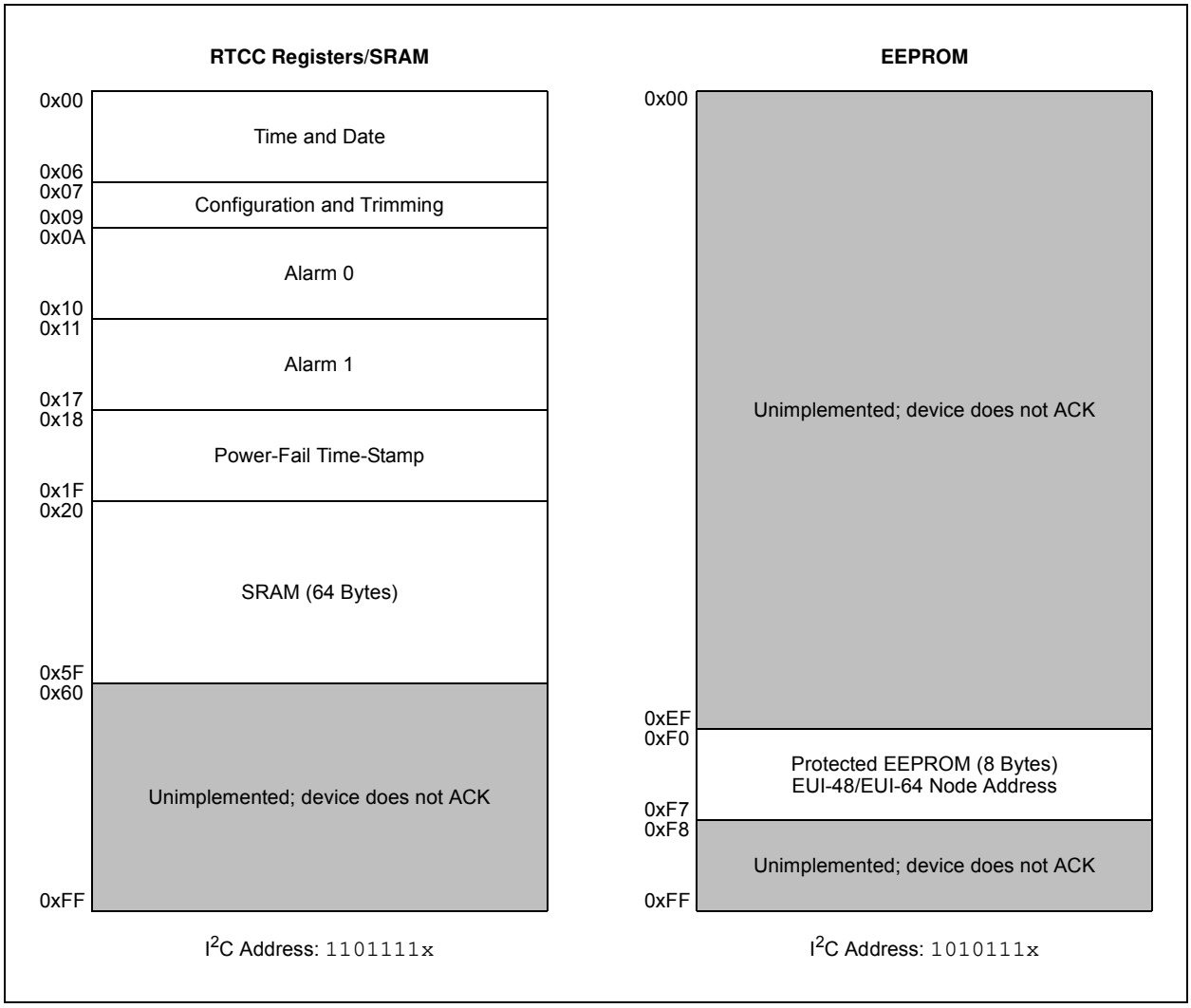


TABLE 5-1: DETAILED RTCC REGISTER MAP

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Section 5.3 "Timekeeping"									
00h	RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
01h	RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
02h	RTCHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
03h	RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
04h	RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
05h	RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
06h	RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
07h	CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
08h	OSCTRIM	SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
09h	EEUNLOCK	Protected EEPROM Unlock Register (not a physical register)							
Section 5.4 "Alarms"									
0Ah	ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
0Bh	ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
0Ch	ALM0HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
0Dh	ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0
0Eh	ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
0Fh	ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
10h	Reserved	Reserved – Do not use							
Section 5.4 "Alarms"									
11h	ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
12h	ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
13h	ALM1HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
14h	ALM1WKDAY	ALMPOL(3)	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0
15h	ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
16h	ALM1MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
17h	Reserved	Reserved – Do not use							
Section 5.7.1 "Power-Fail Time-Stamp"									
18h	PWRDNMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
19h	PWRDNHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Ah	PWRDNDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Bh	PWRDNMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
Section 5.7.1 "Power-Fail Time-Stamp"									
1Ch	PWRUPMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
1Dh	PWRUPHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Eh	PWRUPDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Fh	PWRUPMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0

Note 1: Grey areas are unimplemented.

2: The 12/$\overline{24}$ bits in the ALMxHOUR registers are read-only and reflect the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

3: The ALMPOL bit in the ALM1WKDAY register is read-only and reflects the value of the ALMPOL bit in the ALM0WKDAY register.

5.2 Oscillator Configuration

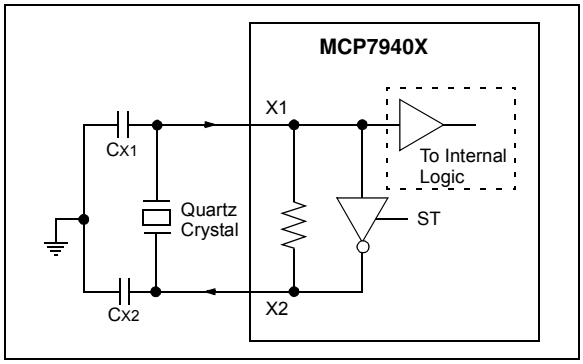
The MCP7940X can be operated in two different oscillator configurations: using an external crystal or using an external clock input.

5.2.1 EXTERNAL CRYSTAL

The crystal oscillator circuit on the MCP7940X is designed to operate with a standard 32.768 kHz tuning fork crystal and matching external load capacitors. By using external load capacitors, the MCP7940X allows for a wide selection of crystals. Suitable crystals have a load capacitance (C_L) of 6-9 pF. Crystals with a load capacitance of 12.5 pF are not recommended.

Figure 5-2 shows the pin connections when using an external crystal.

FIGURE 5-2: CRYSTAL OPERATION



Note 1:	The ST bit must be set to enable the crystal oscillator circuit.
2:	Always verify oscillator performance over the voltage and temperature range that is expected for the application.

5.2.1.1 Choosing Load Capacitors

C_L is the effective load capacitance as seen by the crystal, and includes the physical load capacitors, pin capacitance, and stray board capacitance. Equation 5-1 can be used to calculate C_L.

C_{X1} and C_{X2} are the external load capacitors. They must be chosen to match the selected crystal's specified load capacitance.

Note:	If the load capacitance is not correctly matched to the chosen crystal's specified value, the crystal may give a frequency outside of the crystal manufacturer's specifications.

EQUATION 5-1: LOAD CAPACITANCE CALCULATION

$$C_L = \frac{C_{X1} \times C_{X2}}{C_{X1} + C_{X2}} + C_{STRAY}$$

Where:

C_L = Effective load capacitance
C_{X1} = Capacitor value on X1 + C_{OSC}
C_{X2} = Capacitor value on X2 + C_{OSC}
C_{STRAY} = PCB stray capacitance

5.2.1.2 Layout Considerations

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

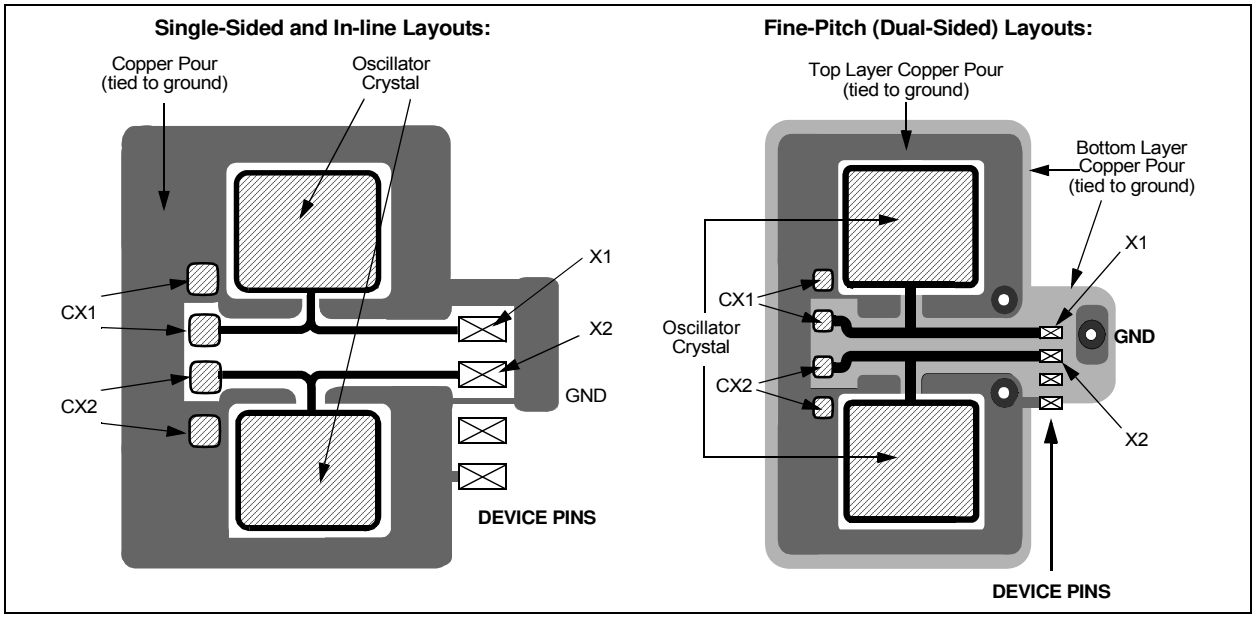
Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to V_{SS}. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 5-3. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN1365, "Recommended Usage of Microchip Serial RTCC Devices"*
- *AN1519, "Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"*

FIGURE 5-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

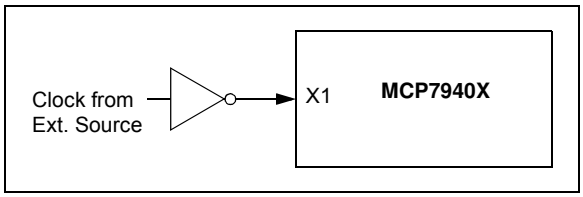


5.2.2 EXTERNAL CLOCK INPUT

A 32.768 kHz external clock source can be connected to the X1 pin (Figure 5-4). When using this configuration, the X2 pin should be left floating.

Note:	The EXTOSC bit must be set to enable an external clock source.

FIGURE 5-4: EXTERNAL CLOCK INPUT OPERATION



5.2.3 OSCILLATOR FAILURE STATUS

The MCP7940X features an oscillator failure flag, OSCRUN, that indicates whether or not the oscillator is running. The OSCRUN bit is automatically set after 32 oscillator cycles are detected. If no oscillator cycles are detected for more than TOSF, then the OSCRUN bit is automatically cleared (Figure 5-5). This can occur if the oscillator is stopped by clearing the ST bit or due to oscillator failure.

FIGURE 5-5: OSCILLATOR FAILURE STATUS TIMING DIAGRAM

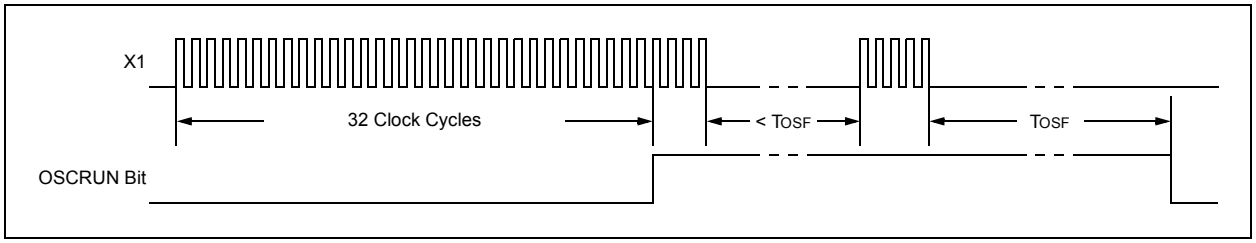


TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH OSCILLATOR CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	16
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	18
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	26

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by oscillator configuration.

5.3 Timekeeping

The MCP7940X maintains the current time and date using an external 32.768 kHz crystal or clock source. Separate registers are used for tracking seconds, minutes, hours, day of week, date, month, and year. The MCP7940X automatically adjusts for months with less than 31 days and compensates for leap years from 2001 to 2399. The year is stored as a two-digit value.

Both 12-hour and 24-hour time formats are supported and are selected using the 12/$\overline{24}$ bit.

The day of week value counts from 1 to 7, increments at midnight, and the representation is user-defined (i.e., the MCP7940X does not require 1 to equal Sunday, etc.).

All time and date values are stored in the registers as binary-coded decimal (BCD) values. The MCP7940X will continue to maintain the time and date while operating off the backup supply.

When reading from the timekeeping registers, the registers are buffered to prevent errors due to rollover of counters. The following events cause the buffers to be updated:

- When a read is initiated from the RTCC registers (addresses 0x00 to 0x1F)
- During an RTCC register read operation, when the register address rolls over from 0x1F to 0x00

The timekeeping registers should be read in a single operation to utilize the on-board buffers and avoid rollover issues.

Note 1: Loading invalid values into the time and date registers will result in undefined operation.

2: To avoid rollover issues when loading new time and date values, the oscillator/clock input should be disabled by clearing the ST bit for external crystal mode and the EXTOSC bit for external clock input mode. After waiting for the OSCRUN bit to clear, the new values can be loaded and the ST or EXTOSC bit can then be re-enabled.

5.3.1 DIGIT CARRY RULES

The following list explains which timer values cause a digit carry when there is a rollover:

- Time of day: from 11:59:59 PM to 12:00:00 AM (12-hour mode) or 23:59:59 to 00:00:00 (24-hour mode), with a carry to the Date and Weekday fields
- Date: carries to the Month field according to Table 5-3
- Weekday: from 7 to 1 with no carry
- Month: from 12/31 to 01/01 with a carry to the Year field
- Year: from 99 to 00 with no carry

TABLE 5-3: DAY TO MONTH ROLLOVER SCHEDULE

Month	Name	Maximum Date
01	January	31
02	February	28 or 29(1)
03	March	31
04	April	30
05	May	31
06	June	30
07	July	31
08	August	31
09	September	30
10	October	31
11	November	30
12	December	31

Note 1: 29 during leap years, otherwise 28.

REGISTER 5-1: RTCSEC: TIMEKEEPING SECONDS VALUE REGISTER (ADDRESS 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **ST:** Start Oscillator bit
1 = Oscillator enabled
0 = Oscillator disabled

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second's Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second's Ones Digit
Contains a value from 0 to 9

REGISTER 5-2: RTCMIN: TIMEKEEPING MINUTES VALUE REGISTER (ADDRESS 0x01)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit
Contains a value from 0 to 9

REGISTER 5-3: RTCHOUR: TIMEKEEPING HOURS VALUE REGISTER (ADDRESS 0x02)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

REGISTER 5-4: RTCWKDAY: TIMEKEEPING WEEKDAY VALUE REGISTER (ADDRESS 0x03)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OSCRUN:** Oscillator Status bit
1 = Oscillator is enabled and running
0 = Oscillator has stopped or has been disabled

bit 4 **PWRFAIL:** Power Failure Status bit(1,2)
1 = Primary power was lost and the power-fail time-stamp registers have been loaded (must be cleared in software). Clearing this bit resets the power-fail time-stamp registers to '0'.
0 = Primary power has not been lost

bit 3 **VBATEN:** External Battery Backup Supply (V_{BAT}) Enable bit
1 = V_{BAT} input is enabled
0 = V_{BAT} input is disabled

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day of Week
Contains a value from 1 to 7. The representation is user-defined.

Note 1: The PWRFAIL bit must be cleared to log new time-stamp data. This is to ensure previous time-stamp data is not lost.

2: The PWRFAIL bit cannot be written to a '1' in software. Writing to the RTCWKDAY register will always clear the PWRFAIL bit.

REGISTER 5-5: RTCDATE: TIMEKEEPING DATE VALUE REGISTER (ADDRESS 0x04)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 5-6: RTCMTH: TIMEKEEPING MONTH VALUE REGISTER (ADDRESS 0x05)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **LPYR:** Leap Year bit
1 = Year is a leap year
0 = Year is not a leap year

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

REGISTER 5-7: RTCYEAR: TIMEKEEPING YEAR VALUE REGISTER (ADDRESS 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **YRTEN<3:0>:** Binary-Coded Decimal Value of Year's Tens Digit
Contains a value from 0 to 9

bit 3-0 **YRONE<3:0>:** Binary-Coded Decimal Value of Year's Ones Digit
Contains a value from 0 to 9

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMEKEEPING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	16
RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	16
RTCHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	17
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	18
RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	18
RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	19
RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	19

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in timekeeping.

5.4 Alarms

The MCP7940X features two independent alarms. Each alarm can be used to either generate an interrupt at a specific time in the future, or to generate a periodic interrupt every minute, hour, day, day of week, or month.

There is a separate interrupt flag, ALMxIF, for each alarm. The interrupt flags are set by hardware when the chosen alarm mask condition matches (Table 5-5). The interrupt flags must be cleared in software.

If either alarm module is enabled by setting the corresponding ALMxEN bit in the CONTROL register, and if the square wave clock output is disabled (SQWEN = 0), then the MFP will operate in alarm interrupt output mode. Refer to **Section 5.5 "Output Configurations"** for details. The alarm interrupt output is available while operating from the backup power supply.

Both Alarm0 and Alarm1 offer identical operation. All time and date values are stored in the registers as binary-coded decimal (BCD) values.

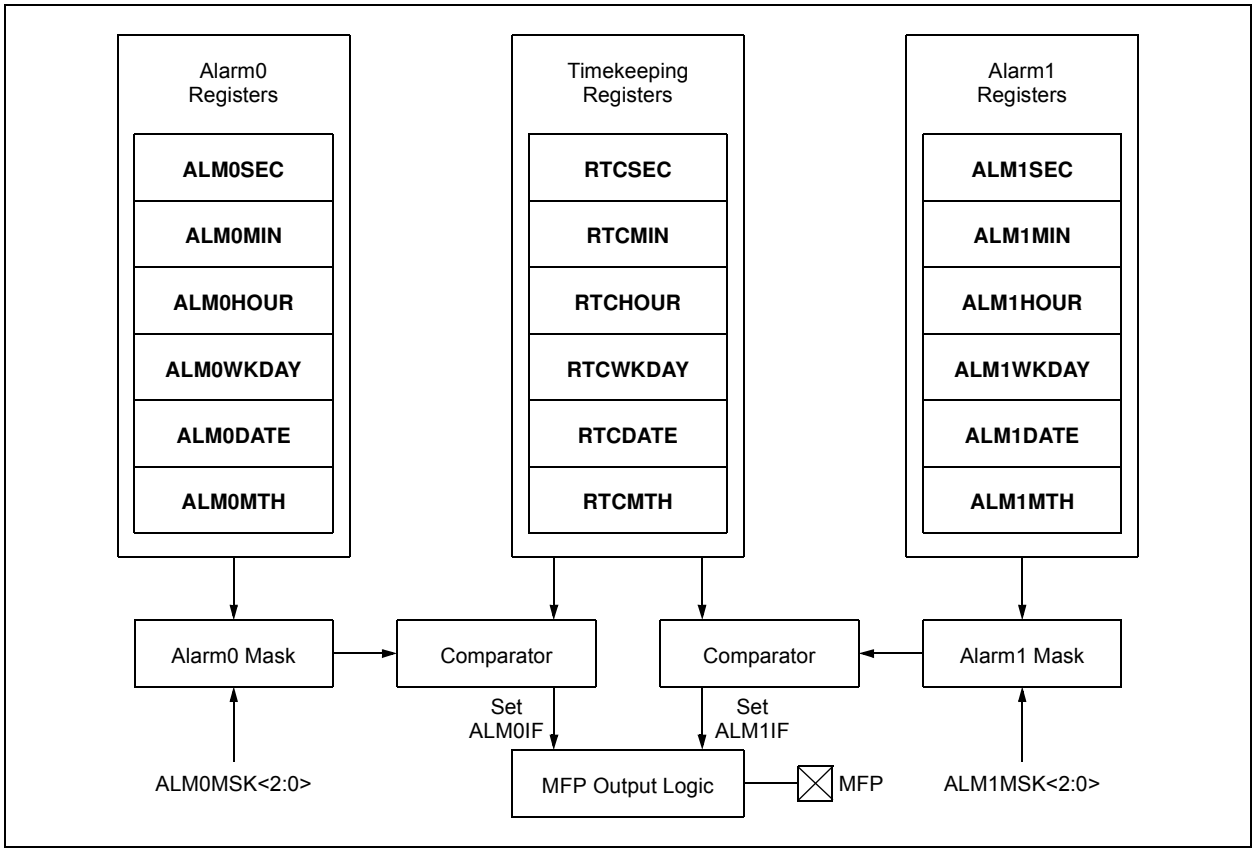
Note:	Throughout this section, references to the register and bit names for the Alarm modules are referred to generically by the use of 'x' in place of the specific module number. Thus, "ALMxSEC" might refer to the seconds register for Alarm0 or Alarm1.

TABLE 5-5: ALARM MASKS

ALMxMSK<2:0>	Alarm Asserts on Match of
000	Seconds
001	Minutes
010	Hours
011	Day of Week
100	Date
101	Reserved
110	Reserved
111	Seconds, Minutes, Hours, Day of Week, Date, and Month

Note 1:	The alarm interrupt flags must be cleared by the user. If a flag is cleared while the corresponding alarm condition still matches, the flag will be set again, generating another interrupt.
2:	Loading invalid values into the alarm registers will result in undefined operation.

FIGURE 5-6: ALARM BLOCK DIAGRAM



5.4.1 CONFIGURING THE ALARM

In order to configure the alarm modules, the following steps need to be performed:

1. Load the timekeeping registers and enable the oscillator
2. Configure the ALMxMSK<2:0> bits to select the desired alarm mask
3. Set or clear the ALMPOL bit according to the desired output polarity
4. Ensure the ALMxIF flag is cleared
5. Based on the selected alarm mask, load the alarm match value into the appropriate register(s)
6. Enable the alarm module by setting the ALMxEN bit

REGISTER 5-8: ALMxSEC: ALARM0/1 SECONDS VALUE REGISTER (ADDRESSES 0x0A/0x11)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-9: ALMxMIN: ALARM0/1 MINUTES VALUE REGISTER (ADDRESSES 0x0B/0x12)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-10: ALMxHOUR: ALARM0/1 HOURS VALUE REGISTER (ADDRESSES 0x0C/0x13)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit[1]
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit[1]
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

Note 1: This bit is read-only and reflects the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

REGISTER 5-11: ALMxWKDAY: ALARM0/1 WEEKDAY VALUE REGISTER (ADDRESSES 0x0D/0x14)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ALMPOL	ALMxMSK2	ALMxMSK1	ALMxMSK0	ALMxIF	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **ALMPOL:** Alarm Interrupt Output Polarity bit
1 = Asserted output state of MFP is a logic high level
0 = Asserted output state of MFP is a logic low level

bit 6-4 **ALMxMSK<2:0>:** Alarm Mask bits
000 = Seconds match
001 = Minutes match
010 = Hours match (logic takes into account 12-/24-hour operation)
011 = Day of week match
100 = Date match
101 = Reserved; do not use
110 = Reserved; do not use
111 = Seconds, Minutes, Hour, Day of Week, Date and Month

bit 3 **ALMxIF:** Alarm Interrupt Flag bit(1,2)
1 = Alarm match occurred (must be cleared in software)
0 = Alarm match did not occur

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits
Contains a value from 1 to 7. The representation is user-defined.

Note 1: If a match condition still exists when this bit is cleared, it will be set again automatically.
2: The ALMxIF bit cannot be written to a 1 in software. Writing to the ALMxWKDAY register will always clear the ALMxIF bit.

REGISTER 5-12: ALMxDATE: ALARM0/1 DATE VALUE REGISTER (ADDRESSES 0x0E/0x15)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 5-13: ALMxMTH: ALARM0/1 MONTH VALUE REGISTER (ADDRESSES 0x0F/0x16)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH ALARMS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	21
ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	21
ALM0HOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	22
ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0	23
ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	23
ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	24
ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	21
ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	21
ALM1HOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	22
ALM1WKDAY	ALMPOL	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0	23
ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	23
ALM1MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	24
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	26

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by alarms.

5.5 Output Configurations

The MCP7940X features Square Wave Clock Output, Alarm Interrupt Output, and General Purpose Output modes. All of the output functions are multiplexed onto MFP according to Table 5-7.

Only the alarm interrupt outputs are available while operating from the backup power supply. If none of the output functions are being used, the MFP can safely be left floating.

Note: The MFP is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ).

TABLE 5-7: MFP OUTPUT MODES

SQWEN	ALM0EN	ALM1EN	Mode
0	0	0	General Purpose Output
0	1	0	Alarm Interrupt Output
0	0	1	
0	1	1	
1	x	x	Square Wave Clock Output

FIGURE 5-7: MFP OUTPUT BLOCK DIAGRAM