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MCP795WXX/MCP795BXX

SPI Real-Time Clock Calendar with Enhanced Features and Battery Switchover

Device Selection Table

Part Number	32 kHz Boot-up	SRAM (Bytes)	EEPROM (Kbits)	Unique ID
MCP795W20	No	64	2	Blank
MCP795W10	No	64	1	Blank
MCP795W21	No	64	2	EUI-48™
MCP795W11	No	64	1	EUI-48™
MCP795W22	No	64	2	EUI-64™
MCP795W12	No	64	1	EUI-64™
MCP795B20	Yes	64	2	Blank
MCP795B10	Yes	64	1	Blank
MCP795B21	Yes	64	2	EUI-48™
MCP795B11	Yes	64	1	EUI-48™
MCP795B22	Yes	64	2	EUI-64™
MCP795B12	Yes	64	1	EUI-64™
Note:	Watchdog Timer and Event Detects in all devices.			

Timekeeping Features:

- Real-Time Clock/Calendar:
  - Hours, Minutes, Seconds, Hundredth of Seconds, Day of Week, Month, Year, Leap Year
- Crystal Oscillator requires External 32,768 kHz Tuning Fork Crystal and Load Capacitors.
- Clock Out Function:
  - 1Hz, 4.096 kHz, 8.192 kHz, 32.768 kHz
- 32 kHz Boot-up Clock at Power-up (MCP795BXX)
- 2 Programmable Alarms – Supports $\overline{IRQ}$ or $\overline{WDO}$
- Programmable open drain output – Alarm or Interrupt
- On-Chip Digital Trimming/Calibration:
  - +/- 255 PPM range in 1 PPM steps
- Power-Fail Time-Stamp @ Battery Switchover:
  - Logs time when V_{CC} fails and V_{CC} is restored

Low-Power Features:

- Wide Operating Voltage:
  - V_{CC}: 1.8V to 5.5V
  - V_{BAT}: 1.3V to 5.5V
- Low Operating Current:
  - V_{CC} Standby Current < 1uA @ 3V
  - V_{BAT} Timekeeping Current: <700nA @ 1.8V
- Automatic Battery Switchover from V_{CC} to V_{BAT}:
  - Backup power for timekeeping and SRAM retention

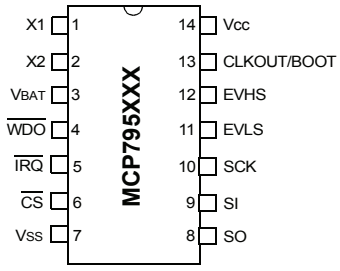
User Memory:

- 64-Byte Battery-Backed SRAM
- 2 Kbit and 1 Kbit EEPROM Memory:
  - Software block write-protect (¼, ½, or entire array)
  - Write Page mode (up to 8 bytes)
  - Endurance: 1M erase/write cycles
- 128-Bit Unique ID in Protected Area of EEPROM:
  - Available blank or preprogrammed
  - EUI-48™ or EUI-64™ MAC address
  - Unlock sequence for user programming

Enhanced Features:

- SPI Clock Speed up to 10 MHz
- Programmable Watchdog Timer:
  - Dedicated watchdog output pin
  - Dual retrigger using SPI bus or EVHS digital input
- Dual Configurable Event Detect Inputs:
  - High-Speed Digital Event Detect (EVHS) with pulse count for 1st, 4th,16th or 32nd event
  - Low-Speed Event Detect (EVLS) with programmable debounce delays of 31 msec and 500 msec
  - Edge triggered (rising or falling)
  - Operates from V_{CC} or V_{BAT}
- Operating Temperature Ranges:
  - Industrial (I Temp): -40°C to +85°C.
- Packages include 14-Lead SOIC and TSSOP

SOIC/TSSOP



Note: MCP795XXX is used in this document as a generic part number for the MCP795WXX, MCP795BXX devices.

Description:

The MCP795XXX is a low-power Real-Time Clock/ Calendar (RTCC) that uses digital trimming compensation for an accurate clock/calendar, an interrupt output to support alarms and events, a power sense circuit that automatically switches to the backup supply, non-volatile memory for safe data storage and several enhanced features that support system requirements.

Along with a low-cost 32,768 kHz crystal, this RTCC tracks time using several internal registers and then communicates the data over a 10 MHz SPI bus that is fast enough to support a programmable millisecond alarm.

The device is fully accessible through the serial interface, while VCC is between 1.8V and 5.5V, but can operate down to 1.3V through the backup supply connected to the VBAT input for timekeeping and SRAM retention only.

As part of the power sense circuit, a time saver function is implemented to store the time when main power is lost and again, when power is restored to log the duration of a power failure.

Along with the onboard serial EEPROM and battery-backed SRAM, a 128-bit protected space is available for a unique ID. This space can be ordered preprogrammed with a MAC address, or blank for the user to program.

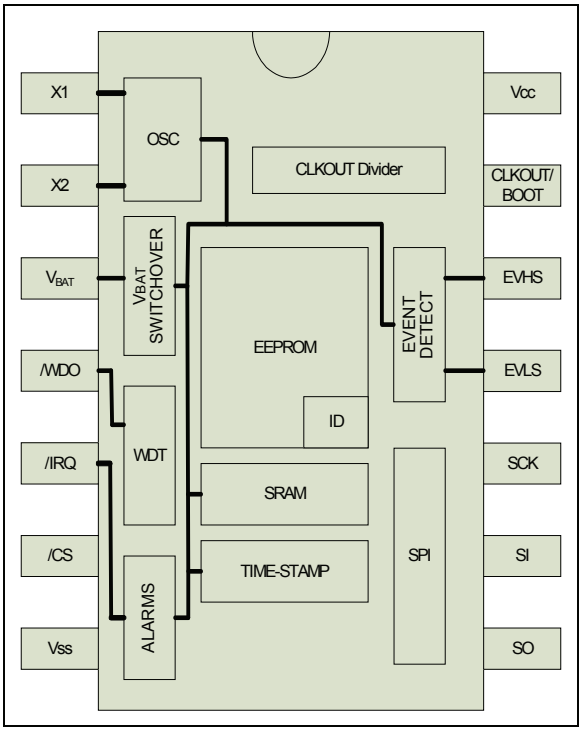
This clock/calendar automatically adjusts for months with fewer than 31 days including corrections for leap years. The clock operates in either 24-hour or 12-hour format with AM/PM indicator and settable alarm(s).

Using the external crystal, the CLKOUT pin can be set to generate a number of output frequencies. In addition, the MCP795BXX devices support a 32 kHz clock output at power-up on the CLKOUT/BOOT pin by using the same crystal driving the RTCC device.

For versatility, a digital event detect with a programmable pulse count can identify the 1st, 4th, 16th or 32nd pulse before sending an interrupt. A second event detect with built-in debounce input filter was also implemented to support noisy mechanical switches.

Since many microcontrollers do not have an integrated Watchdog Timer, this peripheral has been implemented in the RTCC. For many applications, this function must be performed outside the microcontroller for increased robustness.

FIGURE 1-1: BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to +6.5V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +85°C

ESD protection on all pins.....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TAMB = -40°C to +85°C VCC = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-level input voltage	.7 VCC	VCC+1	V	
D002	VIL1	Low-level input voltage	-0.3	0.3VCC	V	VCC ≥ 2.5V
D003	VIL2		-0.3	0.2VCC	V	VCC < 2.5V
D004	VOL	Low-level output voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA
D007	ILI	Input leakage current		±1	µA	$\overline{CS}$ = VCC, VIN = VSS TO VCC
D008	ILO	Output leakage current		±1	µA	$\overline{CS}$ = VCC, VOUT = VSS TO VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz VCC = 5.0V (**Note 1**)
D010	ICC Read	Operating Current	—	3	mA	VCC = 5.5V; FCLK = 10.0 MHz SO = Open
D011	IDD write	Write Current	—	5	mA	VCC = 5.5V
D012	IBAT	VBAT Current	—	700	nA	VBAT = 1.8V @ 25°C (**Note 2**)
D013	VTRIP	VBAT Change Over	1.3	1.7	V	1.5V typical at TAMB = 25°C
D014	VCCFT	VCC Fall Time	300		µs	From VTRIP (max) to VTRIP (min)
D015	VCCRT	VCC Rise Time	0		µs	From VTRIP (min) to VTRIP (max)
D016	VBAT	VBAT Voltage Range	1.3	5.5	V	—
D017	ICCS	Standby Current	—	1	µA	—

Note 1: This parameter is periodically sampled and not 100% tested.

2: With oscillator running.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T_{AMB} = -40°C to +85°C V_{CC} = 1.8V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	— — —	10 5 3	MHz MHz MHz	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	—
5	Tsu	Data Setup Time	10 20 30	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
6	THD	Data Hold Time	20 40 50	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
7	TR	CLK Rise Time	—	100	ns	**(Note 1)**
8	TF	CLK Fall Time	—	100	ns	**(Note 1)**
9	THI	Clock High Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
10	TLO	Clock Low Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
11	TCLD	Clock Delay Time	50	—	ns	—
12	TCLE	Clock Enable Time	50	—	ns	—
13	TV	Output Valid from Clock Low	— — —	50 100 160	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
14	THO	Output Hold Time	0	—	ns	(**Note 1**)
15	TDIS	Output Disable Time	— — —	40 80 160	ns ns ns	4.5V ≤ Vcc ≤ 5.5V (**Note 1**) 2.5V ≤ Vcc < 4.5V (**Note 1**) 1.8V ≤ Vcc < 2.5V (**Note 1**)
16	TWC	Internal Write Cycle Time	—	5	ms	**(Note 3)**
17	—	Endurance	1,000,000	—	E/W Cycles	**(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

3: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

FIGURE 1-1: SERIAL INPUT TIMING

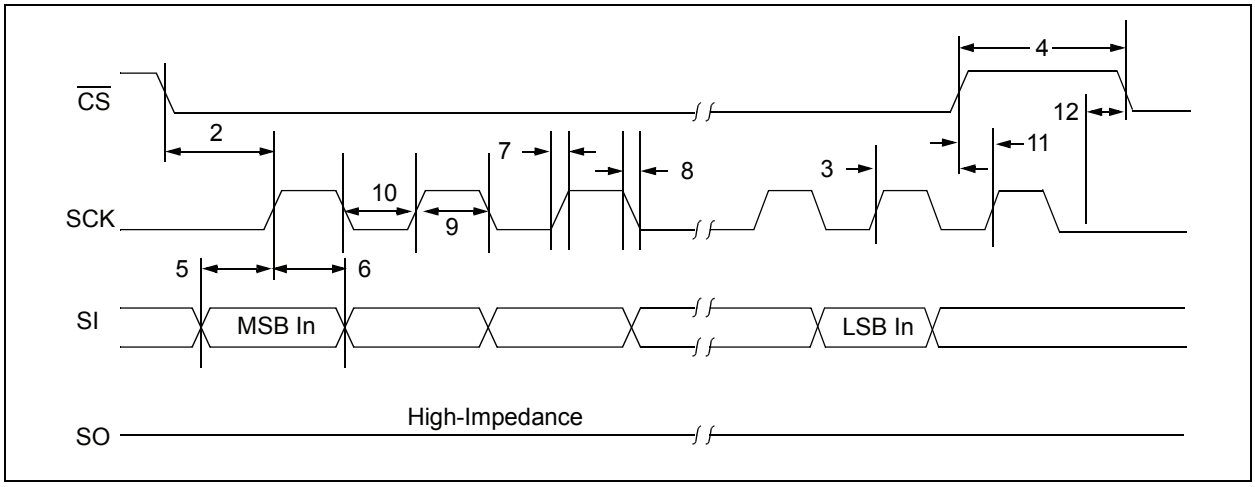
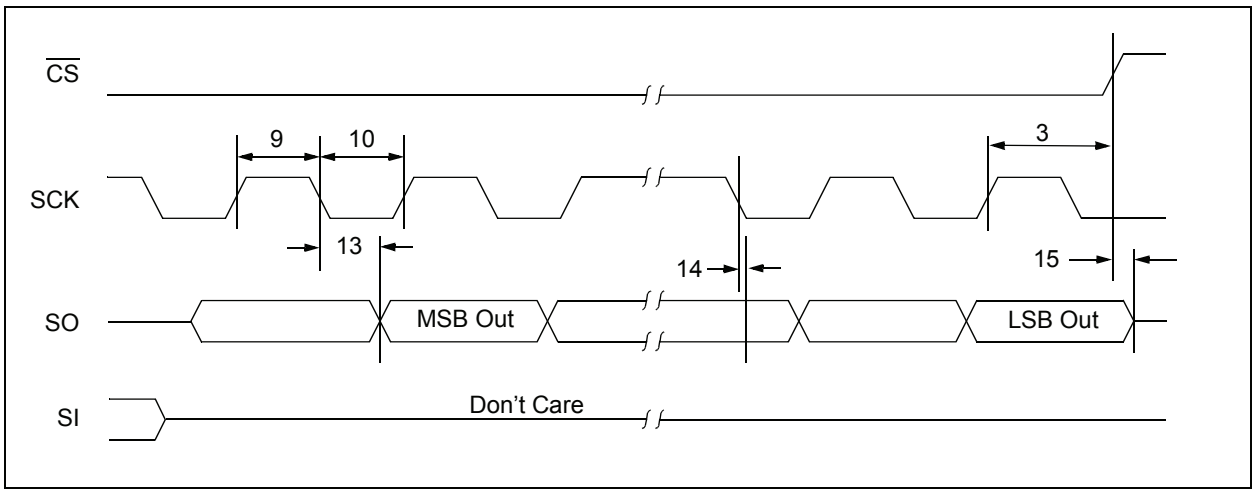


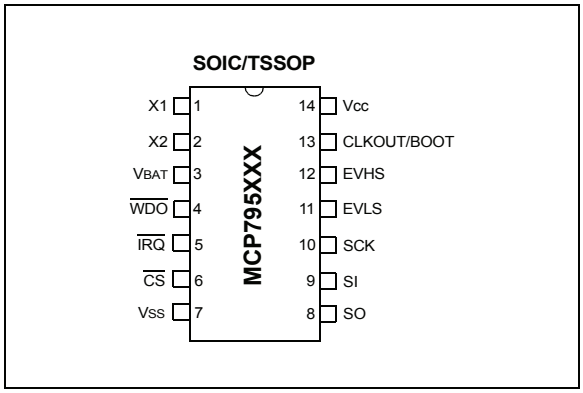
FIGURE 1-2: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

FIGURE 2-1: DEVICE PINOUTS



2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the MCP795XXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Watchdog Output ($\overline{WDO}$)

This pin is a hardware open drain from the internal watchdog circuit. This pin requires an external pull-up to VCC. When a watchdog overflow occurs the onboard N-Channel will pulse this pin low. The pulse duration is user selectable (Address 0x0A:4). This pin has a maximum sink current of 10mA.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the MCP795XXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Interrupt Output ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is shared with the onboard event detect and the Alarms. This pin requires an external pull-up to VCC or VBAT. The onboard N-Channel will pull the pin low during an event detection or an alarm. The pin remains low until such time that the interrupt flag in the register is cleared by software. This pin has a maximum sink current of 10mA.

2.7 X1, X2

The X1 and X2 pins connect to the onboard oscillator block. X1 is the input to the module and X2 is the output of the module. The device can be run from an external CMOS signal by feeding into the X1 pin. If driving X1 the X2 pin should be a No Connect.

2.8 VBAT

The VBAT pin is a secondary supply input to maintain the Clock and SRAM contents when VCC is removed.

2.9 CLKOUT/BOOT

The CLKOUT is a push-pull output that can be used to generate a squarewave or is used for the boot-up clock output at power-up. Please refer to **Section 9.1.2, Clockout Function** for more details.

2.10 EVHS and EVLS

The EVHS and EVLS are inputs for the High and Low Speed Event Detection circuit.

TABLE 2-1: PIN DESCRIPTIONS

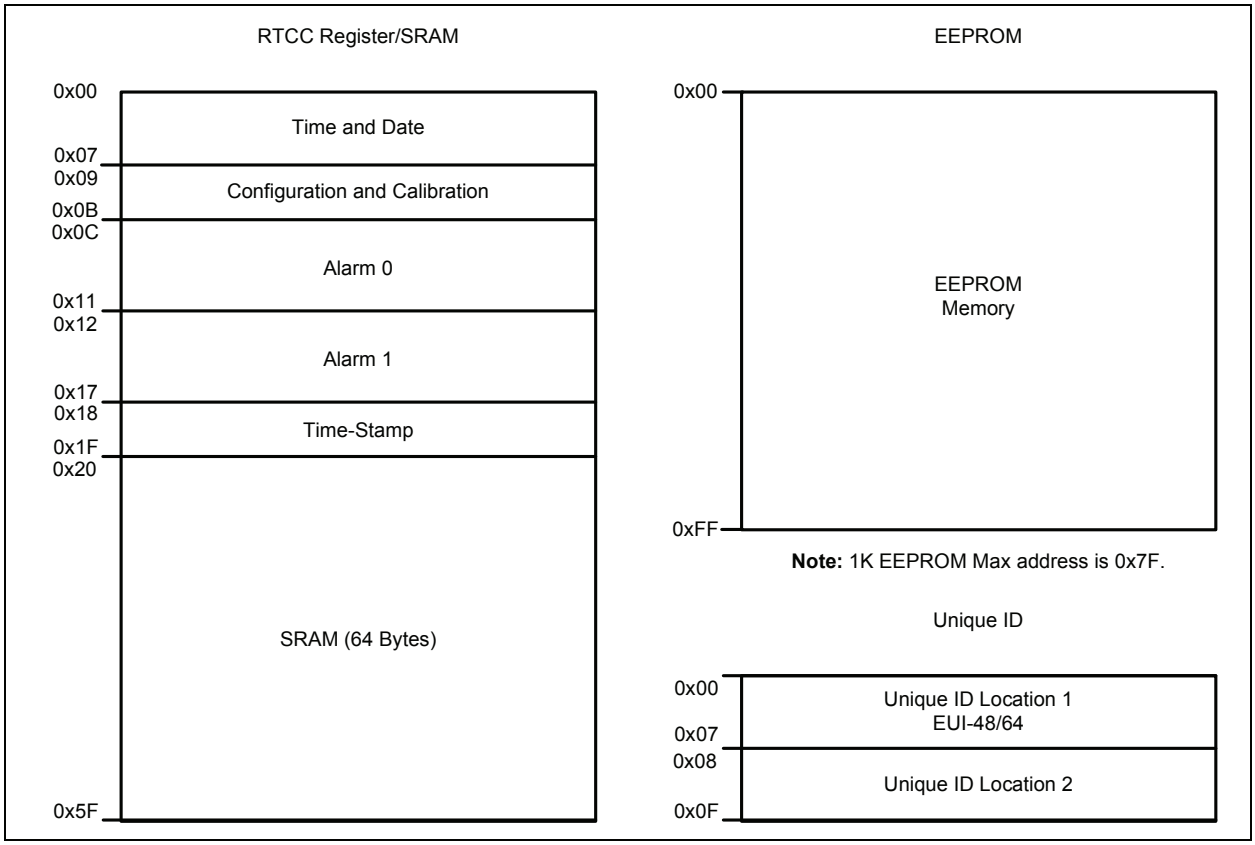
Pin Name	Pin Function
VSS	Ground
X1	Xtal Input, External Oscillator Input
X2	Xtal Output
VBAT	Battery Backup Input (3V Typ)
VCC	+1.8V to +5.5V Power Supply
SI	Serial Input
$\overline{WDO}$	Watchdog Output
SCK	Serial Clock
CLKOUT/ BOOT	Clock Out (Boot Clock on MCP795BXX)
$\overline{CS}$	Chip Select
$\overline{IRQ}$	Interrupt Ouput
EVHS	High-Speed Event Detect Input
EVLS	Low-Speed Event Detect Input
SO	Serial Output

2.11 RTCC Memory Map

The RTCC registers are contained in addresses 0x00h-0x1fh. 64 bytes of user-accessable SRAM are located in the address range 0x20-0x5f. The SRAM memory is a separate block from the RTCC control and Configuration registers. All SRAM locations are battery-backed-up during a VCC power fail. Unused locations are not accessible.

- Addresses 0x00h-0x07h are the RTCC Time and Date registers. These are read/write registers. Care must be taken when writing to these registers with the oscillator running.
- Incorrect data can appear in the Time and Date registers if a write is attempted during the time frame where these internal registers are being incremented. The user can minimize the likelihood of data corruption by ensuring that any writes to the Time and Date registers occur before the contents of the second register reach a value of 0x59H.
- Addresses 0x08h-0x0Bh are the device Configuration, Calibration, Watchdog Configuration and Event Detect Configuration registers.
- Addresses 0x0ch-0x11h are the Alarm 0 registers. These are used to set up the Alarm 0, the interrupt pin and the Alarm 0 compare.
- Addresses 0x12h-0x17h are the Alarm 1 registers. These are used to set up the Alarm 1, the interrupt pin and the Alarm 1 compare, Alarm 1 offers a enhanced resolution of tenth and hundredths of seconds.
- Addresses 0x18h-0x1Fh are used for the Power-Down and Power-Up time-stamp feature. The detailed memory map is shown in Table 4-1. No error checking is provided when loading Time and Date registers.

FIGURE 2-2: MEMORY MAP



3.0 SPI BUS OPERATION

The MCP795XXX is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The MCP795XXX contains an 8-bit instruction register.

The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low.

TABLE 3-1: INSTRUCTION SET SUMMARY

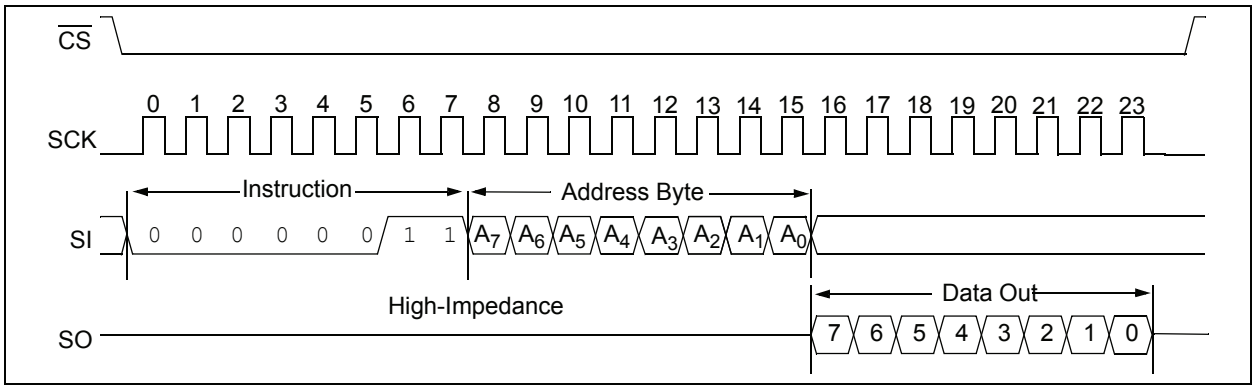
Instruction Name	Instruction Format	Description
EEREAD	0000 0011	Read data from EE memory array beginning at selected address
EEWRITE	0000 0010	Write data to EE memory array beginning at selected address
EEWRDI	0000 0100	Reset the write enable latch (disable write operations)
EEWREN	0000 0110	Set the write enable latch (enable write operations)
SRREAD	0000 0101	Read STATUS register
SRWRITE	0000 0001	Write STATUS register
READ	0001 0011	Read RTCC/SRAM array beginning at selected address
WRITE	0001 0010	Write RTCC/SRAM data to memory array beginning at selected address
UNLOCK	0001 0100	Unlock ID Locations
IDWRITE	0011 0010	Write to the ID Locations
IDREAD	0011 0011	Read the ID Locations
CLRWDT	0100 0100	Clear Watchdog TImer
CLRRAM	0101 0100	Clear RAM Location to '0'

3.1 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The various 8-bit read instructions are transmitted to the MCP795XXX followed by an 8-bit address. See Figure 3-1 for more details.

After the correct instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to the first valid address allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 1-1).

FIGURE 3-1: EEREAD SEQUENCE



3.2 Nonvolatile Memory Write Sequence

Prior to any attempt to write data to the nonvolatile memory (EEPROM, Unique ID and STATUS register) in the MCP795XXX, the write enable latch must be set by issuing the EEWREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the MCP795XXX. After all eight bits of the instruction are transmitted, $\overline{CS}$ must be driven high to set the write enable latch. If the write operation is initiated immediately after the EEWREN instruction without $\overline{CS}$ driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving $\overline{CS}$ low, issuing either an EEWRITE, IDWRITE or a SWRITE instruction, followed by the remainder of the address, and then the data to be written. Up to 8 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with XXXX 0000 and ends with XXXX X111. If the internal address counter reaches XXXX X111 and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and overwrite any data that previously existed in those locations.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the nth data byte has been clocked in. If $\overline{CS}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the nonvolatile memory write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits. Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the nonvolatile memory write cycle is completed, the write enable latch is reset.

FIGURE 3-2: BYTE EEWRITE SEQUENCE

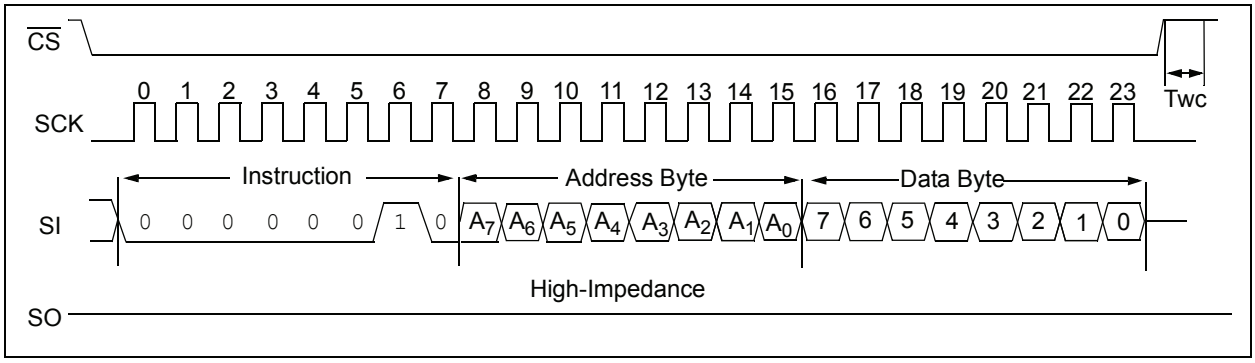
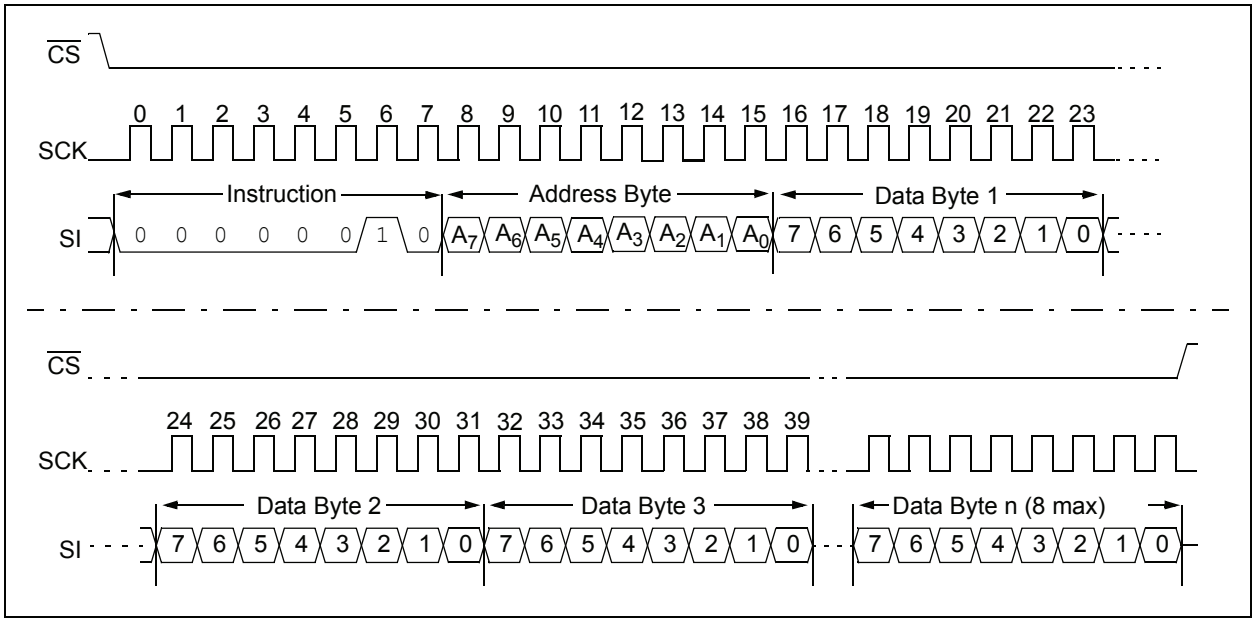


FIGURE 3-3: PAGE EEWRITE SEQUENCE



3.3 Write Enable (EEWREN) and Write Disable (EEWRDI)

The MCP795XXX contains a write enable latch.

This latch must be set before any EEWRITE, SRWRITE and IDWRITE operation will be completed internally. The `EEWREN` instruction will set the latch, and the `EEWRDI` will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- `EEWRDI` instruction successfully executed
- `SRWRITE` instruction successfully executed
- `EEWRITE` instruction successfully executed
- `IDWRITE` instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE (`EEWREN`)

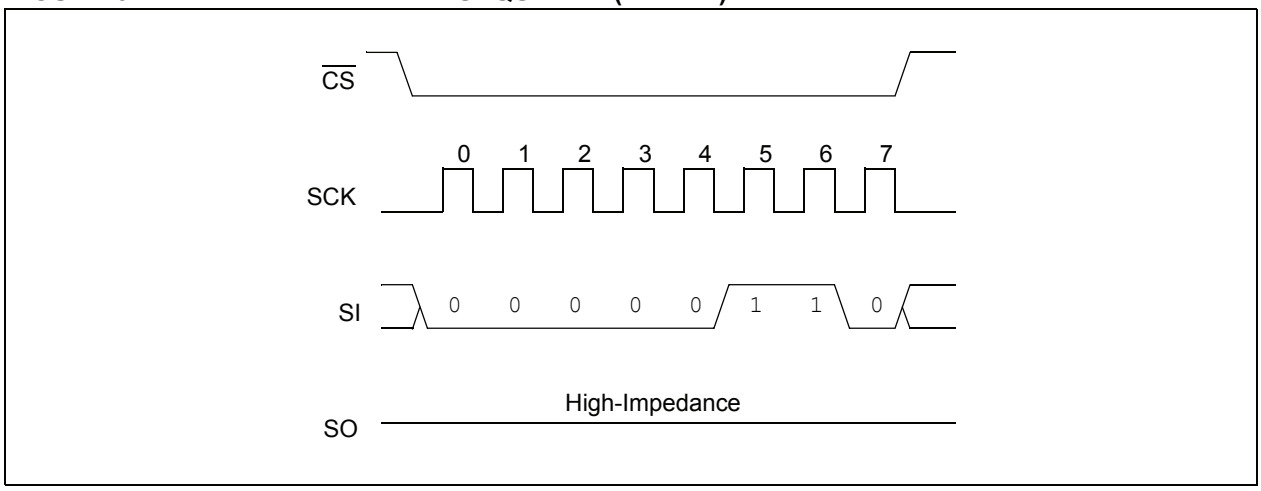
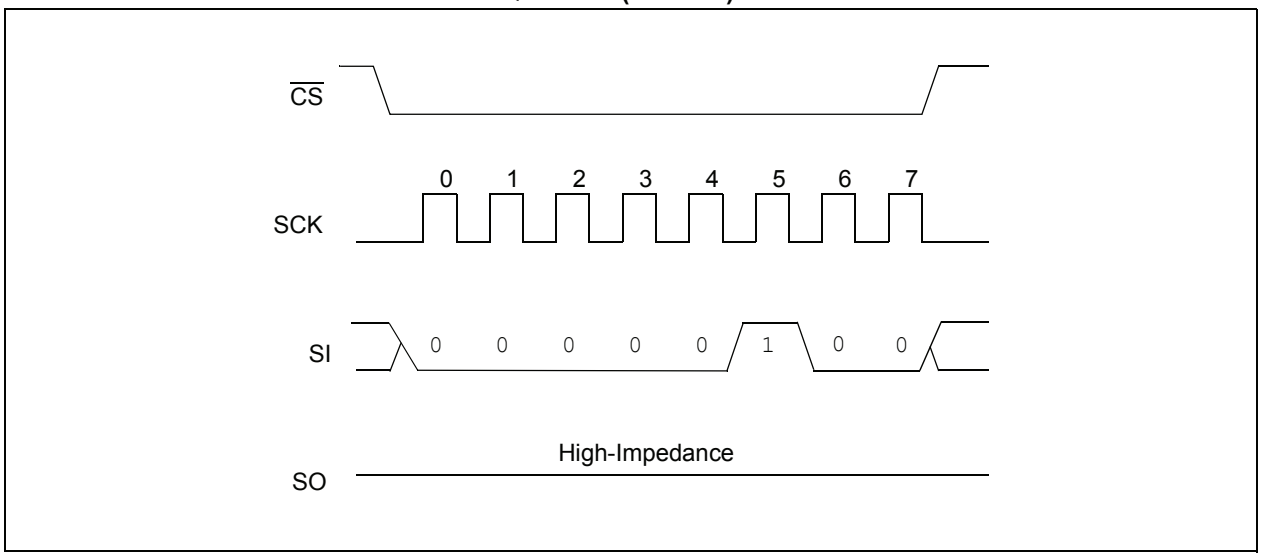


FIGURE 3-5: WRITE DISABLE SEQUENCE (`EEWRDI`)



4.0 RTCC FUNCTIONALITY

4.0.1 RTCC REGISTER MAP

The RTCC register space runs from 0x00 through to 0x1F. Any read or write that is started within the RTCC register address space will wrap to the beginning of the RTCC registers.

All of the RTCC registers are backed up from the V_{BAT} supply when V_{CC} is not available, provided that the VBATEN bit is set. Any unused bits or non implemented addresses read back as '0'. No error checking is provided for any of the RTCC, the user may load any value.

The RTCC register map is shown in Table 4-1.

TABLE 4-1: RTCC REGISTER MAP

Address	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
Time and Configuration Registers										
00h	Tenth Seconds				Hundredths of Seconds				Hundredths of seconds	00-99
01h	ST (CT)	10 Seconds			Seconds				Seconds	00-59
02h		10 Minutes			Minutes				Minutes	00-59
03h	CALSGN	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour				Hours	1-12 + AM/$\overline{PM}$ 00 - 23
04h			OSCON	VBAT	VBATEN	Day			Day	1-7
05h			10 Date		Date				Date	01-31
06h			LP	10 Month	Month				Month	01-12
07h	10 Year				Year				Year	00-99
08h	OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0	Control Reg.	
09h	CALIBRATION								Calibration	
0Ah	WDTEN	WDTIF	WDDEL	WDTPLS	WD3	WD2	WD1	WD0	Watchdog	
0Bh	EVHIF	EVLIF	EVEN1	EVEN0	EVWDT	EVLDB	EVHS1	EVHS0	Event Detect	
Alarm 0 Registers										
0Ch		10 Seconds			Seconds				Seconds	00-59
0Dh		10 Minutes			Minutes				Minutes	00-59
0Eh		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour				Hours	1-12 + AM/$\overline{PM}$ 00-23
0Fh	ALM0PIN	ALM0C2	ALM0C1	ALM0C0	ALM0IF	Day			Day	1-7
10h			10 Date		Date				Date	01-31
11h				10 Month	Month				Month	01-12
Alarm 1 Registers										
12h	Tenth Seconds				Hundredths of seconds				Hundredths of Seconds	00-99
13h		10 Seconds			Seconds				Seconds	00-59
14h		10 Minutes			Minutes				Minutes	00-59
15h		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour				Hours	1-12 + AM/$\overline{PM}$ 00-23
16h	ALM1PIN	ALM1C2	ALM1C1	ALM1C0	ALM1IF	Day			Day	1-7
17h			10 Date		Date				Date	01-31
Power-down Time-stamp Registers										
18h		10 Minutes			Minutes					
19h		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour					
1Ah			10 Date		Date					
1Bh	Day			10 Month	Month					
Power-Up Time-stamp Registers										
1Ch		10 Minutes			Minutes					
1Dh		12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour					
1Eh			10 Date		Date					
1Fh	Day			10 Month	Month					

5.0 TIME AND CONFIGURATION REGISTERS

REGISTER 5-1: HUNDREDTHS OF SECONDS 0x00

RW		RW	
Tenth Seconds		Hundredths of Seconds	
bit 7	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-4 Tenth Seconds

bit 3-0 Hundredths of Seconds

Note: Contains the BCD Tens and Hundredths of seconds

REGISTER 5-2: SECONDS 0x01

RW	RW		RW	
ST (CT)	10 Seconds		Seconds	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 ST (CT)
Setting this bit '1' starts the oscillator and clearing this bit '0' stops the on-board oscillator. For the MCP795BXX devices the ST bit is replaced by the CT bit. Setting this bit starts the timekeeping registers counting.

bit 6-4 10 Seconds

bit 3-0 Seconds

Note: Contains the BCD seconds and 10 seconds. The range is 00 to 59.

REGISTER 5-3: MINUTES 0x02

U	RW		RW	
	10 Minutes		Minutes	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented

bit 6-4 10 Minutes

bit 3-0 Minutes

Note: Contains the BCD minutes and 10 minutes. The range is 00 to 59.

REGISTER 5-4: HOUR 0x03

RW	RW	RW	RW	RW	
CALSGN	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 CALSGN
Bit 7 is the sign bit (CALSGN) for the calibration. Clearing this bit produces a positive calibration, setting this bit produces a negative calibration.

bit 6 12/$\overline{24}$
Clearing this bit to '0' enables 24-hour format, setting this bit '1' enables 12-hour format.

bit 5 10 Hour (AM/$\overline{PM}$ bit for 12-hour time)

bit 4 10 Hour

bit 3-0 Hour

Note: Contains the BCD hour in bits <3:0>. Bits <5:4> contain either the 10-hour in BCD for 24-hour format or the AM/PM indicator and the 10-hour bit for 12-hour format. Bit 5 determines the hour format.

REGISTER 5-5: DAY 0x04

U	U	R	RW	RW	RW	
		OSCON	VBAT	VBATEN	Day	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented bit, read as '0'

bit 5 Bit 5 is the OSCON bit. This is set and cleared by hardware. If this bit is set the oscillator is running, if clear, the oscillator is not running. This bit does not indicate that the oscillator is running at the correct frequency. The bit will wait 32 oscillator cycles before the bit is set.

bit 4 Bit 4 is the VBAT bit. This bit is set by hardware when the VCC fails and the VBAT is used to power the oscillator and the RTCC registers. This bit is cleared by software.

bit 3 Bit 3 is the VBATEN bit. If this bit is set the internal circuitry is connected to the VBAT pin. If this bit is '0' then the VBAT pin is disconnected and the only current drain on the external battery is the VBAT pin leakage.

bit 2-0 Day

Note: Contains the BCD day. The range is 1-7. Also, additional bits are used for configuration and Status.

REGISTER 5-6: DATE 0x05

U	U	RW		RW	
		10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented bit, read as '0'
bit 5-4 10 Date
bit 3-0 Date
Note: Contains the BCD Date and 10 Date. The range is 01-31.

REGISTER 5-7: MONTH 0x06

U	U	R	RW	RW	
		LP	10 Month	Month	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented bit, read as '0'
bit 5 Bit 5 is the Leap Year bit, this is set during a leap year and is read-only.
bit 4 10 Month
bit 3-0 Month
Note: Contains the BCD month. Bit 4 contains the 10 month.

REGISTER 5-8: YEAR 0x07

RW		RW	
10 Year		Year	
bit 7	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-4 10 Year
bit 3-0 Year
Note: Contains the BCD Year and 10 Year. The Range is 00-99.

REGISTER 5-9: CONTROL REG 0x08

RW	RW	RW	RW	RW	RW	RW	RW
OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Bit 7 is the OUT bit, this sets the logic level on the CLKOUT when not using this as a square wave output.

bit 6 Bit 6 is the SQWE bit, setting this bit enables the divided output from the crystal oscillator.

bit 5:4 ALM1 Bits <5:4> determine which alarms are active.
- 00 – No Alarms are active
- 01 – Alarm 0 is active
- 10 – Alarm 1 is active
- 11 – Both Alarms are active

bit 3 Bit 3 is the EXTOSC enable bit. Setting this bit will allow an external 32.768 kHz signal to drive the RTCC registers, eliminating the need for an external crystal.

bit 2:0 RS2 Bits <2:0> set the internal divider for the 32.768 kHz oscillator to be driven to the CLKOUT. The following frequencies are available. The output is responsive to the Calibration register.
- 000 – 1 Hz
- 001 – 4.096 kHz
- 010 – 8.192 kHz
- 011 – 32.768 kHz
- 1XX enables the Cal Output function. Cal output appears on CLKOUT if SQWE is set (1 Hz nominal).

Note: When RS2 is set to enable the Cal Output function, the RTCC counters will continue to increment.

REGISTER 5-10: CALIBRATION 0x09

RW	
CALIBRATION	
bit 7	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-0 Calibration Value

Note: This is an 8-bit register that is used to add or subtract clocks from the RTCC counter every minute. The CALSGN (0x03:7) is the sign bit and indicates if the count should be added or subtracted. The 8 bits in the Calibration register, with each bit adding or subtracting two clocks, gives the user the ability to add or subtract up to 510 clocks per minute.

REGISTER 5-11: WATCHDOG 0x0A

RW	RW	RW	RW	RW	RW	RW	RW
WDTEN	WDTIF	WDDEL	WDTPLS	WD3	WD2	WD1	WD0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Bit 7 is a read/write bit that is set by the user and can be cleared by the user of the hardware. This bit is set to enable the WDT function and cleared to disable the function. This bit is cleared by the hardware when the VCC supply is not present, it is not set again when VCC is present.

bit 6 Bit 6 is a read/write bit that is set in hardware when the WDT times out and the WD pin is asserted. This bit must be cleared in software to restart the WDT.

bit 5 Bit 5 is a read/write bit and is set to enable a 64-second delay before the WDT starts to count. If this bit is set and the WDTIF bit is cleared then there will be a 64 second delay before the WDT starts to count. This bit should be set before the WDTEN bit is set.

bit 4 Bit 4 is a read/write bit that is used to select the pulse width on the WD pin when the WDT times out.
- 0 – 122 us Pulse
- 1 – 125 ms Pulse

bit 3:0 Bits <3:0> are read/write bits that are used to set the WDT time-out period as below (all times are based off the uncalibrated crystal reference). Bit 3 should be cleared and is reserved for future use:
- 000 – 977 us
- 001 – 15.6 ms
- 010 – 62.5 ms
- 011 – 125 ms
- 100 – 1s
- 101 – 16s
- 110 – 32s
- 111 – 64s

Note: Please see **Section 9.1.3, Watchdog Timer** for more information.

REGISTER 5-12: EVENT DETECT 0x0B

RW	RW	RW	RW	RW	RW	RW	RW
EVHIF	EVLIF	EVEN1	EVEN0	EVWDT	EVLDB	EVHS1	EVHS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:	R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 When the configured number of high speed events has occurred the $\overline{IRQ}$ pin is asserted and the EVHIF bit is set in hardware. The clear the $\overline{IRQ}$ pin and reset the EVHIF bit must be cleared in software.

bit 6 When an event occurs on the low-speed pin this $\overline{IRQ}$ pin is asserted and the EVLIF bit is set. This bit must be cleared by software to reset the module and clear the $\overline{IRQ}$ pin.

bit 5:4 <1:0> These two bits determine what combination of the high and low-speed modules are enabled.
- 00 – Both modules are Off
- 01 – Low-speed module enabled, high speed disabled
- 10 – Low-speed module disabled, high speed enabled
- 11 – Both modules are enabled

bit 3 Setting this bit overrides any setting for the High-Speed Event Detection and allows the EVHS pin to clear the Watchdog Timer. This is edge triggered. Either and H-L or L-H transition will clear the WDT.

bit 2 This is the Low-Speed Event Debounce setting. Depending on the state of this bit the low-speed pin will have to remain at the same state for the following periods to be considered valid.
- 0 – 31.25 ms
- 1 – 500 ms

bit 1:0 EVHS <1:0> These bits determine how many high-speed events must occur before the EVHIF bit is set. All of these events must occur within 250 ms (based on the uncalibrated 32.768 kHz clock).
- 00 – 1st Event
- 01 – 4th Event
- 10 – 16th Event
- 11 – 32nd Event

Note: Please see **Section 9.1.4, Event Detection** for more information.

6.0 ALARM 0 REGISTERS

REGISTER 6-1: SECONDS 0x0C

RW	RW	RW
	10 Seconds	Seconds
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6-4 10 Seconds
bit 3-0 Seconds
Note: This contains the seconds match for the Alarm 0.

REGISTER 6-2: MINUTES 0x0D

RW	RW	RW
	10 Minutes	Minutes
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6-4 10 Minutes
bit 3-0 Minutes
Note: This contains the minutes match for the Alarm 0.

REGISTER 6-3: HOURS 0x0E

RW	RW			RW
	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6 12/$\overline{24}$ (this is a copy of bit 6 in the Hours register (0x03)
bit 5 10 Hour AM/$\overline{PM}$
bit 4 10 Hour
bit 3-0 Hour

REGISTER 6-4: DAY 0x0F

RW	RW			RW	RW	
ALM0PIN	ALM0C2	ALM0C1	ALM0C0	ALM0IF	Day	
bit 7	bit6		bit 4	bit 3	bit 2	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Bit 7 configures the pin that is used for the Alarm 0 output. If this bit is clear the $\overline{IRQ}$ pin is used. If set, the $\overline{WDO}$ pin is used. If the WDT is enabled then a valid Alarm will assert the $\overline{WDO}$ pin for 122 us.

BIT 6:4 Bits <6:4> sets the condition on what the Alarm will trigger. The following options are available:
000 – Seconds match
001 – Minutes match
010 – Hours match (logic takes into account 12/24 operation)
011 – Day match. Generates interrupt at 12:00:00 AM
100 – Date match
101 – Unimplemented, do not use
110 – Unimplemented, do not use
111 – Seconds, Minutes, Hour, Day, Date and Month

bit 3 Bit 3 is the ALM0IF bit. This is set by hardware when an alarm condition has be generated. The bit must be cleared in software.

bit 2-0 Day

REGISTER 6-5: DATE 0x10

U	U	RW	RW	RW	
		10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented

bit 5-4 10 Date

bit 3-0 Date

REGISTER 6-6: MONTH 0x11

U	U	U	RW	RW
			10 Month	Month
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-5 Unimplemented
bit 4 10 Month
bit 3-0 Month
Note: Month match is only available on Alarm 0.

7.0 ALARM 1 REGISTERS

REGISTER 7-1: HUNDREDTHS OF SECONDS 0x12

RW		RW	
Tenth Seconds		Hundredths of Seconds	
bit 7	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-4 Tenth Seconds
bit 3-0 Hundredths of Seconds
Note: Hundredths and Tenth seconds only available on Alarm 1.

REGISTER 7-2: SECONDS 0x13

U	RW		RW	
	10 Seconds		Seconds	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6-4 10 Seconds
bit 3-0 Seconds

REGISTER 7-3: MINUTES 0x14

U	RW		RW	
	10 Minutes		Minutes	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6-4 10 Minutes
bit 3-0 Minutes

REGISTER 7-4: HOURS 0x15

U	RW	RW	RW	RW	
	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6 12/$\overline{24}$
bit 5 10 Hour AM/$\overline{PM}$
bit 4 10 Hour
bit 3-0 Hour

REGISTER 7-5: DAY 0x16

RW	RW	RW	RW	RW	RW	
ALM1PIN	ALM1C2	ALM1C1	ALM1C0	ALM1IF	Day	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Bit 7 configures the pin that is used for the Alarm 0 output. If this bit is clear the $\overline{IRQ}$ pin is used. If set, the $\overline{WDO}$ pin is used. If the WDT is enabled then a valid Alarm will assert the $\overline{WDO}$ pin for 122 us.

BIT 6:4 Bits <6:4> sets the condition on what the Alarm will trigger. The following options are available:
000 – Seconds match
001 – Minutes match
010 – Hours match (logic takes into account 12/24 operation)
011 – Day match, generates interrupt at 12:00:00 am
100 – Date match
101 – Hundredths/Tenth of Seconds
110 – Unimplemented do not use
111 – Seconds, Minutes, Hour, Day and Date

bit 3 Bit 3 is the ALM1IF bit. This is set by hardware when an alarm condition has be generated. The bit must be cleared in software.

bit 2-0 Day

REGISTER 7-6: DATE 0x17

U	U	RW		RW		
		10 Date		Date		
bit 7	bit 6	bit 5	bit 4	bit 3		bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented
bit 5-4 10 Date
bit 3-0 Date

8.0 POWER-DOWN TIME-STAMP REGISTERS

Note: It is strongly recommended that the timesaver function only be used when the oscillator is running. This will ensure accurate functionality.

REGISTER 8-1: MINUTES 0x18

U	RW	RW
	10 Minutes	Minutes
bit 7	bit 6 bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6-4 10 Minutes
bit 3-0 Minutes

REGISTER 8-2: HOUR 0x19

U	RW	RW	RW	RW
	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hours	Hour
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7 Unimplemented
bit 6 12/$\overline{24}$ (this is a copy of the status of the bit in register 0x03:6 at the time of the event)
bit 5 10 Hour AM/$\overline{PM}$
bit 4 10 Hour
bit 3-0 Hour

REGISTER 8-3: DATE 0x1A

U	U	RW	RW	RW
		10 Date		Date
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-6 Unimplemented
bit 5-4 10 Date
bit 3-0 Date

REGISTER 8-4: MONTH 0x1B

RW	RW	RW	RW	RW
Day			10 Month	Month
bit 7	bit 6	bit 5	bit 4	bit 3 bit 0

Legend: R = Readable Bit W = Writable Bit U = Unimplemented bit, Read as '0'

bit 7-5 Day
bit 4 10 Month
bit 3-0 Month