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MCP795W1X/MCP795W2X

Battery-Backed SPI Real-Time Clock/Calendar with Enhanced Features

Device Selection Table

Part Number	EEPROM (Kbits)	Protected EEPROM
MCP795W10	1	Blank
MCP795W20	2	Blank
MCP795W11	1	EUI-48™
MCP795W21	2	EUI-48™
MCP795W12	1	EUI-64™
MCP795W22	2	EUI-64™

Timekeeping Features

- Real-Time Clock/Calendar (RTCC):
  - Hours, minutes, seconds, hundredth of seconds, day of week, date, month, year
  - Leap year compensated to 2399
  - 12/24-hour modes
- Oscillator for 32.768 kHz Crystals:
  - Optimized for 6-9 pF crystals
- On-Chip Digital Trimming/Calibration:
  - ±1 ppm resolution
  - ±259 ppm range
- Dual Programmable Alarms
- Clock Output Function with Selectable Frequency
- Power-Fail Timestamp:
  - Time logged on switchover to and from Battery mode

Low-Power Features

- Wide Voltage Range:
  - Operating voltage range of 1.8V to 3.6V
  - Backup voltage range of 1.3V to 3.6V
- Low Typical Timekeeping Current:
  - Operating from V_{CC}: 1.2 µA at 3.0V
  - Operating from V_{BAT}: 1.0 µA at 3.0V
- Automatic Switchover to Battery Backup

Enhanced Features

- Programmable Watchdog Timer:
  - Dedicated output pin
  - Cleared via SPI bus or EVHS input
- Dual Configurable Event Detect Modules:
  - High-Speed Digital Event Detect for programmable pulse count detection
  - Low-Speed Event Detect for programmable switch debouncing

User Memory

- 64-Byte Battery-Backed SRAM
- 1 Kbit or 2 Kbit EEPROM:
  - Software write-protect
  - Page write up to 8 bytes
  - Endurance: 1M erase/write cycles
- 128-Bit Protected EEPROM Area:
  - Robust write unlock sequence
  - EUI-48™ MAC address (MCP795WX1)
  - EUI-64™ MAC address (MCP795WX2)

Operating Ranges

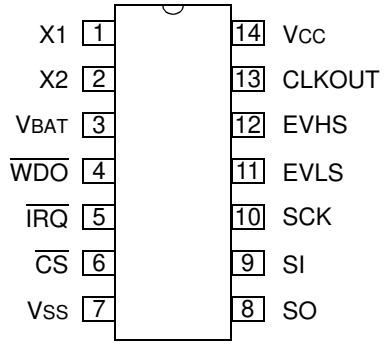
- SPI Serial Interface:
  - SPI clock rate up to 5 MHz
- Temperature Range:
  - Industrial (I): -40°C to +85°C

Packages

- 14-Lead SOIC and TSSOP

Package Types (not to scale)

SOIC/TSSOP



Description

The MCP795WXX Real-Time Clock/Calendar (RTCC) tracks time using internal counters for hours, minutes, seconds, hundredth of seconds, days, months, years and day of week. Alarms can be configured on all counters up to and including months. For usage and configuration, the MCP795WXX supports SPI communications up to 5 MHz.

The MCP795WXX is designed to operate using a 32.768 kHz tuning fork crystal with external crystal load capacitors. On-chip digital trimming can be used to adjust for frequency variance caused by crystal tolerance and temperature.

SRAM and timekeeping circuitry are powered from the backup supply when main power is lost, allowing the device to maintain accurate time and the SRAM contents. The times when the device switches over to the backup supply and when primary power returns are both logged by the power-fail timestamp.

The MCP795WXX features 128 bits of EEPROM which is only writable after an unlock sequence, making it ideal for storing a unique ID or other critical information.

The MCP795WX1 and MCP795WX2 are pre-programmed with EUI-48 and EUI-64 addresses, respectively. Custom programming is also available.

Two event detect modules are included on the MCP795WXX. The high-speed event detect module will generate an interrupt after a programmable number of pulses have been detected. The low-speed event detect module can be used to debounce mechanical switches and includes a selectable debounce period.

The MCP795WXX also features an integrated Watchdog Timer peripheral. This allows applications to improve system robustness by moving this functionality outside of the microcontroller.

The MCP795WXX has versatile output options. There is a dedicated pin for outputting a selectable frequency square wave or for use as a general purpose output. Additionally, the alarms can be assigned to either the Watchdog Timer interrupt output or the event detect interrupt output.

FIGURE 1-1: TYPICAL APPLICATION SCHEMATIC

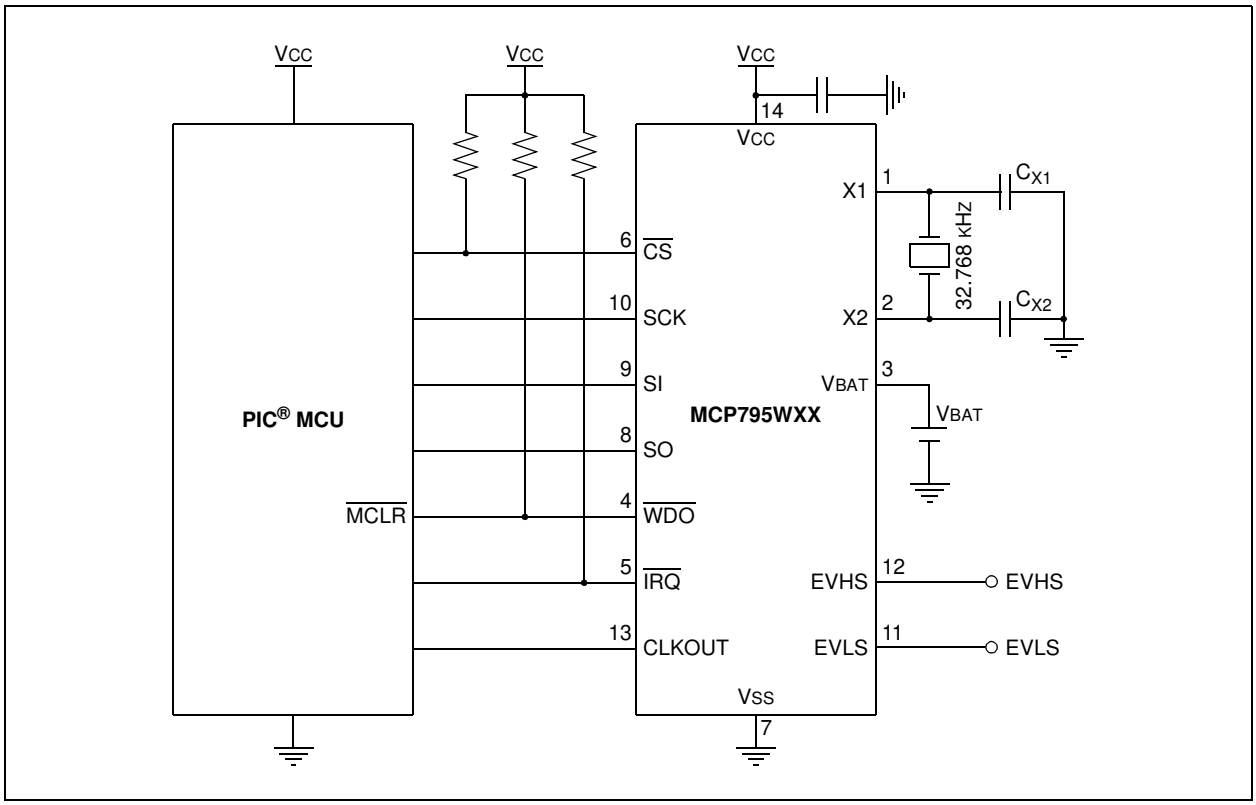
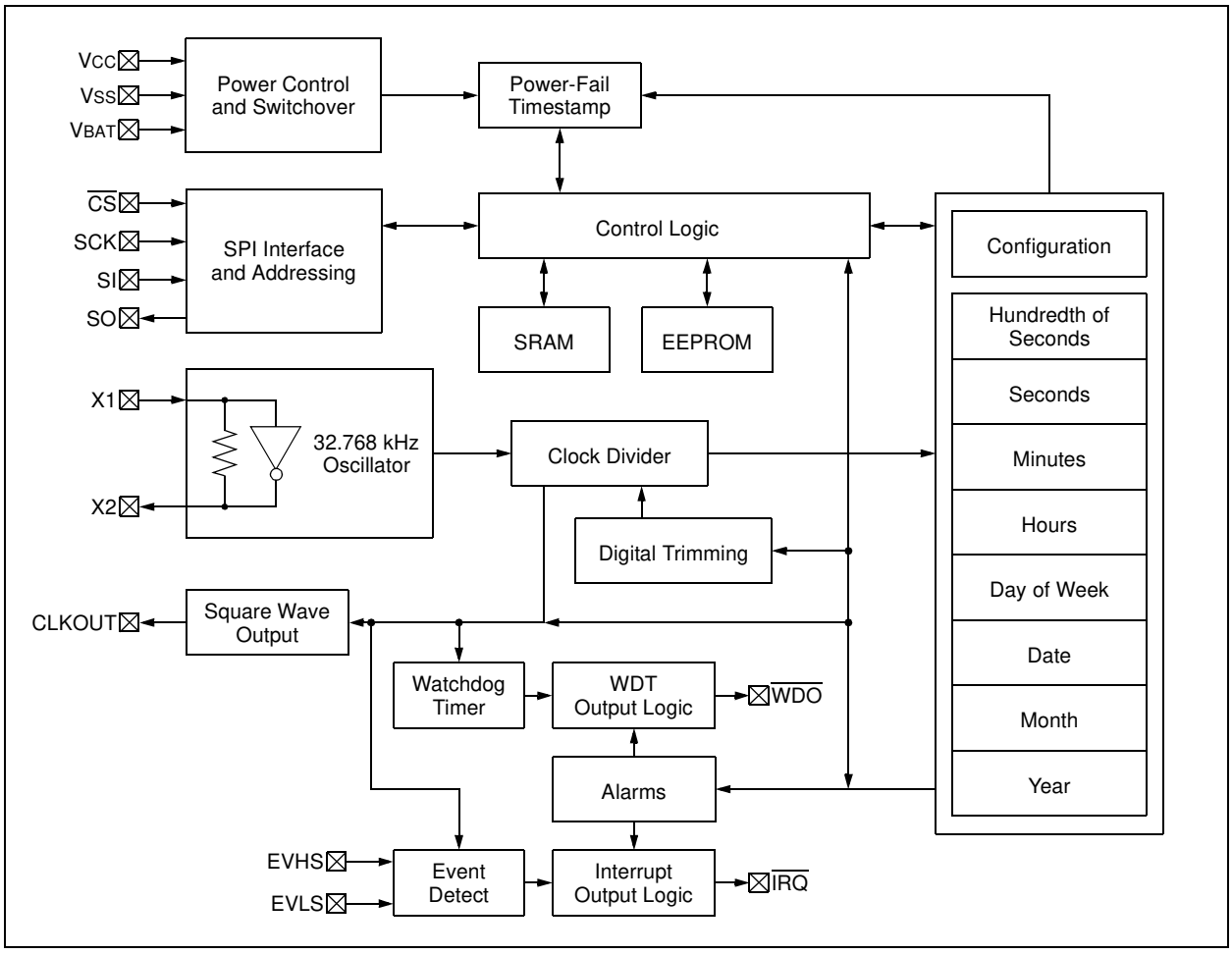


FIGURE 1-2: BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC+1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +85°C

ESD protection on all pins.....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 3.6V				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Test Conditions**
D1	VIH	High-Level Input Voltage	0.7 VCC	—	VCC + 1	V	
D2	VIL	Low-Level Input Voltage	-0.3	—	0.3VCC	V	VCC ≥ 2.5V
			-0.3	—	0.2VCC		VCC < 2.5V
D3	VOL	Low-Level Output Voltage	—	—	0.4	V	IOL = 2.1 mA, VCC ≥ 2.5V
			—	—	0.2		IOL = 1.0 mA, VCC < 2.5V
D4	VOH	High-Level Output Voltage	VCC - 0.5	—	—	V	IOH = -400 µA
D5	ILI	Input Leakage Current	—	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS or VCC
D7	CINT	Pin Capacitance (all inputs and outputs)	—	—	7	pF	VCC = 3.6V **(Note 1)** TA = 25°C, f = 1 MHz
D8	COSC	Oscillator Pin Capacitance (X1, X2 pins)	—	3	—	pF	**Note 1**
D9	ICCEERD	EEPROM Operating Current	—	—	3	mA	VCC = 3.6V, FCLK = 5 MHz SO = Open
	ICCEEWR				5	mA	VCC = 3.6V
D10	ICCREAD	SRAM/RTCC Operating Current	—	—	3	mA	VCC = 3.6V, FCLK = 5 MHz SO = Open
	ICCWRITE				3	mA	VCC = 3.6V, FCLK = 5 MHz
D11	ICCDAT	Vcc Data Retention Current (oscillator off)	—	—	1	µA	VCC = 3.6V

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

DC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 3.6V				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Test Conditions**
D12	ICCT	Timekeeping Current	—	—	1.2	µA	VCC = 1.8V, $\overline{CS}$ = VCC, EVHS = VSS, EVLS = VSS (**Note 1**)
			—	1.2	1.8	µA	VCC = 3.0V, $\overline{CS}$ = VCC, EVHS = VSS, EVLS = VSS (**Note 1**)
			—	—	2.6	µA	VCC = 3.6V, $\overline{CS}$ = VCC, EVHS = VSS, EVLS = VSS (**Note 1**)
D13	VTRIP	Power-Fail Switchover Voltage	1.3	1.5	1.7	V	
D14	VBAT	Backup Supply Voltage Range	1.3	—	3.6	V	
D15	IBATT	Timekeeping Backup Current	—	—	850	nA	VBAT = 1.3V, VCC = VSS (**Note 1**)
			—	1000	1200	nA	VBAT = 3.0V, VCC = VSS (**Note 1**)
			—	—	2300	nA	VBAT = 3.6V, VCC = VSS (**Note 1**)
D16	IBATDAT	VBAT Data-Retention Current (oscillator off)	—	—	850	nA	VBAT = 3.6V, VCC = VSS

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 3.6V				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	—	—	5	MHz	2.5V ≤ Vcc < 3.6V
			—	—	3	MHz	1.8V ≤ Vcc < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	—	ns	
5	TSU	Data Setup Time	20	—	—	ns	2.5V ≤ Vcc < 3.6V
			30	—	—	ns	1.8V ≤ Vcc < 2.5V
6	THD	Data Hold Time	40	—	—	ns	2.5V ≤ Vcc < 3.6V
			50	—	—	ns	1.8V ≤ Vcc < 2.5V
7	TR	SCK Rise Time	—	—	100	ns	**Note 1**
8	TF	SCK Fall Time	—	—	100	ns	**Note 1**
9	THI	Clock High Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
10	TLO	Clock Low Time	100	—	—	ns	2.5V ≤ Vcc < 3.6V
			150	—	—	ns	1.8V ≤ Vcc < 2.5V
11	TCLD	Clock Delay Time	50	—	—	ns	
12	TCLE	Clock Enable Time	50	—	—	ns	
13	TV	Output Valid from Clock Low	—	—	100	ns	2.5V ≤ Vcc < 3.6V
			—	—	160	ns	1.8V ≤ Vcc < 2.5V
14	THO	Output Hold Time	0		—	ns	**Note 1**
15	TDIS	Output Disable Time	—	—	80	ns	2.5V ≤ Vcc < 3.6V **(Note 1)**
			—	—	160	ns	1.8V ≤ Vcc < 2.5V **(Note 1)**
16	TWC	Internal Write Cycle Time	—	—	5	ms	**Note 2**
17	TFVCC	VCC Fall Time	300	—	—	µs	**Note 1**
18	TRVCC	VCC Rise Time	0	—	—	µs	**Note 1**
19	FOSC	Oscillator Frequency	—	32.768	—	kHz	
20	TOSF	Oscillator Timeout Period	—	1	—	ms	**Note 1**
21		Endurance	1M	—	—	E/W cycles	Page Mode, 25°C VCC = 3.6V **(Note 1**

Note 1: This parameter is not tested but ensured by characterization.

2: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

FIGURE 1-1: SERIAL INPUT TIMING

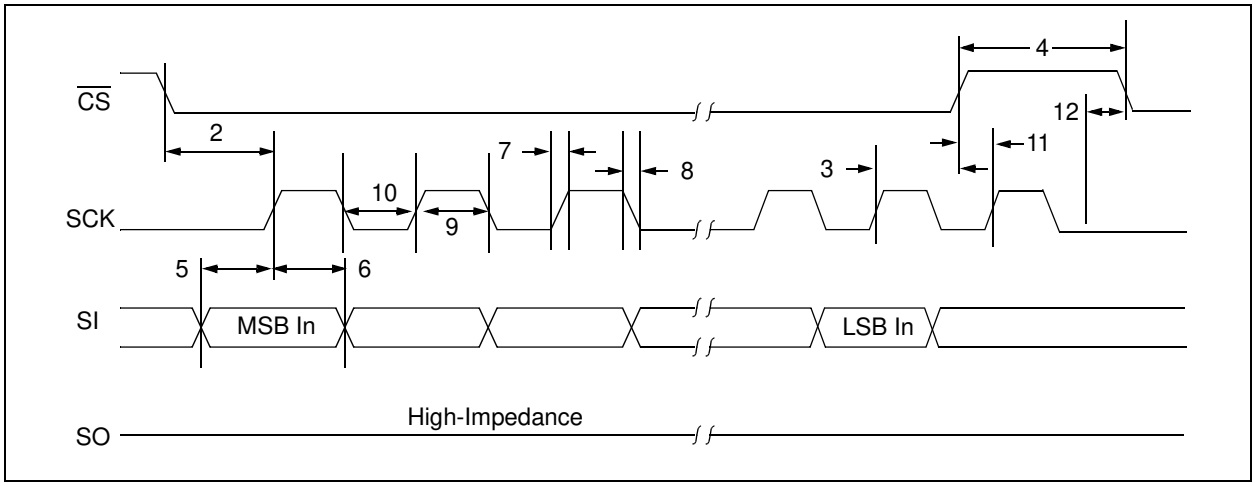


FIGURE 1-2: SERIAL OUTPUT TIMING

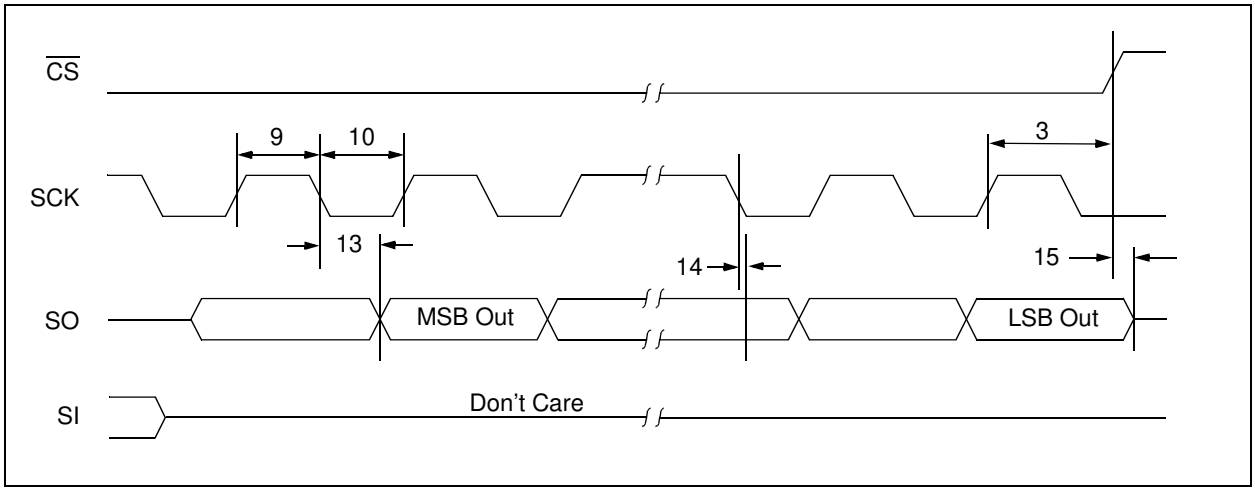
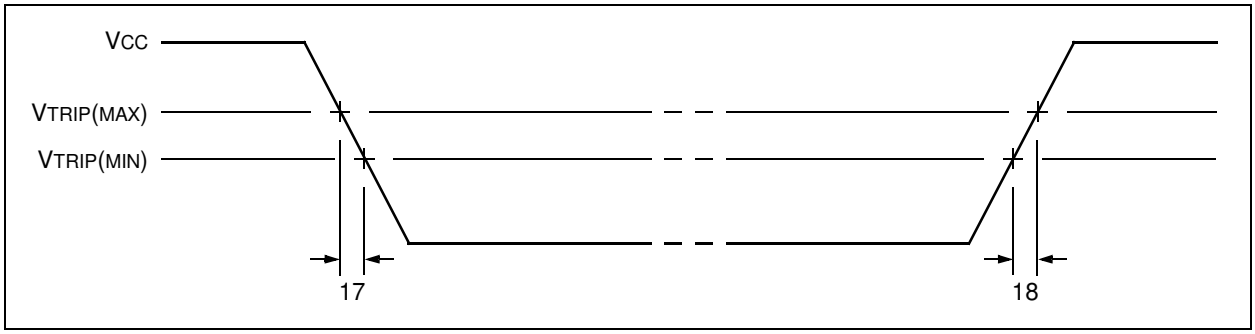


FIGURE 1-3: POWER SUPPLY TRANSITION TIMING



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data represented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 2-1: TIMEKEEPING BACKUP CURRENT VS. BACKUP SUPPLY VOLTAGE

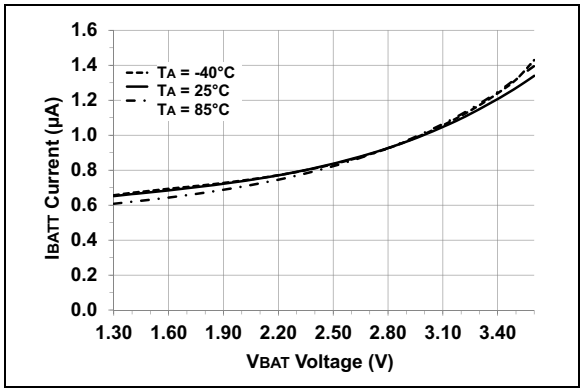
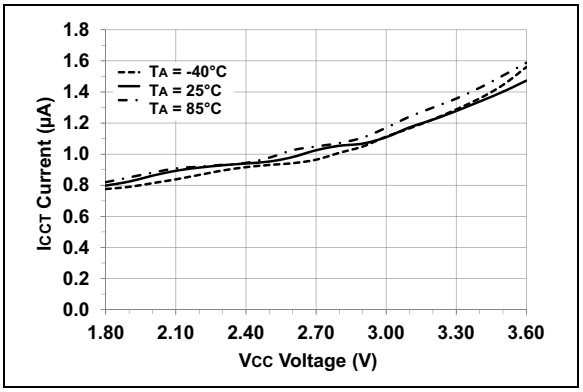


FIGURE 2-2: TIMEKEEPING CURRENT VS. SUPPLY VOLTAGE



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	14-pin SOIC	14-pin TSSOP	Pin Function
X1	1	1	Quartz Crystal Input, External Oscillator Input
X2	2	2	Quartz Crystal Output
VBAT	3	3	Battery Backup Supply Input
$\overline{WDO}$	4	4	Watchdog Output
$\overline{IRQ}$	5	5	Interrupt Output
$\overline{CS}$	6	6	Chip Select Input
VSS	7	7	Ground
SO	8	8	Serial Data Output
SI	9	9	Serial Data Input
SCK	10	10	Serial Clock Input
EVHS	11	11	High-Speed Event Detect Input
EVLS	12	12	Low-Speed Event Detect Input
CLKOUT	13	13	Square Wave Clock Output
VCC	14	14	Primary Power Supply

3.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device, whereas a high level deselects the device. A nonvolatile memory programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. After power-up, a high-to-low transition on $\overline{CS}$ is required prior to any sequence being initiated.

3.2 Serial Clock (SCK)

This pin is used to synchronize the communication between a master and the MCP795WXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.3 Serial Input (SI)

This pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.4 Serial Output (SO)

This pin is used to transfer data out of the MCP795WXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.5 Oscillator Input/Output (X1, X2)

These pins are used as the connections for an external 32.768 kHz quartz crystal and load capacitors. X1 is the crystal oscillator input and X2 is the output. The MCP795WXX is designed to allow for the use of external load capacitors in order to provide additional flexibility when choosing external crystals. The MCP795WXX is optimized for crystals with a specified load capacitance of 6-9 pF.

X1 also serves as the external clock input when the MCP795WXX is configured to use an external oscillator.

3.6 Watchdog Output ($\overline{WDO}$)

This is an output pin for the Watchdog Timer and, optionally, the alarms. During normal operation, the pin remains high. If a Watchdog Timer overflow occurs, the pin outputs a low pulse. The width of the pulse is user-selectable.

If an alarm output is assigned to the $\overline{WDO}$ pin, then the pin will output a low pulse when the alarm triggers.

The $\overline{WDO}$ pin is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ). This pin may be left floating if not used.

3.7 Interrupt Output ($\overline{IRQ}$)

This is an output pin for the event detect modules and, optionally, the alarms. If an event is detected by either module, then this pin will output a low signal until the interrupt flag has been cleared.

If an alarm output is assigned to the $\overline{IRQ}$ pin, then the pin will output a low signal when the alarm triggers. The pin will remain low until the alarm interrupt flag has been cleared.

The $\overline{IRQ}$ pin is an open-drain output and requires a pull-up resistor to VCC or VBAT (typically 10 kΩ). This pin may be left floating if not used.

3.8 Square Wave Clock Output (CLKOUT)

This is the output pin for the square wave output function. This pin may be left floating if not used.

3.9 High-Speed Event Detect Input (EVHS)

This pin is used as the input for the high-speed event detect module.

If the high-speed event detect module is not being used, the EVHS pin should be connected to VCC or VSS.

3.10 Low-Speed Event Detect Input (EVLS)

This pin is used as the input for the low-speed event detect module.

If the low-speed event detect module is not being used, the EVLS pin should be connected to VCC or VSS.

3.11 Backup Supply (VBAT)

This is the input for a backup supply to maintain the RTCC and SRAM registers during the time when VCC is unavailable.

Power should be applied to VCC before VBAT.

If the battery backup feature is not being used, the VBAT pin should be connected to VSS.

4.0 SPI BUS OPERATION

The MCP795WXX is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The MCP795WXX contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low for the entire operation.

Table 4-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low.

TABLE 4-1: INSTRUCTION SET SUMMARY

Instruction Name	Instruction Format	Description
EEREAD	0000 0011	Read data from EEPROM array beginning at selected address
EEWRITE	0000 0010	Write data to EEPROM array beginning at selected address
EEWRDI	0000 0100	Reset the write enable latch (disable write operations)
EEWREN	0000 0110	Set the write enable latch (enable write operations)
SRREAD	0000 0101	Read STATUS register
SRWRITE	0000 0001	Write STATUS register
READ	0001 0011	Read data from RTCC/SRAM array beginning at selected address
WRITE	0001 0010	Write data to RTCC/SRAM array beginning at selected address
UNLOCK	0001 0100	Unlock the protected EEPROM block for a write operation
IDWRITE	0011 0010	Write data to the protected EEPROM block beginning at selected address
IDREAD	0011 0011	Read data from the protected EEPROM block beginning at the selected address
CLRWDT	0100 0100	Clear Watchdog Timer
CLRRAM	0101 0100	Clear all SRAM data to '0'

5.0 FUNCTIONAL DESCRIPTION

The MCP795WXX is a highly-integrated Real-Time Clock/Calendar (RTCC). Using an on-board, low-power oscillator, the current time is maintained in hundredths of seconds, seconds, minutes, hours, day of week, date, month, and year. The MCP795WXX also features 64 bytes of general purpose SRAM, either 2 Kbits (MCP795W2X) or 1 Kbit (MCP795W1X) of EEPROM, and 16 bytes of protected EEPROM. Two alarm modules allow interrupts to be generated at specific times with flexible comparison options. Digital trimming can be used to compensate for inaccuracies inherent with crystals. Using the backup supply input and an integrated power switch, the MCP795WXX will automatically switch to backup power when primary power is unavailable, allowing the current time and the SRAM contents to be maintained. The timestamp module captures the time when primary power is lost and when it is restored. The Watchdog Timer module can be used to reset an application that has become unresponsive. The high-speed event detect module can be used to detect pulse signals recovered from communication links, while the low-speed event detect module can be used to debounce switches and detect button presses.

The RTCC configuration and STATUS registers are used to access all of the modules featured on the MCP795WXX.

5.1 Memory Organization

The MCP795WXX features four different blocks of memory: the RTCC registers, general purpose SRAM, 2 Kbit EEPROM (1 Kbit for the MCP795W1X) with software write-protect, and protected EEPROM. The RTCC registers and SRAM share the same address space and are accessed through the `READ` and `WRITE` instructions. The EEPROM region is accessed using the `EEREAD` and `EEWRITE` instructions, and the protected EEPROM is accessed using the `IDREAD` and `IDWRITE` instructions. Unused locations are not accessible. The MCP795WXX will not acknowledge if the address is out of range, as shown in the shaded region of the memory maps in Figure 5-1 and Figure 5-2.

The RTCC registers are contained in addresses 0x00-0x1F. Table 5-1 shows the detailed RTCC register map. There are 64 bytes of user-accessible SRAM, located in the address range 0x20-0x5F. The SRAM is a separate block from the RTCC registers. All RTCC registers and SRAM locations are maintained while operating from backup power.

FIGURE 5-1: MEMORY MAP FOR MCP795W1X

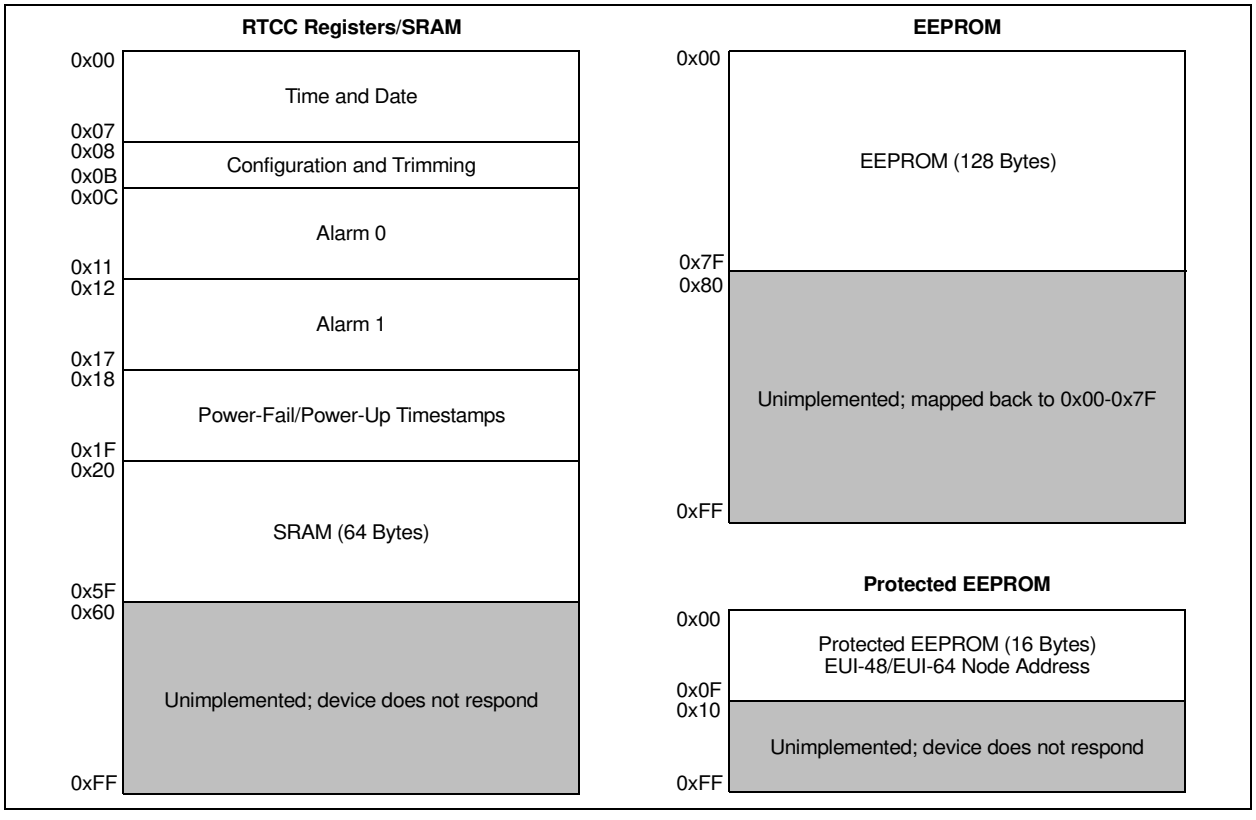


FIGURE 5-2: MEMORY MAP FOR MCP795W2X

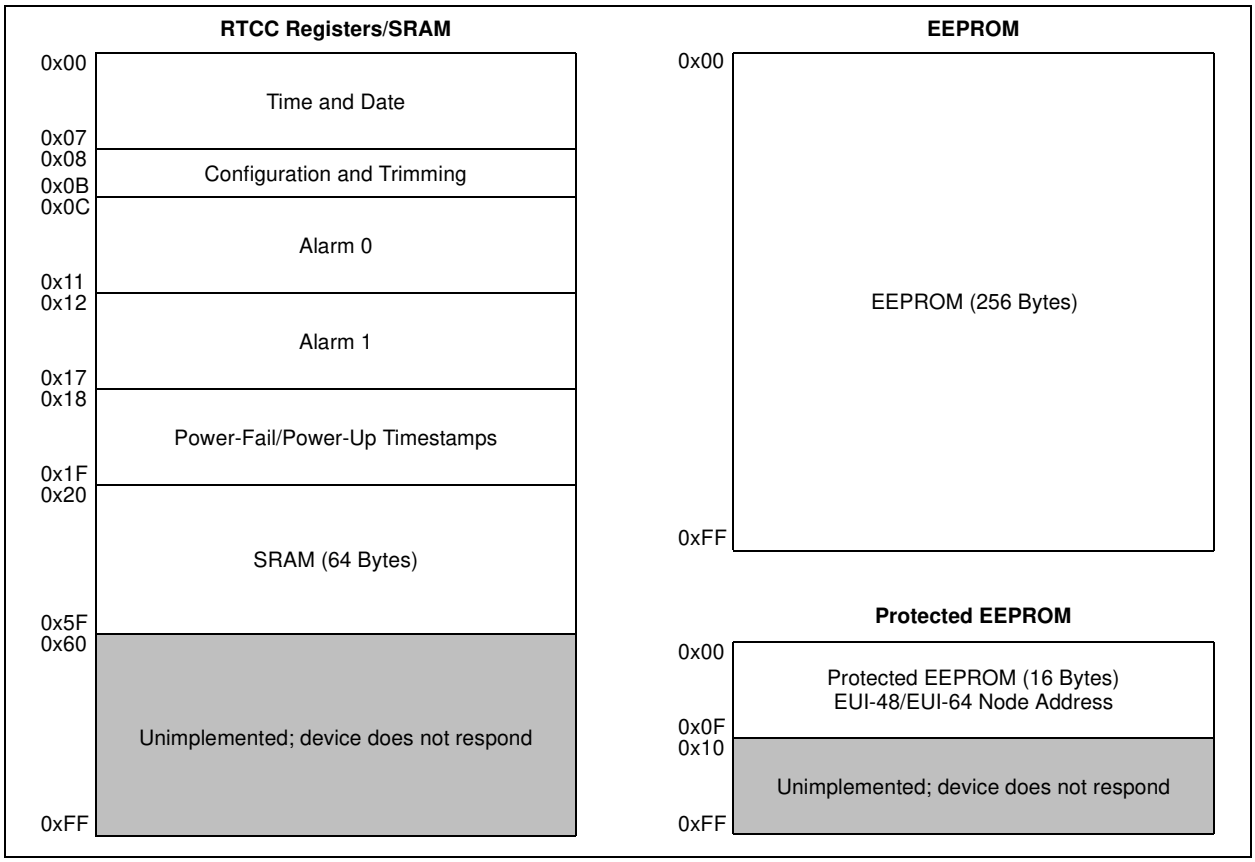


TABLE 5-1: DETAILED RTCC REGISTER MAP

Addr.	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Section 5.3 "Timekeeping"									
00h	RTCHSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
01h	RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
02h	RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
03h	RTCHOUR	TRIMSIGN	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
04h	RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
05h	RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
06h	RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
07h	RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
08h	CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
09h	OSCTRIM	TRIMVAL7	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
Section 5.5 "Watchdog Timer"									
0Ah	WDTCON	WDTEN	WDTIF	WDTDLYEN	WDTPWS	WDTPS3	WDTPS2	WDTPS1	WDTPS0
Section 5.6 "Event Detection"									
0Bh	EVDTCON	EVHIF	EVLIF	EVHEN	EVLEN	EVWDTEN	EVLPS	EVHCS1	EVHCS0
Section 5.4 "Alarms"									
0Ch	ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
0Dh	ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
0Eh	ALM0HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
0Fh	ALM0WKDAY	ALM0PIN	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0
10h	ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
11h	ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
Section 5.4 "Alarms"									
12h	ALM1HSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
13h	ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
14h	ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
15h	ALM1HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
16h	ALM1WKDAY	ALM1PIN	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0
17h	ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
Section 5.10.1 "Power-Fail Timestamp"									
Power-Down Timestamp									
18h	PWRDNMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
19h	PWRDNHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Ah	PWRDNDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Bh	PWRDNMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
Power-Up Timestamp									
1Ch	PWRUPMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
1Dh	PWRUPHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
1Eh	PWRUPDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
1Fh	PWRUPMTH	WKDAY2	WKDAY1	WKDAY0	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0

Note 1: Grey areas are unimplemented.

2: The 12/$\overline{24}$ bits in the ALMxHOUR registers are read-only and reflect the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

5.2 Oscillator Configurations

The MCP795WXX can be operated in two different oscillator configurations: using an external crystal or using an external clock input.

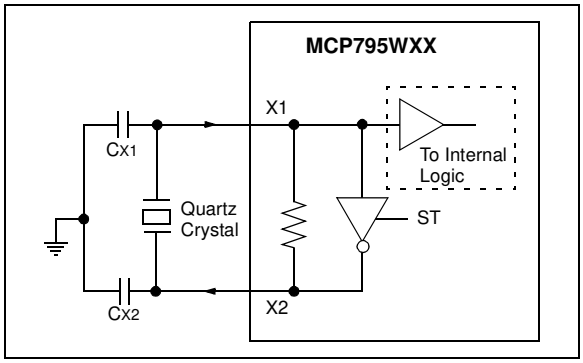
5.2.1 EXTERNAL CRYSTAL

The crystal oscillator circuit on the MCP795WXX is designed to operate with a standard 32.768 kHz tuning fork crystal and matching external load capacitors.

By using external load capacitors, the MCP795WXX allows for a wide selection of crystals. Suitable crystals have a load capacitance (C_L) of 6-9 pF. Crystals with a load capacitance of 12.5 pF are not recommended.

Figure 5-3 shows the pin connections when using an external crystal.

FIGURE 5-3: CRYSTAL OPERATION



Note 1:	The ST bit must be set to enable the crystal oscillator circuit.
2:	Always verify oscillator performance over the voltage and temperature range that is expected for the application.

5.2.1.1 Choosing Load Capacitors

C_L is the effective load capacitance as seen by the crystal, and includes the physical load capacitors, pin capacitance, and stray board capacitance. Equation 5-1 can be used to calculate C_L.

C_{X1} and C_{X2} are the external load capacitors. They must be chosen to match the selected crystal's specified load capacitance.

Note:	If the load capacitance is not correctly matched to the chosen crystal's specified value, the crystal may give a frequency outside of the crystal manufacturer's specifications.

EQUATION 5-1: LOAD CAPACITANCE CALCULATION

$$C_L = \frac{C_{X1} \times C_{X2}}{C_{X1} + C_{X2}} + C_{STRAY}$$

Where:

C_L = Effective load capacitance
C_{X1} = Capacitor value on X1 + C_{OSC}
C_{X2} = Capacitor value on X2 + C_{OSC}
C_{STRAY} = PCB stray capacitance

5.2.1.2 Layout Considerations

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

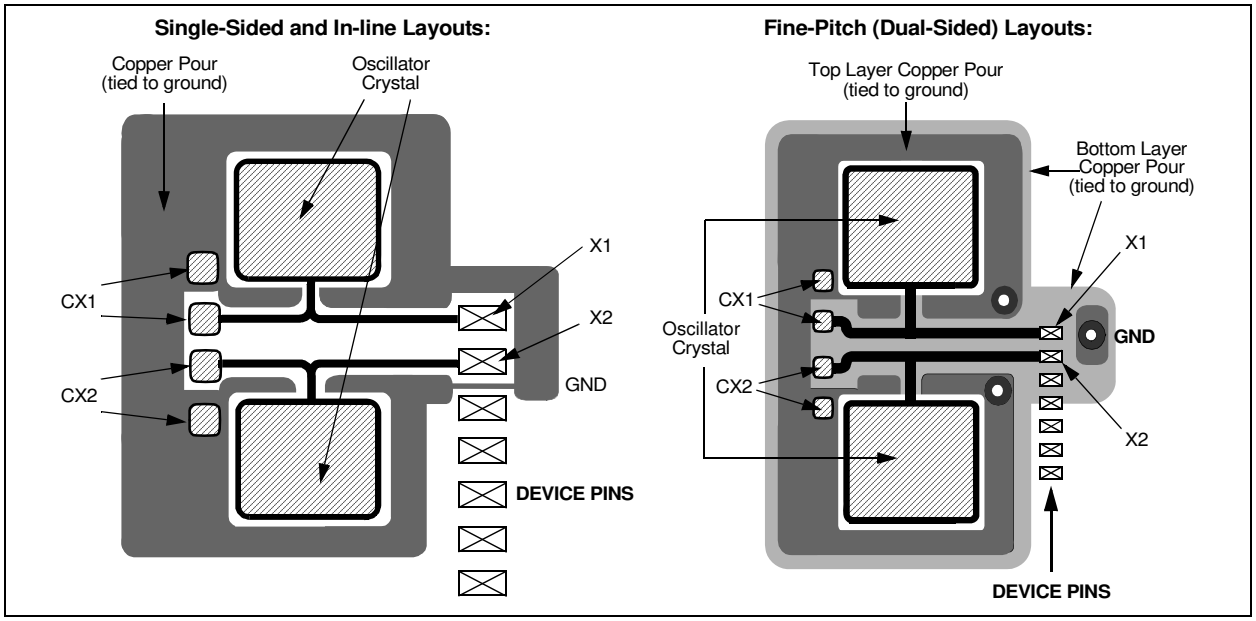
Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to V_{SS}. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 5-4. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- *AN1365, "Recommended Usage of Microchip Serial RTCC Devices"*
- *AN1519, "Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"*

FIGURE 5-4: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

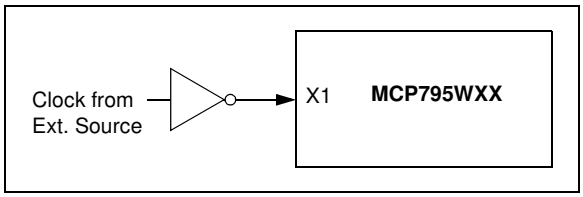


5.2.2 EXTERNAL CLOCK INPUT

A 32.768 kHz external clock source can be connected to the X1 pin (Figure 5-5). When using this configuration, the X2 pin should be left floating.

Note:	The EXTOSC bit must be set to enable an external clock source.

FIGURE 5-5: EXTERNAL CLOCK INPUT OPERATION



5.2.3 OSCILLATOR FAILURE STATUS

The MCP795WXX features an oscillator failure flag, OSCRUN, that indicates whether or not the oscillator is running. The OSCRUN bit is automatically set after 32 oscillator cycles are detected. If no oscillator cycles are detected for more than TOSF, then the OSCRUN bit is automatically cleared (Figure 5-6). This can occur if the oscillator is stopped by clearing the ST bit or due to oscillator failure.

FIGURE 5-6: OSCILLATOR FAILURE STATUS TIMING DIAGRAM

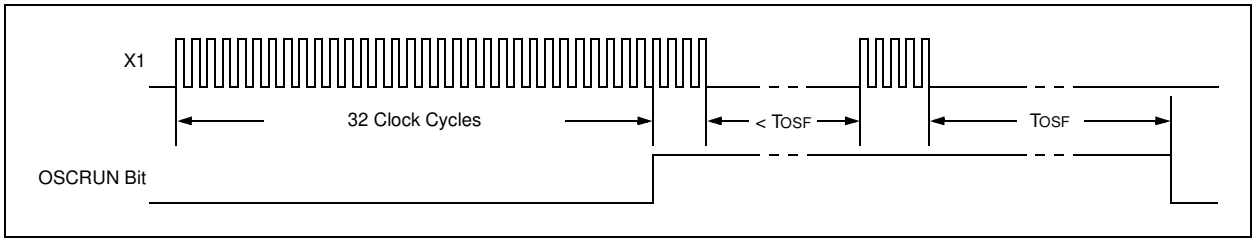


TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH OSCILLATOR CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	18
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	20
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	35

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by oscillator configuration.

5.3 Timekeeping

The MCP795WXX maintains the current time and date using an external 32.768 kHz crystal or clock source. Separate registers are used for tracking hundredths of seconds, seconds, minutes, hours, day of week, date, month, and year. The MCP795WXX automatically adjusts for months with less than 31 days and compensates for leap years from 2001 to 2399. The year is stored as a two-digit value.

Both 12-hour and 24-hour time formats are supported and are selected using the 12/$\overline{24}$ bit.

The day of week value counts from 1 to 7, increments at midnight, and the representation is user-defined (i.e., the MCP795WXX does not require 1 to equal Sunday, etc.).

All time and date values are stored in the registers as binary-coded decimal (BCD) values. The MCP795WXX will continue to maintain the time and date while operating off the backup supply.

When reading from the timekeeping registers, the registers are buffered to prevent errors due to rollover of counters. The following events cause the buffers to be updated:

- When a read is initiated from the RTCC registers (addresses 0x00 to 0x1F)
- During an RTCC register read operation, when the register address rolls over from 0x1F to 0x00

The timekeeping registers should be read in a single operation to utilize the on-board buffers and avoid rollover issues.

Note 1: Loading invalid values into the time and date registers will result in undefined operation.

2: To avoid rollover issues when loading new time and date values, the oscillator/clock input should be disabled by clearing the ST bit for External Crystal mode and the EXTOSC bit for External Clock Input mode. After waiting for the OSCRUN bit to clear, the new values can be loaded and the ST or EXTOSC bit can then be re-enabled.

5.3.1 DIGIT CARRY RULES

The following list explains which timer values cause a digit carry when there is a rollover:

- Time of day: from 11:59:59.99 PM to 12:00:00.00 AM (12-hour mode) or 23:59:59.99 to 00:00:00.00 (24-hour mode), with a carry to the Date and Weekday fields
- Date: carries to the Month field according to Table 5-3
- Weekday: from 7 to 1 with no carry
- Month: from 12/31 to 01/01 with a carry to the Year field
- Year: from 99 to 00 with no carry

TABLE 5-3: DAY TO MONTH ROLLOVER SCHEDULE

Month	Name	Maximum Date
01	January	31
02	February	28 or 29(1)
03	March	31
04	April	30
05	May	31
06	June	30
07	July	31
08	August	31
09	September	30
10	October	31
11	November	30
12	December	31

Note 1: 29 during leap years, otherwise 28.

5.3.2 GENERATING HUNDREDTH OF SECONDS

A special algorithm is required to accurately generate hundredth of seconds. The circuitry utilizes the 4.096 kHz clock signal and counts 41 clock pulses each for 24 increments of the hundredth of seconds count. The circuitry then counts 40 clock pulses for the next increment of the hundredth of second count. This results in every 25 hundredth of seconds increments equaling exactly 250 ms. Long term, the hundredth of seconds frequency will average the desired 100 Hz, while jitter is minimized short term.

EQUATION 5-2: HUNDREDTH OF SECONDS GENERATION

$$\frac{(41\ \text{clocks} \cdot 24\ \text{counts}) + (40\ \text{clocks} \cdot 1\ \text{count})}{4{,}096\ \text{Hz}} = 250\ \text{ms}$$

REGISTER 5-1: RTCHSEC: TIMEKEEPING HUNDREDTH OF SECONDS VALUE REGISTER (ADDRESS 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **HSECTEN<3:0>:** Binary-Coded Decimal Value of Hundredth of Second's Tens Digit
Contains a value from 0 to 9

bit 3-0 **HSECONE<3:0>:** Binary-Coded Decimal Value of Hundredth of Second's Ones Digit
Contains a value from 0 to 9

REGISTER 5-2: RTCSEC: TIMEKEEPING SECONDS VALUE REGISTER (ADDRESS 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **ST:** Start Oscillator bit
1 = Oscillator enabled
0 = Oscillator disabled

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second's Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second's Ones Digit
Contains a value from 0 to 9

REGISTER 5-3: RTCMIN: TIMEKEEPING MINUTES VALUE REGISTER (ADDRESS 0x02)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit
Contains a value from 0 to 9

REGISTER 5-4: RTCHOUR: TIMEKEEPING HOURS VALUE REGISTER (ADDRESS 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIMSIGN	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **TRIMSIGN:** Trim Sign bit
1 = Add clocks to correct for slow time
0 = Subtract clocks to correct for fast time

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **TRIMSIGN:** Trim Sign bit
1 = Add clocks to correct for slow time
0 = Subtract clocks to correct for fast time

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

REGISTER 5-5: RTCWKDAY: TIMEKEEPING WEEKDAY VALUE REGISTER (ADDRESS 0x04)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OSCRUN:** Oscillator Status bit
1 = Oscillator is enabled and running
0 = Oscillator has stopped or has been disabled

bit 4 **PWRFAIL:** Power Failure Status bit(1,2)
1 = Primary power was lost and the power-fail timestamp registers have been loaded (must be cleared in software). Clearing this bit resets the power-fail timestamp registers to '0'.
0 = Primary power has not been lost

bit 3 **VBATEN:** External Battery Backup Supply (VBAT) Enable bit
1 = VBAT input is enabled
0 = VBAT input is disabled

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day of Week
Contains a value from 1 to 7. The representation is user-defined.

Note 1: The PWRFAIL bit must be cleared to log new timestamp data. This is to ensure previous timestamp data is not lost.

2: The PWRFAIL bit can be cleared by writing a '0'. Once cleared, the PWRFAIL bit cannot be written to a '1' in software.

REGISTER 5-6: RTCDATE: TIMEKEEPING DATE VALUE REGISTER (ADDRESS 0x05)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 5-7: RTCMTH: TIMEKEEPING MONTH VALUE REGISTER (ADDRESS 0x06)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **LPYR:** Leap Year bit
1 = Year is a leap year
0 = Year is not a leap year

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

REGISTER 5-8: RTCYEAR: TIMEKEEPING YEAR VALUE REGISTER (ADDRESS 0x07)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **YRTEN<3:0>:** Binary-Coded Decimal Value of Year's Tens Digit
Contains a value from 0 to 9

bit 3-0 **YRONE<3:0>:** Binary-Coded Decimal Value of Year's Ones Digit
Contains a value from 0 to 9

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMEKEEPING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCHSEC	HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0	18
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	18
RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	18
RTCHOUR	TRIMSIGN	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	19
RTCWKDAY	—	—	OSCRUN	PWRFAIL	VBATEN	WKDAY2	WKDAY1	WKDAY0	20
RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	20
RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	21
RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	21

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in timekeeping.

5.4 Alarms

The MCP795WXX features two independent alarms. Each alarm can be used to either generate an interrupt at a specific time in the future, or to generate a periodic interrupt every second (Alarm 1 only), minute, hour, day, day of week, or month.

There is a separate interrupt flag, ALMxIF, for each alarm. The interrupt flags are set by hardware when the chosen alarm mask condition matches (Table 5-5 and Table 5-6). The interrupt flags must be cleared in software.

Each alarm can independently be assigned to either the $\overline{\text{IRQ}}$ pin or the $\overline{\text{WDO}}$ pin by configuring the ALMxPIN bits. Refer to **Section 5.8 "Interrupt Outputs"** for details. The alarm interrupt output is available while operating from the backup power supply, regardless of the output pin assignments.

All time and date values are stored in the registers as binary-coded decimal (BCD) values.

Note:	Throughout this section, references to the register and bit names for the alarm modules are referred to generically by the use of 'x' in place of the specific module number. Thus, "ALMxSEC" might refer to the seconds register for Alarm 0 or Alarm 1.

TABLE 5-5: ALARM 0 MASKS

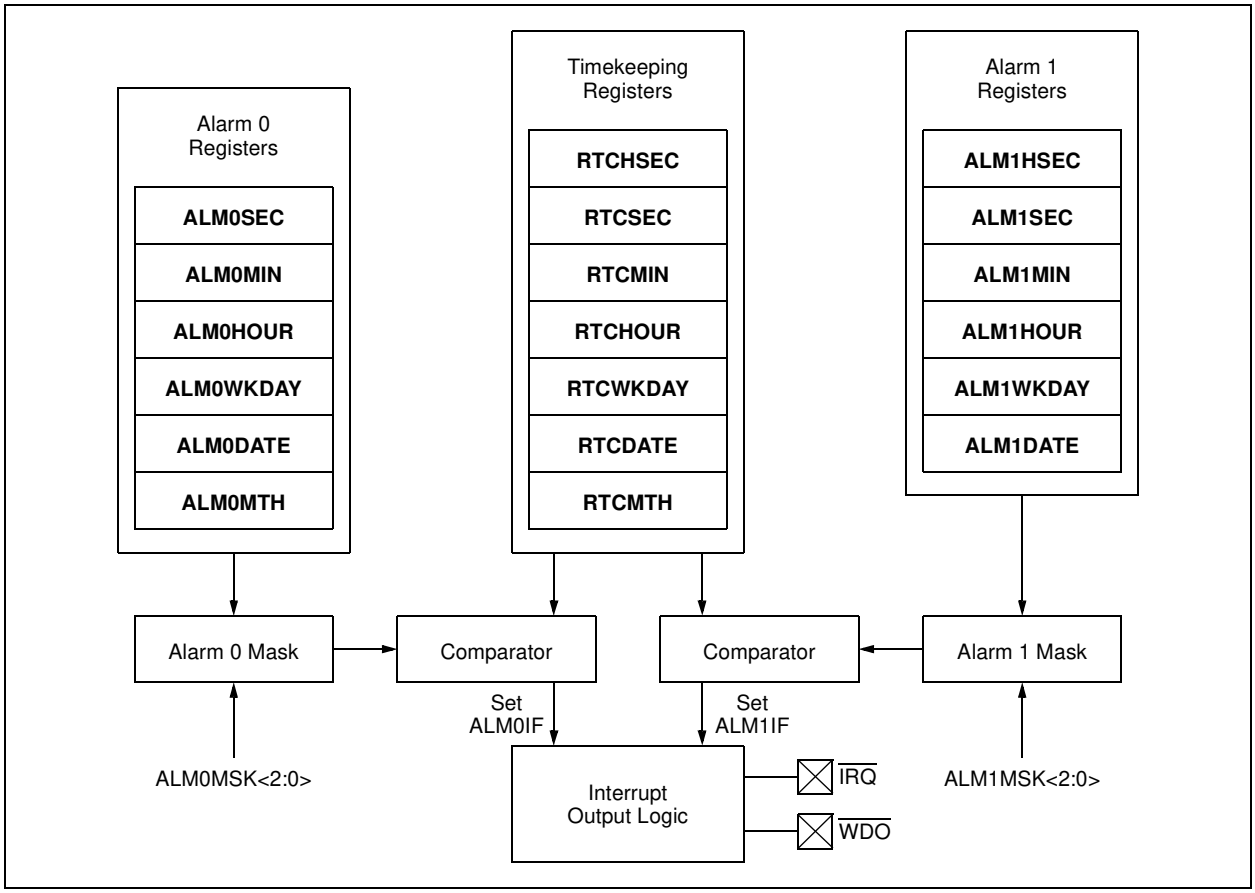
ALM0MSK<2:0>	Alarm 0 Asserts on Match of
000	Seconds
001	Minutes
010	Hours
011	Day of Week
100	Date
101	Reserved
110	Reserved
111	Seconds, Minutes, Hours, Day of Week, Date, and Month

TABLE 5-6: ALARM 1 MASKS

ALM1MSK<2:0>	Alarm 1 Asserts on Match of
000	Seconds
001	Minutes
010	Hours
011	Day of Week
100	Date
101	Hundredth of Seconds
110	Reserved
111	Seconds, Minutes, Hours, Day of Week, and Date

Note 1:	The alarm interrupt flags must be cleared by the user.
2:	Loading invalid values into the alarm registers will result in undefined operation.

FIGURE 5-7: ALARM BLOCK DIAGRAM



5.4.1 CONFIGURING THE ALARM

In order to configure the alarm modules, the following steps need to be performed:

1. Load the timekeeping registers and enable the oscillator.
2. Configure the ALMxMSK<2:0> bits to select the desired alarm mask.
3. Set or clear the ALMxPIN bit according to the desired output pin assignment.
4. Ensure the ALMxIF flag is cleared.
5. Based on the selected alarm mask, load the alarm match value into the appropriate register(s).
6. Enable the alarm module by setting the ALMxEN bit.

REGISTER 5-9: ALM1HSEC: ALARM 1 HUNDREDTHS OF SECONDS VALUE REGISTER (ADDRESS 0x12)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HSECTEN3	HSECTEN2	HSECTEN1	HSECTEN0	HSECONE3	HSECONE2	HSECONE1	HSECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **HSECTEN<3:0>:** Binary-Coded Decimal Value of Hundredth of Second's Tens Digit
Contains a value from 0 to 9

bit 3-0 **HSECONE<3:0>:** Binary-Coded Decimal Value of Hundredth of Second's Ones Digit
Contains a value from 0 to 9

Note 1: Hundredth of seconds matching is only available on Alarm 1.

REGISTER 5-10: ALMxSEC: ALARM 0/1 SECONDS VALUE REGISTER (ADDRESSES 0x0C/0x13)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second's Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second's Ones Digit
Contains a value from 0 to 9

REGISTER 5-11: ALMxMIN: ALARM 0/1 MINUTES VALUE REGISTER (ADDRESSES 0x0D/0x14)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit
Contains a value from 0 to 9

REGISTER 5-12: ALMxHOUR: ALARM 0/1 HOURS VALUE REGISTER (ADDRESSES 0x0E/0x15)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit(1)
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit(1)
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

Note 1: This bit is read-only and reflects the value of the 12/$\overline{24}$ bit in the RTCHOUR register.