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MCP8024

3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module

Features:

- Three Half-bridge Drivers Configured to Drive External High-Side NMOS and Low-Side NMOS MOSFETs:
  - Independent input control for high-side NMOS and low-side NMOS MOSFETs
  - Peak output current: 0.5A @ 12V
  - Shoot-through protection
  - Overcurrent and short circuit protection
- Adjustable Output Buck Regulator (750 mW)
- Fixed Output Linear Regulators:
  - 5V @ 20 mA
  - 12V @ 20 mA
- Internal Bandgap Reference
- Three Operational Amplifiers for Motor Phase Current Monitoring and Position Detection
- Overcurrent Comparator
- Two Level Translators
- Operational Voltage Range 6 - 40V
- Undervoltage Lockout (UVLO): 6V
- Overvoltage Lockout (OVLO): 28V
- Transient (100 ms) Voltage Tolerance: 48V
- Extended Temperature Range: T_A -40 to +150°C
- Thermal Shutdown

Applications:

- Automotive Fuel, Water, Ventilation Motors
- Home Appliances
- Permanent Magnet Synchronous Motor (PMSM) Control
- Hobby Aircraft, Boats, Vehicles

Related Literature:

- AN885, “Brushless DC (BLDC) Motor Fundamentals”, DS00885, Microchip Technology Inc., 2003
- AN1160, “Sensorless BLDC Control with Back-EMF Filtering Using a Majority Function”, DS01160, Microchip Technology Inc., 2008
- AN1078, “Sensorless Field Oriented Control of a PMSM”, DS01078, Microchip Technology Inc., 2010

Description:

The MCP8024 is a 3-Phase Brushless DC (BLDC) power module. The MCP8024 device integrates three half-bridge drivers to drive external NMOS/NMOS transistor pairs configured to drive a 3-phase BLDC motor, a comparator, a voltage regulator to provide bias to a companion microcontroller, power monitoring comparators, an overtemperature sensor, two level translators and three operational amplifiers for motor current monitoring.

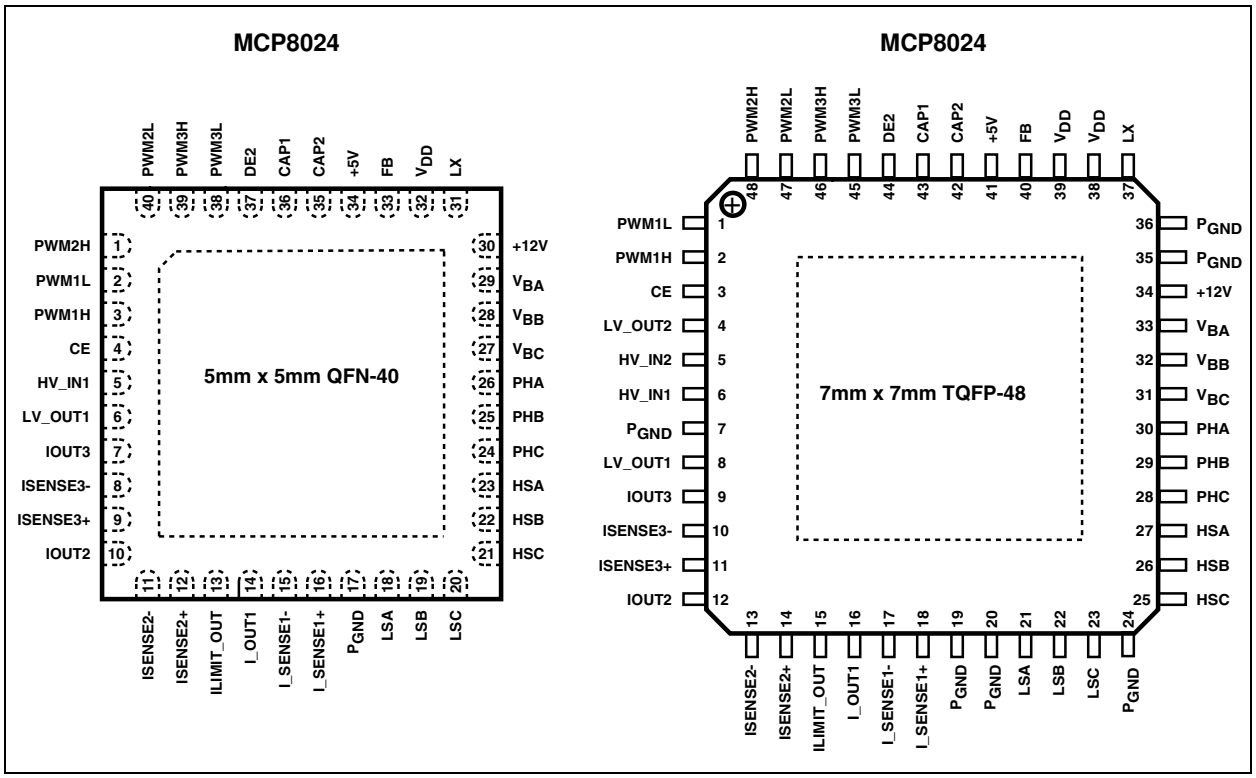
The MCP8024 has three half-bridge drivers capable of delivering a peak output current of 0.5A at 12V for driving high-side and low-side NMOS MOSFET transistors. The drivers have shoot-through, overcurrent, and short-circuit protection.

The MCP8024 buck converter is capable of delivering 750 mW of power for powering a companion microcontroller. The buck regulator may be disabled if not used. The on-board 5V and 12V low dropout voltage regulators are capable of delivering 20 mA of current.

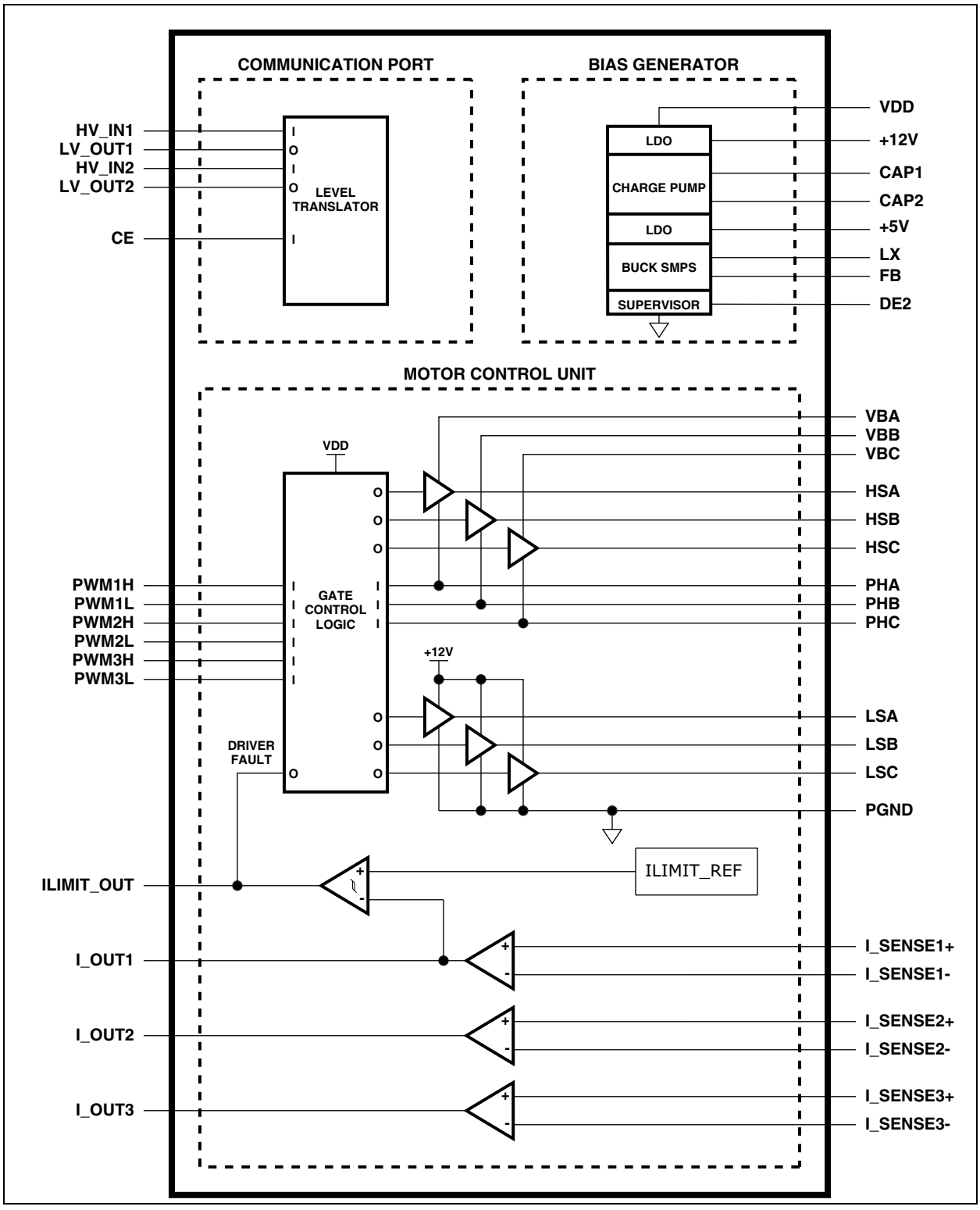
The MCP8024 operation is specified over a temperature range of -40°C to +150°C.

Package options include the 40-lead 5x5 QFN and 48-lead 7x7 TQFP.

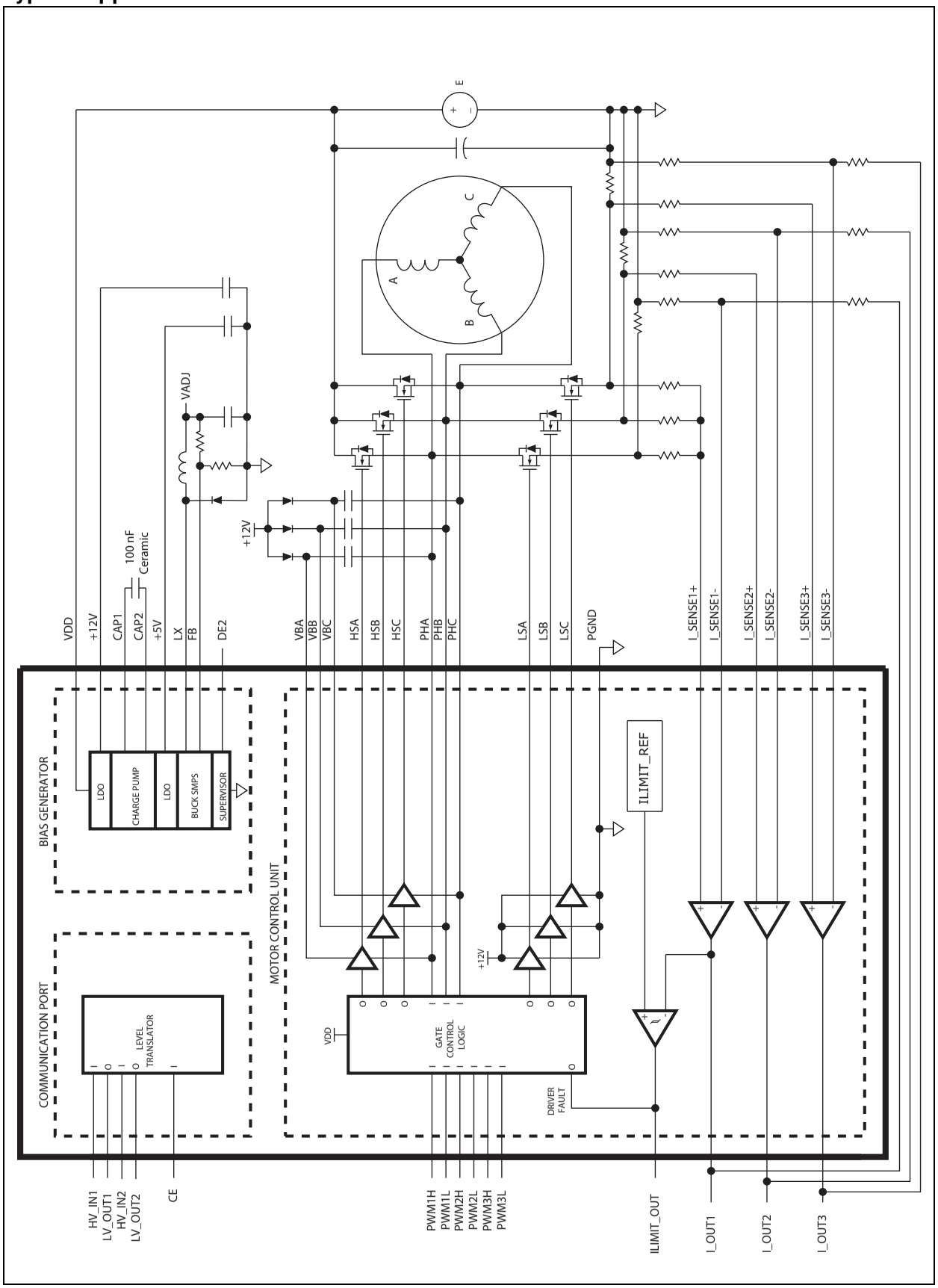
Package Types



Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{DD} ..... +46.0V
Input Voltage, < 100 ms Transient ..... +48.0V
Internal Power Dissipation ..... Internally-Limited
Operating Ambient Temperature Range ..... -40°C to +150°C
Operating Junction Temperature (Note 1) ..... -40°C to +160°C
Transient Junction Temperature* ..... +170°C
Storage temperature (Note 1) ..... -55°C to +150°C
Digital I/O ..... -0.3V to 5.5V
LV Analog I/O ..... -0.3V to 5.5V

ESD and Latch-up protection:
V_{DD}, HV_IN1 pins ..... ≥ 12 kV HMM and ≥ 750V CDM
All other pins ..... ≥ 4 kV HBM and ≥ 750V CDM
Latch-up protection - all pins..... > 100 mA

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

*** Notice:** Transient junction temperatures should not exceed one second in duration. Sustained junction temperatures above 170°C may impact the device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted T_J = -40°C to +150°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Operating Voltage	V_{DD}	6.0 6.0	— —	28.0 40	V	Operating Shutdown
Transient Maximum Voltage	V_{DDmax}	—	—	48	V	< 100 ms
Input Quiescent Current	I_Q	— — — — — —	— 171 197 200 200 900	— 220 — — 500 —	µA	V_{DD} = 13V, disabled, CE = 0V, T_J = 25°C disabled, CE = 0V, T_J = 85°C disabled, CE = 0V, T_J = 130°C disabled, CE = 0V, T_J = 150°C active, CE > $V_{DIG\_HI\_TH}$
Digital Input/Output	$DIGITAL_{I/O}$	0	—	5.5	V	
Digital Open-Drain Drive Strength	$DIGITAL_{IOL}$	—	1	—	mA	V_{DS} < 50 mV
Digital Input Rising Threshold	$V_{DIG\_HI\_TH}$	1.26	—	—	V	
Digital Input Falling Threshold	$V_{DIG\_LO\_TH}$	—	—	0.54	V	
Digital Input Hysteresis	V_{DIG_HYS}	—	500	—	mV	
Digital Input Current	I_{DIG}	— —	30 0.2	100 —	µA	V_{DIG} = 3.0V V_{DIG} = 0V
Analog Low-Voltage Input	$ANALOG_{VIN}$	0	—	5.5	V	Excludes high voltage
Analog Low-Voltage Output	$ANALOG_{VOUT}$	0	—	V_{OUT5}	V	Excludes high voltage
BIAS GENERATOR						
+12V Regulated Charge Pump						
Charge Pump Current	I_{CP}	20	—	—	mA	V_{DD} = 9.0V
Charge Pump Voltage	V_{CP}	+10	2 * V_{DD}	—	V	V_{DD} = 9.0V, I_{CP} = 20 mA
Charge Pump Start	CP_{START}	11.0	11.5	—	V	V_{DD} falling

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 150°C can impact the device reliability and OTP data retention.

2: 1000 hour cumulative maximum for OTP data retention (typical).

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted T_J = -40°C to +150°C.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Charge Pump Stop	CP_{STOP}	—	12.0	12.5	V	V_{DD} rising
Charge Pump Frequency (50% charging / 50% discharging)	CP_{FSW}	— —	76.80 0	— —	kHz	V_{DD} = 9.0V V_{DD} = 12.5V (stopped)
Charge Pump Switch Resistance	CP_{RDSON}	—	14	—	Ω	RDS_{ON} sum of high side and low side
Output Voltage	V_{OUT12}	10	12	—	V	$V_{DD} = V_{OUT12}$ + 1V, I_{OUT} = 1 mA
Output Voltage Tolerance	$\|TOLV_{OUT12}\|$	—	—	4.0	%	$V_{DD} = V_{OUT12}$ + 1V, I_{OUT} = 1 mA
Output Current	I_{OUT}	20	—	—	mA	Average current
Output Current Limit	I_{LIMIT}	30	40	—	mA	Average current
Output Voltage Temperature Coefficient	TCV_{OUT12}	—	50	—	ppm/°C	
Line Regulation	$\|\Delta V_{OUT}/(V_{OUT} X \Delta V_{DD})\|$	—	0.1	0.5	%/V	13V < V_{DD} < 19V, I_{OUT} = 20 mA
Load Regulation	$\|\Delta V_{OUT}/V_{OUT}\|$	—	0.2	0.5	%	I_{OUT} = 0.1 mA to 15 mA
Dropout Voltage	V_{DD}-V_{OUT12}	—	380	—	mV	I_{OUT} = 20 mA, measurement taken when output voltage drops 2% from no-load value.
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA
+5V Linear Regulator						
Output Voltage	V_{OUT5}	—	5	—	V	$V_{DD} = V_{OUT5}$ + 1V, I_{OUT} = 1 mA
Output Voltage Tolerance	$\|TOLV_{OUT5}\|$	—	—	4.0	%	
Output Current	I_{OUT}	20	—	—	mA	Average current
Output Current Limit	I_{LIMIT}	30	40	—	mA	Average current
Output Voltage Temperature Coefficient	$\|TCV_{OUT5}\|$	—	50	—	ppm/°C	
Line Regulation	$\|\Delta V_{OUT}/(V_{OUT} X \Delta V_{DD})\|$	—	0.1	0.5	%/V	6V < V_{DD} < 19V, I_{OUT} = 20 mA
Load Regulation	$\|\Delta V_{OUT}/V_{OUT}\|$	—	0.2	0.5	%	I_{OUT} = 0.1 mA to 15 mA
Dropout Voltage	V_{DD}-V_{OUT5}	—	180	350	mV	I_{OUT} = 20 mA, measurement taken when output voltage drops 2% from no-load value.
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA
Buck Regulator						
Feedback Voltage	V_{FB}	1.19	1.25	1.31	V	
Feedback Voltage Tolerance	$\|TOLV_{FB}\|$	—	—	5.0	%	I_{FB} = 1 µA

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 150°C can impact the device reliability and OTP data retention.

2: 1000 hour cumulative maximum for OTP data retention (typical).

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted T_J = -40°C to +150°C.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Feedback Voltage Line Regulation	$\lvert(\Delta V_{FB}/V_{FB}) / \Delta V_{DD}\rvert$	—	0.1	0.5	%/V	V_{DD} = 6V to 28V
Feedback Voltage Load Regulation	$\lvert\Delta V_{FB} / V_{FB}\rvert$	—	0.1	0.5	%	I_{OUT} = 5 mA to 150 mA
Feedback Input Bias Current	I_{FB}	-100	—	+100	nA	Sink/Source
Switching Frequency	f_{SW}	—	461	—	kHz	
Duty Cycle Range	DC_{MAX}	3	—	96	%	
PMOS Switch On Resistance	R_{DSON}	—	0.6	—	Ω	V_{DD} = 13V, T_J=25°C
PMOS Switch Current Limit	$I_{P(MAX)}$	—	2.5	—	A	
Ground Current – PWM Mode	I_{GND}	—	1.5	2.5	mA	Switching
Quiescent Current – PFM Mode	I_Q	—	150	200	µA	I_{OUT} = 0mA
Output Voltage Adjust Range	V_{OUT}	2.0	—	5.0	V	
Output Current	I_{OUT}	150	—	—	mA	5v
		250	—	—		3v
Output Power	P_{OUT}	—	750	—	mW	$P = I_{OUT} * V_{OUT}$
Voltage Supervisor						
Undervoltage Lockout Start	$UVLO_{STRT}$	—	6.0	6.25	V	V_{DD} rising
Undervoltage Lockout Stop	$UVLO_{STOP}$	5.1	5.5	—	V	V_{DD} falling
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	0.35	0.5	0.65	V	
Overvoltage Lockout All Functions Disabled	$OVLO_{STOP}$	—	32.0	33.0	V	V_{DD} rising
Overvoltage Lockout All Functions Enabled	$OVLO_{STRT}$	29.0	30.0	—	V	V_{DD} falling
Overvoltage Lockout Hysteresis	$OVLO_{HYS}$	1.0	2.0	3.0	V	
Temperature Supervisor						
Thermal Warning Temperature (115°C)	T_{WARN}	—	72	—	%	Rising temperature, percentage of thermal shutdown temperature “MIN”
Thermal Warning Hysteresis	ΔT_{WARN}	—	15	—	°C	Falling temperature
Thermal Shutdown Temperature	T_{SD}	160	170	—	°C	Rising temperature
Thermal Shutdown Hysteresis	ΔT_{SD}	—	25	—	°C	Falling temperature
MOTOR CONTROL UNIT						
Output Drivers						
PWMH/L Input Pull-Down	R_{PULLDN}	32	47	62	kΩ	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 150°C can impact the device reliability and OTP data retention.

2: 1000 hour cumulative maximum for OTP data retention (typical).

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted T_J = -40°C to +150°C.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Driver Source Current	I_{SOURCE}	0.3	—	—	A	V_{DD} = 12V, H[A:C], L[A:C]
Output Driver Sink Current	I_{SINK}	0.3	—	—	A	V_{DD} = 12V, H[A:C], L[A:C]
Output Driver Source Resistance	R_{DSON}	—	17	—	Ω	I_{OUT} = 10 mA, V_{DD} = 12V, H[A:C], L[A:C]
Output Driver Sink Resistance	R_{DSON}	—	17	—	Ω	I_{OUT} = 10 mA, V_{DD} = 12V, H[A:C], L[A:C]
Output Driver UVLO Threshold	D_{UVLO}	7.2	8.0	—	V	
Output Driver Bootstrap Voltage (w/ respect to ground)	$V_{BOOTSTRAP}$	— —	— —	44 48	V	Continuous < 100 ms
Output Driver HS Drive Voltage	V_{HS}	8.0 -5.5	12 —	13.5 —	V	With respect to Phase pin With respect to ground
Output Driver LS Drive Voltage	V_{LS}	8.0	12	13.5	V	With respect to ground
Output Driver Phase Pin Voltage	V_{PHASE}	-5.5V	—	34	V	With respect to ground
Output Driver Short Circuit Protection Threshold	D_{SC}	— — — — —	— 0.250 0.500 0.750 1.000	— — — — —	V	Set by DE2 CONFIG[1:0] word 00 - Default 01 10 11
Output Driver Short Circuit Detected Propagation Delay	D_{SC_DEL}	— — — —	— 430 10 —	— — — —	ns	C_{LOAD} = 1000 pF, V_{DD} =12V, detection after blanking detection during blanking, value is delay after blanking
Output Driver Turn-off Propagation Delay	T_{DEL_OFF}	—	100	250	ns	C_{LOAD} = 1000 pF, V_{DD} =12V,
Output Driver Turn-on Propagation Delay	T_{DEL_ON}	—	100	250	ns	C_{LOAD} = 1000 pF, V_{DD} =12V,
Standby to Motor Operational (C_{LOAD} = 10 µF) CE Low to Standby State CE Fault Clearing Pulse	t_{MOTOR} $t_{STANDBY}$ t_{FAULT_CLR}	— — — 1	10 — 10 —	50 10 — —	µs ms µs µs	CE High-Low-High Transition < 100 µs (Fault Clearing) Standby state to Operational state Time after CE = 0V CE High-Low-High Transition Time
Current Sense Amplifier						
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	V_{CM} = 0V T_A = -40°C to +150°C
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	V_{CM} = 0V
Input Bias Current	I_B	-1	—	+1	µA	
Common Mode Input Range	V_{CMR}	-0.3	—	3.5	V	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 150°C can impact the device reliability and OTP data retention.

2: 1000 hour cumulative maximum for OTP data retention (typical).

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted T_J = -40°C to +150°C.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Common Mode Rejection Ratio	CMRR	65	80	—	dB	Freq = 1 kHz, I_{OUT} = 10 µA
Maximum Output Voltage Swing	V_{OL}, V_{OH}	0.05	—	4.5	V	I_{OUT} = 200 µA
Slew Rate	SR	—	±7	—	V/µs	Symmetrical
Gain Bandwidth Product	GBWP	—	10.0	—	MHz	
Current Comparator Hysteresis	CC_{HYS}	—	10	—	mV	
Current Comparator Common Mode Input Range	V_{CC_CMR}	1.0	—	4.5	V	
Current Limit DAC						
Resolution		—	8	—	Bits	
Output Voltage Range	V_{OL}, V_{OH}	0.991	—	4.503	V	I_{OUT} = 1 mA
Output Voltage	V_{DAC}	— — — —	— 0.991 1.872 4.503	— — — —	V	Code * 13.77 mV/Bit + 0.991V Code 00H Code 40H Code FFH
Input to Output Delay	T_{DELAY}	—	50	—	µs	5 time constants of 100 kHz filter
Integral Nonlinearity	INL	-0.5	—	+0.5	%FSR	%Full Scale Range
Differential Nonlinearity	DNL	-50	—	+50	%LSB	%LSB
ILIMIT_OUT Sink Current (Open-Drain)	IL_{OUT}	—	1	—	mA	V_{ILIMIT_OUT} <= 50mV
Voltage Level Translator						
High-Voltage Input Range	VIN	0	—	VDD	V	
Low-Voltage Output Range	VOUT	0	—	5.0V	V	
Input Pull-up Resistor	RPU	20	30	47	kΩ	
High-Level Input Voltage	VIH	0.60	—	—	V_{DD}	V_{DD} = 15V
Low-Level Input Voltage	VIL	—	—	0.40	V_{DD}	V_{DD} = 15V
Input Hysteresis	VHYS	—	—	0.30	V_{DD}	
Propagation Delay	TLV_OUT	—	3.0	6.0	µs	
Maximum Communication Frequency	FMAX	—	—	20	kHz	
Low-Voltage Output Sink Current (Open-Drain)	IOL	—	1	—	mA	V_{OUT} <= 50 mV
OTP Data Retention						
OTP Cell High Temperature Operating Life	HTOL	—	1000	—	Hours	T_J = 150°C (**Note 2**)
OTP Cell Operating Life		—	10	—	Years	T_J = 85°C

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 150°C can impact the device reliability and OTP data retention.

2: 1000 hour cumulative maximum for OTP data retention (typical).

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges (Notes 1)						
Specified Temperature Range	T_A	-40		+150	°C	
Operating Temperature Range	T_A	-40		+150	°C	
Storage Temperature Range	T_A	-55		+150	°C	(**Note 2**)
Thermal Package Resistance						
5mm x 5mm QFN-40	θ_{JA} θ_{JC}	— —	34 5.2	— —	°C/W	4-Layer JC51-7 standard board, natural convection
7mm x 7mm TQFP-48-EP	θ_{JA} θ_{JC}	— —	30 15	— —	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

2: 1000 hour cumulative maximum for OTP data retention (typical).

ESD, SUSCEPTIBILITY, SURGE, AND LATCH-UP TESTING

Parameter	Standard and Test Condition	Value
Input voltage surges	ISO 16750-2	28V for 1 minute, 45V for 0.5 seconds
ESD HBM with 1.5 kΩ / 100 pF	ESD-STM5.1-2001 JESD22-A114E 2007 CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref_D	±4 kV
ESD CDM (Charged Device Model, field-induced method – replaces machine-model method)	ESD-STM5.3.1-1999	±750 V all pins
Latch-up Susceptibility	AEC Q100-004, 150°C	>100 mA

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

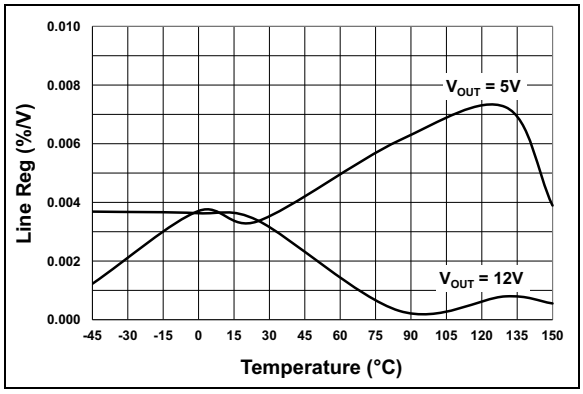


FIGURE 2-1: *LDO Line Regulation vs Temperature.*

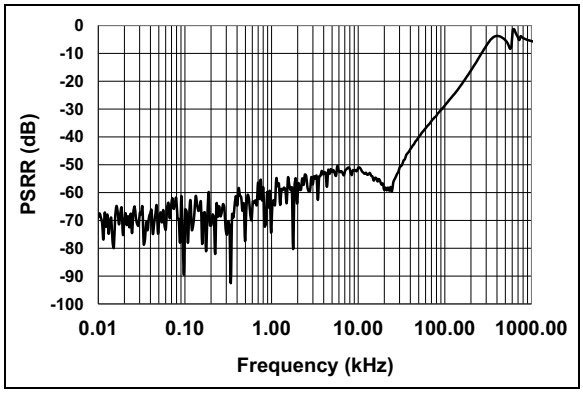


FIGURE 2-4: *12 V LDO Power Supply Ripple Rejection vs Frequency.*

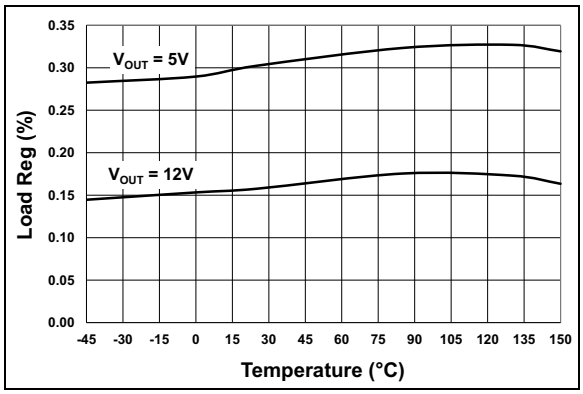


FIGURE 2-2: *LDO Load Regulation vs Temperature.*

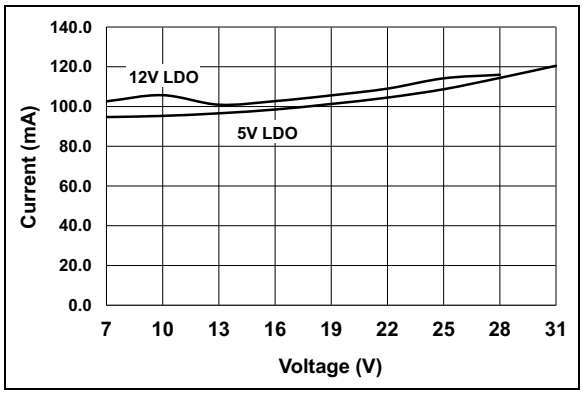


FIGURE 2-5: *LDO Short Circuit Current vs Input Voltage.*

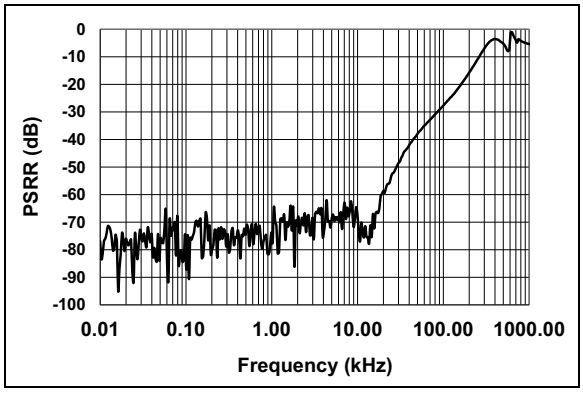


FIGURE 2-3: *5V LDO Power Supply Ripple Rejection vs Frequency.*

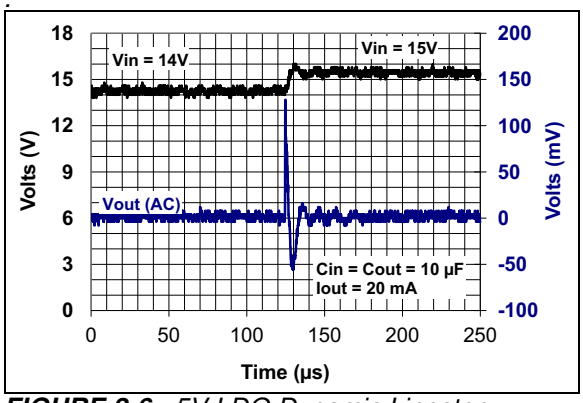


FIGURE 2-6: *5V LDO Dynamic Linestep - Rising V_{DD}.*

Note: Unless otherwise indicated: T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

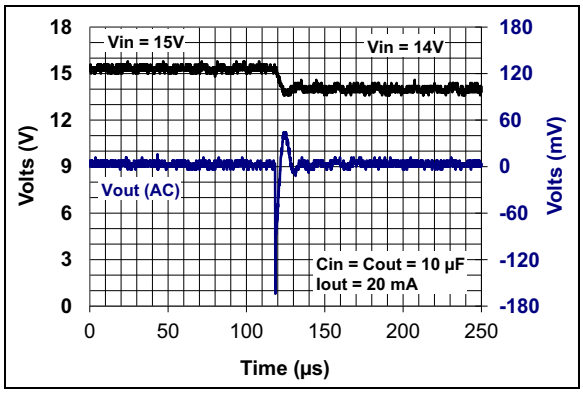


FIGURE 2-7: *5V LDO Dynamic Linestep - Falling V_{DD}.*

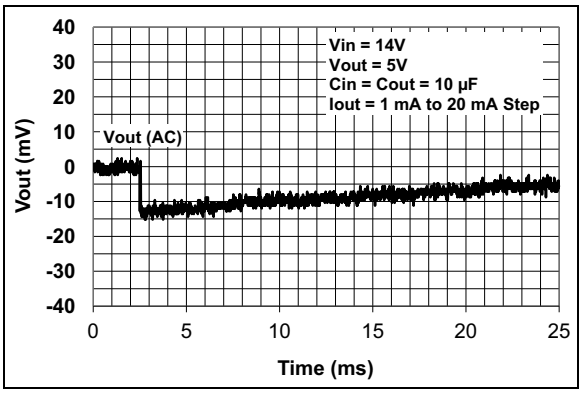


FIGURE 2-10: *5V LDO Dynamic Loadstep - Rising Current.*

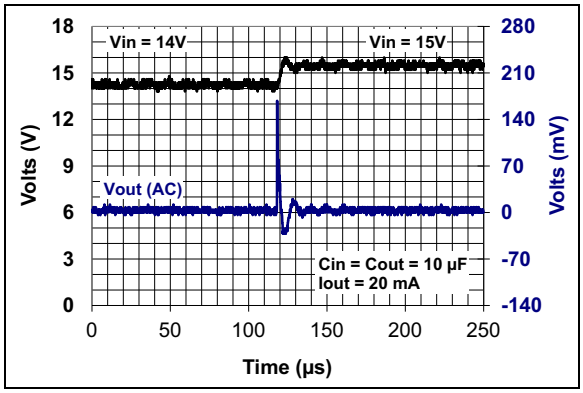


FIGURE 2-8: *12V LDO Dynamic Linestep - Rising V_{DD}.*

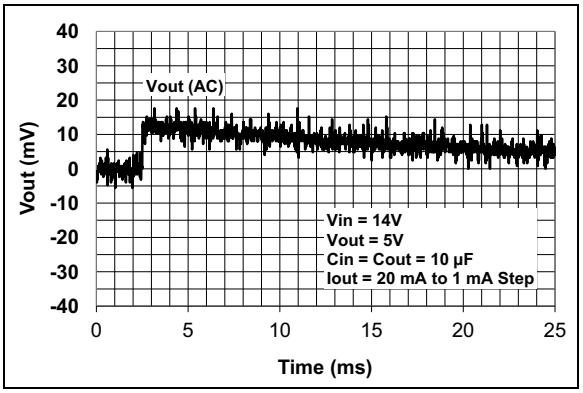


FIGURE 2-11: *5V LDO Dynamic Loadstep - Falling Current.*

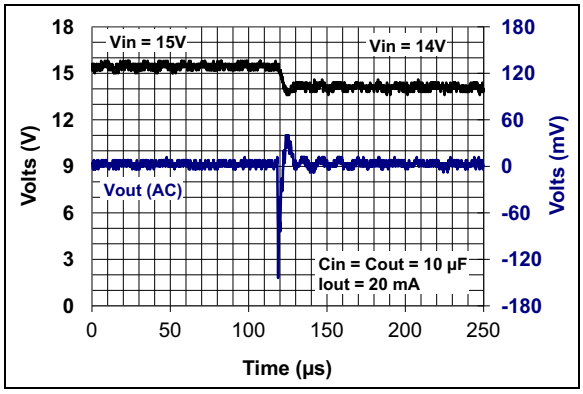


FIGURE 2-9: *12V LDO Dynamic Linestep - Falling V_{DD}.*

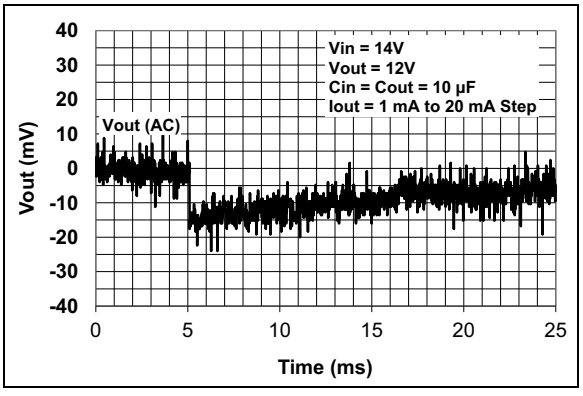


FIGURE 2-12: *12V LDO Dynamic Loadstep - Rising Current.*

Note: Unless otherwise indicated: T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

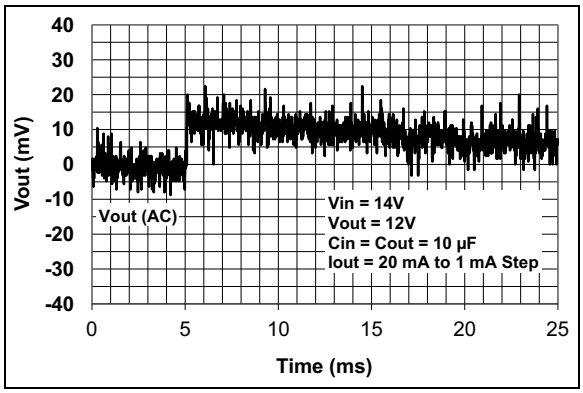


FIGURE 2-13: *12V LDO Dynamic Loadstep - Falling Current.*

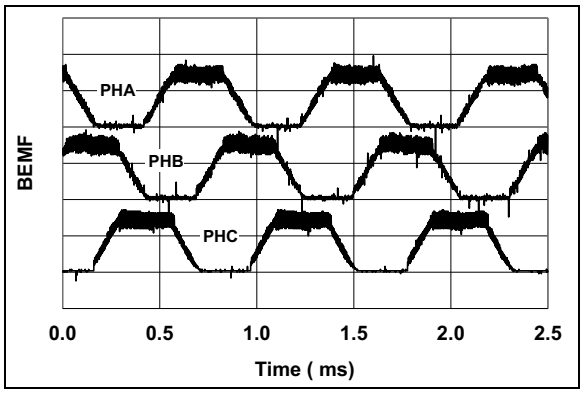


FIGURE 2-16: *Trapezoidal Back EMF.*

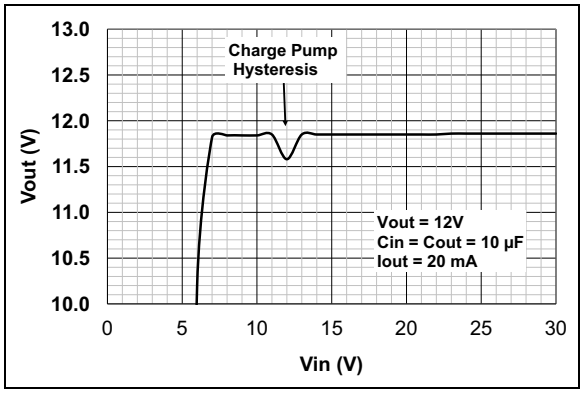


FIGURE 2-14: *12V LDO Output Voltage vs Rising Input Voltage.*

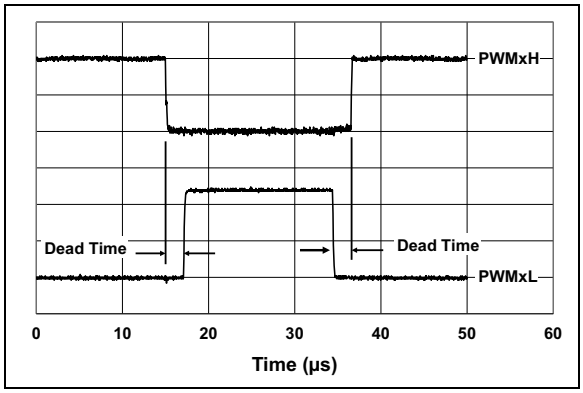


FIGURE 2-17: *PWM Deadtime.*

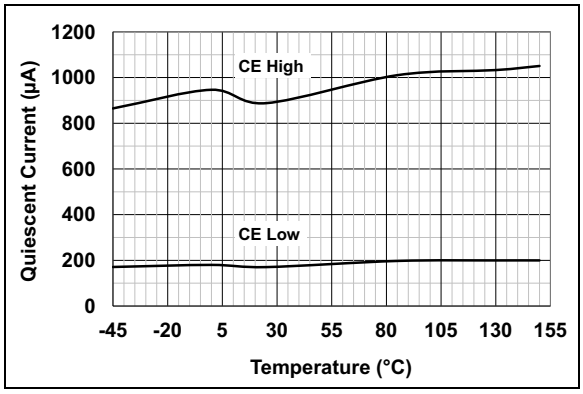


FIGURE 2-15: *Quiescent Current vs Temperature.*

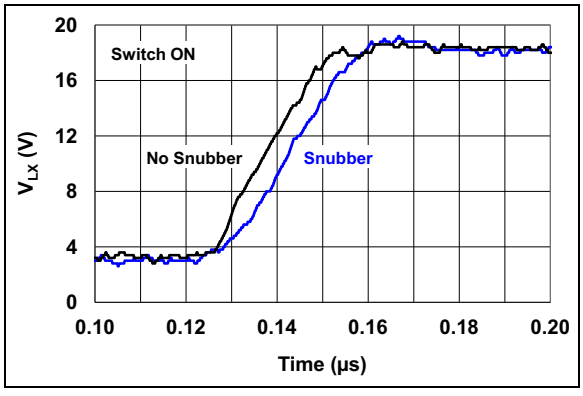


FIGURE 2-18: *Buck Snubber Turn On.*

Note: Unless otherwise indicated: T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

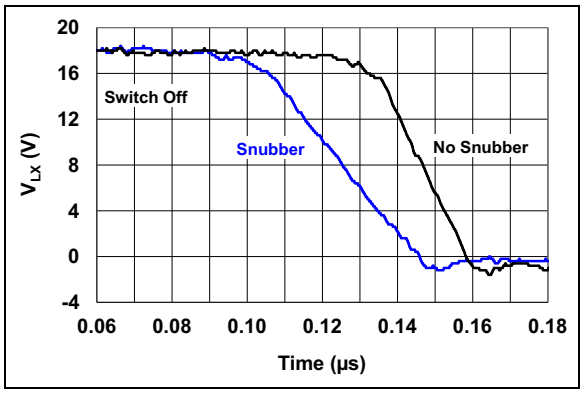


FIGURE 2-19: *Buck Snubber Turn Off.*

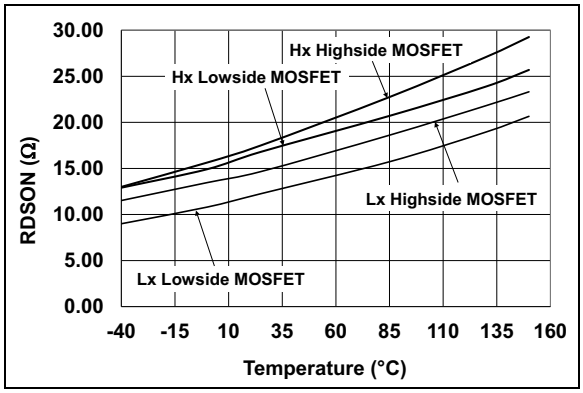


FIGURE 2-20: *Gate Driver RDS_{ON} vs Temperature.*

3.0 PIN DESCRIPTIONS

3.1 Functional Pin Descriptions

Pin No. QFN	Pin No. TQFP	Symbol	I/O	Description
1	48	PWM2H	I	Digital input, phase B high-side control, 47K pulldown
2	1	PWM1L	I	Digital input, phase A low-side control, 47K pulldown
3	2	PWM1H	I	Digital input, phase A high-side control, 47K pulldown
4	3	CE	I	Digital input, device enable, 47K pulldown
-	4	LV_OUT2	O	Digital logic level translated output interface, open drain
-	5	HV_IN2	I	High-voltage input interface, 30K pullup via Configuration register 0 bit 6
5	6	HV_IN1	I	High-voltage input interface, 30K pullup via Configuration register 0 bit 6
-	7	PGND	Power	Power 0V reference
6	8	LV_OUT1	O	Digital logic level translated output interface, open drain
7	9	I_OUT3	O	Motor phase current sense amplifier output
8	10	ISENSE3-	I	Motor phase current sense amplifier inverting input
9	11	ISENSE3+	I	Motor phase current sense amplifier non-inverting input
10	12	I_OUT2	O	Motor phase current sense amplifier output
11	13	ISENSE2-	I	Motor phase current sense amplifier inverting input
12	14	ISENSE2+	I	Motor phase current sense amplifier non-inverting input
13	15	/ILIMIT_OUT	O	Current limit comparator, MOSFET driver fault output, open drain
14	16	I_OUT1	O	Motor current sense amplifier output
15	17	ISENSE1-	I	Motor current sense amplifier inverting input
16	18	ISENSE1+	I	Motor current sense amplifier non-inverting input
17	19,20	PGND	Power	Power 0V reference
18	21	LA	O	Phase A low-side N-Channel MOSFET driver, active-high
19	22	LB	O	Phase B low-side N-Channel MOSFET driver, active-high
20	23	LC	O	Phase C low-side N-Channel MOSFET driver, active-high
-	24	PGND	Power	Power 0V reference
21	25	HC	O	Phase C high-side N-Channel MOSFET driver, active-high
22	26	HB	O	Phase B high-side N-Channel MOSFET driver, active-high
23	27	HA	O	Phase A high-side N-Channel MOSFET driver, active-high
24	28	PHC	I/O	Phase C high-side MOSFET driver reference, back EMF sense input
25	29	PHB	I/O	Phase B high-side MOSFET driver reference, back EMF sense input
26	30	PHA	I/O	Phase A high-side MOSFET driver reference, back EMF sense input
27	31	VBC	Power	Phase C high-side MOSFET driver bias
28	32	VBB	Power	Phase B high-side MOSFET driver bias
29	33	VBA	Power	Phase A high-side MOSFET driver bias
30	34	+12V	Power	Analog circuitry and low-side gate drive bias
-	35,36	PGND	Power	Power 0V reference
31	37	LX	Power	Buck regulator switch node, external inductor connection
32	38, 39	VDD	Power	Input supply
33	40	FB	I	Buck regulator feedback node
34	41	+5V	Power	Internal circuitry bias
35	42	CAP2	Power	Charge pump flying capacitor input
36	43	CAP1	Power	Charge pump flying capacitor input
37	44	DE2	O	Voltage and temperature supervisor output, open drain
38	45	PWM3L	I	Digital input, phase C low-side control, 47K pulldown
39	46	PWM3H	I	Digital input, phase C high-side control, 47K pulldown
40	47	PWM2L	I	Digital input, phase B low-side control, 47K pulldown
EP	EP	PGND	Power	Exposed Pad, Connect to Power 0V reference

3.2 V_{DD}

Connect V_{DD} to the main supply voltage. This voltage must not exceed the maximum operating limits of the device. Connect a bulk capacitor close to this pin for good load step performance and transient protection.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.3 PGND, Exposed Pad (EP)

Device ground. The PCB ground traces should be short, wide, and form a STAR pattern to the power source. The Exposed Pad (EP) PCB area should be a copper pour with thermal vias to help transfer heat away from the device.

3.4 +12V

+12 volt Low Dropout (LDO) voltage regulator output. The +12V LDO may be used to power external devices such as Hall-effect sensors or amplifiers. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the +12V pin as is practical. For most applications, 4.7 µF of capacitance will ensure stable operation of the LDO circuit.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.5 +5V

+5 volt Low Dropout (LDO) voltage regulator output. The +5V LDO may be used to power external devices such as Hall-effect sensors or amplifiers. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the +5V pin as is practical. For most applications, 4.7 µF of capacitance will ensure stable operation of the LDO circuit.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.6 LX

Buck regulator switch node external inductor connection. Connect this pin to the external inductor chosen for the buck regulator.

3.7 FB

Buck regulator feedback node that is compared with internal 1.25V reference voltage. Connect this pin to a resistor divider that sets the buck regulator output voltage. Connecting this pin to the +5V LDO output disables the buck regulator.

3.8 CAP1, CAP2

Charge pump flying capacitor inputs. Connect the charge pump capacitor across these two pins.

3.9 CE

Chip Enable input used to enable/disable the output driver and on-board functions. When CE is high, all device functions are enabled. When CE is low, the device operates in Reduced mode. The H-Bridge, current amplifiers and 12V LDO are disabled. The buck regulator, 5V LDO, DE2, voltage and temperature sensor functions are not affected.

The CE is also used to clear any hardware faults. When a fault occurs, the CE input may be used to clear the fault by setting the pin low and then high again. The fault is cleared by the rising edge of the CE signal if the hardware fault is no longer active.

The CE pin has an internal 47K pulldown.

3.10 I_OUT1, I_OUT2, I_OUT3

Current sense amplifier output. May be used with feedback resistors to set the current sense gain.

3.11 ISENSE1, ISENSE2, ISENSE3 +/-

Current sense amplifier inverting and non-inverting inputs. Used in conjunction with I_OUTx pins to set current sense gain.

3.12 /ILIMIT_OUT

Current limit output signal. The open-drain output goes low when the current sensed by current sense amplifier 1 exceeds the value set by the internal current reference DAC. The DAC has an offset of 0.991V (typical) which represents zero current flow. The open-drain output will also go low while a motor fault is active.

3.13 PWM1H, PWM2H, PWM3H

Digital PWM inputs for high-side driver control. Each input has a 47K pulldown to ground. The PWM signals may contain dead-time timing or the system may use the Configuration register 2 to set the dead time.

3.14 PWM1L, PWM2L, PWM3L

Digital PWM inputs for low-side driver control. Each input has a 47K pulldown to ground. The PWM signals may contain dead-time timing or the system may use the Configuration register 2 to set the dead time.

3.15 LA, LB, LC

Low-side N-channel MOSFET drive signal. Connect to the gate of the external MOSFETs. A low-impedance resistor may be used between these pins and the MOSFET gates to limit current and slew rate.

3.16 HA, HB, HC

High-side N-channel MOSFET drive signal. Connect to the gate of the external MOSFETs. A low-impedance resistor may be used between these pins and the MOSFET gates to limit current and slew rate.

3.17 PHA, PHB, PHC

Phase signals from motor. Provides high-side N-channel MOSFET driver reference and Back EMF sense input. The phase signals are also used with the bootstrap capacitors to provide high-side gate drive via the VBx inputs.

3.18 VBA, VBB, VBC

High-side MOSFET driver bias. Connect these pins between the bootstrap charge pump diode cathode and bootstrap charge pump capacitor. The 12V LDO output is used to provide 12V at the diode anodes. The phase signals are connected to the other side of the bootstrap charge pump capacitors.

3.19 DE2

Open-drain communications node. The DE2 communications is a half-duplex 9600 baud, 8-bit, no parity communications link. The open-drain DE2 pin must be pulled high by an external pull-up resistor.

3.20 HV_IN1, HV_IN2, LV_OUT1,LV_OUT2

Unidirectional digital level translators. Translates digital input signal on the HV_INx pin to a low-level digital output signal on the LV_OUTx pin. The HV_INx pins have internal 30KΩ pullups to V_{DD} that are controlled by Configuration register 0 bit 6. The Configuration register 0 bit 6 is only sampled during CE = 0. The HV_IN1 pin has higher ESD protection than the HV_IN2 pin. The higher ESD protection makes the HV_IN1 pin better suited for connection to external switches.

LV_OUT1 and LV_OUT2 are open-drain outputs. An external pull-up resistor to the low-voltage logic supply is required.

4.0 DETAILED DESCRIPTION

4.1 BIAS GENERATOR

The internal bias generator controls three voltage rails. Two fixed-output low-dropout linear regulators, an adjustable buck switch-mode power converter, and an unregulated charge pump are controlled through the bias generator. In addition, the bias generator performs supervisory functions.

4.1.1 +12V LOW-DROPOUT LINEAR REGULATOR (LDO)

The +12V rail is used for bias of the 3-phase power MOSFET bridge.

The regulator is capable of supplying 20mA of external load current. The regulator has a minimum overcurrent limit of 30 mA.

The low-dropout regulators require an output capacitor connected from VOUT to GND to stabilize the internal control loop. A minimum of 4.7µF ceramic output capacitance is required for the 12V LDO.

4.1.2 +5V LOW-DROPOUT LINEAR REGULATOR (LDO)

The +5V LDO is used for bias of an external microcontroller, the internal current sense amplifier and the gate control logic.

The +5V LDO is capable of supplying 20mA of external load current. The regulator has a minimum overcurrent limit of 30 mA. If additional external current is required, the buck switch-mode power converter should be utilized.

A minimum of 4.7µF ceramic output capacitance is required for the 5V LDO.

4.1.3 BUCK SWITCH-MODE POWER CONVERTER (SMPS)

The SMPS is a high-efficiency, fixed-frequency, step-down DC-DC converter. The SMPS provides all the active functions for local DC-DC conversion with fast transient response and accurate regulation.

During normal operation of the buck power stage, Q1 is repeatedly switched on and off with the on and off times governed by the control circuit. This switching action causes a train of pulses at the LX node which are filtered by the L/C output filter to produce a DC output voltage, V_O. Figure 4-1 depicts the functional block diagram of the SMPS.

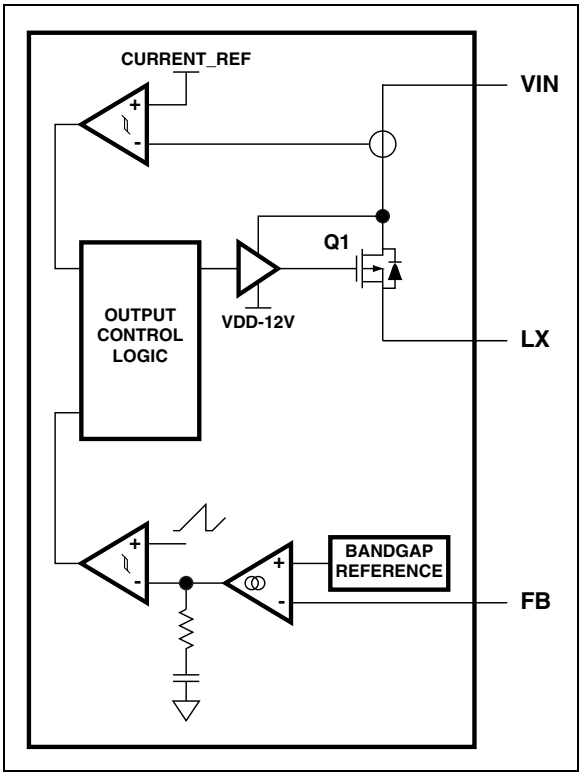


FIGURE 4-1: *SMPS Functional Block Diagram.*

The SMPS is designed to operate in Discontinuous Conduction Mode (DCM) with Voltage mode control and current limit protection. The SMPS is capable of supplying 5V, 150mA to an external load at a fixed switching frequency of 460 kHz with an input voltage of 6V. The output of the SMPS is power limited. Therefore, for a programmed output voltage of 3V, the SMPS will be capable of supplying 250mA to an external load. An external diode is required between the LX pin and ground. The diode will be required to handle the inductor current when the switch is off. The diode is external to the device to reduce substrate currents and power dissipation caused by the switcher. The external diode carries the current during the switch off time, eliminating the current path back through the device.

At light loads the SMPS enters Pulse Frequency Modulation (PFM), improving efficiency at the expense of higher output voltage ripple. The PFM circuitry provides a means to disable the SMPS as well. If the SMPS is not utilized in the application, connecting the feedback pin (FB) to an external 2.5V-to-5.0V supply will force the SMPS to a shutdown state.

The maximum inductor value for operation in Discontinuous Conduction mode can be determined by the following equation.

EQUATION 4-1: L_{MAX} SIMPLIFIED

$$L_{MAX} \leq \frac{V_O \times \left(1 - \frac{V_O}{V_{IN}}\right) \times T}{2 \times I_{O(CRIT)}}$$

Using the L_{MAX} inductor value calculated using Equation 4-1 will ensure Discontinuous Conduction mode operation for output load currents below the critical current level, $I_{O(CRIT)}$. For example, with an output voltage of +5V, a standard inductor value of 4.7µH will ensure Discontinuous Conduction mode operation with an input voltage of 6V, a switching frequency of 468 kHz, and a critical load current of 150 mA.

The output voltage is set by using a resistor divider network. The resistor divider is connected between the inductor output and ground. The divider common point is connected to the FB pin which is then compared to an internal 1.25V reference voltage.

The Buck regulator will set a Status bit and send a status message to the host whenever the input switching current exceeds two amperes peak (typical). The bit will be cleared when the peak input switching current drops back below the two ampere (typical) limit.

The Buck regulator will set a Status bit and send a status message to the host whenever the output voltage drops below 90% of the rated output voltage. The bit will be cleared when the output voltage returns to 94% of rated value.

If the Buck regulator output voltage falls below 80% of rated output voltage, the system will shutdown with a “Brown-out Error”. This will notify the Host of a power failure and subsequent loss of configuration.

The Voltage Supervisor is designed to shutdown the buck regulator when V_{DD} rises above $OVLO_{STOP}$. When shutting down the buck regulator is not desirable, the user should add a voltage suppression device to the V_{DD} input in order to prevent V_{DD} from rising above $OVLO_{STOP}$.

The Voltage Supervisor is also designed to shutdown the buck regulator when V_{DD} falls below $UVLO_{STOP}$.

4.1.4 CHARGE PUMP

An unregulated charge pump is utilized to boost the input to the +12V LDO during low-input conditions. When the input bias to the device (V_{DD}) drops below CP_{START}, the charge pump is activated. When activated, 2 x V_{DD} is presented to the input of the +12V LDO, which maintains a minimum +10V at its output.

The typical charge pump flying capacitor is a 0.1 µF to 1.0 µF ceramic capacitor.

4.1.5 SUPERVISOR

The bias generator incorporates a voltage supervisor and a temperature supervisor.

4.1.5.1 Voltage Supervisor

The voltage supervisor protects the device, external power MOSFETs, and the external microcontroller from damage due to overvoltage or undervoltage of the input supply, VDD.

In the event of an undervoltage condition, V_{DD} < +5.5V, the motor drivers are switched off. The bias generator, communication port, and the remainder of the motor control unit remain active. The failure state is flagged on the DE2 pin with a status message. In extreme overvoltage conditions, V_{DD} > +32V, all functions are turned off.

4.1.5.2 Temperature Supervisor

An integrated temperature sensor self protects the device circuitry. If the temperature rises above the overtemperature shutdown threshold, all functions are turned off. Active operation resumes when the temperature has cooled down below a set hysteresis value and the fault has been cleared by toggling CE.

It is desirable to signal the microcontroller with a warning message before the overtemperature threshold is reached. The microcontroller should take appropriate actions to reduce the temperature rise. The method to signal the microcontroller is through the DE2 pin.

4.2 MOTOR CONTROL UNIT

The motor control unit is comprised of the following:

- External Drive for a 3-Phase Bridge with NMOS/NMOS MOSFET pairs
- Three Motor Current Sense Amplifiers
- Motor Overcurrent Comparator

4.2.1 MOTOR CURRENT SENSE CIRCUITRY

The internal motor current sense circuitry consists of an operational amplifier and comparator. The amplifier output is presented to the inverting comparator input and as an output to the microcontroller. The non-inverting comparator input is connected to an internally programmable 8-bit DAC. A selectable motor current limit threshold may be set with a SET_ILIMIT message from the host to the MCP8024 via the DE2 communications link. The 8-bit DAC is powered by the 5V supply. The DAC output voltage range is 0.991V to 4.503V. The DAC has a bit value of (4.503V - 0.991V) / (2^8 - 1) = 13.77 mV/bit. A DAC input of 00H yields a DAC output voltage of 0.991V. The default power-up DAC value is 40H (1.872V). The DAC uses a 100 kHz filter. Input code to output voltage delay is

approximately five time constants ~= 50 µs. The desired current sense gain is established with an external resistor network.

Note: The motor current limit comparator output is internally 'OR'd with the DRIVER FAULT output of the driver logic block. The microcontroller should monitor the comparator output and take appropriate actions. The motor current limit comparator circuitry does not disable the motor drivers when an overcurrent situation occurs. Only one current limit comparator is provided. The MCP8024 provides three current sense amplifiers which can be used for implementation of advanced control algorithms such as Field Oriented Control (FOC).

The comparator output may be employed as a current limit. Alternatively, the current sense output can be employed in a chop-chop PWM speed loop for any situations where the motor is being accelerated, either positively or negatively. An analog chop-chop speed loop can be implemented by hysteretic control or fixed off-time of the motor current. This makes for a very robust controller as the motor current is always in instantaneous control.

A sense resistor in series with the bridge ground return provides a current signal for both feedback and current limiting. This resistor should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impractical to eliminate, careful layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values, and serve double duty as the half-bridge bypass capacitors.

Note: With a chop-chop control, motor current always flows through the sense resistor. When the PWM is off, however, the flyback diodes, or synchronous rectifiers, conduct, causing the current to reverse polarity through the sense resistor.

The current sense resistor is chosen to establish the peak current limit threshold, which is typically set 20% higher than the maximum current command level to provide overcurrent protection during abnormal conditions. Under normal circumstances with a properly compensated current loop, peak current limit will not be exercised.

4.2.2 MOTOR CONTROL

The commutation loop of a BLDC motor control is a Phase-Locked Loop (PLL) which locks to the rotor's position. Note that this inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity, and the commutation loop locks to the rotor's position to commutate the phases at the correct times.

4.2.2.1 Sensorless Motor Control

Many control algorithms can be implemented with the MCP8024 in conjunction with a microcontroller. The following discussion provides a starting point for implementing the MCP8024 in a sensorless control application of a 3-phase motor. The motor is driven by energizing two windings at a time and sequencing the windings in a six step per electrical revolution method. This method leaves one winding unenergized at all times, and the voltage on that unenergized (Back EMF) winding can be monitored to determine the rotor position.

4.2.2.2 Start-Up Sequence

When the motor being driven is at rest, the back EMF is equal to zero. The motor needs to be rotating for the back EMF sensor to lock onto the rotor position and commutate the motor. The recommended start-up sequence to bring the rotor from rest up to a speed fast enough to allow back EMF sensing is comprised of three modes: Lock or Align mode, Ramp mode, and Run mode. Refer to the commutation state machine in Table 4-1. The order in which the microcontroller steps through the commutation state machine determines the direction the motor rotates.

4.2.2.3 Disabled Mode (CE = 0)

When the driver is disabled (CE = 0), all of the drivers are turned off.

4.2.2.4 Lock Mode

Before the motor can be started, the rotor must be in a known position. In Lock mode, the microcontroller drives phase B low and phases A and C high. This aligns the rotor 30 electrical degrees before the center of the first commutation state. Lock mode must last long enough to allow the motor and its load to settle into this position.

4.2.2.5 Ramp Mode

At the end of Lock mode, Ramp mode is entered. In Ramp mode, the microcontroller steps through the commutation state machine, increasing linearly, until a minimum speed is reached. Ramp mode is an open-loop commutation. No knowledge of the rotor position is used.

4.2.2.6 Run Mode

At the end of the Ramp mode, Run mode is entered. In Run mode, the back EMF sensor is enabled and commutation is now under the control of the phase-locked loop. Motor speed can be regulated by an outer speed control loop.

TABLE 4-1: COMMUTATION STATE MACHINE

STATE	OUTPUTS						BEMF SAMPLE
	HA	HB	HC	LA	LB	LC	
CE = 0	OFF	OFF	OFF	OFF	OFF	OFF	N/A
LOCK	ON	OFF	ON	OFF	ON	OFF	N/A
1	ON	OFF	OFF	OFF	OFF	ON	Phase B
2	OFF	ON	OFF	OFF	OFF	ON	Phase A
3	OFF	ON	OFF	ON	OFF	OFF	Phase C
4	OFF	OFF	ON	ON	OFF	OFF	Phase B
5	OFF	OFF	ON	OFF	ON	OFF	Phase A
6	ON	OFF	OFF	OFF	ON	OFF	Phase C

4.2.2.7 PWM Speed Control

The inner commutation loop is a phase-locked loop, which locks to the rotor's position. This inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. The outer speed loop changes the rotor velocity and the inner commutation loop locks to the rotor's position to commutate the phase at the correct times.

The outer speed loop pulse width modulates (PWMs) the motor drive inverter to produce the desired wave shape and voltage at the motor. The inductance of the motor then integrates this PWM pattern to produce the desired average current, thus controlling the desired torque and speed of the motor. For a trapezoidal BLDC motor drive with six-step commutation, the PWM is used to generate the average voltage to produce the desired motor current and, hence, the motor speed.

There are two basic methods to PWM the inverter switches. The first method returns the reactive energy in the motor inductance to the source by reversing the voltage on the motor winding during the current decay period. This method is referred to as fast decay or chop-chop. The second method circulates the reactive current in the motor with minimal voltage applied to the inductance. This method is referred to as slow decay or chop-coast.

The preferred control method employs a chop-chop PWM for any situations where the motor is being accelerated, either positively or negatively. For improved efficiency, chop-coast PWM is employed during steady-state conditions. The chop-chop speed loop is implemented by hysteretic control, fixed off-time control, or average Current mode control of the motor current. This makes for a very robust controller as the motor current is always in instantaneous control. The motor speed presented to the chop-chop loop is reduced by approximately 9%. A fixed-frequency PWM that only modulates the high-side switches implements the chop-coast loop. The chop-coast loop is presented with the full motor speed, so if it is able to control the speed, the chop-chop loop will never be satisfied and will remain saturated. The chop-chop remains able to assume full control if the motor torque is exceeded, either through a load change or a change in speed that produces acceleration torque. The chop-coast loop will remain saturated, with the chop-chop loop in full control, during start-up and acceleration to full speed. The bandwidth of the chop-coast loop is set to be slower than the chop-chop loop so that any transients will be handled by the chop-chop loop and the chop-coast loop will only be active in steady-state operation.

4.2.3 EXTERNAL DRIVE FOR A 3-PHASE BRIDGE WITH NMOS/NMOS MOSFET PAIRS

Each motor phase is driven with external NMOS/NMOS MOSFET pairs. These are controlled by a low-side and a high-side gate driver. The gate drivers are controlled directly by the digital input pins PWM[1:3]H/L. A logic High turns the associated gate driver ON, and a logic Low turns the associated gate driver OFF. The PWM[1:3]H/L digital inputs are equipped with internal pull-down resistors.

The low-side gate drivers are biased by the +12V LDO output, referenced to ground. The high-side gate drivers are a floating drive biased by a bootstrap capacitor circuit. The bootstrap capacitor is charged by the +12V LDO whenever the accompanying low-side MOSFET is turned on.

4.2.3.1 External Driver Protection Features

Each driver is equipped with Undervoltage Lock Out (UVLO) and short circuit protection features.

4.2.3.1.1 Driver Undervoltage Lock Out (UVLO)

At anytime the driver bias voltage is below the Driver Undervoltage Lock Out threshold (D_{UVLO}), the driver will not turn ON when commanded ON. A driver fault will be indicated to the host microcontroller on the ILIMIT_OUT, open-drain output pin and also via a DE2 communications *Status 1* message. This is a latched fault. Clearing the fault requires either removal of device power or disabling and re-enabling the device via the device enable input (CE). Bit 3 of the Configuration 0 register is used to enable or disable the Driver Undervoltage Lockout feature. This protection feature prevents the external MOSFETs from being controlled with a gate voltage not suitable to fully enhance the device.

4.2.3.1.2 External MOSFET Short Circuit Current

Short circuit protection monitors the voltage across the external MOSFETs during an ON condition. If the voltage rises above a user configurable threshold, all drivers will be turned OFF. A driver fault will be indicated to the host microcontroller on the open-drain ILIMIT_OUT output pin and also via a DE2 communications `Status 1` message. This is a latched fault. Clearing the fault requires either removal of device power or disabling and re-enabling the device via the device enable input (CE). This protection feature helps detect internal motor failures such as winding to case shorts.

Note: The driver short-circuit protection is dependent on application parameters. A configuration message is provided for a set number of threshold levels. In addition, Driver UVLO and/or short-circuit protection has the option to be disabled.

The short-circuit voltage may be set via a DE2 *Set_Cfg_0* message. Bits 0 and 1 are used to select the voltage level for the short circuit comparison. If the voltage across the MOSFET drain-source exceeds the selected voltage level, a fault will be triggered. The selectable voltage levels are 250 mV, 500 mV, 750 mV, and 1000 mV. Bit 2 of the Configuration 0 register is used to enable or disable the short-circuit detection.

4.2.3.2 Gate Control Logic

The gate control logic provides level shifting of the digital inputs, polarity control, and cross conduction protection. Cross conduction protection is performed in two ways.

4.2.3.2.1 Cross Conduction Protection

First, logic prevents switching ON one power MOSFET while the opposite one in the same half-bridge is already switched ON. If both MOSFETs in the same half-bridge are commanded on simultaneously by the digital inputs, both will be turned OFF.

4.2.3.2.2 Programmable Dead Time

Second, the gate control logic employs a break-before-make dead-time delay that is programmable. A configuration message is provided to configure the driver dead time. The allowable dead times are 250 ns, 500 ns, 1 µs and 2 µs.

4.2.3.2.3 Programmable Blanking Time

A configuration message is provided to configure the driver current limit blanking time. The blanking time allows the system to ignore any current spikes that may occur when switching outputs. The allowable blanking times are 500 ns, 1 µs, 2µs, and 4µs (default). The blanking time will start after the dead time circuitry has timed out.

4.3 CHIP ENABLE (CE)

The Chip Enable (CE) pin allows the device to be disabled by external control. When the Chip Enable pin is not active, the following subsystems are disabled:

- high side gate drives (HA, HB, HC)
- low side gate drives (LA, LB, LC)
- 12V LDO
- 30K pull-up resistor connected to the level translator is switched out of the circuit to minimize current consumption (configurable).

The 5V LDO and Buck Regulator stay enabled. The DE2 communications port remains active but the port may only respond to commands. When CE is inactive, the DE2 port is prevented from initiating communications in order to conserve power.

The total current consumption of the device when CE is inactive (device disabled) stays within the “input quiescent current” limits specified in the device characteristics table.

4.4 COMMUNICATION PORTS

The communication ports provide a means of communicating to the host system.

4.4.1 DE2 COMMUNICATIONS PORT

A half-duplex 9600 baud UART interface is available to communicate with an external host. The port is used to configure the MCP8024 and also for status and fault messages.

4.4.2 LEVEL TRANSLATOR

The level translator is an interface between the companion microcontrollers logic levels and the input voltage levels from the system. Typically, the input is driven from the Engine Control Unit (ECU). The level translator is a unidirectional translator. Signals on the high-voltage input are translated to low-voltage signals on the low-voltage outputs. The high-voltage HV_INx inputs have a configurable 30K pullup. The pullup is configured via a *SET_CFG_0* message. Bit 6 of the register controls the state of the pullup. The bit may only be changed when the CE pin is active. The low-voltage LV_OUTx outputs are open-drain outputs.

Note: The TQFP package has two level translators. The second level translator typically interfaces to an Ignition Key ON/OFF signal.

4.5 HOST COMMUNICATIONS

4.5.1 DE2 COMMUNICATIONS

A single-wire, half-duplex, 9600 baud, 8-bit bidirectional communications interface is implemented using the open-drain DE2 pin. The interface consists of eight data bits, one Stop bit, and one Start bit. The implementation of the interface is described in the following sections. A 2K resistor should typically be used between the host transmit pin and the MCP8024 DE2 pin to allow the MCP8024 to drive the DE2 line when the host TX pin is at an idle high level.

The DE2 communications is active when CE = 0 with the constraint that the MCP8024 will not initiate any messages. The host processor may initiate messages regardless of the state of the CE pin. The MCP8024 will respond to host commands when the CE pin is low.

4.5.2 PACKET FORMAT

Every internal status change will provide a communication to the microcontroller. The interface uses a standard UART baud rate of 9600 bits per second.

In the DE2 protocol, the transmitter and the receiver do not share a clock signal. A clock signal does not emanate from one transmitter to the other receiver. Due to this reason the protocol is asynchronous. The protocol uses only one line to communicate, so the transmit/receive packet must be done in Half-Duplex mode. A new transmit message is allowed only when a complete packet has been transmitted.

The Host must listen to the DE2 line in order to check for contentions. In case of contention, the host must release the line and wait for at least three packet-length times before initiating a new transfer.

Figure 4-2 illustrates a basic DE2 data packet.

4.5.3 PACKET TIMING

While no data is being transmitted, a logic '1' must be placed on the open-drain DE2 line by an external pull-up resistor. A data packet is composed of one Start bit, which is always a logic '0', followed by eight data bits, and a Stop bit. The Stop bit must always be a logic '1'. It takes 10 bits to transmit a byte of data.

The device detects the Start bit by detecting the transition from logic 1 to logic 0 (note that while the data line is idle, the logic level is high). Once the Start bit is detected, the next data bit's "center" can be assured to be 24 ticks minus 2 (worst case synchronizer uncertainty) later. From then on, every next data bit center is 16 clock ticks later. **Figure 4-3** illustrates this point.

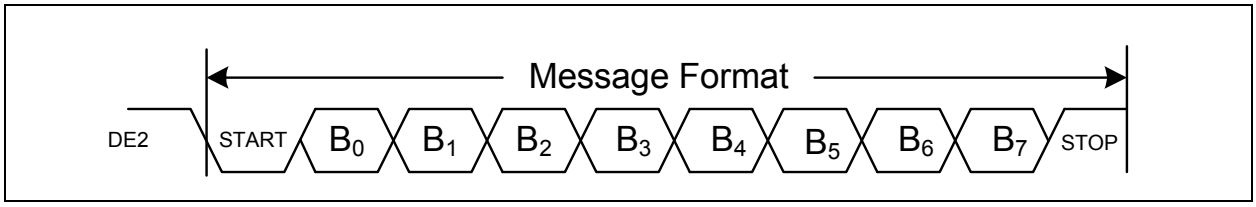


FIGURE 4-2: DE2 PACKET FORMAT.

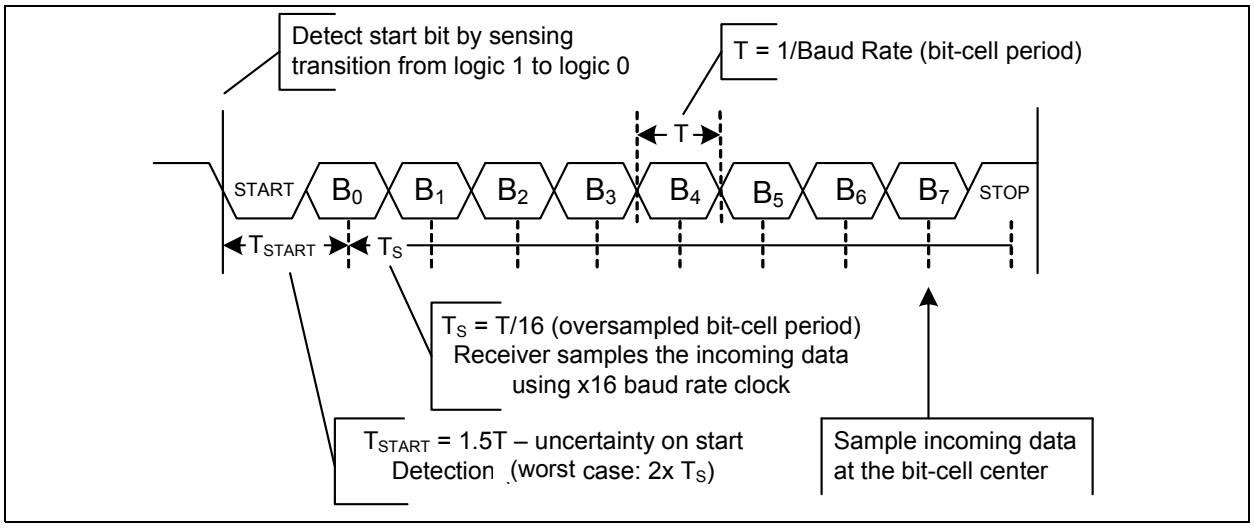


FIGURE 4-3: DE2 PACKET TIMING.

4.5.4 MESSAGING INTERFACE

A command byte will always have the most significant bit 7 (msb) set to '1'. Bits 6 and 5 are reserved for future use and should be set to '0'. Bits 4:0 are used for commands. That allows for 32 possible commands.

4.5.4.1 Host to MCP8024

Messages sent from the host to the MCP8024 device consist of either one or two eight-bit bytes. The first byte transmitted is the command byte. The second byte transmitted, if required, is the data for the command.

4.5.4.2 MCP8024 to Host

A solicited response byte from the MCP8024 device will always echo the command byte with bit 7 set to '0' (Response) and with bit 6 set to '1' for Acknowledged (ACK) or '0' for Not Acknowledged (NACK). The second byte, if required, will be the data for the host command. Any command that causes an error or is not supported will receive a NACK response.

The MCP8024 may send unsolicited command messages to the host controller. All messages to the host controller do not require a response from the host controller.

4.5.4.3 Messages

4.5.4.3.1 SET_CFG_0

There is a SET_CFG_0 message that is sent by the host to the MCP8024 device to configure the device. The SET_CFG_0 message may be sent to the device at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_0 message. The SET_CFG_0 message format is indicated in Table 4-2. The response is indicated in Table 4-3.

4.5.4.3.2 GET_CFG_0

There is a GET_CFG_0 message that is sent by the host to the MCP8024 device to retrieve the device configuration register. The GET_CFG_0 message format is indicated in Table 4-2. The response is indicated in Table 4-3.

4.5.4.3.3 STATUS_0/1

There is a STATUS_0/1 message that is sent by the host to the MCP8024 device to retrieve the device STATUS register. The STATUS_0/1 message may also be sent to the host by the MCP8024 device to inform the host of status changes. The STATUS_0/1 message format is indicated in Table 4-2. The response is indicated in Table 4-3.

The Brown-out Reset - Config Lost bit 4 of status message 1 will be set every time the device restarts due to a brown-out event or a normal start-up. When the bit is set, an unsolicited message will be sent to the host indicating a Reset has taken place and that the configuration data may have been lost. The flag is reset by a “Status 1 Ack” (01000110 (46H)) from the device in response to a Host Status Request command.

4.5.4.3.4 SET_CFG_1

There is a SET_CFG_1 message that is sent by the host to the MCP8024 device to configure the motor current limit reference DAC. The SET_CFG_1 message may be sent to the device at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_1 message. The SET_CFG_1 message format is indicated in Table 4-2. The response is indicated in Table 4-3.

4.5.4.3.5 GET_CFG_1

There is a GET_CFG_1 message that is sent by the host to the MCP8024 device to retrieve the motor current limit reference DAC Configuration register. The GET_CFG_1 message format is indicated in Table 4-2. The response is indicated in Table 4-3.

4.5.4.3.6 SET_CFG_2

There is a SET_CFG_2 message that is sent by the host to the MCP8024 device to configure the driver current limit blanking time. The SET_CFG_2 message may be sent to the device at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_2 message. The SET_CFG_2 message format is indicated in Table 4-2. The response is indicated in Table 4-3.

4.5.4.3.7 GET_CFG_2

There is a GET_CFG_2 message that is sent by the host to the MCP8024 device to retrieve the device Configuration register #2. The GET_CFG_2 message format is indicated in Table 4-2. The response is indicated in Table 4-3.