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MCP8025/6

3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode, and LIN Transceiver

Features

- AEC-Q100 Grade 0 Qualified
- Quiescent Current:
  - Sleep Mode: 5 µA Typical
  - Standby Mode: < 200 µA
- LIN Transceiver Interface (**MCP8025**):
  - Compliant with LIN Bus Specifications 1.3, 2.2, and SAE J2602
  - Supports baud rates up to 20K baud
  - Internal pull-up resistor and diode
  - Protected against ground shorts
  - Protected against loss of ground
  - Automatic thermal shutdown
  - LIN Bus dominant timeout
- Three Half-Bridge Drivers Configured to Drive External High-Side NMOS and Low-Side NMOS MOSFETs:
  - Independent input control for high-side NMOS and low-side NMOS MOSFETs
  - Peak output current: 0.5A @ 12V
  - Shoot-through protection
  - Overcurrent and short-circuit protection
- Adjustable Output Buck Regulator (750 mW)
- Fixed Output Linear Regulators:
  - 5V @ 30 mA
  - 12V @ 30 mA
- Operational Amplifiers:
  - one in MCP8025
  - three in MCP8026
- Overcurrent Comparator with DAC Reference
- Phase Comparator with Multiplexer (**MCP8025**)
- Neutral Simulator (**MCP8025**)
- Level Translators (**MCP8026**)
- Input Voltage Range: 6V to 40V
- Operational Voltage Range:
  - 6V to 19V (**MCP8025**)
  - 6V to 28V (**MCP8026**)
- Buck Regulator Undervoltage Lockout: 4.0V
- Undervoltage Lockout (UVLO): 5.5V (except Buck)
- Overvoltage Lockout (OVLO)
  - 20V (**MCP8025**)
  - 32V (**MCP8026**)
- Transient (100 ms) Voltage Tolerance: 48V
- Extended Temperature Range (T_A): -40 to +150°C
- Thermal Shutdown

Applications

- Automotive Fuel, Water, Ventilation Motors
- Home Appliances
- Permanent Magnet Synchronous Motor (PMSM) Control
- Hobby Aircraft, Boats, Vehicles

Description

The MCP8025/6 devices are 3-phase brushless DC (BLDC) power modules containing three integrated half-bridge drivers capable of driving three external NMOS/NMOS transistor pairs. The three half-bridge drivers are capable of delivering a peak output current of 0.5A at 12V for driving high-side and low-side NMOS MOSFET transistors. The drivers have shoot-through, overcurrent and short-circuit protection. A Sleep mode has been added to achieve a typical “key-off” quiescent current of 5 µA.

The MCP8025 device integrates a comparator, a buck voltage regulator, two LDO regulators, power monitoring comparators, an overtemperature sensor, a LIN transceiver, a zero-crossing detector, a neutral simulator and an operational amplifier for motor current monitoring. The phase comparator and multiplexer allow for hardware commutation detection. The neutral simulator allows commutation detection without a neutral tap in the motor. The buck converter is capable of delivering 750 mW of power for powering a companion microcontroller. The buck regulator may be disabled if not used. The on-board 5V and 12V low-dropout voltage regulators are capable of delivering 30 mA of current.

The MCP8026 replaces the LIN transceiver, neutral simulator and zero-crossing detector in MCP8025 with two level shifters and two additional op amps.

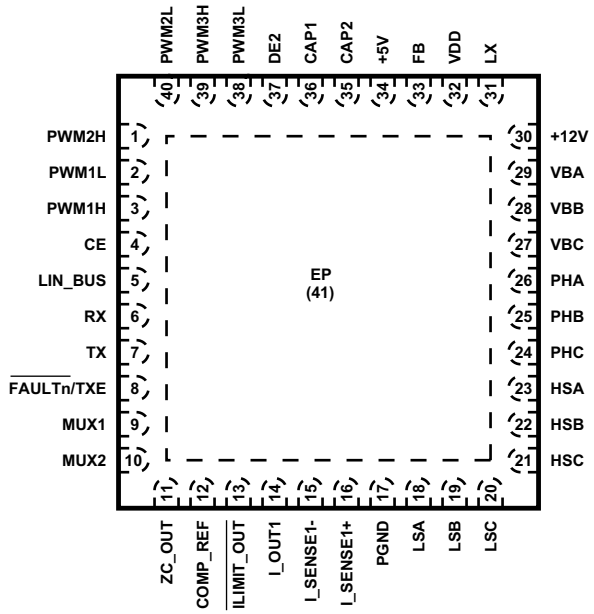
The MCP8025/6 operation is specified over a temperature range of -40°C to +150°C.

Package options include 40-lead 5x5 QFN and 48-lead 7x7 TQFP with Exposed Pad (EP).

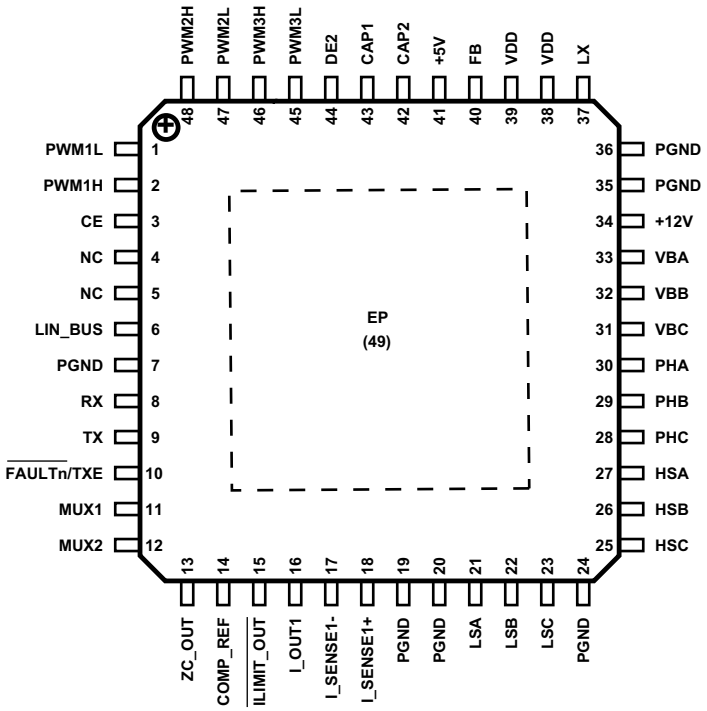
LOCAL INTERCONNECT NETWORK

Package Types – MCP8025

5 mm x 5 mm QFN-40*



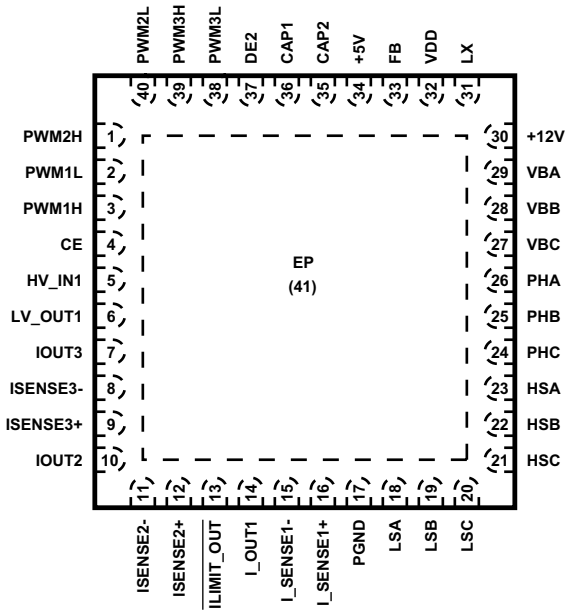
7 mm x 7 mm TQFP-48*



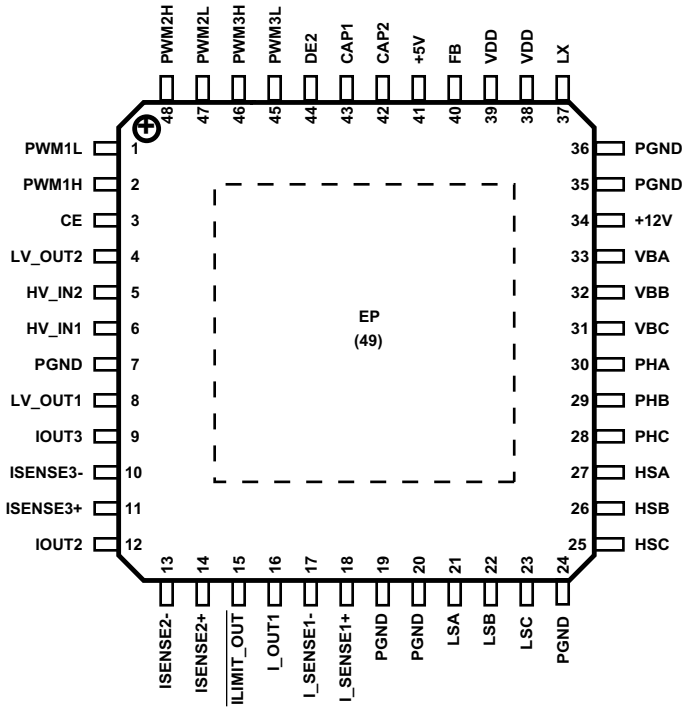
* Includes Exposed Thermal Pad (EP), see Table 3-1.

Package Types – MCP8026

5 mm x 5 mm QFN-40*

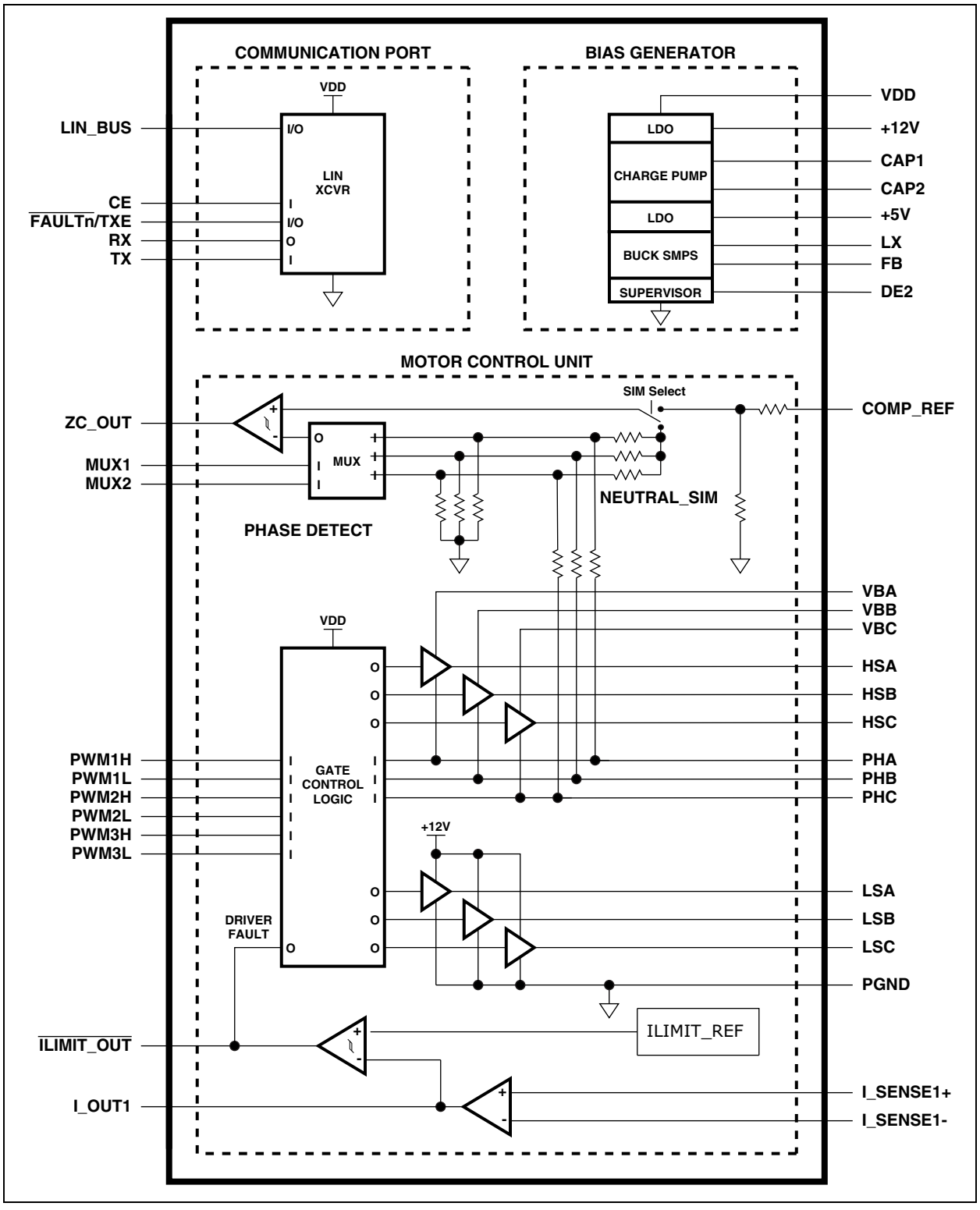


7 mm x 7 mm TQFP-48*

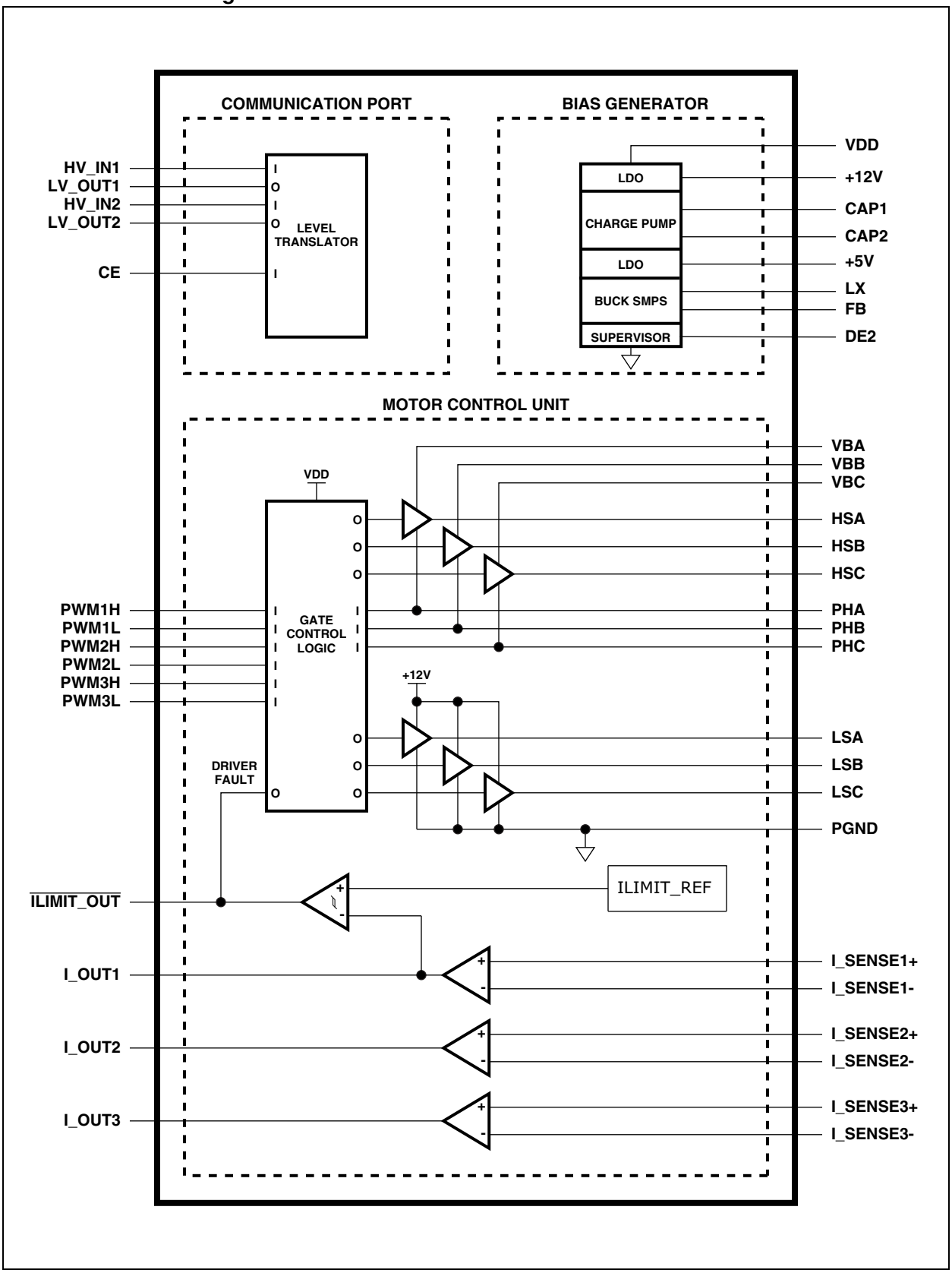


* Includes Exposed Thermal Pad (EP), see Table 3-2.

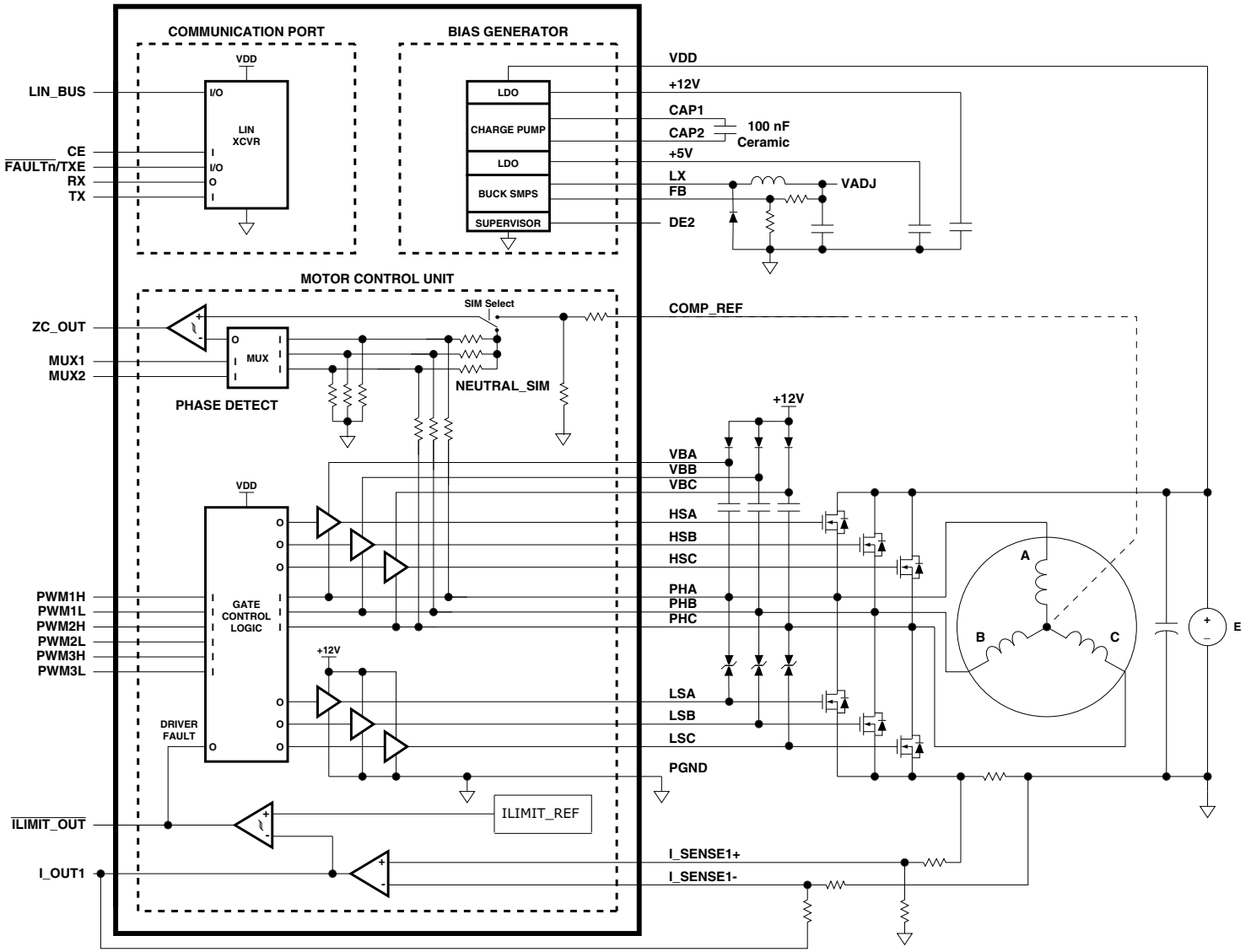
Functional Block Diagram – MCP8025



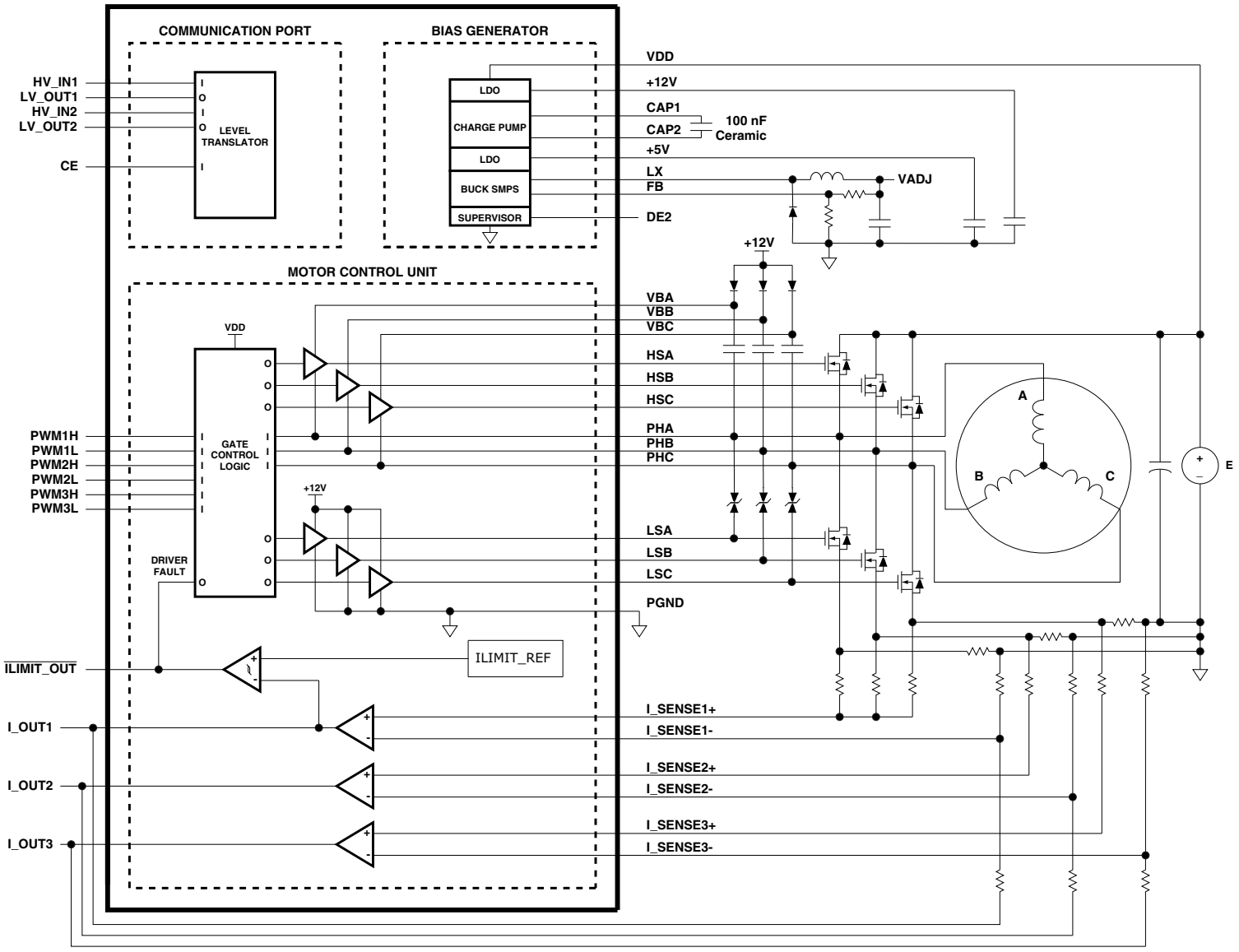
Functional Block Diagram – MCP8026



Typical Application Circuit – MCP8025



Typical Application Circuit – MCP8026



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{DD} ..... (GND – 0.3V) to +46.0V
Input Voltage, < 100 ms Transient ..... +48.0V
Internal Power Dissipation ..... Internally-Limited
Operating Ambient Temperature Range ..... -40°C to +150°C
Operating Junction Temperature **(Note 1)** .... -40°C to +160°C
Transient Junction Temperature **(Note 2)** ..... +170°C
Storage Temperature **(Note 1)** ..... -55°C to +150°C
Digital I/O ..... -0.3V to 5.5V
LV Analog I/O ..... -0.3V to 5.5V
VBx ..... (GND – 0.3V) to +46.0V
PHx, HSx ..... (GND – 5.5V) to +46.0V
ESD and Latch-Up Protection:
VDD, LIN_BUS/HV_IN1 ..... ≥ 8 kV HBM and ≥ 750V CDM
All other pins ..... ≥ 2 kV HBM and ≥ 750V CDM
Latch-up protection – all pins ..... > 100 mA

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation may cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 150°C can impact the device reliability and ROM data retention.

2: Transient junction temperatures should not exceed one second in duration. Sustained junction temperatures above 170°C may impact the device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
POWER SUPPLY INPUT						
Input Operating Voltage	V_{DD}	6.0	—	19.0	V	Operating **(MCP8025)**
		6.0	—	28.0		Operating **(MCP8026)**
		6.0	—	40.0		Shutdown
		4.0	—	32.0		Buck Operating Range
Transient Maximum Voltage	V_{DDmax}	—	—	48.0	V	< 100 ms
Input Current **(MCP8025)**	I_{DD}	—	—	—	µA	V_{DD} > 13V
		—	5	15		Sleep mode
		—	175	—		Standby, CE = 0V, T_J = -45°C
		—	175	—		Standby, CE = 0V, T_J = +25°C
		—	195	300		Standby, CE = 0V, T_J = +150°C
		—	940	—		Active, CE > $V_{DIG\_HI\_TH}$
		—	1150	—		Active, V_{DD} = 6V, T_J = +25°C
Input Current **(MCP8026)**	I_{DD}	—	—	—	µA	V_{DD} > 13V
		—	5	15		Sleep mode
		—	120	—		Standby, CE = 0V, T_J = -45°C
		—	120	—		Standby, CE = 0V, T_J = +25°C
		—	144	300		Standby, CE = 0V, T_J = +150°C
		—	950	—		Active, CE > $V_{DIG\_HI\_TH}$
		—	1090	—		Active, V_{DD} = 6V, T_J = +25°C
Digital Input/Output	$DIGITAL_{I/O}$	0	—	5.5	V	
Digital Open-Drain Drive Strength	$DIGITAL_{IOL}$	—	1	—	mA	V_{DS} < 50 mV

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).
2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Input Rising Threshold	$V_{DIG\_HI\_TH}$	1.26	—	—	V	
Digital Input Falling Threshold	$V_{DIG\_LO\_TH}$	—	—	0.54	V	
Digital Input Hysteresis	V_{DIG_HYS}	—	500	—	mV	
Digital Input Current	I_{DIG}	—	30	100	µA	V_{DIG} = 3.0V
		—	0.2	—		V_{DIG} = 0V
Analog Low-Voltage Input	$ANALOG_{VIN}$	0	—	5.5	V	Excludes LIN and high-voltage pins
Analog Low-Voltage Output	$ANALOG_{VOUT}$	0	—	V_{OUT5}	V	Excludes LIN and high-voltage pins
BIAS GENERATOR						
+12V Regulated Charge Pump						
Charge Pump Current	I_{CP}	20	—	—	mA	V_{DD} = 9.0V
Charge Pump Start	CP_{START}	11.0	11.5	—	V	V_{DD} falling
Charge Pump Stop	CP_{STOP}	—	12.0	12.5	V	V_{DD} rising
Charge Pump Frequency (50% charging/ 50% discharging)	CP_{FSW}	—	76.80	—	kHz	V_{DD} = 9.0V
		—	0	—		V_{DD} = 13V (stopped)
Charge Pump Switch Resistance	CP_{RDSON}	—	14	—	Ω	RDS_{ON} sum of high side and low side
Output Voltage	V_{OUT12}	—	12	—	V	$V_{DD} \geq$ 7.5V, C_{PUMP} = 100 nF I_{OUT} = 20 mA
		—	9	—		V_{DD} = 5.1V, C_{PUMP} = 260 nF I_{OUT} = 15 mA
Output Voltage Tolerance	$\lvert TOLV_{OUT12} \rvert$	—	—	4.0	%	I_{OUT} = 1 mA
Output Current	I_{OUT}	30	—	—	mA	Average current
Output Current Limit	I_{LIMIT}	40	50	—	mA	Average current
Output Voltage Temperature Coefficient	TCV_{OUT12}	—	50	—	ppm/°C	
Line Regulation	$\lvert \Delta V_{OUT} / (V_{OUT} \times \Delta V_{DD}) \rvert$	—	0.1	0.5	%/V	13V < V_{DD} < 19V I_{OUT} = 20 mA
Load Regulation	$\lvert \Delta V_{OUT} / V_{OUT} \rvert$	—	0.2	0.5	%	I_{OUT} = 0.1 mA to 15 mA
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz I_{OUT} = 10 mA
+5V Linear Regulator						
Output Voltage	V_{OUT5}	—	5	—	V	V_{DD} = V_{OUT5} + 1V I_{OUT} = 1 mA
Output Voltage Tolerance	$\lvert TOLV_{OUT5} \rvert$	—	—	4.0	%	
Output Current	I_{OUT}	30	—	—	mA	Average current
Output Current Limit	I_{LIMIT}	40	50	—	mA	Average current
Output Voltage Temperature Coefficient	$\lvert TCV_{OUT5} \rvert$	—	50	—	ppm/°C	

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Line Regulation	$\lvert\Delta V_{OUT}/(V_{OUT} \times \Delta V_{DD})\rvert$	—	0.1	0.5	%/V	6V < V_{DD} < 19V I_{OUT} = 20 mA
Load Regulation	$\lvert\Delta V_{OUT}/V_{OUT}\rvert$	—	0.2	0.5	%	I_{OUT} = 0.1 mA to 15 mA
Dropout Voltage	$V_{DD} - V_{OUT5}$	—	180	350	mV	I_{OUT} = 20 mA measurement taken when output voltage drops 2% from no-load value
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz I_{OUT} = 10 mA
Buck Regulator						
Feedback Voltage	V_{FB}	1.19	1.25	1.31	V	
Feedback Voltage Tolerance	$\lvert TOLV_{FB}\rvert$	—	—	5.0	%	I_{FB} = 1 µA
Feedback Voltage Line Regulation	$\lvert(\Delta V_{FB}/V_{FB})/\Delta V_{DD}\rvert$	—	0.1	0.5	%/V	V_{DD} = 6V to 28V
Feedback Voltage Load Regulation	$\lvert\Delta V_{FB}/V_{FB}\rvert$	—	0.1	0.5	%	I_{OUT} = 5 mA to 150 mA
Feedback Input Bias Current	I_{FB}	-100	—	+100	nA	Sink/Source
Feedback Voltage To Shutdown Buck Regulator	V_{BUCK_DIS}	2.5	—	5.5	V	V_{DD} > 6V
Switching Frequency	f_{SW}	—	461	—	kHz	
Duty Cycle Range	DC_{MAX}	3	—	96	%	
PMOS Switch On Resistance	R_{DSON}	—	0.6	—	Ω	T_J = 25°C
PMOS Switch Current Limit	$I_{P(MAX)}$	—	2.5	—	A	
Ground Current – PWM Mode	I_{GND}	—	1.5	2.5	mA	Switching
Quiescent Current – PFM Mode	I_Q	—	150	200	µA	I_{OUT} = 0 mA
Output Voltage Adjust Range	V_{OUT}	2.0	—	5.0	V	
Output Current	I_{OUT}	150	—	—	mA	5V, $V_{DD} - V_{OUT}$ > 0.5V
		250	—	—		3V, $V_{DD} - V_{OUT}$ > 0.5V
Output Power	P_{OUT}	—	750	—	mW	P = I_{OUT} x V_{OUT} 2.5A peak current
Voltage Supervisor						
Buck Input Undervoltage Lock-out – Start-Up	$UVLO_{BK\_STRT}$	—	4.3	4.5	V	V_{DD} rising
Buck Input Undervoltage Lock-out – Shutdown	$UVLO_{BK\_STOP}$	3.8	4.0	—	V	V_{DD} falling
Buck Input Undervoltage Lockout Hysteresis	$UVLO_{BK\_HYS}$	—	0.3	—	V	
5V LDO Undervoltage Fault Inactive	$UVLO_{5VLDO\_INACT}$	—	4.5	—	V	V_{OUT5} rising
5V LDO Undervoltage Fault Active	$UVLO_{5VLDO\_ACT}$	—	4.0	—	V	V_{OUT5} falling

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
5V LDO Undervoltage Fault Hysteresis	$UVLO_{5VLDO\_HYS}$	—	0.5	—	V	
Input Undervoltage Lockout – Start-Up	$UVLO_{STRT}$	—	6.0	6.25	V	V_{DD} rising
Input Undervoltage Lockout – Shutdown	$UVLO_{STOP}$	5.1	5.5	—	V	V_{DD} falling
Input Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	0.20	0.45	0.70	V	
Input Overvoltage Lockout – Driver Disabled **(MCP8025)**	$DOVLO_{STOP}$	—	20.0	20.5	V	V_{DD} rising
Input Overvoltage Lockout – Driver Enabled **(MCP8025)**	$DOVLO_{STRT}$	18.75	19.5	—	V	V_{DD} falling
Input Overvoltage Lockout Hysteresis **(MCP8025)**	$DOVLO_{HYS}$	0.15	0.5	0.75	V	
Input Overvoltage Lockout – All Functions Disabled	$AOVLO_{STOP}$	—	32.0	33.0	V	V_{DD} rising
Input Overvoltage Lockout – All Functions Enabled	$AOVLO_{STRT}$	29.0	30.0	—	V	V_{DD} falling
Input Overvoltage Lockout Hysteresis	$AOVLO_{HYS}$	1.0	2.0	3.0	V	
Temperature Supervisor						
Thermal Warning Temperature	T_{WARN}	—	72	—	$\%T_{SD}$	Rising temperature (115°C)
Thermal Warning Hysteresis	ΔT_{WARN}	—	15	—	°C	Falling temperature
Thermal Shutdown Temperature	T_{SD}	160	170	—	°C	Rising temperature
Thermal Shutdown Hysteresis	ΔT_{SD}	—	25	—	°C	Falling temperature
MOTOR CONTROL UNIT						
Output Drivers						
PWMH/L Input Pull Down	R_{PULLDN}	—	47	—	kΩ	
Output Driver Source Current	I_{SOURCE}	0.3	—	—	A	V_{DD} = 12V, HS[A:C], LS[A:C]
Output Driver Sink Current	I_{SINK}	0.3	—	—	A	V_{DD} = 12V, HS[A:C], LS[A:C]
Output Driver Source Resistance	R_{DSON}	—	17	—	Ω	I_{OUT} = 10 mA, V_{DD} = 12V HS[A:C], LS[A:C]
Output Driver Sink Resistance	R_{DSON}	—	17	—	Ω	I_{OUT} = 10 mA, V_{DD} = 12V HS[A:C], LS[A:C]
Output Driver Blanking	t_{BLANK}	500	—	4000	ns	Configurable
Output Driver UVLO Threshold	D_{UVLO}	7.2	8.0	—	V	Config Register 0 bit 3 = 0
Output Driver UVLO Minimum Duration	t_{DUVLO}	t_{BLANK} + 700	—	t_{BLANK} + 1400	ns	Fault latched after t_{DUVLO}
Output Driver HS Drive Voltage	V_{HS}	8.0	12	13.5	V	With respect to the phase pin
		-5.5	—	—		With respect to ground
Output Driver LS Drive Voltage	V_{LS}	8.0	12	13.5	V	With respect to ground
Output Driver Bootstrap Voltage	$V_{BOOTSTRAP}$	—	—	—	V	With respect to ground
		—	—	44		Continuous
		—	—	48		< 100 ms

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Driver Phase Pin Voltage	V_{PHASE}	—	—	—	V	With respect to ground
		-5.5	—	44		Continuous
		-5.5	—	48		< 100 ms
Output Driver Short-Circuit Protection Threshold High Side (V_{DD} – V_{PHx}) Low Side (V_{PHx} – P_{GND})	D_{SC_THR}	—	—	—	V	Set In Register CFG0
		—	0.250	—		00 (Default)
		—	0.500	—		01
		—	0.750	—		10
		—	1.000	—		11
Output Driver Short-Circuit Detected Propagation Delay	T_{SC_DLY}	—	—	—	ns	C_{LOAD} = 1000 pF, V_{DD} = 12V
		—	430	—		Detection after blanking
		—	10	—		Detection during blanking, value is delay after blanking
Output Driver OVLO Turn-Off Delay	T_{OVLO_DLY}	3	5	—	µs	Detection synchronized with internal clock **(Note 2)**
Power-Up or Sleep to Standby	t_{POWER}	—	—	—	ms	CE High-Low-High Transition < 100 µs (Fault Clearing)
		—	10	—		**MCP8025**
		—	5	—		**MCP8026**
Standby to Motor Operational	t_{MOTOR}	—	5	—	µs	CE High-Low-High Transition < 0.9 ms (Fault Clearing)
		—	—	5	ms	Standby state to Operational state **(MCP8025)** **(Note 2)**
		—	—	10	ms	Standby state to Operational state (**MCP8026**) **(Note 2)**
Fault to Driver Output Turn-Off	T_{FAULT_OFF}	—	—	—	µs	C_{LOAD} = 1000 pF, V_{DD} = 12V Time after fault occurs
		—	1	—		UVLO, OCP faults
		—	10	—		All other faults
CE Low to Driver Output Turn-Off	T_{DEL_OFF}	—	100	250	ns	C_{LOAD} = 1000 pF, V_{DD} = 12V Time after CE = Low **(Note 2)**
CE Low to Standby State	$t_{STANDBY}$	—	1	—	ms	Time after CE = Low SLEEP bit = 0
CE Low to Sleep State	t_{SLEEP}	—	1	—	ms	Time after CE = Low SLEEP bit = 1
CE Fault Clearing Pulse	t_{FAULT_CLR}	1	—	900	µs	CE High-Low-High Transition Time **(Note 2)**

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Current Sense Amplifier						
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	V_{CM} = 0V T_A = -40°C to +150°C
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	V_{CM} = 0V
Input Bias Current	I_B	-1	—	+1	µA	
Common Mode Input Range	V_{CMR}	-0.3	—	3.5	V	
Common Mode Rejection Ratio	CMRR	—	80	—	dB	Freq = 1 kHz I_{OUT} = 10 µA
Maximum Output Voltage Swing	V_{OL}, V_{OH}	0.05	—	4.5	V	I_{OUT} = 200 µA
Slew Rate	SR	—	±7	—	V/µs	Symmetrical
Gain Bandwidth Product	GBWP	—	10.0	—	MHz	
Current Comparator Hysteresis	CC_{HYS}	—	10	—	mV	
Current Comparator Common Mode Input Range	V_{CC_CMR}	1.0	—	4.5	V	
Current Limit DAC						
Resolution		—	8	—	bits	
Output Voltage Range	V_{OL}, V_{OH}	0.991	—	4.503	V	I_{OUT} = 1 mA
Output Voltage	V_{DAC}	—	—	—	V	CFG1 Code x 13.77 mV/bit + 0.991V
		—	0.991	—		Code 00H
		—	1.872	—		Code 40H
		—	4.503	—		Code FFH
Input to Output Delay	T_{DELAY}	—	50	—	µs	
Integral Nonlinearity	INL	-0.5	—	+0.5	%FSR	%Full Scale Range (**Note 2**)
Differential Nonlinearity	DNL	-50	—	+50	%LSB	%LSB (**Note 2**)
$\overline{\text{ILIMIT\_OUT}}$ Sink Current (Open-Drain)	IL_{OUT}	—	1	—	mA	$V_{ILIMIT\_OUT} \leq$ 50 mV
ZC Back EMF Sampler Comparator (MCP8025)						
Maximum Output Voltage Swing	ZCV_{OL}, ZCV_{OH}	0.05	—	5.0	V	I_{OUT} = 1 mA
Reference Input Impedance	ZC_{ZREF}	—	83	—	kΩ	
Input to Output Delay	ZC_{DELAY}	—	—	500	ns	V_{IN_STEP} = 500 mV (**Note 2**)
Voltage Divider RC Time Constant	ZC_{TRC}	—	100	—	ns	
ZC Output Pull-Up Range	$ZC_{RPULLUP}$	3.3	10	—	kΩ	
ZC Output Sink Current (Open-Drain)	ZC_{IOL}	—	1	—	mA	$V_{OUT} \leq$ 50 mV

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Back EMF Sampler Phase Multiplexer (MCP8025)						
MUX[1:2] Input Pull Down	R_{PULLDN}	—	47	—	kΩ	
Transition Time	t_{TRAN}	—	150	250	ns	**(Note 2)**
Delay from MUX Select to ZC Out	MUX_{DELAY}	—	210	—	ns	
Phase Filter Capacitors	C_{PHASE}	—	1.5	—	pF	MUX input to ground
COMMUNICATION PORTS						
Standard LIN (MCP8025)						
Microcontroller Interface						
TX Input Pull-Up Resistor	R_{PUTXD}	—	48	—	kΩ	Pull up to 5V
Bus Interface						
LIN Bus High-Level Input Voltage	V_{HI}	0.6 x V_{DD}	—	—	V	Recessive state
LIN Bus Low-Level Input Voltage	V_{LO}	—	—	0.4 x V_{DD}	V	Dominant state
LIN Bus Input Hysteresis	V_{HYS}	—	—	0.175 x V_{DD}	V	$V_{HI} - V_{LO}$
LIN Bus Low-Level Output Current	I_{OL}	7.3	—	—	mA	V_O = 0.2 x V_{DD}, V_{DD} = 8V
		16.5	—	—		V_O = 0.2 x V_{DD}, V_{DD} = 18V
		30.6	—	—		V_O = 0.251 x V_{DD}, V_{DD} = 18V
LIN Bus Input Pull-Up Current	I_{PU}	5	—	180	µA	
LIN Bus Short-Circuit Current Limit	I_{SC}	50	—	200	mA	
LIN Bus Low-Level Output Voltage	V_{OL}	—	—	0.2 x V_{DD}	V	
LIN Bus Input Leakage Current (at receiver during dominant bus level)	$I_{BUS\_PAS\_DOM}$	-1	—	—	mA	Driver OFF V_{BUS} = 0V V_{DD} = 12V
LIN Bus Input Leakage Current (at receiver during recessive bus level)	$I_{BUS\_PAS\_REC}$	—	12	20	µA	Driver OFF $V_{BUS} \geq V_{DD}$ 7V < V_{BUS} < 19V 7V < V_{DD} < 19V
LIN Bus Input Leakage Current (disconnected from ground)	$I_{BUS\_NO\_GND}$	-1	—	1	mA	GND = V_{DD} = 12V 0V < V_{BUS} < 19V
LIN Bus Input Leakage Current (disconnected from V_{DD})	$I_{BUS\_NO\_BAT}$	—	—	10	µA	V_{DD} = 0V 0V < V_{BUS} < 19V
Receiver Center Voltage	V_{BUS_CNT}	0.475 x V_{DD}	0.5 x V_{DD}	0.525 x V_{DD}	V	$V_{BUS\_CNT} = (V_{HI} - V_{LO})/2$
LIN Bus Slave Pull-Up Resistance	R_{PULLUP}	20	30	47	kΩ	
LIN Dominant State Timeout	t_{DOM_TOUT}	—	25	—	ms	
Propagation Delay	T_{RX_PD}	—	3.0	6.0	µs	Propagation delay of receiver

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Symmetry	T_{RX_SYM}	-2	—	+2	µs	Symmetry of receiver propagation delay rising edge w.r.t.falling edge
Voltage Level Translators (MCP8026)						
High-Voltage Input Range	V_{IN}	0	—	V_{DD}	V	
Low-Voltage Output Range	V_{OUT}	0	—	5.0V	V	
Input Pull-Up Resistor	RPU	—	30	—	kΩ	
High-Level Input Voltage	V_{IH}	0.60	—	—	V_{DD}	V_{DD} = 15V
Low-Level Input Voltage	V_{IL}	—	—	0.40	V_{DD}	V_{DD} = 15V
Input Hysteresis	V_{HYS}	—	—	0.30	V_{DD}	
Propagation Delay	T_{LV_OUT}	—	3.0	6.0	µs	**(Note 2)**
Maximum Communication Frequency	F_{MAX}	—	—	20	kHz	**(Note 2)**
Low-Voltage Output Sink Current (Open-Drain)	I_{OL}	—	1	—	mA	$V_{OUT} \leq$ 50 mV
DE2 Communications						
Baud Rate	BAUD	—	9600	—	bps	
Power-Up Delay	PU_DELAY	—	1	—	ms	Time from rising $V_{DD} \geq$ 6V to DE2 active
DE2 Sink Current	$DE2_{iSINK}$	1	—	—	mA	$V_{DE2} \leq$ 50 mV **(Note 2)**
DE2 Message Response Time	$DE2_{RSP}$	0	—	—	µs	Time from last received Stop bit to Response Start bit **(Note 2)**
DE2 Host Wait Time	$DE2_{WAIT}$	3.125	—	—	ms	Minimum time for host to wait for response. Three packets based on 9600 baud **(Note 2)**
DE2 Message Receive Timeout	$DE2_{RCVTOUT}$	—	5	—	ms	Time between message bytes
INTERNAL ROM (READ-ONLY MEMORY) DATA RETENTION						
Cell High Temperature Operating Life	HTOL	—	1000	—	Hours	T_J = 150°C **(Note 1)**
Cell Operating Life		—	10	—	Years	T_J = 85°C

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are by design, not production tested.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges (Note 1)						
Specified Temperature Range	T_A	-40		+150	°C	
Operating Temperature Range	T_A	-40		+150	°C	
	T_J	-40		+160	°C	
Storage Temperature Range	T_A	-55		+150	°C	**(Note 2)**
Package Thermal Resistances						
Thermal Resistance, 5 mm x 5 mm 40LD-QFN	θ_{JA}	—	37	—	°C/W	4-Layer JC51-5 standard board Natural convection
	θ_{JC}	—	6.9	—		
Thermal Resistance, 7 mm x 7 mm 48LD-TQFP with Exposed Pad	θ_{JA}	—	30	—	°C/W	
	θ_{JC}	—	15	—		

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 160°C rating. Sustained junction temperatures above 160°C can impact the device reliability.

2: 1000 hour cumulative maximum for ROM data retention (typical).

ESD, SUSCEPTIBILITY, SURGE AND LATCH-UP TESTING

Parameter	Standard and Test Condition	Value
Input voltage surges	ISO 16750-2	28V for 1 minute, 45V for 0.5 seconds
ESD according to IBEE LIN EMC – Pins LIN_BUS, VDD (HMM)	Test specification 1.0 following IEC 61000-4.2	± 8 kV
ESD HBM with 1.5 kΩ/100 pF	CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref E JEDEC JS-001-2012	± 2 kV
ESD HBM with 1.5 kΩ/100 pF – Pins LIN_BUS, VDD, HV_IN1 against PGND	CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref E JEDEC JS-001-2012	± 8 kV
ESD CDM (Charged Device Model, field-induced method – replaces machine-model method)	ESD-STM5.3.1-1999	± 750V all pins
Latch-Up Susceptibility	AEC Q100-004, 150°C	> 100 mA

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

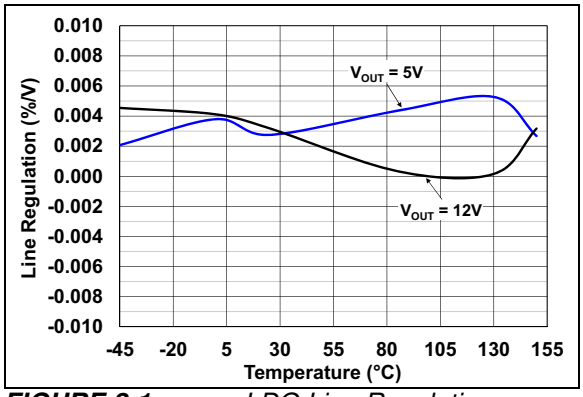


FIGURE 2-1: *LDO Line Regulation vs. Temperature.*

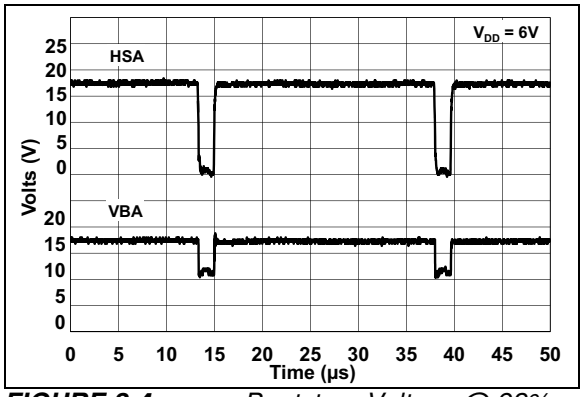


FIGURE 2-4: *Bootstrap Voltage @ 92% Duty Cycle.*

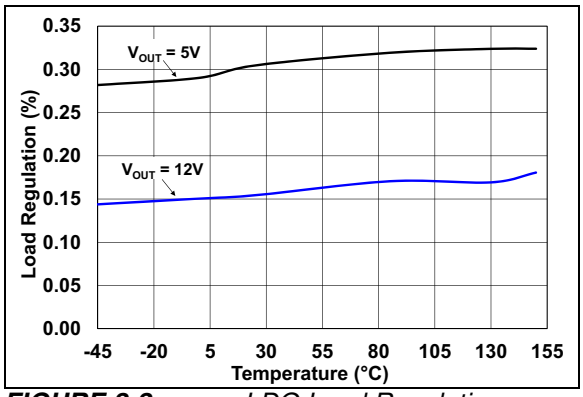


FIGURE 2-2: *LDO Load Regulation vs. Temperature.*

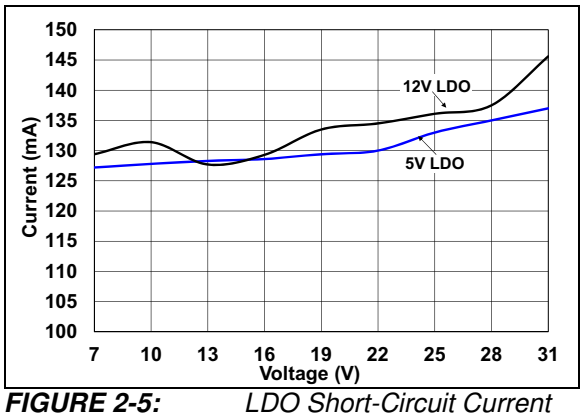


FIGURE 2-5: *LDO Short-Circuit Current vs. Input Voltage.*

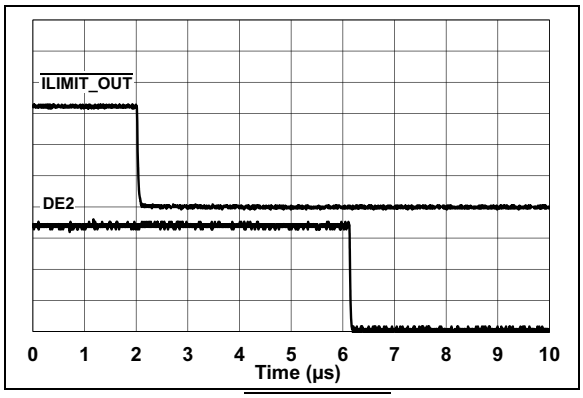


FIGURE 2-3: *$\overline{ILIMIT\_OUT}$ Low to DE2 Message Delay.*

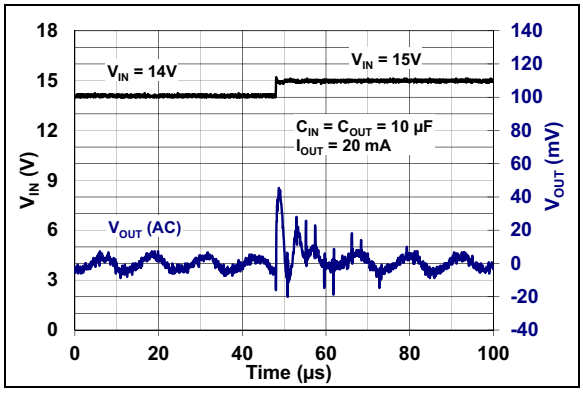


FIGURE 2-6: *5V LDO Dynamic Linestep – Rising V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

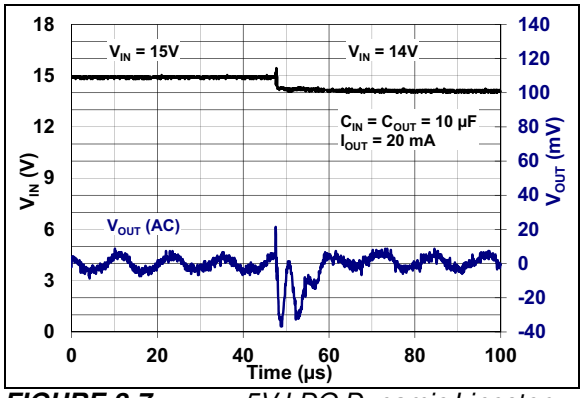


FIGURE 2-7: *5V LDO Dynamic Linestep – Falling V_{DD}.*

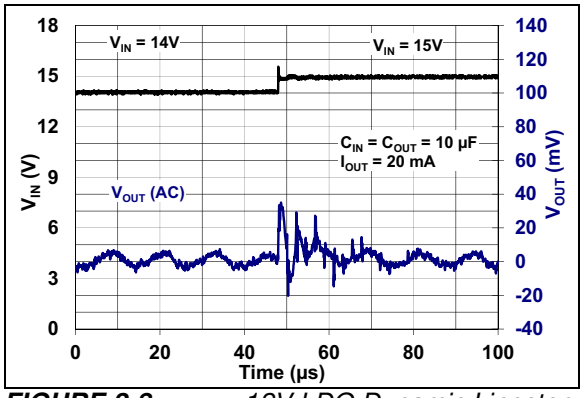


FIGURE 2-8: *12V LDO Dynamic Linestep – Rising V_{DD}.*

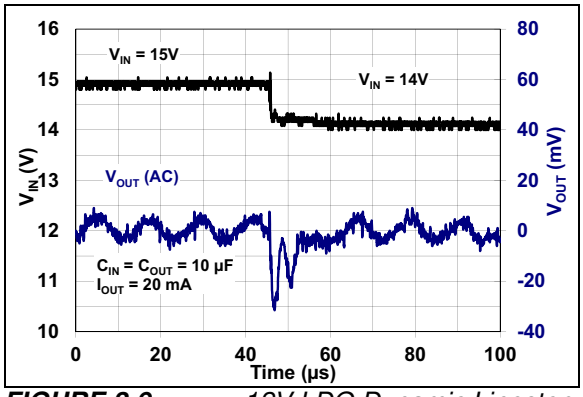


FIGURE 2-9: *12V LDO Dynamic Linestep – Falling V_{DD}.*

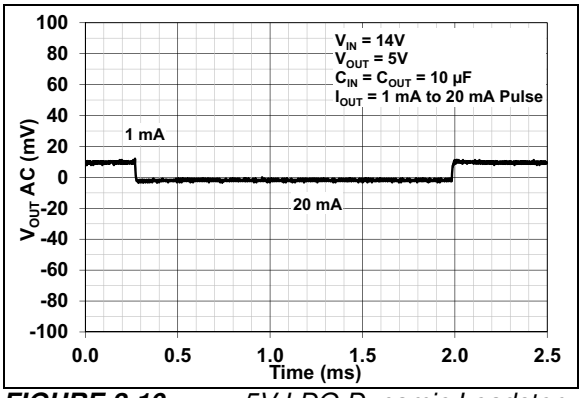


FIGURE 2-10: *5V LDO Dynamic Loadstep.*

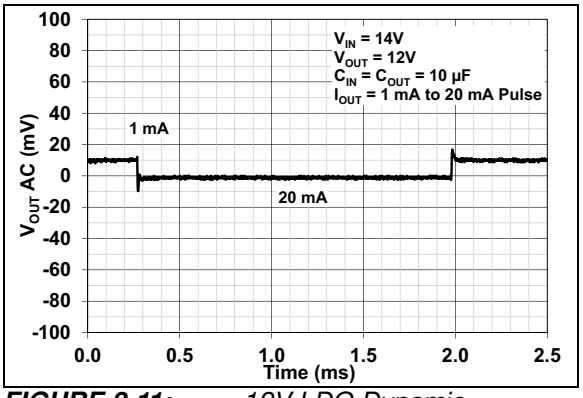


FIGURE 2-11: *12V LDO Dynamic Loadstep.*

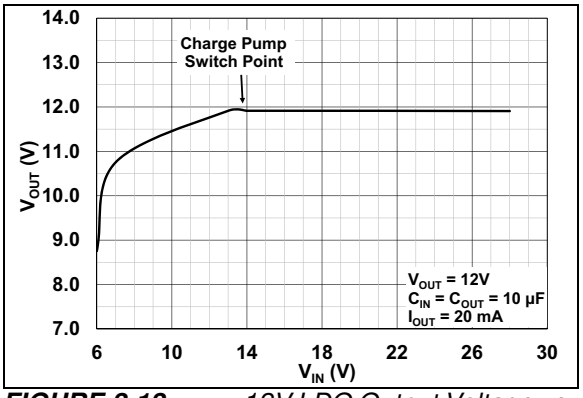


FIGURE 2-12: *12V LDO Output Voltage vs. Rising Input Voltage.*

Note: Unless otherwise indicated, T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

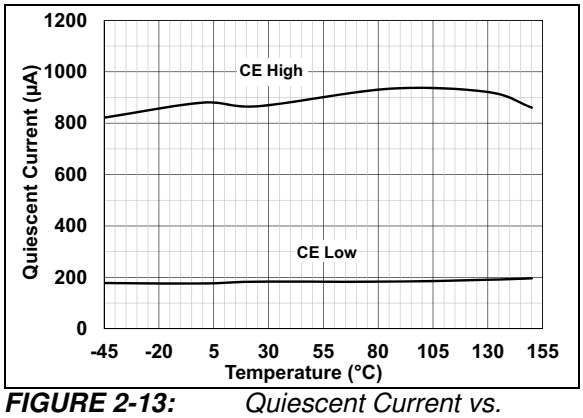


FIGURE 2-13: *Quiescent Current vs. Temperature* ***(MCP8025)****.*

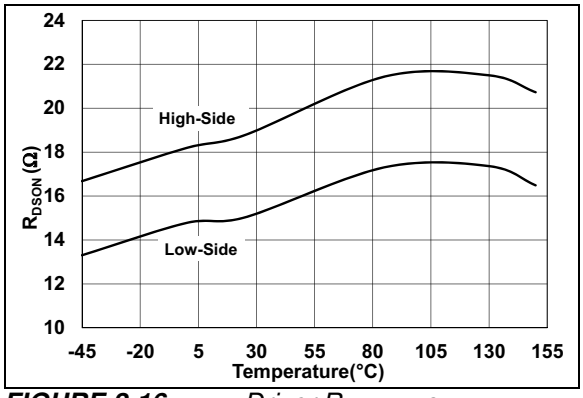


FIGURE 2-16: *Driver R_{DSON} vs. Temperature.*

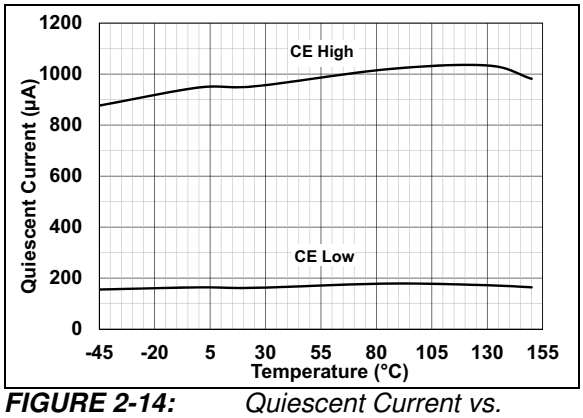


FIGURE 2-14: *Quiescent Current vs. Temperature* ***(MCP8026)****.*

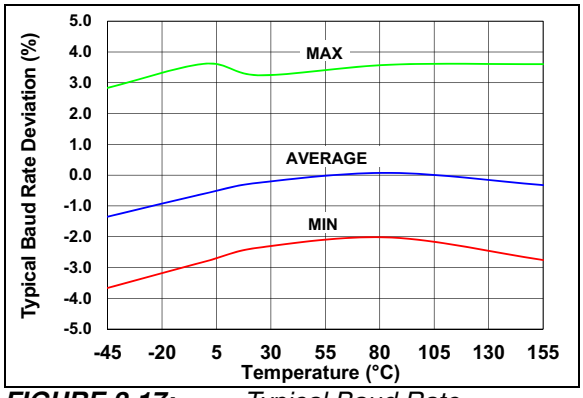


FIGURE 2-17: *Typical Baud Rate Deviation.*

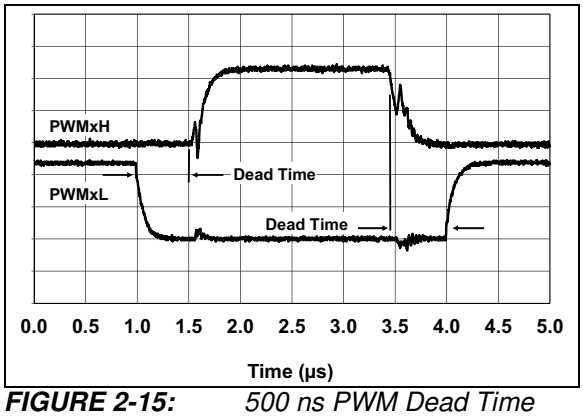


FIGURE 2-15: *500 ns PWM Dead Time Injection.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Tables 3-1 and 3-2.

TABLE 3-1: MCP8025 – PIN FUNCTION TABLE

QFN	TQFP	Symbol	I/O	Description
2	1	PWM1L	I	Digital input, phase A low-side control, 47 kΩ pull down
3	2	PWM1H	I	Digital input, phase A high-side control, 47 kΩ pull down
4	3	CE	I	Digital input, device enable, 47 kΩ pull down
—	4	NC	—	No connection
—	5	NC	—	No connection
5	6	LIN_BUS	I/O	LIN Bus physical layer
—	7	PGND	Power	Power 0V reference
6	8	RX	O	LIN Bus receive data, open-drain
7	9	TX	I	LIN Bus transmit data
8	10	$\overline{\text{FAULT}}$n/TXE	I/O	LIN transceiver fault and transmit enable
9	11	MUX1	I	Digital input Back EMF sampler phase multiplexer control, 47 kΩ pull down
10	12	MUX2	I	Digital input Back EMF sampler phase multiplexer control, 47 kΩ pull down
11	13	ZC_OUT	O	Back EMF sampler comparator output, open-drain
12	14	COMP_REF	I	Back EMF sampler comparator reference
13	15	$\overline{\text{ILIMIT\_OUT}}$	O	Current limit comparator, MOSFET driver fault output, open-drain
14	16	I_OUT1	O	Motor current sense amplifier output
15	17	ISENSE1-	I	Motor current sense amplifier inverting input
16	18	ISENSE1+	I	Motor current sense amplifier non-inverting input
17	19,20	PGND	Power	Power 0V reference
18	21	LSA	O	Phase A low-side N-channel MOSFET driver, active high
19	22	LSB	O	Phase B low-side N-channel MOSFET driver, active high
20	23	LSC	O	Phase C low-side N-channel MOSFET driver, active high
—	24	PGND	Power	Power 0V reference
21	25	HSC	O	Phase C high-side N-channel MOSFET driver, active high
22	26	HSB	O	Phase B high-side N-channel MOSFET driver, active high
23	27	HSA	O	Phase A high-side N-channel MOSFET driver, active high
24	28	PHC	I/O	Phase C high-side MOSFET driver reference, Back EMF sense input
25	29	PHB	I/O	Phase B high-side MOSFET driver reference, Back EMF sense input
26	30	PHA	I/O	Phase A high-side MOSFET driver reference, Back EMF sense input
27	31	VBC	Power	Phase C high-side MOSFET driver bias
28	32	VBB	Power	Phase B high-side MOSFET driver bias
29	33	VBA	Power	Phase A high-side MOSFET driver bias
30	34	+12V	Power	Analog circuitry and low-side gate drive bias
—	35, 36	PGND	Power	Power 0V reference
31	37	LX	Power	Buck regulator switch node, external inductor connection
32	38, 39	VDD	Power	Input Supply
33	40	FB	I	Buck regulator feedback node
34	41	+5V	Power	Internal circuitry bias
35	42	CAP2	Power	Charge pump flying capacitor input
36	43	CAP1	Power	Charge pump flying capacitor input
37	44	DE2	O	Voltage and temperature supervisor output, open-drain
38	45	PWM3L	I	Digital input, phase C low-side control, 47 kΩ pull down
39	46	PWM3H	I	Digital input, phase C high-side control, 47 kΩ pull down
40	47	PWM2L	I	Digital input, phase B low-side control, 47 kΩ pull down
1	48	PWM2H	I	Digital input, phase B high-side control, 47 kΩ pull down
EP	EP	PGND	Power	Exposed Pad. Connect to Power 0V reference.

TABLE 3-2: MCP8026 – PIN FUNCTION TABLE

QFN	TQFP	Symbol	I/O	Description
2	1	PWM1L	I	Digital input, phase A low-side control, 47 kΩ pull down
3	2	PWM1H	I	Digital input, phase A high-side control, 47 kΩ pull down
4	3	CE	I	Digital input, device enable, 47 kΩ pull down
—	4	LV_OUT2	O	Level Translator 2 logic level translated output, open-drain
—	5	HV_IN2	I	Level Translator 2 high-voltage input, 30 kΩ configurable pull up
5	6	HV_IN1	I	Level Translator 1 high-voltage input, 30 kΩ configurable pull up
—	7	PGND	Power	Power 0V reference
6	8	LV_OUT1	O	Level Translator 1 logic level translated output, open-drain
7	9	I_OUT3	O	Motor phase current sense amplifier 3 output
8	10	ISENSE3-	I	Motor phase current sense amplifier 3 inverting input
9	11	ISENSE3+	I	Motor phase current sense amplifier 3 non-inverting input
10	12	I_OUT2	O	Motor phase current sense amplifier 2 output
11	13	ISENSE2-	I	Motor phase current sense amplifier 2 inverting input
12	14	ISENSE2+	I	Motor phase current sense amplifier 2 non-inverting input
13	15	$\overline{\text{ILIMIT\_OUT}}$	O	Current limit comparator, MOSFET driver fault output, open-drain
14	16	I_OUT1	O	Motor current sense amplifier 1 output
15	17	ISENSE1-	I	Motor current sense amplifier 1 inverting input
16	18	ISENSE1+	I	Motor current sense amplifier 1 non-inverting input
17	19,20	PGND	Power	Power 0V reference
18	21	LSA	O	Phase A low-side N-Channel MOSFET driver, active high
19	22	LSB	O	Phase B low-side N-Channel MOSFET driver, active high
20	23	LSC	O	Phase C low-side N-Channel MOSFET driver, active high
—	24	PGND	Power	Power 0V reference
21	25	HSC	O	Phase C high-side N-Channel MOSFET driver, active high
22	26	HSB	O	Phase B high-side N-Channel MOSFET driver, active high
23	27	HSA	O	Phase A high-side N-Channel MOSFET driver, active high
24	28	PHC	I/O	Phase C high-side MOSFET driver reference, Back EMF sense input
25	29	PHB	I/O	Phase B high-side MOSFET driver reference, Back EMF sense input
26	30	PHA	I/O	Phase A high-side MOSFET driver reference, Back EMF sense input
27	31	VBC	Power	Phase C high-side MOSFET driver bias
28	32	VBB	Power	Phase B high-side MOSFET driver bias
29	33	VBA	Power	Phase A high-side MOSFET driver bias
30	34	+12V	Power	Analog circuitry and low-side gate drive bias
—	35,36	PGND	Power	Power 0V reference
31	37	LX	Power	Buck regulator switch node, external inductor connection
32	38, 39	VDD	Power	Input supply
33	40	FB	I	Buck regulator feedback node
34	41	+5V	Power	Internal circuitry bias
35	42	CAP2	Power	Charge pump flying capacitor input
36	43	CAP1	Power	Charge pump flying capacitor input
37	44	DE2	O	Voltage and temperature supervisor output, open-drain
38	45	PWM3L	I	Digital input, phase C low-side control, 47 kΩ pull down
39	46	PWM3H	I	Digital input, phase C high-side control, 47 kΩ pull down
40	47	PWM2L	I	Digital input, phase B low-side control, 47 kΩ pull down
1	48	PWM2H	I	Digital input, phase B high-side control, 47 kΩ pull down
EP	EP	PGND	Power	Exposed Pad. Connect to Power 0V reference.

3.1 Low-Side PWM Inputs (PWM1L, PWM2L, PWM3L)

Digital PWM inputs for low-side driver control. Each input has a 47 kΩ pull down to ground. The PWM signals may contain dead-time timing or the system may use configuration register 2 (CFG2) to set the dead time.

3.2 High-Side PWM Inputs (PWM1H, PWM2H, PWM3H)

Digital PWM inputs for high-side driver control. Each input has a 47 kΩ pull down to ground. The PWM signals may contain dead-time timing or the system may use the configuration register 2 (CFG2) to set the dead time.

3.3 No Connect (NC)

Reserved. Do not connect.

3.4 Chip Enable Input (CE)

Chip Enable input is used to enable/disable the output driver and on-board functions. When CE is high, all device functions are enabled. When CE is low, the device operates in Standby or Sleep mode. When Standby mode is active, the current amplifiers and the 12V LDO are disabled. The buck regulator, the DE2 pin, the voltage and temperature sensor functions are not affected. The 5V LDO is disabled on the MCP8026. The H-bridge driver outputs are all set to a low state within 100 ns of CE = 0. The device transitions to Standby or Sleep mode 1 ms after CE = 0.

The CE pin may be used to clear any hardware faults. When a fault occurs, the CE input may be used to clear the fault by setting the pin low and then high again. The fault is cleared by the rising edge of the CE signal if the hardware fault is no longer active.

The CE pin is used to enable Sleep mode when the SLEEP bit in the CFG0 configuration register is set to '1'. CE must be low for a minimum of 1 ms before the transition to Standby or Sleep mode occurs. This allows time for CE to be toggled to clear any faults without going into Sleep mode.

The CE pin is used to awaken the device from the Sleep mode state. To awaken the device from a Sleep mode state, the CE pin must be set low for a minimum of 250 µs. The device will then wake up with the next rising edge of the CE pin.

The CE pin has an internal 47 kΩ pull down.

3.5 Level Translators (HV_IN1, HV_IN2, LV_OUT1, LV_OUT2)

Unidirectional digital level translators. These pins translate digital input signal on the HV_INx pin to a low-level digital output signal on the LV_OUTx pin. The HV_INx pins have internal 30 kΩ pull ups to V_{DD} that are controlled by bit PU30K in the CFG0 configuration register. The PU30K bit is only sampled during CE = 0.

The HV_IN1 pin has higher ESD protection than the HV_IN2 pin. The higher ESD protection makes the HV_IN1 pin better suited for connection to external switches.

LV_OUT1 and LV_OUT2 are open-drain outputs. An external pull-up resistor to the low-voltage logic supply is required.

The HV_IN1 pin may be used to awaken the device from the Sleep mode state. The MCP8026 will awaken on the rising edge of the pin after detecting a low state lasting > 250 µs on the pin.

3.6 LIN Transceiver Bus (LIN_BUS)

The bidirectional LIN_BUS interface pin connects to the LIN Bus network. The LIN_BUS driver is controlled by the TX pin. The driver is an open-drain output. The MCP8025 device contains a LIN Bus 30 kΩ pull-up resistor that may be enabled or disabled by setting the PU30K bit in the CFG0 configuration register. The pull up may only be changed while in Standby mode. During normal operation, the 30 kΩ pull up is always enabled. In Sleep mode, the 30 kΩ pull up is always disabled.

The LIN bus may be used to awaken the device from the Sleep mode state. When a LIN wake-up event is detected on the LIN_BUS pin, the device will wake up. The MCP8025 will awaken on the rising edge of the bus after detecting a dominant state lasting > 150 µs on the bus. The LIN Bus master must provide the dominant state for > 250 µs to meet the LIN 2.2A specifications.

3.7 Power Ground (PGND), Exposed Pad (EP)

Device ground. The PCB ground traces should be short and wide and should form a STAR pattern to the power source. The Exposed Pad (EP) must be soldered to the PCB. The PCB area below the EP should be a copper pour with thermal vias to help transfer heat away from the device.

3.8 LIN Transceiver Received Data Output (RX)

The RX output pin follows the state of the LIN_BUS pin. The data received from the LIN bus is output on the RX pin for connection to a host MCU.

The RX pin is an open-drain output.

3.9 LIN Transceiver Transmit Data Input (TX)

The TX input pin is used to send data to the LIN Bus. The LIN_BUS pin is low (dominant) when TXD is low and high (recessive) when TXD is high. Data to be transmitted from a host MCU is sent to the LIN bus via the TX pin.

3.10 LIN Transceiver Fault/ Transmit Enable (FAULTn/TXE)

Fault Detect output and Transmitter Enable input bidirectional pin. The FAULTn/TXE pin will be driven low whenever a LIN fault occurs. There is a 47 kΩ resistor between the internal fault signal and the FAULTn/TXE pin to allow the pin to be externally driven high after a fault has occurred. The FAULTn/TXE pin must be pulsed high to start a transmit. If there is no fault present when the pin is pulsed, the FAULTn/TXE pin will latch and be driven high by an internal 47 kΩ impedance. The FAULTn/TXE pin may then be monitored for faults.

No external pull up is needed. The microcontroller pin controlling the FAULTn/TXE pin must be able to switch between output and input modes.

3.11 Zero-Crossing Multiplexer Inputs (MUX1, MUX2)

The MUX1 and MUX2 multiplexer inputs select the desired phase winding to be used as the zero-crossing Back EMF phase reference. The output of the multiplexer connects to one input of the zero-crossing comparator. The other zero-crossing comparator input connects to the neutral voltage. The MUX1 and MUX2 inputs must be driven by the host processor synchronously with the motor commutation.

3.12 Zero-Crossing Detector Output (ZC_OUT)

The ZC_OUT output pin is the output of the zero-crossing comparator. When the phase voltage selected by the multiplexer inputs crosses the neutral voltage, the zero-crossing detector will change the output state.

The ZC_OUT output is an open-drain output.

3.13 Neutral Voltage Reference Input (COMP_REF)

The COMP_REF input pin is used to connect to the neutral point of a motor if the neutral point is available. The COMP_REF input may be selected via a configuration register as the neutral voltage reference used by the zero-crossing comparator.

3.14 Current Limit and Driver Fault Output (ILIMIT_OUT)

Dual-purpose output pin. The open-drain output goes low when the current sensed by current sense amplifier 1 exceeds the value set by the internal current reference DAC. The DAC has an offset of 0.991V (typical) which represents the zero current flow.

The open-drain output will also go low while a fault is active. Table 4-1 shows the faults that cause the ILIMIT_OUT pin to go low.

The ILIMIT_OUT pin is able to sink 1 mA of current while maintaining less than a 50 mV drop across the output.

3.15 Operational Amplifier Outputs (I_OUT1, I_OUT2, I_OUT3)

Current sense amplifier outputs. May be used with feedback resistors to set the current sense gain. The amplifiers are disabled when CE = 0.

3.16 Operational Amplifier Inputs (ISENSE1 +/-, ISENSE2 +/-, ISENSE3 +/-)

Current sense amplifier inverting and non-inverting inputs. Used in conjunction with the I_OUTn pin to set the current sense gain. The amplifiers are disabled when CE = 0.

3.17 Low-Side N-Channel MOSFET Driver Outputs (LSA, LSB, LSC)

Low-side N-channel MOSFET drive signal. Connect to the gate of the external MOSFETs. A low-impedance resistor may be used between these pins and the MOSFET gates to limit current and slew rate.

3.18 High-Side N-Channel MOSFET Driver Outputs (HSA, HSB, HSC)

High-side N-channel MOSFET drive signal. Connect to the gate of the external MOSFETs. A low-impedance resistor may be used between these pins and the MOSFET gates to limit current and slew rate.

3.19 Driver Phase Inputs (PHA, PHB, PHC)

Phase signals from motor. These signals provide high-side N-channel MOSFET driver reference and Back EMF sense input. The phase signals are also used with the bootstrap capacitors to provide high-side gate drive via the VBx inputs.

3.20 Driver Bootstrap Inputs (VBA, VBB, VBC)

High-side MOSFET driver bias. Connect these pins between the bootstrap charge pump diode cathode and the bootstrap charge pump capacitor. The 12V LDO output is used to provide 12V at the diode anodes. The phase signals are connected to the other side of the bootstrap charge pump capacitors. The bootstrap capacitors charge to 12V when the phase signals are pulled low by the low-side drivers. When the low-side drivers turn off and the high-side drivers turn on, the phase signal is pulled to V_{DD}, causing the bootstrap voltage to rise to V_{DD} + 12V.

3.21 12V LDO (+12V)

+12-volt Low Dropout (LDO) voltage regulator output. The +12V LDO may be used to power external devices such as Hall-effect sensors or amplifiers. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the +12V pin as is practical. For most applications, 4.7 µF of capacitance will ensure stable operation of the LDO circuit. The +12V LDO is supplied by the internal charge pump when the charge pump is active. When the charge pump is inactive, the +12V LDO is supplied by V_{DD}.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.22 Buck Regulator Switch Output (LX)

Buck regulator switch node external inductor connection. Connect this pin to the external inductor chosen for the buck regulator.

3.23 Power Supply Input (VDD)

Connect VDD to the main supply voltage. This voltage should be the same as the motor voltage. The driver overcurrent and overvoltage shutdown features are relative to the VDD pin. When the VDD voltage is separate from the motor voltage, the overcurrent and overvoltage protection features may not be available.

The VDD voltage must not exceed the maximum operating limits of the device. Connect a bulk capacitor close to this pin for good loadstep performance and transient protection.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.24 Buck Regulator Feedback Input (FB)

Buck regulator feedback node that is compared to an internal 1.25V reference voltage. Connect this pin to a resistor divider that sets the buck regulator output voltage. Connecting this pin to a separate +2.5V to +5.5V supply will disable the buck regulator. The FB pin should not be connected to the +5V LDO to disable the buck because the +5V LDO starts after the buck in the internal state machine. The lack of voltage at the FB pin would cause a buck UVLO fault.

3.25 5V LDO (+5V)

+5-volt Low Dropout (LDO) voltage regulator output. The +5V LDO may be used to power external devices, such as Hall-effect sensors or amplifiers. The +5V LDO is disabled on the MCP8026 when CE = 0. The internal state machine starts the buck regulator before the +5V LDO, so the +5V LDO should not be connected to the buck FB pin to disable the buck regulator. A buck UVLO fault will occur if the +5V LDO is used to disable the buck regulator. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the +5V pin as is practical. For most applications, 4.7 µF of capacitance will ensure stable operation of the LDO circuit.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.26 Charge Pump Flying Capacitor (CAP1, CAP2)

Charge pump flying capacitor connections. Connect the charge pump capacitor across these two pins. The charge pump flying capacitor supplies the power for the 12V LDO when the charge pump is active.

3.27 Communications Port (DE2)

Open-drain communication node. The DE2 communication is a half-duplex, 9600 baud, 8-bit, no parity communication link. The open-drain DE2 pin must be pulled high by an external pull-up resistor. The pin has a minimum drive capability of 1 mA resulting in a V_{DE2} of $\leq$ 50 mV when driven low.

4.0 DETAILED DESCRIPTION

4.1 State Diagrams

4.1.1 MCP8025 STATE DIAGRAM

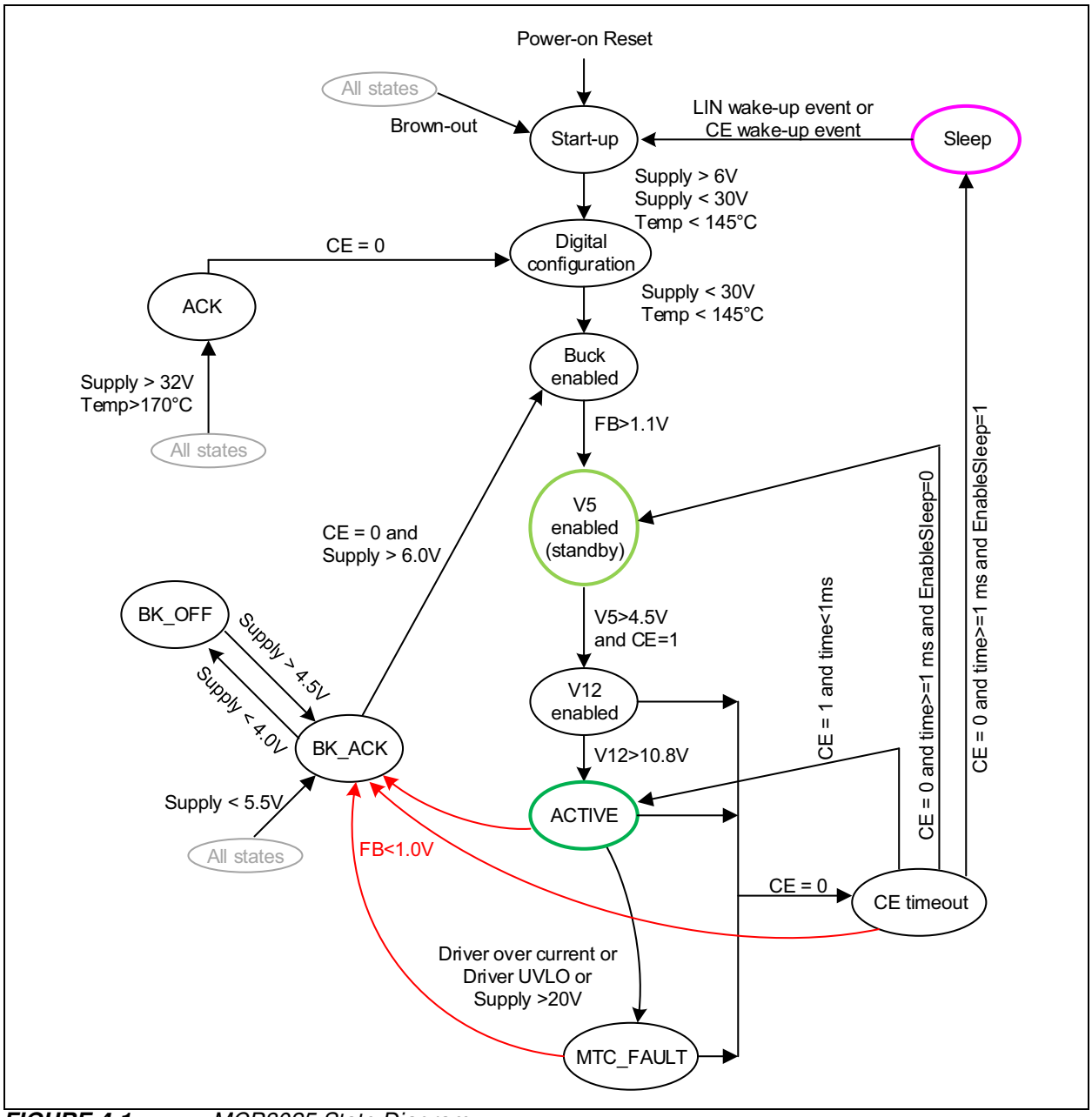


FIGURE 4-1: *MCP8025 State Diagram.*