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MCR20A 2.4 GHz Low-Power Transceiver Reference Manual

Supports: MCR20AVHM

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Chapter 1
Introduction to MCR20A

1.1 Introduction

The MCR20A transceiver is a 2.4 GHz Industrial, Scientific and Medical (ISM) and Medical Body Area Network (MBAN) transceiver intended for the IEEE® 802.15.4 Standard. The MCR20A device is a standalone transceiver that is normally combined with a software stack and a Kinetis K series, M series or other microcontroller (MCU) to implement an IEEE 802.15.4 Standard platform solution.

The MCR20A transceiver contains a complete 802.15.4 physical layer (PHY) modem designed for the IEEE® 802.15.4 Standard that operates in the 2.4 GHz ISM frequency band and supports 2.36 to 2.4 GHz Medical Band (MBAN) frequencies. The transceiver includes antenna diversity, 1mW nominal output power, hardware acceleration for dual PAN modes, integrated transmit/receive switch, on-board power supply regulation, and full spread-spectrum encoding and decoding. Additionally, the transceiver includes a PA with internal voltage controlled oscillator (VCO), integrated transmit/receive switch, on-board power supply regulation.

The MCR20A transceiver supports peer-to-peer, star, and mesh networking and when combined with an appropriate MCU, the MCR20A transceiver provides a cost-effective solution for short-range data links and networks. Interface with the MCU is accomplished using a four wire serial peripheral interface (SPI) connection and an interrupt request output that allows for the use of a variety of processors. The software and processor can be scaled to fit applications ranging from simple point-to-point systems through complete mesh networking. The MCR20A transceiver provides the IEEE 802.15.4 Standard PHY/MAC for use with the Kinetis K20 or Cortex M0 family of MCUs.

This table lists the MCR20A device ordering, temperature range, and package information.

Table 1-1. Ordering Information

Device	Operating Temp Range (TA)	Package
MCR20AVHM(R)	-40° to 105° C	MLGA-32 (R: tape and reel)

Target markets include, but are not limited, to the following:

- Smart Energy
  - Meter
  - ESI (Energy Service Interface)
  - IHD (In Home Display)
  - Gateway
  - Appliance
  - PHEV (Plug-in Hybrid Electric Vehicle)
- Building Control and Home Automation
  - Lighting
  - HVAC
  - Security
- Medical / Personal Health Care
  - Patient Monitoring
  - Institutional Care
- Industrial Control (3rd party stacks - (Low PAN, ISA100, Wireless HART)

1.2 Block Diagram

This figure shows a simplified block diagram of the MCR20A transceiver, which is an 802.15.4 Standard compatible transceiver that provides functions required in the physical layer (PHY) and media access control (MAC) specifications.

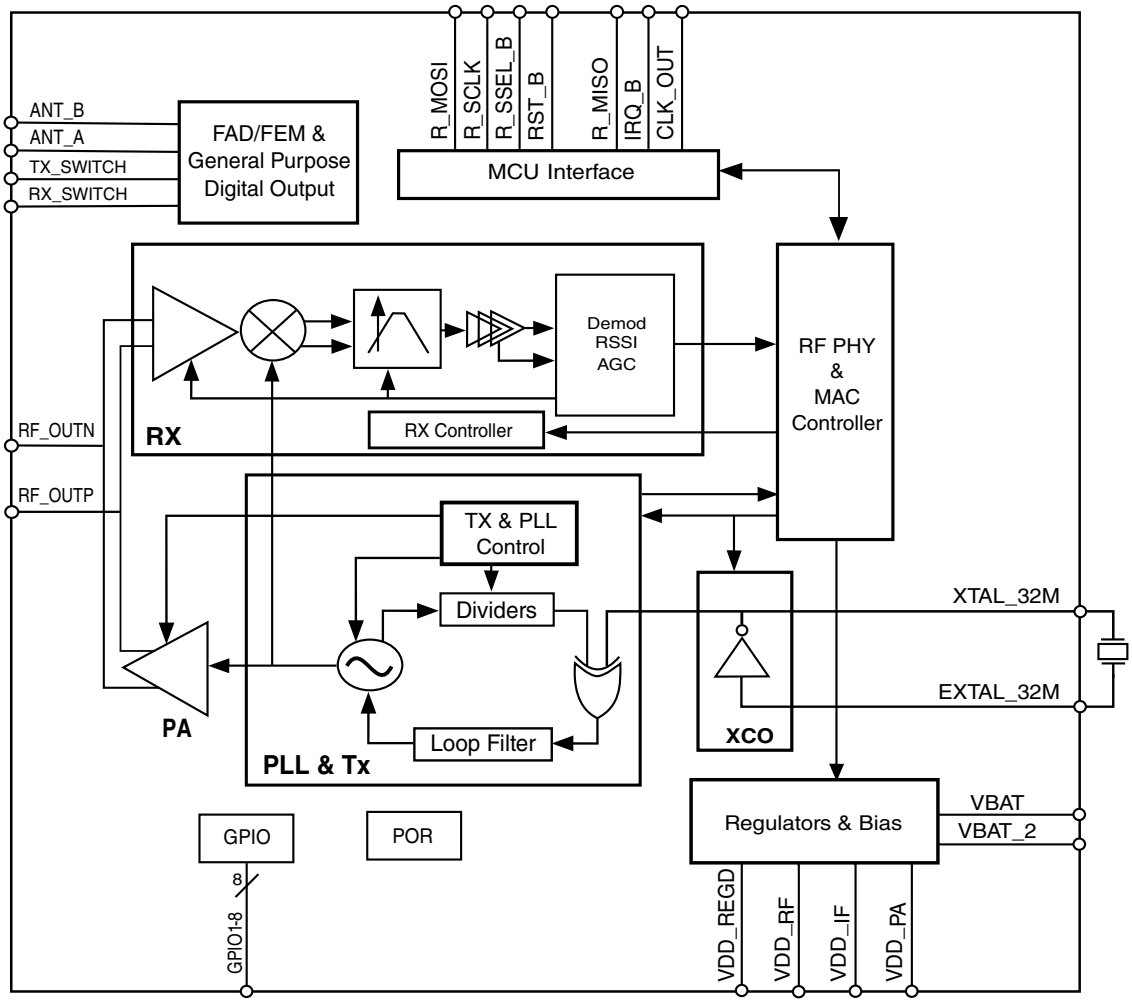

Figure 1-1. Modem Simplified Block Diagram

The modem is used in concert with an MCU. Interface between the devices is accomplished through a 4-wire SPI port and interrupt request line. The media access control (MAC), drivers, and network and application software (as required) reside on the host processor.

1.3 Modem Features Summary

The transceiver has the following features:

- Fully compliant IEEE 802.15.4 Standard 2006 transceiver supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode, and also extends radio operation to the 2.36 GHz to 2.40 GHz Medical Band (MBAN) frequencies with IEEE 802.15.4j channel, spacing and modulation requirements.

- 2.4GHz frequency band of operation (ISM).
- 250kbps data rate with O-QPSK modulation in 5.0 MHz channels with direct sequence spread spectrum (DSSS) encode and decode.
- Operates on one of 16 selectable ISM channels per IEEE 802.15.4 specification.
- Programmable output power
- Supports 2.36 GHz to 2.40 GHz Medical Band (MBAN) frequencies with IEEE 802.15.4j channel, spacing and modulation requirements.

- Small RF foot print
  - Differential input/output port used with external balun for single port operation.
  - Supports antenna diversity operation with external front end (FE).
  - Low external component count.
- Hardware acceleration for IEEE® 802.15.4 Standard
  - Complete 802.15.4 onboard modem
  - IEEE 802.15.4 Standard 2006 packet processor/sequencer with receiver frame filtering
  - Random number generator
  - Support for dual PAN ID mode
  - Internal event timer block with four comparators to assist sequencer and provide timer capability
- 32 MHz crystal reference oscillator with onboard trim capability to supplement external load capacitors
- Programmable frequency clock output (CLK_OUT) for use by MCU
- SPI Command Channel interface slave port with burst mode operation
- Interrupt request output (IRQ) - provides interrupt request capability to MCU
- 128-byte RAM data buffer to store 802.15.4 packet contents for transceiver sequences
- Eight (8) software programmable GPIOs
- Low power operational modes with single SPI command device wake-up (SPI communication is enabled in LP mode)

- 1.8 V to 3.6 V operating voltage with on chip voltage regulators
- -40C to +105C temperature range
- RoHS compliant, 5 mm x 5 mm, 32-pin, MLGA package

1.4 RF Interface and Usage

The modem RF interface provides a bidirectional, differential port that connects directly to a balun. The balun connects directly to a single-ended antenna and converts that interface to a fully differential, bidirectional, on-chip interface with transmit/receive switch, LNA, and complementary PA outputs. This combination allows for a small footprint and low cost RF solution.

In additional the modem provides dedicated output signals that can be used to control external RF components. These outputs are hardware switched and also support antenna diversity.

1.5 Radio Architecture

The radio structure is built upon the IEEE 802.15.4 Standard packet structure.

1.5.1 Packet Structure

The following figure shows the packet structure.

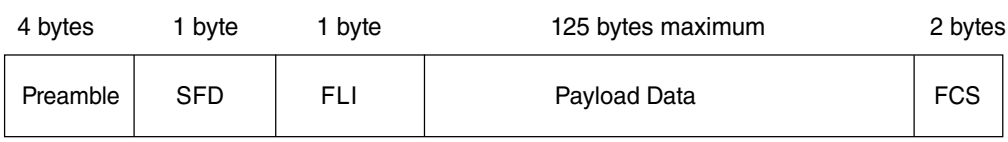

Figure 1-2. MCR20A Transceiver Packet Structure

1.5.2 Receive Path Description

The receive path operates in duplex with the transmit mode having an additional feature to operate in a low power run state that can also be considered as a partial power down mode. Architecture is Near Zero IF (NZIF) having front end amplification, one (1) mixed

signal down conversion to IF that is filtered, demodulated and digitally processed. The RF Front End (FE) is differential and shares the same off chip matching network with the transmit path.

1.5.3 Transmit Path Description

The modem transmits OQPSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The PA differential outputs share the pins with the front end.

1.6 IEEE 802.15.4 Acceleration Hardware

The 802.15.4 transceiver has several hardware features that reduce the software stack size, off-load functions from the CPU, and improve performance:

- Fully supports 2003 & 2006 versions of the IEEE 802.15 Standard.
- Supports slotted and unslotted modes
- Supports beacon enabled and non-beacon enabled networks
- Onboard 128-byte packet data buffering
- Random number generator
- 802.15.4 Sequence support
  - RX (conditionally followed by TXAck)
  - TX
  - CCA (used for CCA and ED cycles)
  - Tx/Rx (Tx followed by unconditional Rx or RCACK)
  - Continuous CCA
- 802.15.4 Receiver Frame filtering.

1.7 Advanced Security Module (ASM) Overview

The ASM engine encrypts using the Advanced Encryption Standard (AES). It can perform "Counter" (CTR), Cipher Block Chaining (CBC) and plain AES mode encryption. The combination of CTR and CBC modes of encryption is known as CCM mode encryption. CCM is short for Counter with CBC-MAC. CCM is a generic authenticate and encrypt block cipher mode. CCM is only defined for use with 128 bit block ciphers, such as AES.

The ASM has the following features:

- CTR encryption in 11 bus clock cycles.
- CBC encryption in 11 bus clock cycles
- AES encryption in 11 bus clock cycles.
- Encrypts 128 bits as a unit.

The ASM is designed to be loaded with data and then started with a self-clearing "start" bit. Sixteen 8 bit registers of a key plus sixteen 8 bit registers of a counter plus sixteen 8 bit registers of text are necessary for "Counter" mode encryption. Cipher Block Chaining (CBC) mode needs only a key field and a text field programmed. Typically, only the text fields and counter fields need to be continuously written since the key field won't change.

The module has a built in self test that must be initiated by the software to make the module usable. Until this test is run and passes the ASM module is disabled.

A simple block diagram of the ASM module is shown in the following figure.

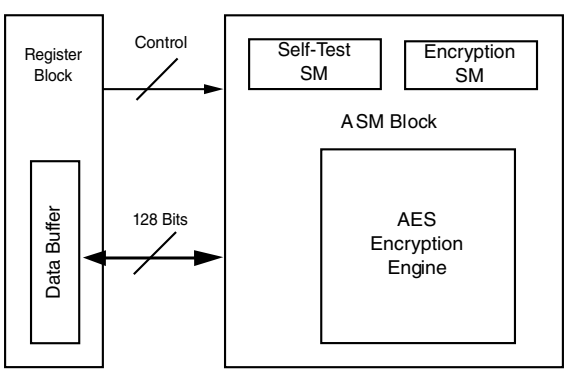

Figure 1-3. ASM Block Diagram

1.8 MCU Interface with SPI Overview

The following figure illustrates the microcontroller interface with the modem for the SiP. The typical required signals are:

- 4-wire SPI port - slave mode only
  - Maximum bitrate is 16 MHz for writes and 9 MHz for reads
  - Clock phase and polarity - CPHA=0 and CPOL=0
  - MSB first shifting
  - Supports Register Access and Packet Buffer accesses in bursts of byte transfers
  - Most registers and Packet Buffer accessible with crystal "on" or "off"
- Interrupt request output - active low
- Device asynchronous hardware reset RST_B - active low

The SPI interface provides communication between the MCU and the modem's register set and Packet Buffer. The modem SPI is a slave-only interface; the MCU must drive R_SSEL_B, R_SCLK and R_MOSI. Write and read access to both Direct and Indirect registers is supported, and transfer length can be single-byte or bursts of unlimited length. Write and read access to the Packet buffer can also be single-byte or a burst mode of unlimited length.

The SPI interface is asynchronous to the rest of the device. No relationship between R_SCLK and the modem's internal oscillator is assumed. All synchronization of the SPI interface to modem takes place inside the SPI module and is done for both register writes and reads.

The SPI is capable of operation in all power modes except reset. Operation in the Hibernate state means radio’s crystal oscillator is disabled; effectively no XTAL connected in hibernate mode. Most radio registers, direct and indirect, can be accessed, both read and write, during Hibernate; and includes the complete Packet Buffer. All GPIO-related registers are accessible in Hibernate. In this state minimal power consumption will be realized especially during the register-initialization phase.

The SPI design features a compact, single-byte control word reducing SPI access latency to a minimum. Most SPI access types require only a single-byte control word with the address embedded in the control word. During control word transfer (the first byte of any

SPI access), the contents of the IRQSTS1 register (highest-priority status register) are are always shifted out so that the MCU gets access to IRQSTS1 with the minimum possible latency on every SPI access.

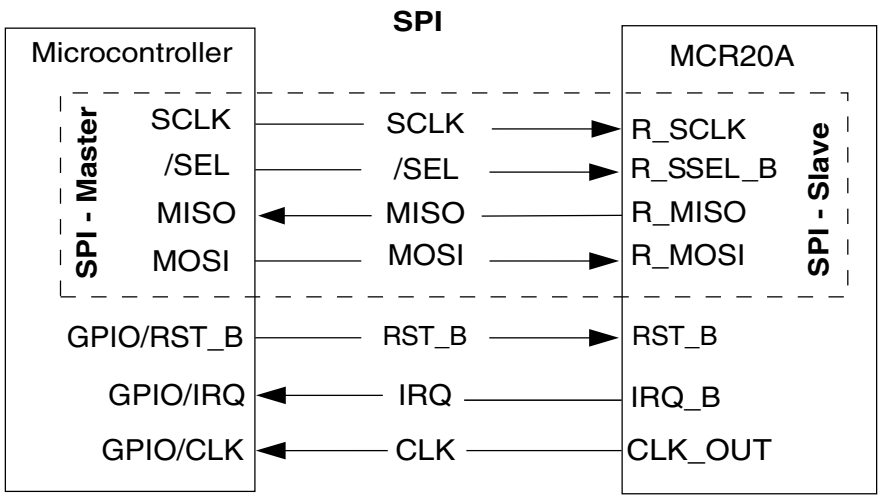

Figure 1-4. Microcontroller to modem interface block diagram

1.8.1 Transceiver Control Overview

The transceiver is controlled by a bank of registers (Direct Register Space) accessed via the SPI interface. The transmit and receive packet data (stored in a 128-byte buffer) is also accessed via the SPI. The onboard registers provide control and status for the entire device.

1.8.1.1 Interrupt Request Overview

The modem has up to 13 individual sources of interrupt request to the MCU. These are all capable of individual control, and are logically OR-combined to drive a single, active low, interrupt request pin (IRQ_B) to the external MCU.

- The IRQ_B pin is configured as actively-driven high by the modem.
- Each interrupt source has its own interrupt status bit in Direct Register space.
- Each interrupt can be individually controlled by an interrupt mask - The IRQ is issued when the mask is cleared to 0.
- There is also a global interrupt mask, TRCV_MSK, which can enable/disable all IRQ_B assertions by programming a single masking bit.

- All status bits use a write-1-to-clear protocol - interrupt status bits are not affected by reads.
- IRQ_B will remain asserted until all active interrupt sources are cleared or masked.

1.8.1.2 Event Timer Overview

The modem features a 24-bit Event Timer that can be used in conjunction with the sequencer to provide protocol control as well as timing interrupts. The Event Timer consists of a continuously running counter and four (4) separate 24-bit comparators:

- The Event Timer counter runs at the 802.15.4 bit rate of 250 kHz (programmable).
- Each comparator has an individual interrupt request capability - the compare status is set when there is a match between the comparator and the timer counter. Each status can be enabled to generate an IRQ.
- In addition, a separate 16-bit T2PRIMECMP comparator is provided, which uses only the *lower 16 bits* of Event Timer, rather than require a full 24-bit compare.

1.9 Clock Output, RF Control, and GPIO Summary

The modem provides a set of I/O pins useful for supplying a system clock to the MCU, controlling external RF LNA/PA or antenna diversity circuitry and GPIO. The following sections discuss these options.

1.9.1 CLK_OUT Reference

The CLK_OUT digital output can be enabled to drive the system clock to the MCU. This provides a highly accurate clock source based on the transceiver reference oscillator. The clock is programmable over a wide range of frequencies divided down from its 32 MHz reference.

1.9.2 RF Control Signals

The modem provides four dedicated signals for control of external RF components. These signals designated as ANT_A, ANT_B, RX_SWITCH, and TX_SWITCH can be enabled to control external amplifiers, antenna switches, and other modules. When enabled they are switched via an internal hardware state machine. Typical uses include:

- Antenna diversity
- External PA
- External LNA
- T/R switching

1.9.3 Antenna Diversity

To improve the reliability of RF connectivity to long range applications, Antenna Diversity feature is supported without using the MCU through use of four dedicated control pins by direct register antenna selection. The digital regulator supplies bias to analog switches for control of external PA/LNA. These switches are programmable to sink and source two levels of current (2-3 mA and 10 mA) or can operate in a high impedance mode.

1.9.4 General Purpose Input Output (GPIO)

In addition eight (8) GPIO are provided for general use. Features for these pins include:

- Programmable output drive strength
- Programmable output slew rate
- Hi-Z mode
- Programmable as outputs or inputs (default)
- No IRQ capability

1.10 Modem Operational Modes

The modem has six operating modes which include:

- Reset / Power-down
- Low Power (LP) / Hibernate
- Doze (low power with reference oscillator active)
- Idle
- Receive
- Transmit

The following table describes these modes:

Table 1-2. Modem Mode Definitions and Transition Times

Mode	Definition	Transition Time To or From Idle
Off	All modem functions Off, Leakage only. $\overline{RST}$ asserted. Digital outputs are tri-stated including IRQ	500 µs
Hibernate	Crystal Reference Oscillator Off. Modem responds to SPI activity.	250 µs
Doze	Crystal reference oscillator ON but CLK_OUT output available only if selected. Digital regulator in Low Power mode.	< 1 µs[1]
Reset	Crystal reference oscillator ON, enable CLK_OUT output at 4 MHz and 32.787 kHz.	376 µs
Receive	Crystal reference oscillator ON. Receiver ON.	144 µs
Transmit	Crystal reference oscillator ON. Transmitter ON.	144 µs

1. At 9 MHz, the doze to idle transistion time will be less than 2 SPI writes (1.8 µs).

1.11 External PA and LNA

The modem supports features to add either an external PA, LNA or RF switch which can extend the range or add antenna diversity to the target application. The following hardware features aid in the configuration of an FEM:

- Four dedicated programmable pins to sink and source 1mA, 2mA, 4mA and 8mA currents to control FEM (Front End Module) features such as a PA, LNA and RF switches for antenna diversity, etc.
- Balun used to optimize performance and provide a differential RX/TX output to single ended feature. Modem RX/TX outputs are differential “I” and “Q” and can be utilized in that format if desired.

Chapter 2
Signal Multiplexing and Signal Descriptions

2.1 Pin assignments

This figure shows the MCR20A transceiver's package pin assignment.

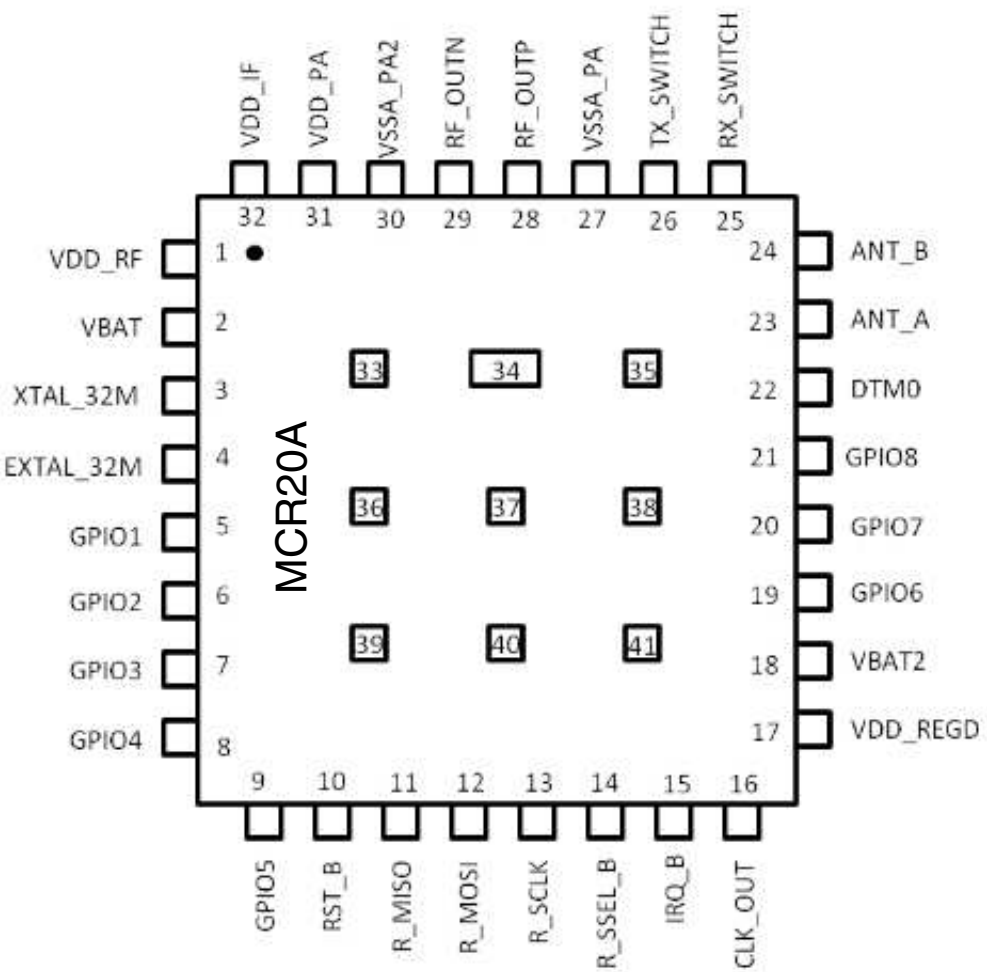

Figure 2-1. Pin assignment