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# **Sensitive Gate Silicon Controlled Rectifiers**

# **Reverse Blocking Thyristors**

Designed primarily for half-wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half-wave, silicon gate-controlled devices are needed.

### **Features**

- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- Blocking Voltage to 800 V
- On–State Current Rating of 8 A RMS at 80°C
- High Surge Current Capability 80 A
- Rugged, Economical TO-220AB Package
- Glass Passivated Junctions for Reliability and Uniformity
- Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- Immunity to dv/dt 5 V/usec Minimum at 110°C
- These are Pb-Free Devices\*

# **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage (Note 1) (T <sub>J</sub> = -40 to 110°C, Sine Wave, 50 to 60 Hz)  MCR8SDG MCR8SMG MCR8SNG	V <sub>DRM,</sub> V <sub>RRM</sub>	400 600 800	<b>V</b>
On-State RMS Current (180° Conduction Angles; T <sub>C</sub> = 80°C)	I <sub>T(RMS)</sub>	8.0	Α
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T <sub>J</sub> = 110°C)	I <sub>TSM</sub>	80	Α
Circuit Fusing Consideration (t = 8.33 ms)	I <sup>2</sup> t	26.5	A <sup>2</sup> sec
Forward Peak Gate Power (Pulse Width $\leq$ 10 $\mu$ s, T <sub>C</sub> = 80°C)	P <sub>GM</sub>	5.0	W
Forward Average Gate Power (t = 8.3 ms, T <sub>C</sub> = 80°C)	P <sub>G(AV)</sub>	0.5	W
Forward Peak Gate Current (Pulse Width $\leq$ 10 $\mu$ s, T <sub>C</sub> = 80°C)	I <sub>GM</sub>	2.0	Α
Operating Junction Temperature Range	TJ	-40 to 110	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

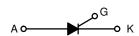
 V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

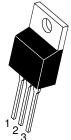


# ON Semiconductor®

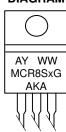
www.onsemi.com

# SCRs 8 AMPERES RMS 400 thru 800 VOLTS





# MARKING DIAGRAM



TO-220AB CASE 221A-09 STYLE 3

= Assembly Location

Y = Year

WW = Work Week

x = D, M, or N

G = Pb-Free Package

AKA = Diode Polarity

PIN ASSIGNMENT				
1	Cathode			
2	Anode			
3	Gate			
4	Anode			

# ORDERING INFORMATION

Device	Package	Shipping
MCR8SDG	TO-220AB (Pb-Free)	50 Units / Rail
MCR8SMG	TO-220AB (Pb-Free)	50 Units / Rail
MCR8SNG	TO-220AB (Pb-Free)	50 Units / Rail

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case Junction-to-Ambient	$R_{ heta JC} \ R_{ heta JA}$	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	TL	260	°C

Characteristic			Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (Note 3) $(V_D = Rated \ V_{DRM} \ and \ V_{RRM}; \ R_{GK} = 1 \ k\Omega)$	T <sub>J</sub> = 25°C T <sub>J</sub> = 110°C	I <sub>DRM</sub> , I <sub>RRM</sub>	- -	_ _	10 500	μΑ
ON CHARACTERISTICS						
Peak Forward On–State Voltage (Note 2) (I <sub>TM</sub> = 16 A)		V <sub>TM</sub>	-	_	1.8	V
Gate Trigger Current (Continuous dc) (Note 4) $(V_D = 12 \ V; \ R_L = 100 \ \Omega)$		I <sub>GT</sub>	5.0	25	200	μΑ
Holding Current (Note 3) (V <sub>D</sub> = 12 V, Gate Open, Initiating Current = 200 mA)		I <sub>H</sub>	-	0.5	6.0	mA
Latch Current (Note 4) $(V_D = 12 \text{ V, } I_G = 200  \mu\text{A})$		ΙL	-	0.6	8.0	mA
Gate Trigger Voltage (Continuous dc) (Note 4) $(V_D = 12 \text{ V}; R_L = 100 \Omega)$	$T_{J} = 25^{\circ}C$ $T_{J} = -40^{\circ}C$	V <sub>GT</sub>	0.3	0.65 -	1.0 1.5	V
Gate Non–Trigger Voltage $(V_D = 12 \text{ V}, R_L = 100 \Omega)$	T <sub>J</sub> = 110°C	$V_{GD}$	0.2	-	-	V
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off–State Voltage $(V_D=67\%\ V_{DRM},\ R_{GK}=1\ K\Omega,\ C_{GK}=0.1\ \mu F,\ T_J=110^{\circ}C)$		dv/dt	5.0	15	_	V/μs
Critical Rate of Rise of On–State Current IPK = 50 A, Pw = 40 μsec, diG/dt = 1 A/μsec, lgt = 10 mA		di/dt	-	-	100	A/μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

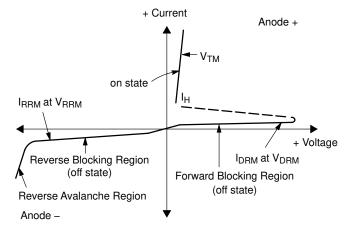
3. R<sub>GK</sub> = 1000 Ohms included in measurement.

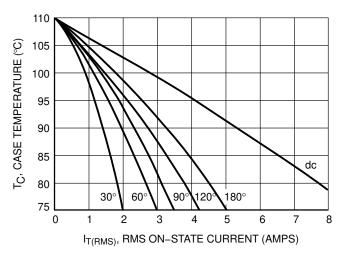
<sup>4.</sup> Does not include R<sub>GK</sub> in measurement.

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# **Voltage Current Characteristic of SCR**

Symbol	Parameter
V <sub>DRM</sub>	Peak Repetitive Off State Forward Voltage
I <sub>DRM</sub>	Peak Forward Blocking Current
V <sub>RRM</sub>	Peak Repetitive Off State Reverse Voltage
I <sub>RRM</sub>	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
I <sub>H</sub>	Holding Current

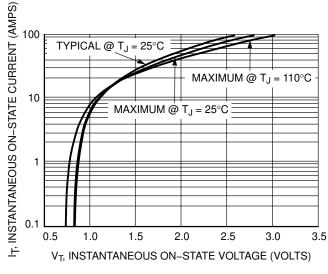




P(AV), AVERAGE POWER DISSIPATION (WATTS) dc 12 9 180° 120 90° 60° 6 30 3 3 5 8 I<sub>T(AV)</sub>, AVERAGE ON-STATE CURRENT (AMPS)

Figure 1. Typical RMS Current Derating

Figure 2. On-State Power Dissipation



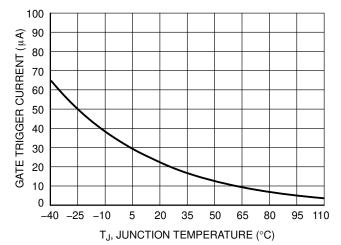
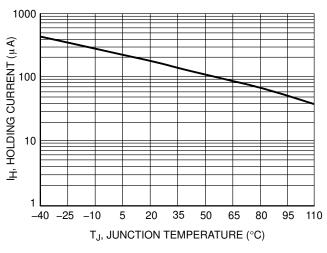


Figure 3. Typical On-State Characteristics

Figure 4. Typical Gate Trigger Current versus **Junction Temperature** 



V<sub>GT</sub>, GATE TRIGGER VOLTAGE (VOLTS) 1.0 0.9 8.0 0.7 0.6 0.5 0.4 0.3 0.2 **-40 -25** -10 20 35 50 65 95 110 T<sub>J</sub>, JUNCTION TEMPERATURE (°C)

Figure 5. Typical Holding Current versus Junction Temperature

Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

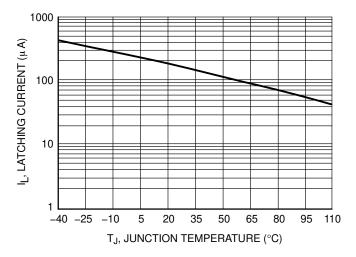
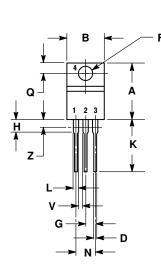
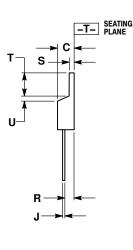


Figure 7. Typical Latching Current versus Junction Temperature

# PACKAGE DIMENSIONS

TO-220 CASE 221A-09 **ISSUE AH** 





### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.415	9.66	10.53
С	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

### STYLE 3:

PIN 1. CATHODE

- 2. ANODE
- GATE
- ANODE

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