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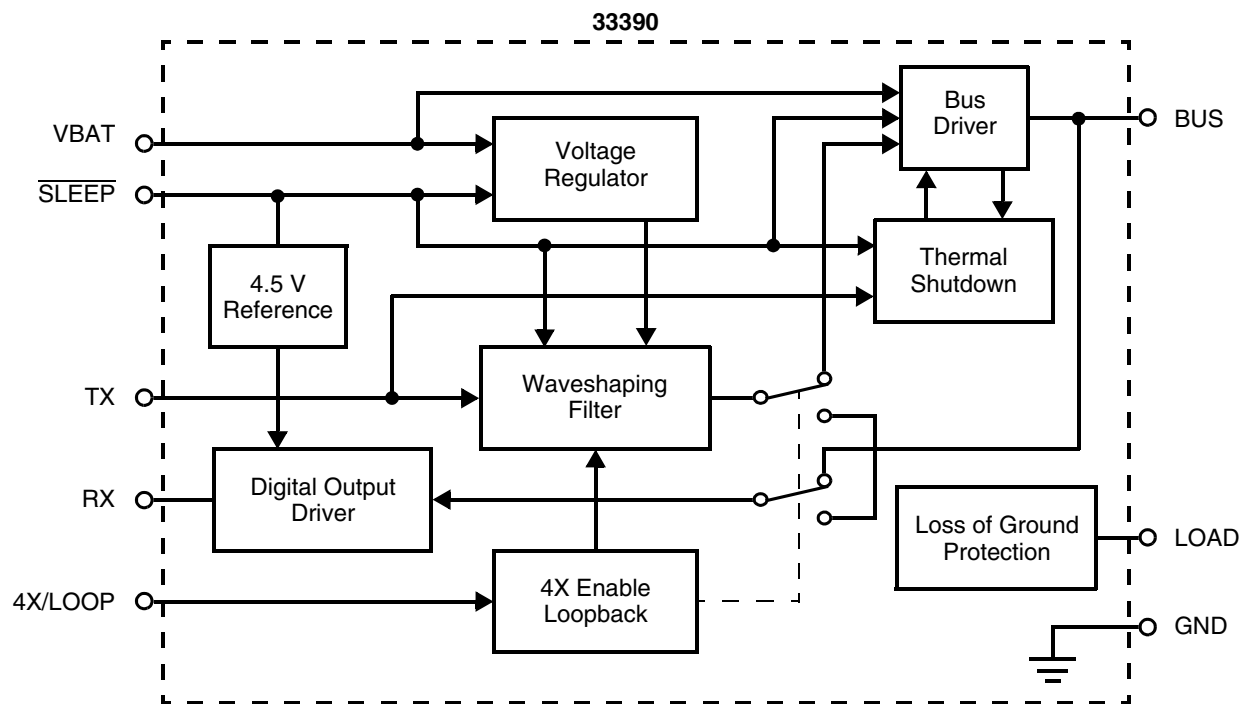
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INTERNAL BLOCK DIAGRAM



Note This device contains approximately 400 active transistors and 250 gates.

Figure 2. 33390 Simplified Internal Block Diagram

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of $7.0\text{ V} \leq V_{\text{BAT}} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_{\text{A}} \leq 125^\circ\text{C}$, SLEEP = 5.0 V unless otherwise noted. Typical values reflect the parameter's approximate midpoint average value with $V_{\text{BAT}} = 13\text{ V}$, $T_{\text{A}} = 25^\circ\text{C}$. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER CONSUMPTION					
Operational Battery Current (RMS with Tx = 7.812 kHz Square Wave) BUS Load = 1380 Ω to GND, 3.6 nF to GND BUS Load = 257 Ω to GND, 20.2 nF to GND	$I_{\text{BAT(OP1)}}$ $I_{\text{BAT(OP2)}}$	– –	3.0 22.4	11.5 32	mA
Battery Bus Low Input Current After SLEEP Toggle Low to High; Prior to Tx Toggling After Tx Toggle High to Low	$I_{\text{BAT(BUS L1)}}$ $I_{\text{BAT(BUS L2)}}$	– –	1.1 6.4	3.0 8.5	mA
Sleep State Battery Current $V_{\text{SLEEP}} = 0\text{ V}$	$I_{\text{BAT(SLEEP)}}$	–	38.2	65	μA
BUS					
BUS Input Receiver Threshold ⁽⁶⁾ Threshold High (Bus Increasing until Rx $\geq 3.0\text{ V}$) Threshold Low (Bus Decreasing until Rx $\leq 3.0\text{ V}$) Threshold in Sleep State ($\overline{\text{SLEEP}} = 0\text{ V}$) Hysteresis ($V_{\text{BUS(IH)}} - V_{\text{BUS(IL)}}$, $\overline{\text{SLEEP}} = 0\text{ V}$)	$V_{\text{BUS(IH)}}$ $V_{\text{BUS(IL)}}$ $BUS_{\text{TH(SLEEP)}}$ $V_{\text{BUS(HYST)}}$	4.25 – 2.4 0.1	3.9 3.7 3.0 0.2	– 3.5 3.4 0.6	V
BUS-Out Voltage ($257\ \Omega \leq R_{\text{BUS(L)}} \leq 1380\ \Omega$) $8.2\text{ V} \leq V_{\text{BAT}} \leq 16\text{ V}$, Tx = 5.0 V $4.25\text{ V} \leq V_{\text{BAT}} \leq 8.2\text{ V}$, Tx = 5.0 V Tx = 0 V	$V_{\text{BUS(OUT1)}}$ $V_{\text{BUS(OUT2)}}$ $V_{\text{BUS(OUT3)}}$	6.25 $V_{\text{BAT}} - 1.6$ –	6.9 – 0.27	8.0 V_{BAT} 0.7	V
BUS Short Circuit Output Current Tx = 5.0 V, $-2.0\text{ V} \leq V_{\text{BUS}} \leq 4.8\text{ V}$	$I_{\text{BUS(SHORT)}}$	60	129	170	mA
BUS Leakage Current $-2.0\text{ V} \leq V_{\text{BUS}} \leq 0\text{ V}$ $0\text{ V} \leq V_{\text{BUS}} \leq V_{\text{BAT}}$	$I_{\text{BUS(LEAK1)}}$ $I_{\text{BUS(LEAK2)}}$	-500 –	-55 189	– 500	μA
BUS Thermal Shutdown ⁽⁷⁾ (Tx = 5.0 V, $I_{\text{BUS}} = -0.1\text{ mA}$) Increase Temperature until $V_{\text{BUS}} \leq 2.5\text{ V}$	$T_{\text{BUS(LIM)}}$	150	170	190	$^\circ\text{C}$
BUS Thermal Shutdown Hysteresis ⁽⁸⁾ $T_{\text{BUS(LIM)}} - T_{\text{BUS(REEN)}}$	$T_{\text{BUS(LIMHYS)}}$	10	12	15	$^\circ\text{C}$
BUS and LOAD Current with Loss of V_{BAT} or GND ($I_{\text{BAT}} = 0\ \mu\text{A}$) (see Figure 4) $-18\text{ V} \leq V_{\text{BUS}} \leq 9.0\text{ V}$ $-18\text{ V} \leq V_{\text{LOAD}} \leq 9.0\text{ V}$	$I_{\text{BUS(LOSS)}}$ $I_{\text{LOAD(LOSS)}}$	– –	0.00 0.00	0.1 0.1	mA

Notes

- Typical threshold value is the approximate actual occurring switch point value with $V_{\text{BAT}} = 13\text{ V}$, $T_{\text{A}} = 25^\circ\text{C}$.
- Device characterized but not production tested for thermal shutdown.
- Device characterized but not production tested for thermal shutdown hysteresis.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions of $7.0 \text{ V} \leq V_{\text{BAT}} \leq 16 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, SLEEP = 5.0 V unless otherwise noted. Typical values reflect the parameter's approximate midpoint average value with $V_{\text{BAT}} = 13 \text{ V}$, $T_A = 25^\circ\text{C}$. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS (CONTINUED)					
LOAD Output $I_L = 6.0 \text{ mA}$	L_{ON}	–	0.07	0.2	V
Unpowered LOAD Output $V_{\text{BAT}} = 0 \text{ V}$, $I_L = 6.0 \text{ mA}$	L_{DIO}	0.3	0.56	0.9	V
TX					
Tx Input Voltage Tx Input Logic Low Level Tx Input Logic High Level	$V_{\text{Tx(IL)}}$ $V_{\text{Tx(IH)}}$	– 3.5	– –	0.8 –	V
Tx Input Current $V_{\text{Tx}} = 5.0 \text{ V}$ $V_{\text{Tx}} = 0 \text{ V}$	$I_{\text{Tx(IH)}}$ $I_{\text{Tx(IL)}}$	50 -2.0	106 0.23	200 2.0	μA
LOOP					
4X/LOOP Input Current $V_{4\text{X/LOOP}} = 0 \text{ V}$ (Normal Mode) $V_{4\text{X/LOOP}} = 5.0 \text{ V}$ (4X Mode)	$I_{4\text{X/LOOP(IL)}}$ $I_{4\text{X/LOOP(IH)}}$	-200 -200	-60 110	200 200	μA
4X/LOOP Input Threshold (Tx = 4096 Hz Square Wave) Normal Mode to Loopback Mode Loopback Mode to 4X Mode	$V_{4\text{X/LOOP(IL)}}$ $V_{4\text{X/LOOP(IH)}}$	1.1 3.2	1.31 3.43	1.5 3.6	V
RX					
Rx Output Voltage Low $V_{\text{BUS}} = 0 \text{ V}$, $I_{\text{Rx}} = 1.6 \text{ mA}$	$V_{\text{Rx(LOW)}}$	0.01	0.18	0.4	V
Rx Output Voltage High $V_{\text{BUS}} = 7.0 \text{ V}$, $I_{\text{Rx}} = -200 \mu\text{A}$	$V_{\text{Rx(HIGH)}}$	4.25	4.58	4.75	V
Rx Output Current $V_{\text{Rx}} = \text{High}$; Short Circuit Protection Limits	I_{Rx}	2.0	3.67	8.0	mA
SLEEP					
SLEEP Input Current $V_{\text{SLEEP}} = 0 \text{ V}$ $V_{\text{SLEEP}} = 5.0 \text{ V}$	$I_{\text{SLEEP(IL)}}$ $I_{\text{SLEEP(IH)}}$	– 1.0	-0.23 6.21	-2.0 20	μA

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33390 is a serial transceiver device designed to meet the SAE Standard J-1850 Class B performance for bi-directional half-duplex communication. The device is packaged in an economical surface-mount SOIC plastic package. An internal block diagram of the device is shown in [Figure 2](#).

The 33390 derives its robustness to temperature and voltage extremes from being built on a SMARTMOS process,

incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Though the 33390 was principally designed for automotive applications requiring SAE J-1850 Class B standards, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ and $7.0 \text{ V} \leq V_{\text{BAT}} \leq 16 \text{ V}$ supply. The economical 8-pin SOICN surface mount plastic package makes the device a cost-effective solution.

FUNCTIONAL PIN DESCRIPTION

Input Power (VBAT)

This is the only required input power source necessary to operate the 33390. The internal voltage reference of the 33390 will remain fully operational with a minimum of 9.0 V on this pin. Bus transmissions can continue with battery voltages down to 5.0 V. The bus output voltage will follow the battery voltage down and, in doing so, track approximately 1.6 V below the battery voltage. The device will continue to receive and transmit bus data to the microcontroller with battery voltages as low as 4.25 V. The pin can withstand voltages from -0.3 V to 40 V. If reverse battery protection is required, an appropriate diode must be placed in series with this pin to protect the IC.

Sleep Input (SLEEP)

This input is used to enable and disable the Class B transmitter. The Class B receiver is always enabled so long as adequate V_{BAT} pin voltage is applied. When the $\overline{\text{SLEEP}}$ pin voltage is 5.0 V, the Class B transmitter is enabled. If this input is 0 V, the Class B transmitter will be disabled and less than 65 μA of current will be drawn by the V_{BAT} pin. The pin also provides a 5.0 V reference, internal to the device, used to establish the Rx output level and slew rate times.

Class B Functional Description

The transmitter provides an analog waveshaped 0 V to 7.0 V waveform on the BUS output. It also receives waveforms and transmits a digital level signal back to a logic IC. The transmitter can drive up to 32 secondary Class B transceivers (see [Figures 10](#) and [11](#)). These secondary nodes may be at ground potentials that are $\pm 2.0 \text{ V}$ relative to the control assembly. Waveshaping will only be maintained during 2 of the 4 corners when the 0 to $\pm 2.0 \text{ V}$ ground potential difference condition exists. The 33390 is a secondary node on the Class B bus. Each secondary transceiver has a $470 \pm 10\%$ pF capacitor on its output for EMI suppression purposes, as well as a $10.6 \text{ k}\Omega \pm 5\%$ pull-down resistor to ground. The primary node has a $3300 \pm 10\%$ pF capacitor on its output for EMI suppression, as well as a $1.5 \text{ k}\Omega \pm 5\%$ pull-down resistor to ground. With more than 26 nodes, there is no primary node (see [Figure 12](#)). All nodes will have a $470 \pm 10\%$ pF capacitor and a $10.6 \text{ k}\Omega \pm 5\%$ pull-

down resistor. No matter how many secondary nodes are on the Class B bus, the RC time constant of the Class B bus is maintained at approximately 5.0 μs . The minimum and maximum capacitance and resistance on the Class B bus is given by the expressions shown in [Table 5](#), page [10](#).

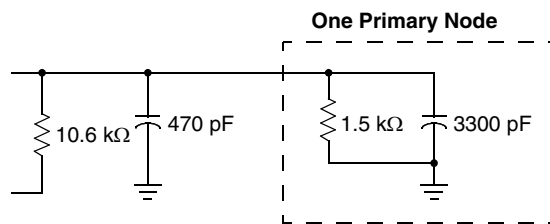


Figure 10. Minimum Bus Load

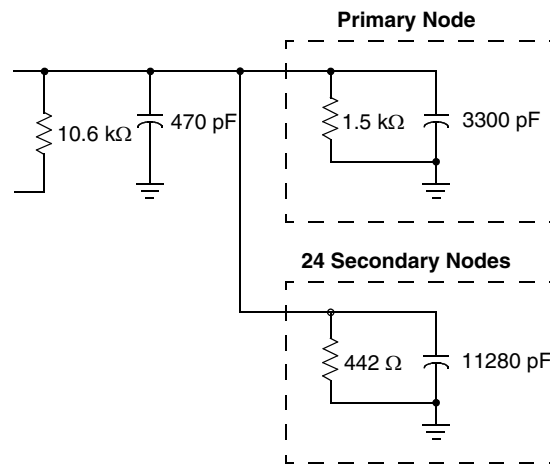


Figure 11. Maximum Number of Nodes

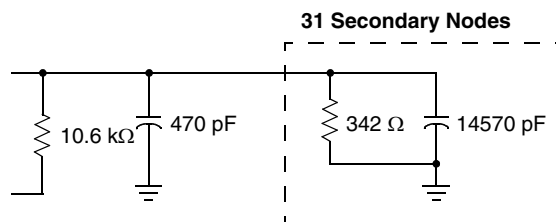


Figure 12. Maximum Bus Load

TYPICAL APPLICATIONS

Class B Module Inputs

Transmitter Data from the MCU (Tx)

The Tx input is a push-pull (N-channel/P-channel FETs) buffer with hysteresis for noise immunity purposes. This pin is a 5.0 V CMOS logic level input from the MCU following a true logic protocol. A logic [0] input drives the BUS output to 0 V (via the external pull-down resistor to ground on each node), while a logic [1] input produces a high voltage at the BUS output. A logic [0] input level is guaranteed when the Tx input pin is open-circuited by virtue of an internal 40 k Ω pull-down resistor. No external resistor is required for its operation.

Waveshaping and 4X/Loop

This input is a tristateable input: 0 V = normal waveshaping, 5.0 V = waveshaping is disabled for 4X transmitting, and high impedance = loopback mode of operation. This is a logic level input used to select whether waveshaping for the Class B output is enabled or disabled. A logic [0] enables waveshaping, while a logic [1] disables waveshaping. In the 4X mode, the BUS output rise time is less than 2.0 μ s and the fall time is less than 5.0 μ s (owing to the external RC pull-down to ground). In the loopback condition, the Tx signal is fed back to the Rx output *after* waveshaping *without* being transmitted onto the BUS. This mode of operation is useful for system diagnostic purposes.

Class B Module Outputs

Transceiver Output (BUS)

This is the output driver stage that sources current to the bus. Its output follows the waveshaped waveform input. Its output voltage is limited to 6.25 V to 8.0 V under normal battery level conditions. The limited level is controlled by an internal regulator/clamp circuit. Once the battery voltage drops below 9.0 V, the regulator/clamp circuit saturates, causing the bus voltage to track the battery voltage. A 1.5 k Ω \pm 5% external resistor (as well as any 10.6 k Ω pull-down resistors of any secondary nodes) sinks the current to discharge the capacitors during high-to-low transitions. This sourcing output is short circuit-protected (60 mA to 170 mA) against a short to -2.0 V and sinks less than 1.0 mA when shorted to VBAT. If a short occurs, the overtemperature shutdown circuit protects the source driver of the device. In the event battery power is lost to the assembly, the bus transmitter's output stage will be disabled and the leakage current from the BUS output will not source or sink more than 100 μ A of current. The transceiver will operate with a remote ground offset of \pm 2.0 V, but the lower corners of transmission will *not* be rounded during this condition.

Receiver Output to the Microcontroller (Rx)

This is a 5.0 V CMOS compatible push-pull output used to send received data to the microcontroller. It does not require an external pull-up resistor to be used. The receiver is always enabled and draws less than 65 μ A of current from V_{BAT} . The receive threshold is dependent on the state of the SLEEP pin. The receiver circuitry is able to operate with V_{BAT} voltages as low as 4.25 V and still remains capable of "waking up" the 33390 when remote Class B activity is detected.

When the \overline{SLEEP} pin is 0 V and message activity occurs on the bus, the receiver passes the bus message through to the microcontroller. The 33390 does not automatically "wake up" from a sleep state when bus activity occurs: the microcontroller must tell it to do so.

In the Static Electrical Characteristics table, the maximum voltage for Rx is specified as 4.75 V over an operating range of -40°C to 125°C temperature and 7.0 V to 16 V V_{BAT} . This maximum Rx voltage is compatible with the minimum V_{DD} voltage of microcontrollers to prevent the 33390 from sourcing current to the microcontroller's output.

Switched Ground Output (LOAD)

Normally this output is a saturated switch to ground, which pulls down the external resistor between the BUS and LOAD outputs. In the event ground is lost to the assembly, the LOAD output will bias itself "off" and will not leak more than 100 μ A of current out of this pin.

Overtemperature Shutdown

If the BUS output becomes shorted to ground for any duration, an overtemperature shutdown circuit "latches off" the output source transistor whenever the die temperature exceeds 150°C to 190°C. The output transistor remains latched off until the Tx input is toggled from a logic [0] to a logic [1]. The rising edge provides the clearing function, provided the locally sensed temperature is 10°C to 15°C below the latch-off temperature trip temperature.

Waveshaping

Waveshaping is incorporated into the 33390 to minimize radiated EMI emissions.

Receiver Protocol

The Class B communication scheme uses a variable pulse width (VPW) protocol. The microcontroller provides the VPW decoding function. Once the receiver detects a transition on Rx, it starts an internal counter. The initial "start of frame" bit is a logic [1] and lasts 200 μ s. For subsequent bits, if there is a bus transition before 96 μ s, one logic state is inferred. If there is a bus transition after 96 μ s, the other logic state is inferred. The "end of data" bit is a logic [0] and lasts 200 μ s. If there is no activity on the bus for 280 μ s to 320 μ s following a broadcast message, multiple unit nodes may arbitrate for control of the next message. During an arbitration, after the

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