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Quad DSI 2.02 Master with Differential Drive and Frequency Spreading

The 33781 is a master device for four differential DSI 2.02 buses. It contains the logic to interface the buses to a standard serial peripheral interface (SPI) port and the analog circuitry to drive data and power over the bus, as well as receive data from the remote slave devices.

The differential mode of the 33781 generates lower electromagnetic interference (EMI) in situations where data rates and wiring make this a problem. Frequency spreading further reduces interference by spreading the energy across many frequencies, reducing the energy in any single frequency.

Features

- Four independent differential DSI (DBUS) channels
- Dual SPI interface
- Enhanced bus fault performance
- Automatic message cyclical redundancy checking (CRC) generation and checking for each channel
- Enhanced register set with addressable buffer allows queuing of 4 independent slave commands at one time for each channel
- 8- to 16-Bit messages with 0- to 8-Bit CRC
- Independent frequency spreading for each channel
- Pseudo bus switch feature on channel 0
- Pb-free packaging designated by suffix code EK

33781

DIFFERENTIAL DSI 2.02 MASTER



ORDERING INFORMATION		
Device	Temperature Range (T _A)	Package
MCZ33781EK/R2	-40°C to 90°C	32 SOICW EP

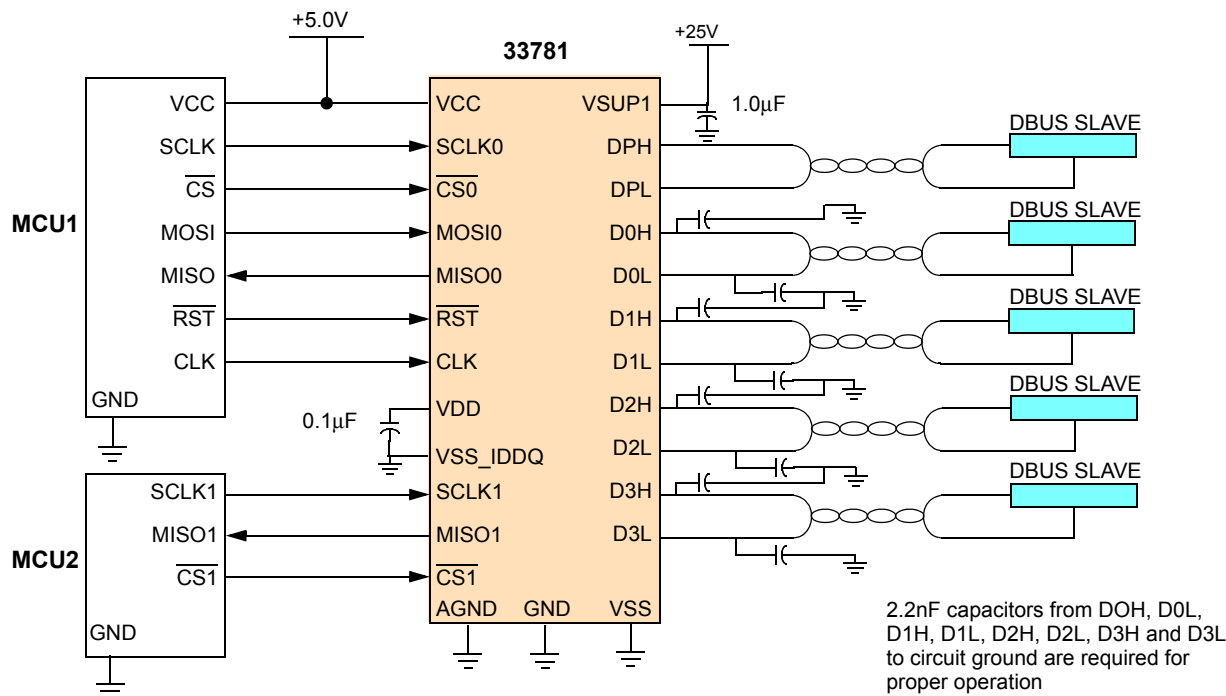


Figure 1. 33781 Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.
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INTERNAL BLOCK DIAGRAM

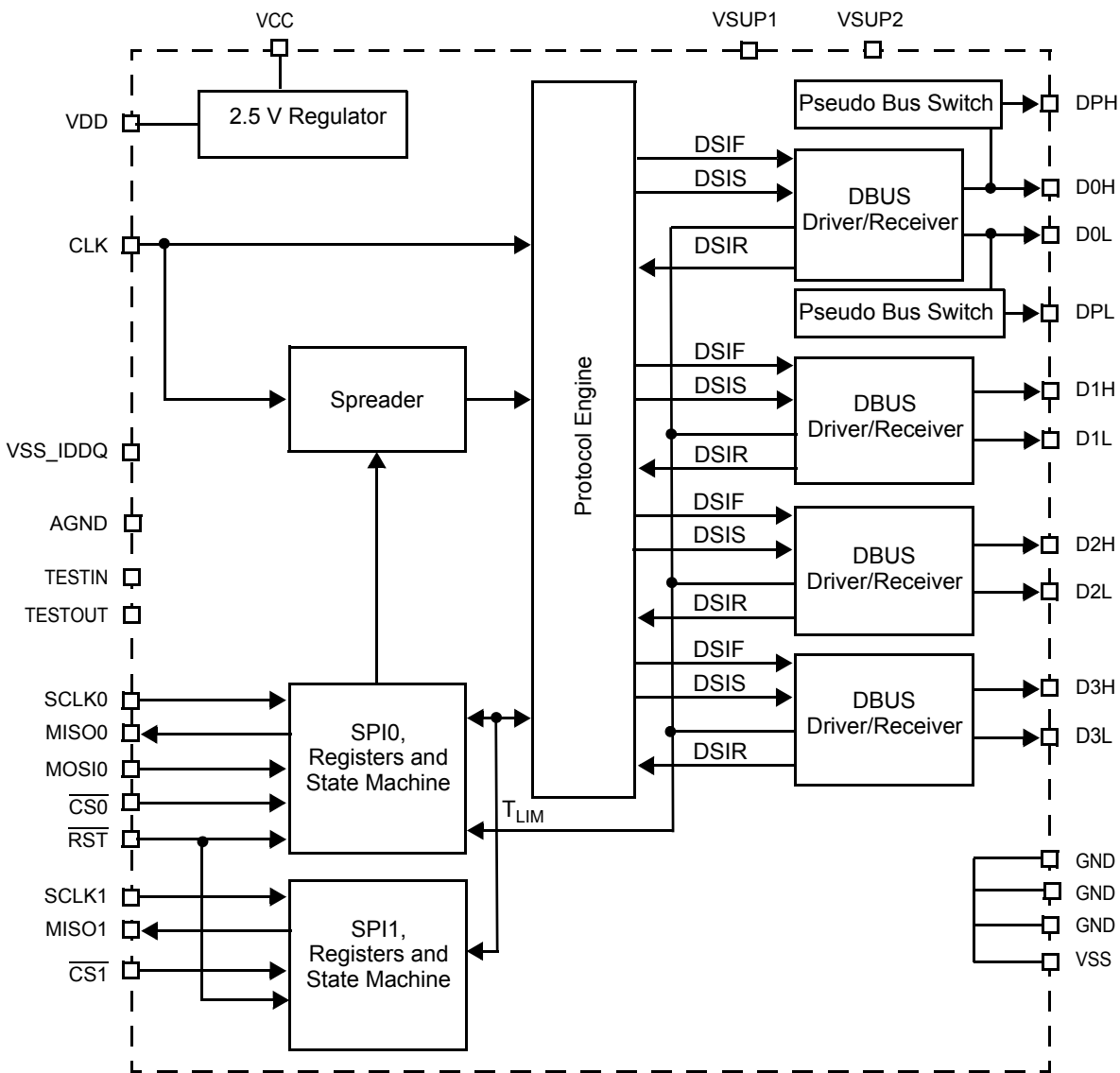


Figure 2. 33781 Internal Block Diagram

PIN CONNECTIONS

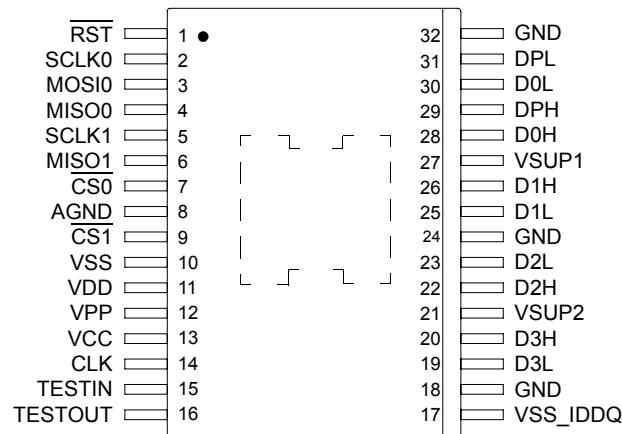


Figure 3. 33781 Pin Connections

Table 1. 33781 Pin Definitions

A functional description of each Pin can be found in the Functional Pin Descriptions section beginning on [page 15](#).

Pin	Pin Name	Pin Function	Formal Name	Definition
1	$\overline{\text{RST}}$	Reset	IC Reset	A low level on this pin returns all registers to a known state as indicated in the sections entitled SPI0 Register and Bit Descriptions and SPI1 Communications .
2	SCLK0	Input	SPI0 Serial Data Clock	Clocks data in from and out to SPI0. MISO0 data changes on the negative transition of SCLK0. MOSI0 is sampled on the positive edge of SCLK0.
3	MOSI0	Input	SPI0 Master Out Slave In	SPI data into SPI0. This data input is sampled on the positive edge of SCLK0
4	MISO0	Output	SPI0 Master In Slave Out	SPI0 data sent to the MCU by this device. This data output changes on the negative edge of SCLK0. When $\overline{\text{CS0}}$ is high, this Pin is high-impedance.
5	SCLK1	Input	SPI1 Serial Data Clock	Clocks data out from SPI1. MISO1 data changes on the negative transition of SCLK1.
6	MISO1	Output	SPI1 Master In Slave Out	SPI1 data sent to the MCU by this device. This data output changes on the negative edge of SCLK1. When $\overline{\text{CS1}}$ is high, this Pin is high-impedance.
7	$\overline{\text{CS0}}$	Input	SPI0 Chip Select	When this signal is high, SPI signals on SPI0 are ignored. Asserting this pin low starts an SPI0 transaction. The SPI0 transaction is signaled as completed when this signal returns high.
8	AGND	Ground	Analog Ground	Ground for the analog circuits. This pin is not connected internally to the other grounds on the chip. It should be connected to a quiet ground on the board.
9	$\overline{\text{CS1}}$	Input	SPI1 Chip Select	When this signal is high, SPI signals on SPI1 are ignored. Asserting this pin low starts an SPI1 transaction. The SPI1 transaction is signaled as completed when this signal returns high.
10	VSS	Ground	Digital Ground	Digital ground connected internally to the other on-chip grounds. This ground is connected to circuits that will consume current during IDDQ testing.
11	VDD	Power	Digital Voltage	Output of the Internal 2.5V regulator for the digital circuits. No external current draw is allowed from this pin.

Table 1. 33781 Pin Definitions

A functional description of each Pin can be found in the Functional Pin Descriptions section beginning on [page 15](#).

Pin	Pin Name	Pin Function	Formal Name	Definition
12	VPP	Input	Test Mode	A high-voltage on this pin puts the device in test mode for IC manufacturing test. It must be grounded in the application.
13	VCC	Input	Logic Supply	Regulated 5V input
14	CLK	Input	Clock Input	4.0MHz clock input
15	TESTIN	Test	Test Input	Input pin for device test. This pin must be tied to ground in the application.
16	TESTOUT	Test	Test Output	Output pin for device test. This pin is left floating in the application.
17	VSS_IDDQ	Ground	Digital Ground and IDDQ Test	Ground reference for the digital circuits that should not consume current during IDDQ testing. This ground is not connected to the other grounds internally.
18	GND	Ground	Power Ground	Bus power return
19	D3L	Output Driver	Low Side Bus 3	Bus 3 low side
20	D3H	Output Driver	High Side Bus 3	Bus 3 high side
21	VSUP2	Power	Positive Supply for Bus Outputs	This supply input is used to provide the positive level output of buses 2 and 3.
22	D2H	Output Driver	High Side Bus 2	Bus 2 high side
23	D2L	Output Driver	Low Side Bus 2	Bus 2 low side
24	GND	Ground	Power Ground	Bus power return
25	D1L	Output Driver	Low Side Bus 1	Bus 1 low side
26	D1H	Output Driver	High Side Bus 1	Bus 1 high side
27	VSUP1	Power	Positive Supply for Bus Outputs	This supply input is used to provide the positive level output of buses 0 and 1.
28	D0H	Output Driver	High Side Bus 0	Bus 0 high side
29	DPH	Output Driver	High Side Pseudo Bus	Pseudo Bus high side
30	D0L	Output Driver	Low Side Bus 0	Bus 0 low side
31	DPL	Output Driver	Low Side Pseudo Bus	Pseudo Bus low side
32	GND	Ground	Power Ground	Bus power return

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to GND unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltages			V
VSUPn	V_{SUP1} and V_{SUP2}	-0.3 to 26.5	
Load Dump VSUPn (300ms maximum - either pin)	V_{SUPLD}	40	
VCC	V_{CC}	-0.3 to 7.0	
VDD	V_{DD}	-0.3 to 3.1	
VPP	V_{PP}	-0.3 to 10.0	
Maximum Voltage on Logic Input/Output Pins	–	-0.3 to $V_{CC} + 0.3$	V
Maximum Voltage on DBUS Pins	V_{DBUS}	-0.3 to $V_{SUPn} + 0.3$	V
Maximum DBUS Pin Current	I_{DBUS}	400	mA
Maximum Logic Pin Current	I_{LOGIC}	20	mA
ESD Voltage ⁽¹⁾			V
Human Body Model (HBM)	V_{ESD}	±2000	
Machine Model (MM)		±200	
Charge Device Model (CDM)			
Corner pins		±750	
All other pins		±500	
THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Ambient Temperature	T_A	-40 to 90	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Thermal Shutdown (Bus Drivers and Pseudo Bus Switch)	T_{SD}	155 to 190	°C
Resistance, Junction-to-Ambient	$R_{\theta JA}$	71	°C/W
Resistance, Junction-to-Board	$R_{\theta JB}$	6	°C/W
Soldering Reflow Temperature	T_{SOLDER}	260	°C
Peak Package Reflow Temperature During Reflow ^{(2), (3)}	T_{PPRT}	Note 3	°C

Notes

- ESD1 testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP} = 100\text{pF}$, $R_{ZAP} = 1500\Omega$); ESD2 testing is performed in accordance with the Machine Model (MM) ($C_{ZAP} = 200\text{pF}$, $R_{ZAP} = 0\Omega$); and Charge Body Model (CBM).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $4.75V \leq V_{CC} \leq 5.25V$, $9.0V \leq V_{SUPn} \leq 25V$, $-40^{\circ}C \leq T_A \leq 90^{\circ}C$, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT REQUIREMENTS (VSUPn, VCC)					
I_{VSUPn} Supply Current (Test Mode, CLK = 4.0MHz) High Z	I_{VSUPn}	-	-	16	mA
Signal, Idle ($I_{bus} = 0$)					
Signal, Idle ($I_{bus} = 10mA$ on all channels, a total of 40mA)					
I_{VCC} Supply Current (CLK = 4.0MHz, RST = high) Signal, Idle ($I_{bus} = 0$)	I_{VCC}	-	-	10.0	mA
Signal, Idle ($I_{bus} = 10mA$ on all channels, a total of 40mA)					
V_{SUPn} Low Detect Threshold $V_{CC} > 4.75V$	$V_{VSUPnLO}$	9.1	-	9.9	V
V_{SUPn} Low Mask Time $V_{CC} > 4.75V$	t_{MASK}	20	-	25	μs

MICROCONTROLLER INTERFACE (\overline{RST} , \overline{CSn} , MOSI0, MISO_n, SCLK_n, and CLK)

I/O Logic Levels (RST, CS _n , MOSI0, SCLK _n , and CLK) Input High Voltage	V_{IH}	2.0	-	$V_{CC} + 0.3$	V
Input Low Voltage					
Input Hysteresis ⁽⁴⁾					
Input Capacitance ⁽⁴⁾ CS _n , MOSI0, and SCLK _n	C_I	-	-	10	pF
RST and CLK					
Output Low Voltage MISO _n Pin = 0.3mA	V_{OL}	0	-	0.8	V
Output High Voltage MISO _n Pin = -0.3mA	V_{OH}	$V_{CC} - 0.8$	-	V_{CC}	V
Output Leakage Current MISO _n Pin = 0V	I_{MISO}	-10	-	10	μA
MISO _n Pin = V_{CC}		-10	-	10	
SCLK _n , CS _n Pull-up Current $V_{OUT} = V_{CC} - 2.0 V$	I_{PU}	-50	-30	-10	μA
\overline{RST} Pull-down Current $V_{OUT} = 1.0V$	$I_{\overline{RST}PD}$	5.0	-	13	μA
CLK, MOSI0 Pull-down Current $V_{OUT} = 1.0V$	I_{PD}	5.0	10	13	μA

Notes

4. Not measured in production.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions $4.75V \leq V_{CC} \leq 5.25V$, $9.0V \leq V_{SUPn} \leq 25V$, $-40^{\circ}C \leq T_A \leq 90^{\circ}C$, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER (DnH, DnL)					
Output Bus Idle Voltage (Drop) $I_{nH} = -200mA$, $I_{nL} = 200mA$ ⁽⁶⁾	$V_{DnD(Drop)}$ ⁽⁷⁾⁽⁸⁾	–	–	1.6	V
Output Signal High Voltage (Differential) $-12.5mA \leq I_{nH} \leq 1.0mA$, $-1.0mA \leq I_{nL} \leq 12.5mA$ ⁽⁶⁾	$V_{DnD(HIGH)}$ ⁽⁷⁾	4.175	4.5	4.825	V
Output Signal Low Voltage (Differential) $-12.5mA \leq I_{nH} \leq 1.0mA$, $-1.0mA \leq I_{nL} \leq 12.5mA$ ⁽⁶⁾	$V_{DnD(LOW)}$ ⁽⁷⁾	1.175	1.5	1.825	V
Vmid, (DnH + DnL)/2 (Voltage Halfway Between Bus High Side and Bus Low Side)	V_{MID} ⁽⁸⁾	$V_{SUPn}/2 - 0.8$	$V_{SUPn}/2$	$V_{SUPn}/2 + 0.8$	V
VCM Peak to Peak (Maximum Vmid-Minimum Vmid) For Vmid (Idle), Vmid (Signal_H), Vmid (Signal_L) ⁽⁵⁾	V_{CMP}	0	–	30	mV
Bus Driver Vmid Peak to Peak, (DnH+DnL)/2 ⁽⁵⁾ For Signal to Idle, Idle, Idle to Signal, $V_{midPP(Idle)} = V_{mid(Max)} - V_{mid(Min)}$	$V_{MIDPP(IDLE)}$	–	–	300	mV
Bus Driver Vmid Peak to Peak (DnH+DnL)/2 ⁽⁵⁾ For Signal_H to Signal_L, Signal_L, Signal_L to Signal_H, Signal_H $V_{midPP(Signal)} = V_{mid(Max)} - V_{mid(Min)}$	$V_{MIDPP(SIGNAL)}$	–	–	80	mV
Output High Side (DnH) Driver Current Limit Fault Condition: DnH = 0V Normal Operation Fault Condition: DnH = V_{SUPn}	$I_{CL(HIGH)}$	-600 -400 150	– – –	-200 -200 350	mA
Output Low Side (DnL) Driver Current Limit Fault Condition: DnL = 0V Fault Condition: DnL = V_{SUPn}	$I_{CL(LOW)}$	-350 200	– –	-150 400	mA
Signal mode Over-current Shutdown I _{ISSD} DnH, DnL	I_{SSD}	20		60	mA
Disabled High Side (DnH) Bus Leakage (DnL open) DnH = 0V DnH = V_{SUPn}	$I_{LK(HIGH)}$	-1.0 -1.0	– –	1.0 1.0	mA
Disabled Low Side (DnL) Bus Leakage (DnH open) ⁽⁹⁾ DnL = 0V DnL = V_{SUPn}	$I_{LK(LOW)}$	-1.0 -1.0	– –	1.0 1.0	mA

Notes

- Not measured in production.
- I_{nH} =bus current at DnH, I_{nL} =bus current at DnL
- $V_{DnD} = V_{DnH} - V_{DnL}$
- $\text{Max } V_{DnD} = V_{SUPn} - 2 * V_{MID_OFFSET} - V_{DnD(Drop)}$, $V_{MID_OFFSET} = |V_{MID} - V_{SUPn} / 2|$
- Worst Case Disabled Low Side Bus Leakage for DnL occurs with DnL = V_{SUP} and DnH = 0V. In this configuration, the DnL leakage current can exceed 1mA. This is not measured in production.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions $4.75V \leq V_{CC} \leq 5.25V$, $9.0V \leq V_{SUPn} \leq 25V$, $-40^{\circ}C \leq T_A \leq 90^{\circ}C$, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER (DnH, DnL) (CONTINUED)					
High Side Pseudo Bus Switch Resistance $I_{SWH}=160mA$	R_{SWH}	–	8.0	16.0	Ω
Low Side Pseudo Bus Switch Resistance $I_{SWL}=160mA$	R_{SWL}	–	8.0	16.0	Ω
Pseudo Bus Switch Matching	$R_{PSMATCH}$	–	–	1.0	Ω
High Side Pseudo Bus Switch Leakage Current DPH = Open: CH0 drivers in Idle, DPH = 0V or CH0 drivers in Signal_H, DPH = 25V	I_{DPHLK}	-20	–	20	μA
Low Side Pseudo Bus Switch Leakage Current DPL = Open: CH0 drivers in Idle, DPL = 25V, or CH0 drivers in Signal_H, DPL = 0V	I_{DPLLK}	-20	–	20	μA
BUS RECEIVER (DnH, DnL)					
Comparator Trip Point for High Side	$COMP_{HIGH}$	5.0	6.0	7.0	mA
Comparator Trip Point for Low Side	$COMP_{LOW}$	5.0	6.0	7.0	mA
Comparator Trip Point for Adder	$COMP_{ADD}$	6.0	12	18	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $4.75V \leq V_{CC} \leq 5.25V$, $9.0V \leq V_{SUPn} \leq 25V$, $-40^{\circ}C \leq T_A \leq 90^{\circ}C$, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CLOCK					
CLK Periods (System requirement) ⁽¹⁰⁾					ns
Time High	t_{CLKHI}	75	–	–	
Time Low	t_{CLKLO}	75	–	–	
Period	t_{CLKPER}	245	250	255	
CLK Transition (System requirement) ⁽¹⁰⁾					ns
Time for Low-to-High Transition of the CLK Input Signal	t_{CLKLH}	–	–	100	
Time for High-to-Low Transition of the CLK Input Signal	t_{CLKHL}	–	–	100	
Reset Low Time	t_{RSTLO}	100	–	–	ns
SPI INTERFACE TIMING					
SPI Clock Cycle Time	t_{CYC}	100	–	–	ns
SPI Clock High Time	t_{HI}	40	–	–	ns
SPI Clock Low Time	t_{LO}	40	–	–	ns
SPI \overline{CSn} Lead Time ⁽¹¹⁾	t_{LEAD}	50	–	–	ns
SPI \overline{CSn} Lag Time ⁽¹¹⁾	t_{LAG}	50	–	–	ns
SPI $\overline{CS0}$ Time Between Bursts ⁽¹⁰⁾	$t_{\overline{CS0}HI}$	80	–	–	ns
SPI $\overline{CS1}$ Time Between Bursts ⁽¹⁰⁾	$t_{\overline{CS1}HI}$	300	–	–	ns
Data Setup Time	t_{SU}				ns
MOSI0 Valid Before SCLK0 Rising Edge ⁽¹¹⁾		10	–	–	
Data Hold Time					ns
MOSI0 Valid After SCLK0 Rising Edge ^{(11),(10)}	t_H	10	–	–	
Data Valid Time	t_V				ns
SCLKn Falling Edge to MISO _n Valid, C = 50pF ⁽¹²⁾		–	–	25	
Output Disable Time	t_{DIS}				ns
\overline{CSn} Rise to MISO _n Hi-Z		–	–	50	
Rise Time (30% V_{CC} to 70% V_{CC}) ⁽¹⁰⁾	t_R				ns
SCLKn, MOSI0		–	–	10	
Fall Time (70% V_{CC} to 30% V_{CC}) ⁽¹⁰⁾	t_F				ns
SCLKn, MOSI0		–	–	10	

Notes

10. Not measured in production.
11. SPI signal timing from the production test equipment is programmed to ensure compliance.
12. Conditions are verified indirectly during test.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $4.75V \leq V_{CC} \leq 5.25V$, $9.0V \leq V_{SUPn} \leq 25V$, $-40^{\circ}C \leq T_A \leq 90^{\circ}C$, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER					
Idle-to-Signal and Signal-to-Idle Slew Rate ⁽¹³⁾	$t_{SLEW(IDLE)}$	3.0	6.0	8.0	V/ μ s
Signal High-to-Low and Signal Low-to-High Slew Rate ^{(13),(14)} (See Data Valid DSIS to DnD Timing)	$t_{SLEW(SIGNAL)}$	3.0	6.0	8.0	V/ μ s
Communication Data Rate Capability ⁽¹⁴⁾ (Ensured by Transmitter Data Valid and Receiver Delay Measurements) Data Rate(before frequency spreading)	D_{RATE}	77.1	–	200	kbps
Signal Bit Time ($1 / D_{RATE}$) ⁽¹⁴⁾ The Max value depends on the settings in the FSEL bits	t_{BIT}	5.0	–	–	μ s
DBUS Start Delay, $\overline{CS0}$ Rising Edge to DBUS ⁽¹⁴⁾ note: DLY is the inter-message delay selected in the DnCTRL register	$t_{DBUSSTART2}$	$2/3t_{BIT} + (DLY-2) * t_{BIT}$	–	$5/3t_{BIT} + (DLY-2) * t_{BIT}$	μ s
Data Valid ⁽¹³⁾ DSIF = $0.5 * V_{CC}$ to DnD Fall = 5.5 V ($9V \leq V_{SUPn} \leq 40V$) DSIS = $0.5 * V_{CC}$ to DnD Fall = 2.8V ($9V \leq V_{SUPn} \leq 40V$) DSIS = $0.5 * V_{CC}$ to DnD Rise = 3.2V ($9V \leq V_{SUPn} \leq 40V$) DSIF = $0.5 * V_{CC}$ to DnD Rise = 6.5 V ($9V \leq V_{SUPn} \leq 40V$)	t_{DVLD1} t_{DVLD2} t_{DVLD3} t_{DVLD4}	– – – –	– – – –	5.3 1.0 1.0 1.0	μ s
Signal mode Over-current Shutdown Delay ⁽¹⁴⁾	t_{OC}	3.0	5.0	7.0	μ s
Signal Low Time for Logic Zero 33.3% Duty Cycle ($2/3 * t_{BIT}$) \pm 10% for threshold delta	t_{0LO}	$0.6 * t_{BIT}$	$2/3 * t_{BIT}$	$0.73 * t_{BIT}$	μ s
Signal Low Time for Logic One 66.7% Duty Cycle ($1/3 * t_{BIT}$) \pm 10% for threshold delta	t_{1LO}	$0.3 * t_{BIT}$	$1/3 * t_{BIT}$	$0.37 * t_{BIT}$	μ s

Notes

- 13. C = 2.8nF from DnH to DnL and 2.2nF from DnH and DnL to GND, capacitor tolerance = $\pm 10\%$.
- 14. Not measured in production.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $4.75V \leq V_{CC} \leq 5.25V$, $9.0V \leq V_{SUPn} \leq 25V$, $-40^{\circ}C \leq T_A \leq 90^{\circ}C$, unless otherwise noted. Voltages relative to GND, unless otherwise noted. Typical values noted reflect the approximate mean values of the parameter at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS RECEIVER					
Receiver Delay Time ($I_{RSP} = 0mA / 11mA$ step) ⁽¹⁵⁾					ns
$I_{RSP} = -6.0mA$ to DSIR = $0.5 * V_{CC}$	t_{DRH}	–	–	500	
$I_{RSP} = -6.0mA$ to DSIR = $0.5 * V_{CC}$	t_{DRL}	–	–	500	
Common Mode Current Noise Rejection (2.5ms max.)	I_{CMNR}	-50	–	+50	mA
SPREAD SPECTRUM					
Base Frequency Range	f_{CEN}	77.1 - 2%	–	200 + 2%	kHz
PSEUDO BUS					
Pseudo Bus On Delay Time	t_{PBD1}	–	5	10	μs
Pseudo Bus Off Delay Time	t_{PBD2}	–	5	10	μs

Notes

15. Not measured in production.

TIMING DIAGRAMS

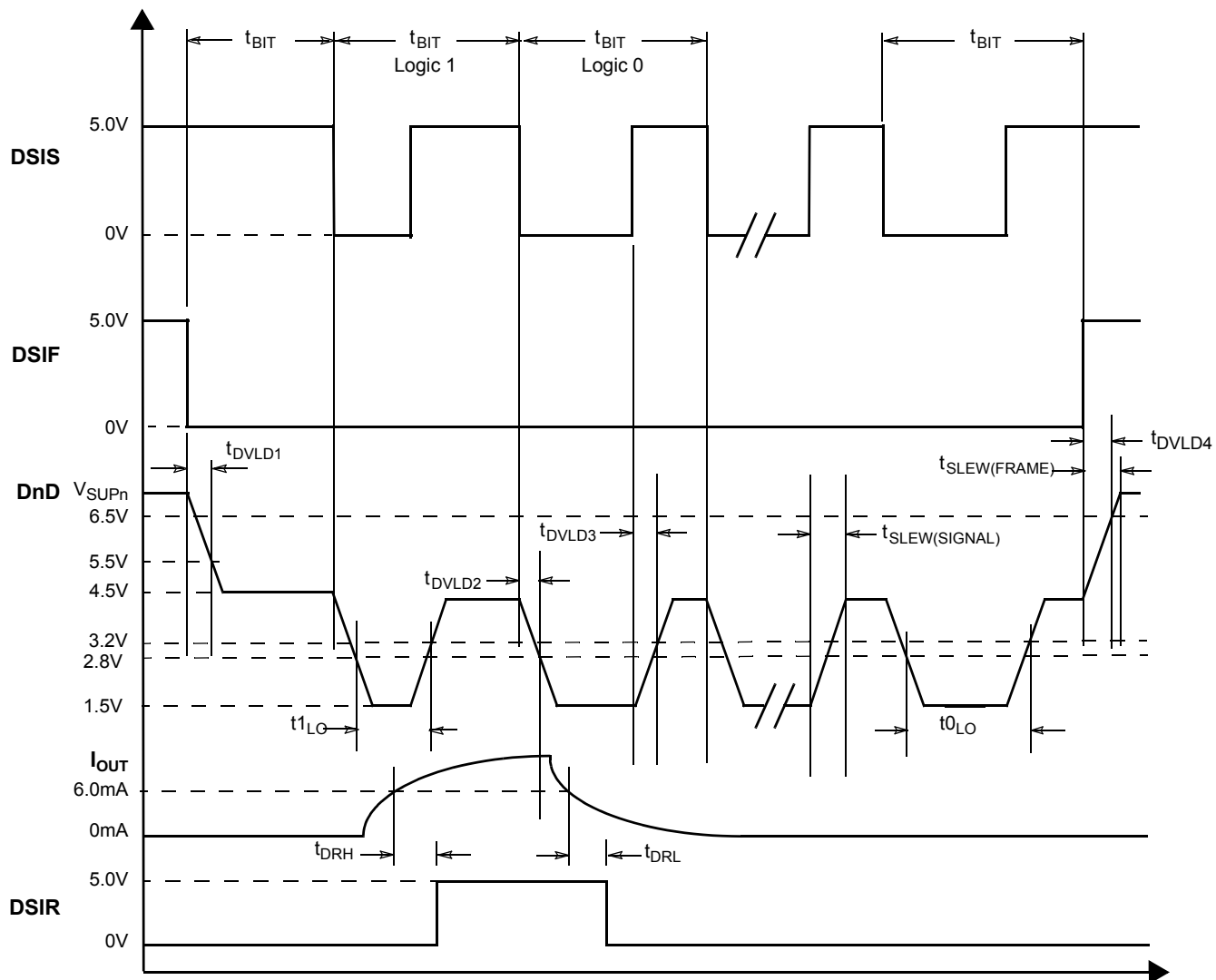


Figure 4. DBUS Timing Characteristics

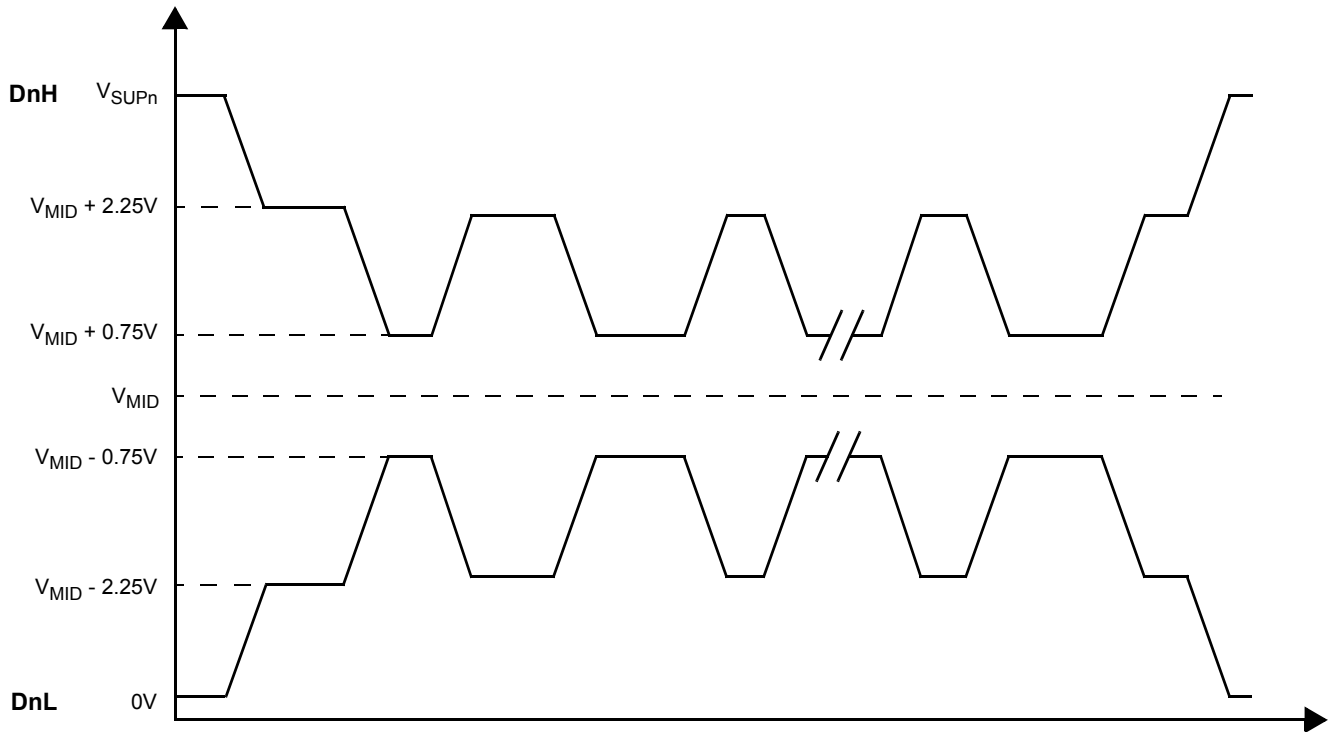


Figure 5. DBUS Normal Bus Waveforms

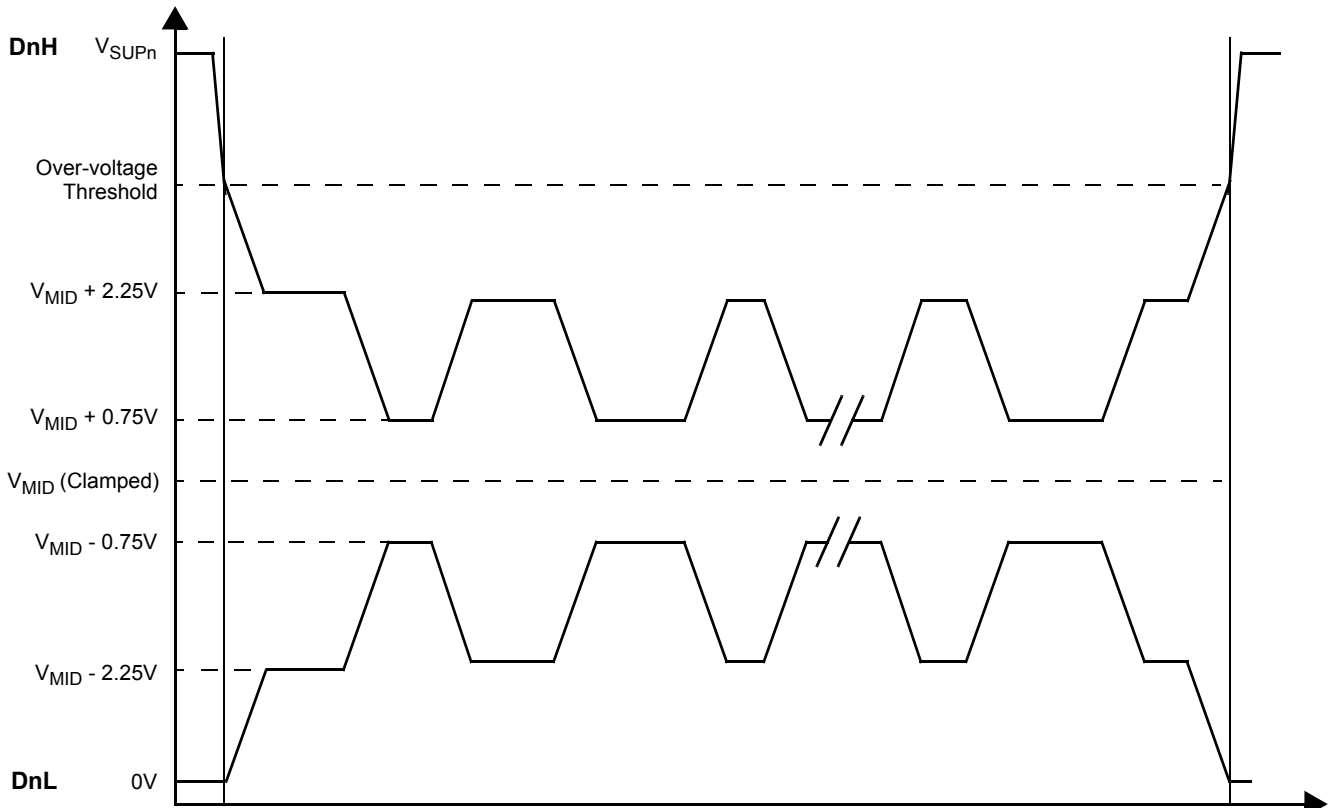


Figure 6. DBUS Over-voltage Bus Waveforms

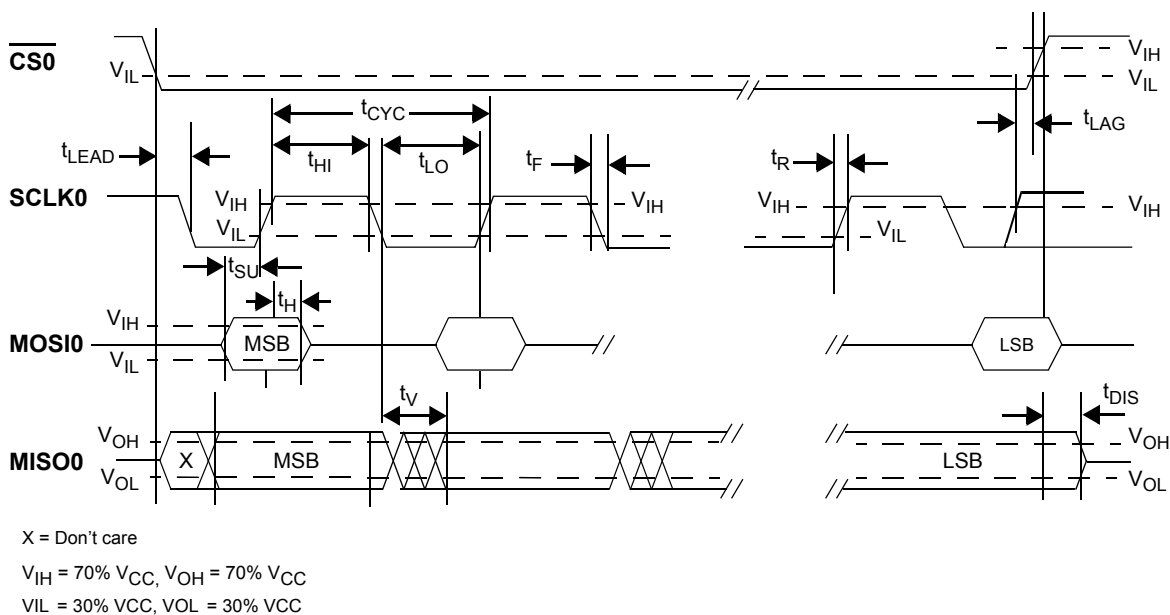


Figure 7. SPI0 Interface Timing

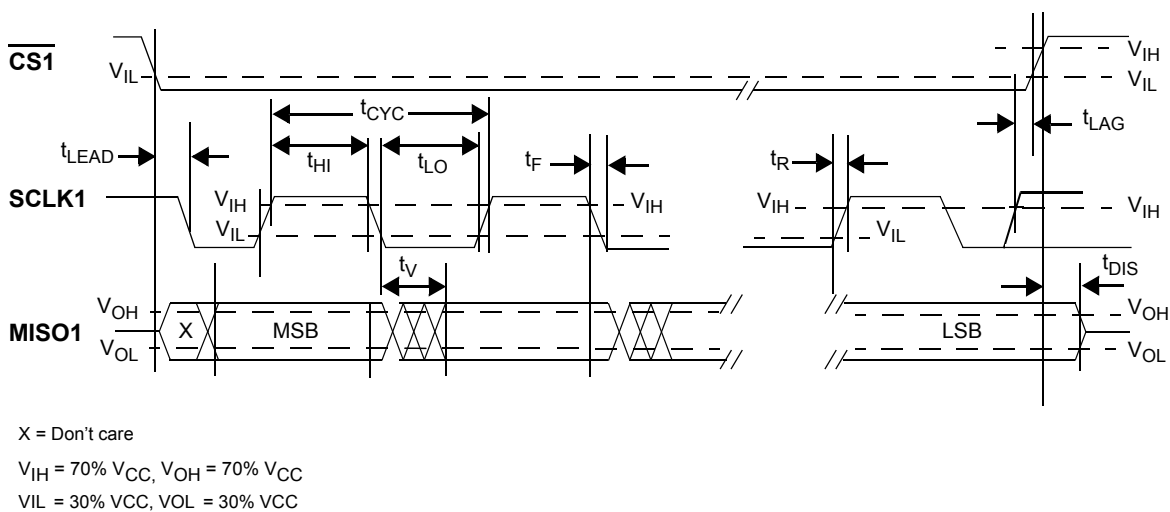


Figure 8. SPI1 Interface Timing

FUNCTIONAL DESCRIPTIONS

INTRODUCTION

The 33781 is intended to be used as a master device in a distributed system. It contains both protocol generators and physical interfaces, to allow an MCU to communicate with devices on the bus using two different SPI interfaces. Four differential buses are provided. The physical layer uses a two-wire bus to carry power and signal. The physical layer uses wave-shaped voltage signals for commands from the master and wave-shaped current signals for responses from the slaves. The protocol and physical layer conform to the DSI 2.02 specification.

The equivalent bus capacitance consists of capacitors connected between the two bus wires and capacitors between the bus wires and ground. Because the voltage change on either of the bus wires to ground is only 1/2 the

amount of change between the two bus wires, the capacitance to ground only conducts half as much current as it would if connected directly across the bus. The equivalent bus capacitance of a capacitor to ground from the bus wires is one half of the actual amount of the capacitor. The amount of capacitance from either bus wire to ground should be kept the same in order to achieve the lowest radiated EMI energy. The 2.2nF capacitors required between the bus wires and ground result in an equivalent of 1.1nF of capacitance across the bus as seen by either bus wire.

[Table 5](#) shows the voltages used for operation. Low side (LS) is the bus wire that is the most negative and high side (HS) is the bus wire that is the most positive. [Figure 5](#) shows the bus waveforms in normal operation.

Table 5. High Side and Low Side Typical Voltages (Voltage Relative to Ground)

Low Side			High Side		
IDLE	HIGH	LOW	IDLE	HIGH	LOW
0	Vmid-2.25 ⁽¹⁶⁾	Vmid-0.75 ⁽¹⁶⁾	V _{SUPn}	Vmid+2.25 ⁽¹⁶⁾	Vmid+0.75 ⁽¹⁶⁾

Notes

16. $V_{MID} = V_{SUPn}/2$.

FUNCTIONAL PIN DESCRIPTIONS

RESET (\overline{RST})

When pulled low, this will reset all internal registers to a known state as indicated in the section entitled [SPI0 Register and Bit Descriptions on page 29](#).

CHIP SELECT n (\overline{CSn})

This input is used to select the SPIn port when pulled to ground. When high, the associated SPIn port signals are ignored. The SPIn transaction is signaled as completed when this signal returns high.

MASTER OUT/SLAVE IN 0 (MOSI0)

This is the SPI data input to the device. This data is sampled on the positive (rising) edge of SCLK0. There is no MOSI pin or function for SPI1.

SERIAL CLOCK (SCLKn)

This is the clock signal from the SPIn master device. It controls the clocking of data to SPIn and data reads from the SPIn.

MASTER IN/SLAVE OUT (MISON)

This is the SPIn data from SPIn to the SPIn master. Data changes on the negative (falling) transition of the associated SCLKn.

CLOCK (CLK)

This is the main clock source for the internal logic. It must be 4.0MHz.

GROUND (GND)

Ground source for DSI/DBUS return.

DIGITAL GROUND (VSS)

Ground source for logic.

DIGITAL GROUND AND IDDQ (VSS_IDDQ)

Used for IDDQ testing during IC manufacturing test.

ANALOG GROUND (AGND)

Ground source for analog circuits.

POWER SOURCE (VCC)

Nominal +5.0V Regulated Input.

DIGITAL REGULATOR OUTPUT (VDD)

Nominal +2.5V internal regulator Pin. This must be bypassed with a small capacitor to ground (100nF)

LOW SIDE BUS (DnL)

There are four independent low side outputs, D0L, D1L, D2L and D3L. They comprise the low side differential output signal of the DBUS physical layer as shown in [Figure 5](#). They also provide power to the slave modules during the DBUS idle time. The output of DnL should have a bypass capacitor of 2.2nF to ground.

HIGH SIDE BUS (DnH)

There are four independent high side outputs, D0H, D1H, D2H, and D3H. They comprise the high side differential output signal of the DBUS physical layer. They also provide power to the slave modules during the DBUS idle time. See [Figure 5](#). The output of DnH should have a bypass capacitor of 2.2nF to ground.

POSITIVE SUPPLY FOR BUS OUTPUT (VSUPn)

This 9.0V to 25V power supply is used to provide power to the slave devices attached to the DBUS. During the bus idle time, the storage capacitors in the slave modules are charged

up to maintain a regulated supply to the slave device. V_{SUP1} powers devices DBUS0 and DBUS1, and V_{SUP2} powers devices on DBUS2 and DBUS3. See [Figure 9](#).

The two supplies are interdependent internally, however, as can be seen in [Figure 9](#): V_{SUP1} is used to create the V_{CM_REF} voltage for all four driver buffers, and V_{SUP2} is used to supply the charge pump voltage. Consequently, both V_{SUP1} and V_{SUP2} are required for internal functions: for example, the internal voltage regulator V_{REG_8V} is supplied from V_{SUP1} , but uses the V_{SUP2} -derived charge pump voltage to supply the output NMOS devices.

PSEUDO BUS (DPH AND DPL)

These bus high and bus low pins are created by closing the pseudo bus switches attached to the D0H and D0L bus lines internal to the 33781. This allows a second external set of bus lines to communicate over the D0 Channel. The pseudo bus switches are controlled by the system MCU through SPI0.

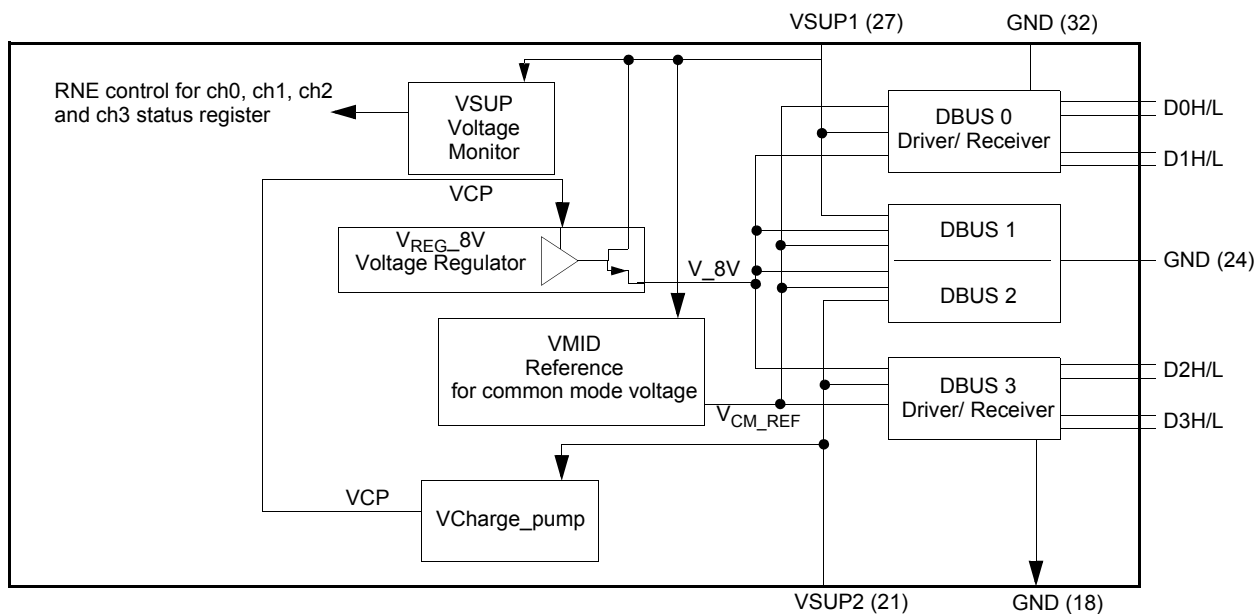


Figure 9. VSUP Block Diagram

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

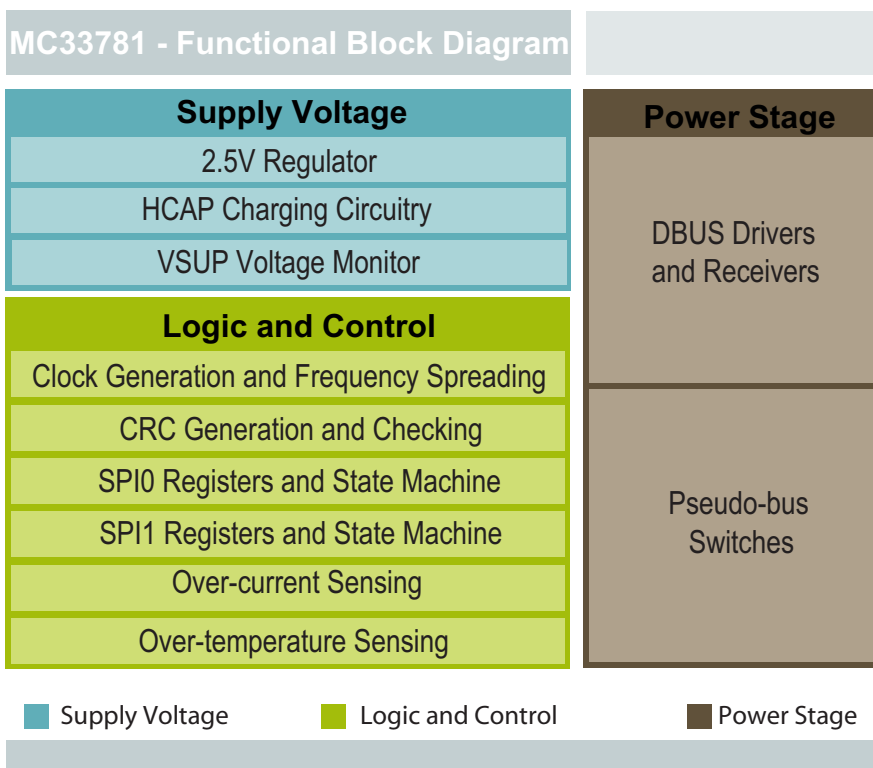


Figure 10. Block Illustration

The 33781 is controlled by an MCU through the SPI0 interface. It handles the digital and physical layer portions of a DBUS master node. Four separate DBUS channels are included. The physical layer uses a two-wire bus with analog wave-shaped voltage and current signals. Refer to [Figure 1](#).

Major subsystems include the following:

- SPI0 interface and registers to a main MCU
- SPI1 interface and registers to a second MCU
- Four channels of DSI 2.02 protocol state logic
- CRC block for each channel
- Control and status registers
- Four addressable register sets per channel for queuing up to four commands and data per bus. The addressable buffer acts as a circular buffer for command writes and data reads.
- Pseudo Bus Switch from D0H/L to DPH/L

SPI0 AND REGISTERS

This block contains the SPI0 interface logic and the control and response registers that are written to and read from the SPI interface.

The IC is an SPI slave-type device, so MOSI0 (Master-Out-Slave-In) is an input and MISO0 (Master-In-Slave-Out) is an output. $\overline{CS0}$ and SCLK0 are also inputs.

The SPI0 port can handle 2-byte and 4-byte transfers. It addresses 87 registers. The organization of the registers is described in the section entitled [SPI0 Register and Bit Descriptions on page 29](#).

SPI1 AND REGISTERS

The 33781 has a second SPI port (called SPI1) that allows valid response data from Bus Channel 2 and 3, along with the slave address, to be read independently by a second MCU. This block contains the SPI1 interface logic and the response registers that are read from the SPI1 interface.

The IC is an SPI slave-type device, so MISO1 (Master-In-Slave-Out) is an output, and $\overline{CS1}$ and SCLK1 are inputs. SPI1 does not use the MOSI (Master-Out-Slave-In) pin or function as it does not receive commands.

The SPI1 port handles only 16-bit transfers. It addresses eight registers which are read only.

PROTOCOL ENGINE

This block converts the data to be transmitted from the registers into the DBUS sequences, and converts DBUS response sequences to data in the registers.

The DBUS transmit protocol uses a *return to 1* type data with a duty cycle determined by the logic state. The protocol includes Cyclical Redundancy Check (CRC) generation and validation.

VSUP_n VOLTAGE MONITOR

This function monitors the voltage on the V_{SUPn} pin. If the voltage on the pin drops below the defined voltage threshold for longer than the voltage threshold mask time, the 33781 will continue to send queued DBUS commands, but not set any RNE bits in the DnSTAT registers to 1, until either the

device is reset by the $\overline{\text{RST}}$ pin or the EN bits in the DnEN registers are first set to zero, and then to one (disabled and then enabled). By monitoring the RNE bits the MCU will know that communications have been disrupted and can take the appropriate action.

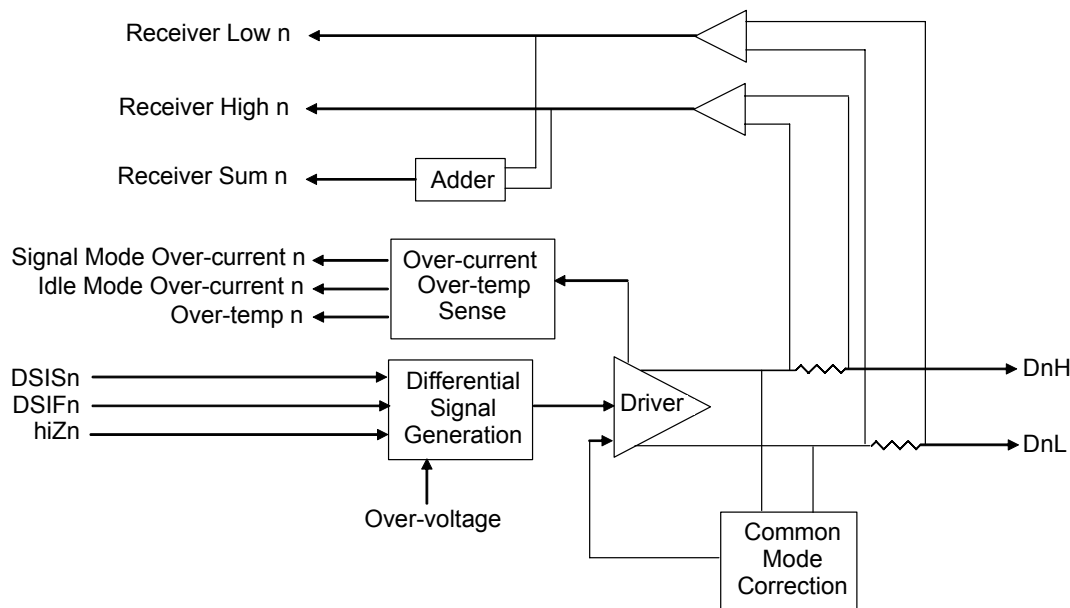


Figure 11. Driver/Receiver Block Diagram

DBUS DRIVER /RECEIVER (PHYSICAL LAYER)

There are four independent differential bus driver/receiver blocks on the 33781. These blocks translate the transmit data to the voltage and current needed to drive the DBUS. They also detect the response current from the slave devices and translate that current into digital levels. These circuits can drive their outputs to the levels listed in [Table 5](#).

The DBUS driver/receiver block diagram is shown in [Figure 11](#). The circuit uses a common driver for both the Idle and Signal modes to minimize common mode noise. The drivers are disabled in HiZ.

During Idle mode the driver is required to supply a high current to recharge the Slave device storage capacitors. In both Idle and Signal modes it is required to drive the DBUS load capacitances and control the slew rate over a wide supply voltage range and load conditions. Current limit, over-current shutdown and thermal shutdown are included to protect the device from fault conditions. More information can be found in the Protection and Diagnostic Features and SPI0 Register and Bit Descriptions sections.

To ensure stability of the bus drivers, capacitors must be connected between each output and ground. These are the DBUS common mode capacitors. In addition, a bypass capacitor is required at V_{SUPn}. These capacitors must be located close to the IC Pins and provide a low-impedance path to ground.

The internal signal DSIF controls the Idle to Signalling state change, and internal signal DSIS controls the signal level, high or low. DSIR is the slave device response signal to the logic. This is shown in [Table 6](#).

Table 6. Internal Signal Truth Table

DSIF	DSIS	T _S	DSIR	DnD
0	0	0	Return Data	Signal Low
0	1	0	Return Data	Signal High
1	0	0	0	High-impedance
1	1	0	0	Idle
X	X	1	0	High-impedance

Bus wire faults on a bus do not disrupt communications on another bus. In addition, each bus channel has independent thermal shutdown protection. Once the channel thermal limit is reached the bus drivers become high-impedance, the TS bit is set to a 1 and the EN bit set to 0 in the channel DEN register. In addition the channel address buffer registers and pointers are reset. There is a 4 usec filter on Tlim to prevent false triggering.

The *Differential Signal Generation* block converts the DSIS signal to the DBUS differential signal voltage levels. This differential signal is buffered and slew rate controlled by

the driver. The over-voltage input causes the driver characteristics to be modified under over-voltage conditions. This is described in more detail in the [Load Dump Operation](#) section.

A special requirement of the differential bus is to maintain a low common mode voltage. This is accomplished by monitoring the common mode voltage and modifying the driver slew rates. This is the function of the *Common Mode Correction* block.

Current signals sent by the slave are detected on both the high side and the low side of the bus using a differential current sense architecture. Sense resistors between the Signal driver and the DnH and DnL outputs detect the slave device response current. Sensing the current on both bus lines improves the fault diagnostics of the bus. Also included is an adder circuit which is used to improve the reception of sensor data in the presence of common mode noise. The comparators in the blocks output a high or low value depending on if the input is above or below the signal threshold.

The Receiver High, Receiver Low, and Receiver Sum outputs are sent to the device logic block which is shown in [Figure 23](#). The data is sampled at the falling edge of DSIS. In the presence of faults or common mode noise it is possible that all three receiver circuits will not produce the same bit pattern. To check for this, each of the three receiver filter

outputs is passed to a CRC generation and checking block. A logic block determines which (if any) of the receiver filter blocks has produced the correct result, by comparing the CRC results along with the bit-by-bit XOR of the high side and low side bit pattern. [Table 7](#) shows how the logic determines which (if any) receiver outputs contain a valid response. The data is selected from either the Receiver High, Receiver Low or Receiver Sum circuit and the ER bit is set accordingly in the DnRnSTAT register.

If either Receiver High or Receiver Low has all 1's for data, including the CRC bits, then the ER bit will be set. For either of these two conditions, the ER bit will be set regardless of the Receiver Sum data value and regardless of whether or not all the 1's caused a CRC error on the High or Low side.

Note that SPI0 and SPI1 do not use the same sources for their respective output data streams. SPI0 chooses between Receiver High or Receiver Sum0; SPI1 chooses between Receiver Low and Receiver Sum1.

In order to provide the maximum protection against a single-point failure causing a disruption in communication, the decision paths for the two SPI channels are internally independent. For example, Receiver Sum0 and Receiver Sum1 use different holding registers in the Receiver logic. These registers are duplicates, although they will always hold the same data unless there is a fault in one of the data paths.

Table 7. Receiver Decision Logic

Bus Pin Conditions	Receiver High 6 ± 1 mA	Receiver Low 6 ± 1 mA	Receiver Sum 12 ± 6 mA	High and Low XOR (bit/bit)	High and Sum XOR (bit/bit)	Low and Sum XOR (bit/bit)	ER Bit	SPI0 DnRnxData	SPI1 DnRnxData
Normal	CRC Ok	CRC Ok	CRC Ok	H*L Ok	N/A	N/A	0	Receiver High	Receiver Low
				H*L Not OK			1	Receiver High	Receiver Low
Out of Spec	CRC Ok	CRC Ok	Bad CRC	H*L Ok	N/A	N/A	0	Receiver High	Receiver Low
				H*L Not OK			1	Receiver High	Receiver Low
Fault	CRC Ok	Bad CRC	CRC Ok	N/A	H*S Ok	N/A	0	Receiver High	Receiver Sum1
					H*S Not OK		1	Receiver High	Receiver Low
Fault L	CRC Ok	Bad CRC	Bad CRC	N/A	N/A	N/A	1	Receiver High	Receiver Low
Fault	Bad CRC	CRC OK	CRC OK	N/A	N/A	L*S Ok	0	Receiver Sum0	Receiver Low
						L*S Not OK	1	Receiver High	Receiver Low
Fault H	Bad CRC	CRC Ok	Bad CRC	N/A	N/A	N/A	1	Receiver High	Receiver Low
Common Mode Noise	Bad CRC	Bad CRC	CRC Ok	N/A	N/A	N/A	0	Receiver Sum0	Receiver Sum1
Fault	Bad CRC	Bad CRC	Bad CRC	N/A	N/A	N/A	1	Receiver High	Receiver Low

PSEUDO BUS SWITCHES

Pseudo Bus Switches are provided on the Channel 0 bus. They allow one channel to communicate via two external bus wire sets (D0H/D0L and DPH/DPL). There is a pseudo bus switch on both the bus high and bus low driver. Upon device reset the bus switches are open. This allows the master to initialize devices on D0H/D0L. After all of these slaves are initialized, the pseudo bus switches can be closed, allowing the devices on DPH/DPL to be initialized.

The Pseudo Bus Switches can only be commanded closed by the BSWH and BSWL bits in the D0EN register. These bits can also open the switch at any time.

The Pseudo Bus Switches have independent thermal shutdown protection. Once the thermal shutdown point is reached, the bus switch is opened (becoming high-impedance) and the BSWH and/or BSWL bit is cleared in the channel 0 DEN register. If this occurs, the Pseudo Bus Switches can only be closed again by setting the BSWH and/or BSWL bit to a 1 with a write command to the channel 0 DEN register.

SPREAD SPECTRUM

The dominant source of radiated electromagnetic interference (EMI) from the DBUS bus is due to the regular periodic frequency of the data bits. At a steady bit rate, the time period for each bit is the same, which results in a steady fundamental frequency plus harmonics. This results in undesired signals appearing at multiples of the frequency that can be strong enough to interfere with a desired signal.

A significant decrease in radiated EMI can be achieved by randomly changing the duration of each bit. This can significantly reduce the amplitude by having the signal spend a much smaller percentage of time at any specific frequency. The signal strength of the fundamental and harmonics are reduced directly by the percentage of time it spends on a specific frequency.

A circuit to do this is included in this IC, and can perform the *spreading* of the signal independently for each channel, while generating the bit clock timing for the channel. This is done in the Spread Spectrum (SS) Block Diagram shown in [Figure 12](#).

To implement the channel bit clock a common 64MHz clock is created from the on board 4MHz oscillator using a digital PLL. Multiples of this clock period (15.625 nsec) are used to select the minimum channel bit time. The Spread

Spectrum block does this by multiplying the 8-bit value in the DxFSSEL register by 2 and then adding it to the number 320 (decimal). The user must choose a minimum bit time appropriate for his system. Factors which must be considered are the slave response time, bus wire delays, and the minimum idle time needed to recharge the slave H_CAPs for the channel.

To spread the spectrum beyond this minimum bit time a random delay based on a multiple of 1/64 MHz periods can be added to each bit. This delay is created by a Pseudo Random Bit Sequence Generator from which a 7-bit random number is created. This number is further qualified by the maximum number of counts (chosen by the DEV[2:0] bits in

the DxSSCTL registers) allowed beyond the base time period. The resulting value is added to the minimum bit time and fed to the bit clock logic, which generates the DSI bit clock.

It is important for the user to select a maximum deviation value that is appropriate for the system. A larger maximum deviation results in spreading the bit energy to more frequencies. However, this number also establishes the maximum period for any random bit on that channel. If the system requires that a minimum number of bits be transferred within a fixed time period, then the user must select a minimum base bit time and maximum deviation time that will meet the criteria.

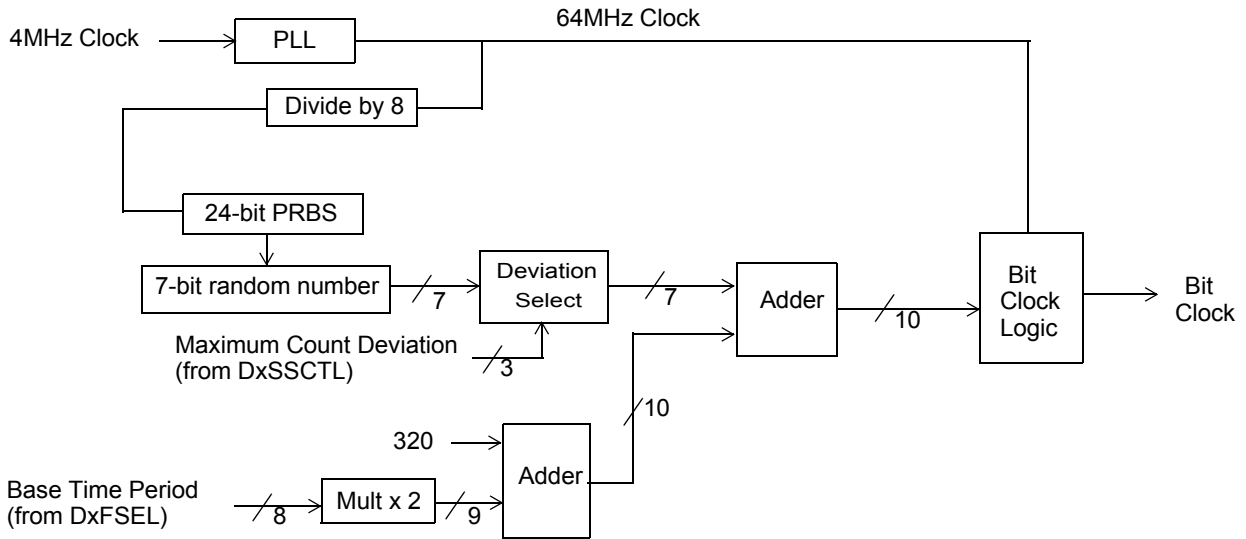


Figure 12. Spread Spectrum Block Diagram

FUNCTIONAL DEVICE OPERATION

LOGIC COMMANDS AND REGISTERS

SPI0 COMMUNICATIONS

All SPI0 transactions are either 16 or 32-bits long. They start with a command byte and can be followed by 1 or 3 bytes of data. The start of an SPI transaction is signaled by CS0 being asserted low. The first bit sent (bit 7) of the first byte signals a read or write (write = 1) of data. The last seven bits (bits 6–0) of the command set a pointer to the desired register. The 33781 uses 16-bit commands to access control registers, and 32-bit commands to access both control registers, and to queue up transfers over the DBUS.

[Figure 13](#) is a diagram of 16-bit transfers and [Figure 14](#) is a diagram of 32-bit transfers. In these multi-byte transfers, as long as CS0 is asserted low, each additional byte sent over the SPI will be a read/write of data to the sequential next register.

33781 utilizes, transmit, and receive addressable FIFOs for sending commands and responses over the DBUS. There are separate command and response registers, and a transmit queue is used to allow up to 4 bus commands to be scheduled for each bus. The transmit queue schedules

commands as a circular buffer, accessing the appropriate command register for the command and data to be sent as the bus becomes available. Data received in response to the commands is queued up for sequential response back to the MCU during the next set of SPI commands. If an SPI0 attempts to write to a transmit register that is not empty the new command will be ignored.

[Figure 14](#) shows an example of a write operation. During the first byte of the SPI transaction, the first MOSI bit is 1 (write), and the last seven are the address of the register to be accessed. During this command byte, MISO returns dummy bits set to all zeros. During the next SPI transactions, MOSI updates the data in the register pointed to in the previous byte with new data, while reading back the old data via MISO.

During an SPI0 transaction the 33781 checks for SPI framing errors. A framing error is defined as any number of clocks received that is not either 16 or 32. If that occurs, all bits sent by the SPI master are discarded and no registers are update.

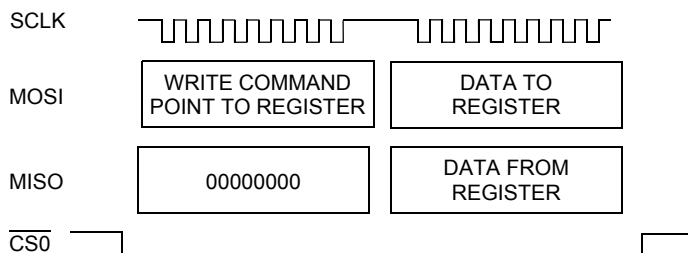


Figure 13. SPI0 16-Bit Burst Transfer Example.

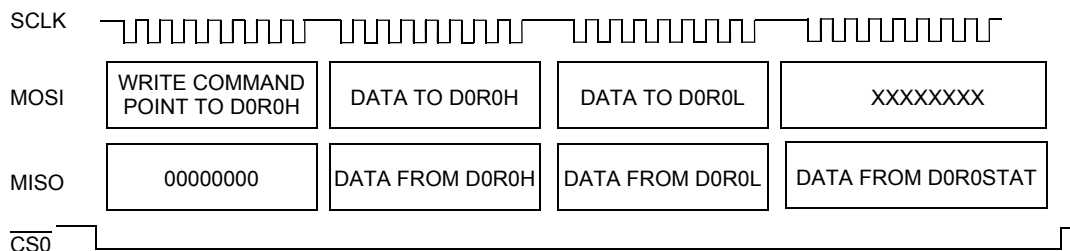


Figure 14. SPI0 32-Bit Burst Transfer Example

The bit definitions for SPI0 depend on the type of SPI transfer, and if the transfer will be to/from the addressable FIFOs, whether the DBUS for that channel is set for Long Words or Enhanced Short words.

[Figure 13](#) shows the bit encoding for 16-bit SPI0 burst transfers. In this transfer the first byte contains the address of the control register to be written to or read from, and the second byte is the data to be written. The SPI0 response is the data from that register, latched at the falling edge of CS0. If the address pointed to by the first byte is not a control

register, the transfer is considered to have a framing error and no write will occur.

[Figure 16](#) shows the bit encoding for 32-bit SPI0 burst transfers when the DBUS channel is set for long words. In this transfer, the first byte contains the address of the control register to be written to and read from, the second byte is the data to/from that register, and the next two bytes are the data to/from the next numerically successive registers. In the case of reading or writing from the addressable FIFO registers, the 1st data byte would be the DnRnH byte, the next byte would be the DnRnL byte, and the third byte would be the DnRnSTAT byte as shown in [Figure 15](#). Notice that in this case, the 4th Tx byte is don't care and is not written. If this transfer would be sent to an address in the control register section of the register bank, the bytes sent and returned would be first the addressed register, and then the next consecutive registers.

[Figure 17](#) shows the bit encoding for 32-bit SPI0 burst transfers when the DBUS channel is set for enhanced short words. This transfer mode is only valid when accessing the

addressable FIFO portion of the register set. In this case, the first byte is again the 1st address of the register to be accessed in this read/write, the second byte contains the upper two bits of the data to be written, and the third byte is the lower 8-bits of data to be written. The SPI0 response encoding begins with the 2nd byte in the transfer with the 4-bit DBUS address of the slave, which sent the data contained in the rest of the word. This is followed by the 10-bits of data from the DBUS slave, and then the value in the DnRnSTAT register.

Although it looks like the read and write for an address are occurring at the same time, the changes caused earlier during the same burst would not be reflected by the data returned, because the DnRnSTAT register is latched at CS0 going low.

Refer to the section [SPI0 Register and Bit Descriptions on page 29](#) for the bit descriptions in [Figure 15](#), [Figure 16](#), and [Figure 17](#).

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First TX Byte	R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Second TX Byte	D7	D6	D5	D4	D3	D2	D1	D0
	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First RX Byte	0	0	0	0	0	0	0	0
Second RX Byte	D7	D6	D5	D4	D3	D2	D1	D0

Figure 15. SPI0 Communications, 16-Bit Burst Transfer Bit Definitions

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First TX Byte	R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Second TX Byte	D15	D14	D13	D12	D11	D10	D9	D8
Third TX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth TX Byte	X	X	X	X	X	X	X	X
	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First RX Byte	0	0	0	0	0	0	0	0
Second RX Byte	D15	D14	D13	D12	D11	D10	D9	D8
Third RX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth RX Byte	ER	TE	SDS	RNE	ICL	0	FIX1	FIX0

Figure 16. SPI0 Communications, 32-Bit Burst Transfer Long Word DBUS Transfer Bit Definitions

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First TX Byte	R/W	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Second TX Byte	X	X	X	X	X	X	D9	D8
Third TX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth TX Byte	X	X	X	X	X	X	X	X

	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First RX Byte	0	0	0	0	0	0	0	0
Second RX Byte	SA3	SA2	SA1	SA0	0	0	D9	D8
Third RX Byte	D7	D6	D5	D4	D3	D2	D1	D0
Fourth RX Byte	ER	TE	SDS	RNE	ICL	0	FIX0	FIX1

Figure 17. SPI0 Communications, 32-Bit Burst Transfer Enhanced Short Word DBUS Bit Definitions

SPI1 COMMUNICATIONS

All SPI1 transactions are read only, are 16-bits in length, and are asynchronous to SPI0. There is no MOSI pin or function associated with SPI1, since there are no commands sent. [Figure 18](#) shows the signals associated with an SPI1 transfer, and [Figure 19](#) contains the order of bits sent for each SPI1 transaction.

SPI1 transfers start with the 1st SCLK1 transition after CS1 asserts and ends once CS1 negates. The start of an SPI transaction is signaled by CS1 being asserted low. If the SPI1 logic sees more than 16 SCLK1 pulses while CS1 is asserted, zeros are returned for all additional bits (bits beyond bit 15). If a SPI1 transaction contains less than 16-bits (too few SCLK cycles), the data that was in process of being sent during the transaction is discarded and not saved for retry.

There are eight registers which can be read by SPI1 in a cyclic fashion. Four of these registers are associated with bus channel 2, and four are associated with bus channel 3. Data is deposited into these registers under the following conditions:

When the bus channel 2 is set for enhanced 10-bit short words, the SPI1 state machine monitors outgoing bus addresses and commands on the channel. If the command sent is \$2 (Request AN0), the address portion of the command is saved. The response received on the next command is stored into one of the four 16-bit register pointed to by the channel 2 cyclic buffer write pointer, along with the address that generated that response (saved from the previous transaction) with the bits “01”, completing the 16 bit

write. These last two bits indicate that the transaction occurred on channel 2. The data bits will only be written if the status bits for that bus transaction all indicate no errors. If a status error is indicated, the address and channel indicator bits are stored as described, but the data bits are all set to zeros. If there was a bus driver shutdown during the transaction, no buffer write will occur. Further transactions are written to the next cyclic buffer register in the same way, overwriting data if necessary.

This same sequence occurs for channel three transactions, except that the channel indicator bits are “10”, and writes occur to a separate set of four 16-bit cyclic registers.

If the channel has been put into loop mode, the same sequence is used except the buffer write occurs only if the data is all ones or all zeros, and the saved address from the previous transaction is the complement of the data. The channel indicator bits are written the same as if the channel were in normal mode. The buffer pointer always advances, even if the buffer is not written, so that it is synchronous with the SPI0 RX buffer pointer.

The channel buffers are not cleared, in the case of a channel abort.

Reads from this register by the SPI1 master are also accomplished in a cyclic buffer way, except the two channels are concatenated, with channel 3 following channel 2 in the cyclic sequence. During these buffer reads, if a buffer position does not contain data, it is skipped. After each buffer location is read it is cleared by the SPI1 logic.

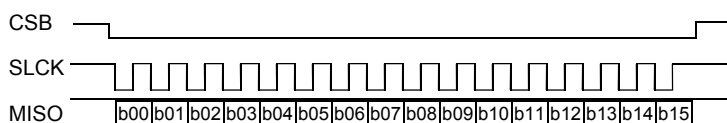


Figure 18. SPI1 16-Bit Burst Transfer Example

SPI Data Bit	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
Read Only	DO0	DO1	DO2	DO3	DO4	DO5	DO6	DO7	DO8	DO9	A0	A1	A2	A3	C0	C1

Figure 19. SPI1 Bit Encoding

DO[0:9]- Data Bits

The received data bits from the bus channel transaction. If the transaction had any CRC or SDS errors (See page 32 and page 33), then these bits are set to all zeros.

A[0:3] - Sensor Address Bits

The address of the slave that sent the data. This is a copy of the address sent out during the previous bus transaction.

C[0:1] - Channel indicator Bits

The bits indicate which bus channel the data came from. "01" indicates channel 2, and "10" indicates channel 3.

DBUS COMMUNICATIONS

The DBUS messages contain data from the DnH and DnL registers. A CRC pattern is automatically appended to each message. The data and CRC lengths are programmed by the DnLENGTH register. Figure 20 shows the structure of the DBUS message.

Bit n	Bit 0	CRC n	CRC 0
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Figure 20. DBUS Communications Message

DBUS Driver/Receiver communications involve a frame (DSIF), a data signal (DSIS), and a data return (DSIR) signal. These are signals internal to the IC associated with the protocol engine.

A message starts with a falling edge on the DSIF signal, which marks the start of a frame. There is a one bit-time delay before the MSB of data appears on DSIS. Data bits start with a falling edge on DSIS. The low time is 1/3 of the bit time for a 1, and 2/3 of a bit time for a 0. Data is transmitted on DSIS and received on DSIR simultaneously. Receive data is the captured level on DSIR at the end of each bit time. As a message is received, it is stored bit-by-bit into the appropriate receive register. For each data value received, there is a one-bit status flag (ER) to indicate whether or not there was a CRC error while receiving the data. At the end of the bit time for the last CRC bit, DSIF returns to a logic high (Idle level). A minimum delay is imposed between successive frames as determined by the DnCTRL register.

Users initiate a message by writing (via the SPI0 interface from the MCU) to the high and low byte of the data registers (DnRnH/L). Transactions are scheduled once the CS0 for that transfer rises. When 9- to 16-bit messages are to be sent, the user writes to the DnH register first, and then the DnL register, before the combined 9 to 16-bit data value DnH:DnL is sent on the DBUS. The user should first check the TE status flag to be sure the command register is not full before writing a new data value to DnH and/or DnL. When the minimum inter-frame delay has been satisfied, and CS0 has risen, and if no SPI0 framing error has occurred, DSIF will go low, indicating the start of a new transfer frame.

At the end of a DBUS transfer (and after the CRC error status is stable), the RNE flag is set to indicate there is data in the register available to be read.

DATA RATE

The base data rate is determined by the system clock (CLK) and the values in the DnFSEL register. The CLK is assumed to be 4MHz. The CLK is converted to a 64MHz internal clock with a digital PLL, which is used to form the bit rate clock. The minimum bit clock period which may be programmed is:

$$(1/16 * f_{CLK}) \times 320 = 5 \text{ usec}$$

However, this period may not meet overall system requirements for minimum bit time. Longer base clock periods can be selected by using the DxFSSEL register. There are 8 bits in the DxFSSEL register representing values from 0 to 255. The complete equation for determining the base clock period is:

$$((1/16 * f_{CLK}) \times (320 + 2x)) \text{ where } x = 0 \text{ to } 255$$

Table 8 gives some examples of the base data rate for $f_{CLK} = 4.0\text{MHz}$.

Table 8. Examples of Base Data Rate

FSEL	Base Bit Period (usec)	Base Bit Frequency (kbps)
00000000	5.000	200.0
00000001	5.031	198.8
00001101	5.406	184.9
00101000	6.250	160.0
11111110	12.938	77.3
11111111	12.969	77.1