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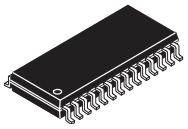
System basis chip (SBC) with low speed fault tolerant CAN interface

33889

SYSTEM BASIS CHIP



EG SUFFIX (PB-FREE)
PLASTIC PACKAGE
98ASB42345B
28-PIN SOICW

The 33889 is an SBC having a fully protected, fixed 5.0 V low drop-out regulator, with current limit, overtemperature prewarning and reset. An SBC device is a monolithic IC combining many functions repeatedly found in standard microcontroller-based systems, e.g., protection, diagnostics, communication, power, etc.

An output drive with sense input is also provided to implement a second 5.0 V regulator using an external PNP. The 33889 has Normal, Standby, Stop and Sleep modes; an internally switched high-side power supply output with two wake-up inputs; programmable timeout or window watchdog, Interrupt, Reset, serial peripheral interface (SPI) input control, and a low-speed fault tolerant CAN transceiver, compatible with CAN 2.0 A and B protocols for module-to-module communications. The combination is an economical solution for power management, high-speed communication, and control in MCU-based systems. This device is powered by SMARTMOS technology.

Features

- VDD1: 5.0 V low drop voltage regulator, current limitation, overtemperature detection, monitoring and reset function with total current capability 200 mA
- V2: tracking function of VDD1 regulator; control circuitry for external bipolar ballast transistor for high flexibility in choice of peripheral voltage and current supply
- Four operational modes
- Low standby current consumption in Stop and Sleep modes
- Built-in low speed 125 kbps fault tolerant CAN physical interface.
- External high voltage wake-up input, associated with HS1 V_{BAT} switch
- 150 mA output current capability for HS1 V_{BAT} switch allowing drive of external switches pull-up resistors or relays

ORDERING INFORMATION		
Device (Add R2 Suffix for Tape and Reel)	**Temperature Range (T_A)**	**Package**
MC33889BPEG	-40 to 125 °C	28 SOICW
*MC33889DPEG		

*Recommended for new designs

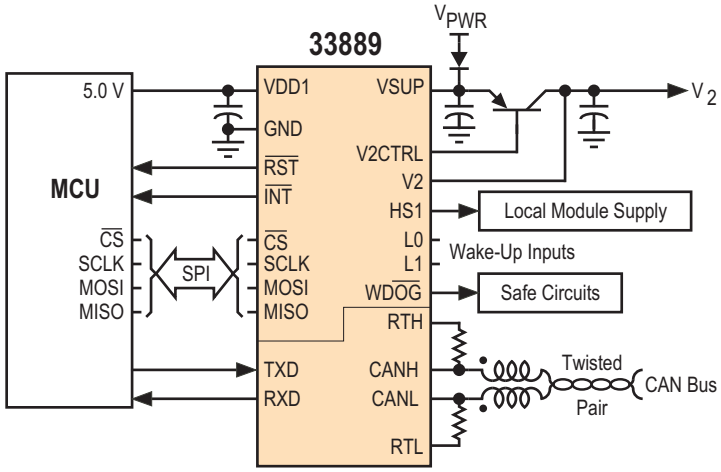


Figure 1. 33889 simplified application diagram

1 Device variations

Table 1. Device variations between the 33889D and 33889B versions [(1)]

Parameters	Symbol	Trait	Device part number	
			MC33889B[(2)]	MC33889D[(2)]
Differential Receiver, Recessive To Dominant Threshold (By Definition, $V_{DIFF} = V_{CANH}-V_{CANL}$)	V_{DIFF1}	Min.	3.2 V	3.5 V
		Typ	2.6 V	3.0 V
		Max.	2.1 V	2.5 V
Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5)	V_{DIFF2}	Min.	3.2 V	3.5 V
		Typ	2.6 V	3.0 V
		Max.	2.1 V	2.5 V
CANH Output Current (V_{CANH} = 0; TX = 0.0)	I_{CANH}	Min.	50 mA	50 mA
		Typ	75 mA	100 mA
		Max.	110 mA	130 mA
CANL Output Current (V_{CANL} = 14 V; TX = 0.0)	I_{CANL}	Min.	50 mA	50 mA
		Typ	90 mA	140 mA
		Max.	135 mA	170 mA
Detection threshold for Short circuit to Battery voltage	Vcanh	Max.	Vsup/2 + 5V	Vsup/2 + 4.55V
loop time Tx to Rx, no bus failure, ISO configuration	tLOOPRD	Max.	N/A	1.5us
loop time Tx to Rx, with bus failure, ISO configuration	tLOOPRD-F	Max.	N/A	1.9us
loop time Tx to Rx, with bus failure and +-1.5V gnd shift, 5 node network, ISO configuration	tLOOPRD/DR-F+GS		N/A	3.6us
Minimum Dominant time for Wake up on CANL or CANH (Tem Vbat mode)	tWAKE	Min.	N/A	8
		typ	30	16
		Max.	N/A	30
T2SPI timing	T2spi	Min.	not specified, 25us spec applied	25us
Device behavior				
CANH or CANL open wire recovery principle	Reference MC33889B on page 32		after 4 non consecutive pulses	after 4 consecutive pulses
Rx behavior in TermVbat mode	Reference MC333889D on page 32		Rx recessive, no pulse	Rx recessive, dominant pulse to signal bus traffic

Notes

1. This datasheet uses the term 33889 in the inclusive sense, referring to both the D version (33889D) and the B version (33689B).
2. The 33889D and 33889B versions are nearly identical. However, where variations in characteristic occur, these items will be separated onto individual lines.

2 Internal block diagram

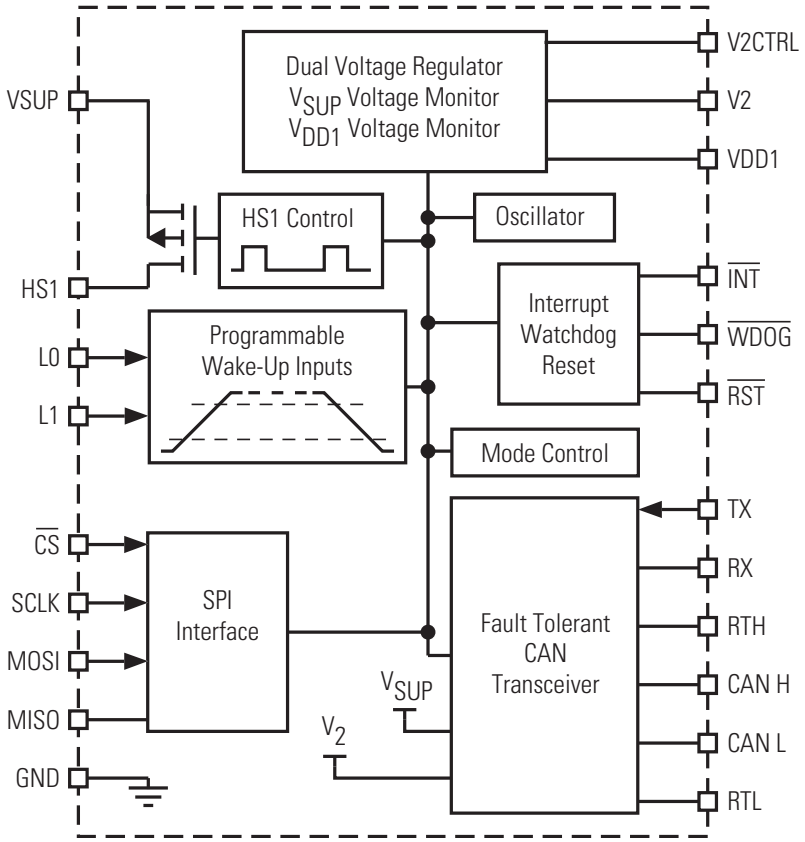


Figure 2. 33889 internal block diagram

3 Pin connections

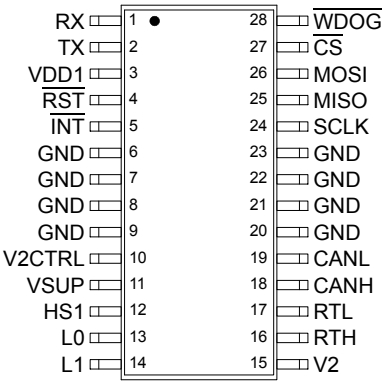


Figure 3. 33889 pin connections

A functional description of each pin can be found in the Functional pin description section page 20.

Table 2. Pin definitions

Pin	Pin name	Pin function	Formal Name	Definition
1	RX	Output	Receiver Data	CAN bus receive data output pin
2	TX	Input	Transmitter Data	CAN bus receive data input pin
3	VDD1	Power Output	Voltage Regulator One	5.0 V pin is a 2% low drop voltage regulator for to the microcontroller supply.
4	$\overline{\text{RST}}$	Output	Reset	This is the device reset output pin whose main function is to reset the MCU.
5	$\overline{\text{INT}}$	Output	Interrupt	This output is asserted LOW when an enabled interrupt condition occurs.
6 -9, 20 - 23	GND	Ground	Ground	These device ground pins are internally connected to the package lead frame to provide a 33889-to-PCB thermal path.
10	V2CTRL	Output	Voltage Source 2 Control	Output drive source for the V2 regulator connected to the external series pass transistor.
11	VSUP	Power Input	Voltage Supply	Supply input pin.
12	HS1	Output	High-Side Output	Output of the internal high-side switch.
13 - 14	L0, L1	Input	Level 0 - 1 Inputs	Inputs from external switches or from logic circuitry.
15	V2	Input	Voltage Regulator Two	5.0 V pin is a low drop voltage regulator dedicated to the peripherals supply.
16	RTH	Output	RTH	Pin for connection of the bus termination resistor to CANH.
17	RTL	Output	RTL	Pin for connection of the bus termination resistor to CANL.
18	CANH	Output	CAN High	CAN high output pin.
19	CANL	Output	CAN Low	CAN low output pin.
24	SCLK	Input	System Clock	Clock input pin for the Serial Peripheral Interface (SPI).
25	MISO	Output	Master In/Slave Out	SPI data sent to the MCU by the 33889. When CS_{LOW} is HIGH, the pin is in the high impedance state.
26	MOSI	Input	Master Out/Slave In	SPI data received by the 33889.
27	$\overline{\text{CS}}$	Input	Chip Select	The CS_{LOW} input pin is used with the SPI bus to select the 33889. When the CS_{LOW} is asserted LOW, the 33889 is the selected device of the SPI bus.
28	WDOG	Output	Watchdog	The WDOG output pin is asserted LOW if the software watchdog is not correctly triggered.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Max.	Unit	Notes
Electrical ratings				
V_{SUP}	Supply Voltage at VSUP Continuous voltage Transient voltage (Load dump)	 -0.3 to 27 40	 V	
V_{LOG}	Logic Signals (RX, TX, MOSI, MISO, $\overline{CS}$, SCLK, $\overline{RST}$, $\overline{WDOG}$, $\overline{INT}$)	-0.3 to V_{DD1} +0.3	V	
I	Output current VDD1	Internally Limited	mA	
V I	HS1 Voltage Output Current	 -0.2 to V_{SUP} +0.3 Internally Limited	 V A	
V_{WU} I_{WU} V_{TRWU}	L0, L1 DC Input voltage DC Input current Transient input voltage (according to ISO7637 specification) and with external component per Figure 4.	 -0.3 to 40 -2.0 to 2.0 +-100	 V mA V	
V_{2INT}	DC voltage at V2 (V2INT)	0 to 5.25	V	
V_{BUS}	DC Voltage On Pins CANH, CANL	-20 to +27	V	
V_{CANH}/V_{CANL}	Transient Voltage At Pins CANH, CANL 0.0 < V2-INT < 5.5 V; VSUP = 0.0; T < 500 ms	-40 to +40	V	
V_{TR}	Transient Voltage On Pins CANH, CANL (Coupled Through 1.0 nF Capacitor)	-150 to +100	V	
V_{RTL}, V_{RTH}	DC Voltage On Pins RTH, RTL	-0.3 to +27	V	
V_{RTH}/V_{RTL}	Transient Voltage At Pins RTH, RTL 0.0 < V2-INT < 5.5 V; VSUP = 0.0; T < 500 ms	-0.3 to +40	V	
V_{ESDH}	ESD voltage (HBM 100 pF, 1.5 k) CANL, CANH, HS1, L0, L1 RTH, RTL All other pins	 ±4.0 ±3.0 ±2.0	kV	(3)
V_{ESD-MM}	ESD voltage (Machine Model) All pins, MC33889B	±200	V	(3) (4)
$V_{ESD-CDM}$	ESD voltage (CDM) All pins, MC33889D Pins 1,14,15, & 28 All other pins	 750 500	V	(4)
R_T	RTH, RTL Termination Resistance	500 to 16000	Ω	

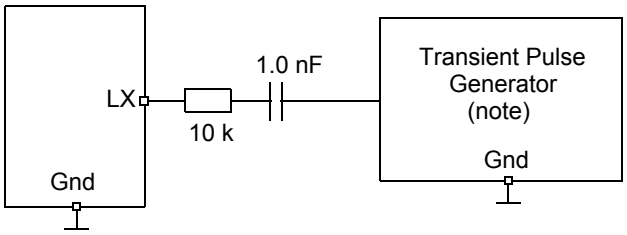
Table 3. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Max.	Unit	Notes
Thermal ratings				
T_J	Junction Temperature	-40 to 150	°C	
T_S	Storage Temperature	-55 to 165	°C	
T_A	Ambient Temperature (for info only)	-40 to 125	°C	
$R_{THJ/P}$	Thermal resistance junction to gnd pin (5)	20	°C/W	

Notes:

3. Testing done in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD machine model (MM) is for MC33889B only. MM is now replaced by CDM (Charged Discharged model).
5. Gnd pins 6,7,8,9,20, 21, 22, 23.



Note: Waveform in accordance to ISO7637 part1, test pulses 1, 2, 3a and 3b.

Figure 4. Transient test pulse for L0 and L1 inputs

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions - V_{SUP} From 5.5 V to 18 V and T_J from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Input pin (VSUP)						
V_{SUP}	Nominal DC Voltage range	5.5	-	18	V	
$V_{SUP-EX1}$	Extended DC Voltage range 1 Reduced functionality	4.5	-	5.5	V	(6)
$V_{SUP-EX2}$	Extended DC Voltage range 2	18	-	27	V	(8)
V_{SUPLD}	Input Voltage during Load Dump Load dump situation	-	-	40	V	
V_{SUPJS}	Input Voltage during jump start Jump start situation	-	-	27	V	
I_{SUP} (SLEEP1)	Supply Current in Sleep Mode V_{DD1} & V2 off, $V_{SUP} \leq 12$ V, oscillator running	-	95	130	µA	(7) (10)
I_{SUP} (SLEEP2)	Supply Current in Sleep Mode V_{DD1} & V2 off, $V_{SUP} \leq 12$ V, oscillator not running	-	55	90	µA	(7)
I_{SUP} (SLEEP3)	Supply current in sleep mode V_{DD1} & V2 off, V_{SUP} = 18 V, oscillator running	-	170	270	µA	(7) (10)
$I_{SUP(STDBY)}$	Supply Current in Stand-by Mode I_{OUT} at V_{DD1} = 40 mA, CAN recessive state or disabled	-	42	45	mA	(7),(9)
$I_{SUP(NORM)}$	Supply Current in Normal Mode I_{OUT} at V_{DD1} = 40 mA, CAN recessive state or disabled	-	42.5	45	mA	(7)
I_{SUP} (STOP1)	Supply Current in Stop mode I_{OUT} V_{DD1} < 2.0 mA, V_{DD1} on , $V_{SUP} \leq 12$ V, oscillator running	-	120	150	µA	(7),(9)(10) (11)
I_{SUP} (STOP2)	Supply Current in Stop mode I_{OUT} V_{DD1} < 2.0 mA, V_{DD1} on, $V_{SUP} \leq 12$ V, oscillator not running	-	80	110	µA	(7),(9)(10) (11)
I_{SUP} (STOP3)	Supply Current in Stop mode Iout V_{DD1} < 2.0 mA, V_{DD1} on, V_{SUP} = 18 V, oscillator running	-	200	285	µA	(7),(9)(10) (11)
V_{THRESH}	Supply Fail Flag internal threshold	1.5	3.0	4.0	V	
$V_{DETHYST}$	Supply Fail Flag hysteresis	-	1.0	-	V	(12)
BF_{EW}	Battery fall early warning threshold In normal & standby mode	5.8	6.1	6.4	V	
BF_{EWH}	Battery fall early warning hysteresis In normal & standby mode	0.1	0.2	0.3	V	(12)

Notes

6. V_{DD1} > 4.0 V, reset high, if R_{STTH-2} selected and I_{OUT} V_{DD1} reduced, logic pin high level reduced, device is functional.
7. Current measured at V_{SUP} pin.
8. Device is fully functional. All modes available and operating, Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0 and L1 inputs operating, SPI read write operation. Over temperature may occur.
9. Measured in worst case condition with 5.0 V at V2 pin (V2 pin tied to VDD1).
10. Oscillator running means “Forced Wake-up” or “Cyclic Sense” or “Software Watchdog” timer activated. Software Watchdog is available in stop mode only.
11. V_{DD1} is ON with 2.0 mA typical output current capability.
12. Guaranteed by design

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions - V_{SUP} From 5.5 V to 18 V and T_J from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Output pin (VDD1) (14)						
V_{DD1OUT}	VDD1 Output Voltage I_{DD1} from 2.0 to 200 mA 5.5 V < V_{SUP} < 27 V 4.5 V < V_{SUP} < 5.5 V	 4.9 4.0	 5.0 -	 5.1 -	V	
$V_{DD1DROP}$	Drop Voltage V_{SUP} > V_{DDOUT} I_{DD1} = 200 mA	-	0.2	0.5	V	
V_{DD1DP2}	Drop Voltage V_{SUP} > V_{DDOUT}, limited output current I_{DD1} = 50 mA 4.5 V < V_{SUP} < 27 V	-	0.1	0.25	V	
I_{DD1}	I_{DD1} Output Current Internally limited	200	270	350	mA	
V_{DDSTOP}	VDD1 Output Voltage in stop mode I_{OUT} < 2.0 mA	4.75	5.00	5.25	V	
$I_{DD1S-WU1}$	I_{DD1} stop output current to wake-up SBC Default value after reset.	2.0	3.5	6.0	mA	(15)
$I_{DD1S-WU2}$	I_{DD1} stop output current to wake-up SBC	10	14	18	mA	(15)
$I_{DD1-DGIT11}$	I_{DD1} overcurrent wake deglitcher (with $I_{DD1S-WU1}$ selected)	40	55	75	µs	(13)
$I_{DD1-DGIT2}$	I_{DD1} overcurrent wake deglitcher (with $I_{DD1S-WU2}$ selected)	-	150	-	µs	(13)
T_{SD}	Thermal Shutdown Normal or standby mode	160	-	190	°C	
T_{PW}	Overtemperature prewarning VDDTEMP bit set	130	-	160	°C	
T_{SD}-T_{PW}	Temperature Threshold difference	20	-	40	°C	
$V_{RST-TH1}$	Reset threshold 1 Default value after reset. (15)	4.5	4.6	4.7	V	
$V_{RST-TH2}$	Reset threshold 2 (15)	4.1	4.2	4.3	V	
RESET-DUR	Reset duration	0.85	1.0	2.0	ms	
V_{DD}	VDD1 range for Reset Active	1.0	-	-	V	
t_D	Reset Delay Time Measured at 50% of reset signal. (13)	5.0	-	20	µs	
LR1	Line Regulation 9.0 V < V_{SUP} < 18 V, I_{DD} = 10 mA	-	5.0	25	mV	
LR2	Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA	-	10	25	mV	
LD	Load Regulation 1.0 mA < I_{IDD} < 200 mA	-	25	75	mV	
THERMS	Thermal stability V_{SUP} = 13.5 V, I = 100 mA	-	5.0	-	mV	

Notes

13. Guaranteed by design
14. I_{DD1} is the total regulator output current. VDD specification with external capacitor C ≥ 22 µF and ESR < 10 Ω.
15. Selectable by SPI

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions - V_{SUP} From 5.5 V to 18 V and T_J from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V2 regulator (V2) (16)						
V2	V2 Output Voltage I2 from 2.0 to 200 mA, 5.5 V < V_{SUP} < 27 V (17)	0.99	1.0	1.01	V_{DD1}	
I2	I2 output current (for information only) Depending on the external ballast transistor	200	-	-	mA	
$I2_{CTRL}$	V2 CTRL sink current capability	10	-	-	mA	
$V2L_{TH}$	V2LOW flag threshold	3.75	4.0	4.25	V	
I_{V2RS}	Internal V2 Supply Current (CAN and SBC in Normal Mode). TX = 5.0 V, CAN in Recessive State	3.8	5.6	6.8	mA	
I_{V2DS}	Internal V2 Supply Current (CAN and SBC in Normal Mode). TX = 0.0 V, No Load, CAN in Dominant State	4.0	5.8	7.0	mA	
I_{V2R}	Internal V2 Supply Current (CAN in Receive Only Mode, SBC in Normal mode). V_{SUP} = 12 V	-	80	120	µA	
I_{V2BT}	Internal V2 Supply Current (CAN in Bus TermVbat mode, SBC in normal mode), V_{SUP} = 12 V	-	35	60	µA	
Logic output pins (MISO)						
V_{OL}	Low Level Output Voltage I_{OUT} = 1.5 mA	-	-	1.0	V	
V_{OH}	High Level Output Voltage I_{OUT} = -250 µA	$V_{DD1-0.9}$	-	-	V	
I_{HZ}	Tri-state MISO Leakage Current 0.0 V < V_{MISO} < V_{DD}	-2.0	-	+2.0	µA	
Logic input pins (MOSI, SCLK, CS)						
V_{IH}	High Level Input Voltage	$0.7V_{DD1}$	-	V_{DD1}+0.3V		
V_{IL}	Low Level Input Voltage	-0.3	-	0.3 V_{DD1}	V	
I_{IH} I_{IL}	Input Current on $\overline{CS}$ V_I = 4.0 V V_I = 1.0 V	-100	-	-20	µA	
I_{IL}	Low Level Input Current $\overline{CS}$ V_I = 1.0 V	-100	-	-20	µA	
I_{IN}	MOSI, SCLK Input Current 0.0 < V_{IN} < V_{DD}	-10	-	10	µA	
Reset pin (RST)						
I_{OH}	High Level Output current 0.0 < V_{OUT} < 0.7 V_{DD}	-350	-250	-150	µA	
V_{OL}	Low Level Output Voltage (I_0 = 1.5 mA) 5.5 V < V_{SUP} < 27 V 1.0 V < V_{DD1}	 0.0 0.0	 - -	 0.9 0.9	V	
I_{PDW}	Reset pull-down current	2.3	-	5.0	mA	

Notes

16. V2 tracking voltage regulator - V2 specification with external capacitor
- option 1: C ≥ 22 µF and ESR < 10 Ω. Using a resistor of 2 kΩ or less between the base and emitter of the external PNP is recommended.
- option2: 1.0 µF < C < 22 µF and ESR < 10 Ω. In this case depending on the ballast transistor gain an additional resistor and capacitor network between emitter and base of PNP ballast transistor might be required. Refer to NXP application information or contact your local technical support.
- option 3: 10 uF < C < 22 µF ESR > 0.2 Ω: a resistor of 2 kΩ or less is required between the base and emitter of the external PNP.

17. For I_{VDD1} > 10 mA

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions - V_{SUP} From 5.5 V to 18 V and T_J from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Watchdog pin (Wdog)						
V_{OL}	Low Level Output Voltage (I_0 = 1.5 mA) 5.5 V < V_{SUP} < 27 V	0.0	-	0.9	V	
V_{OH}	High Level Output Voltage (I_0 = -250 µA)	V_{DD1} -0.9	-	V_{DD1}	V	
Interrupt Pin (INT)						
V_{OL}	Low Level Output Voltage (I_0 = 1.5 mA)	0.0	-	0.9	V	
V_{OH}	High Level Output Voltage (I_0 = -250 µA)	V_{DD1} -0.9	-	V_{DD1}	V	
High-side output pin (HS1)						
R_{DSON25}	R_{DSON} at Tj = 25 °C, and I_{OUT} -150 mA V_{SUP} > 9.0 V	-	-	2.5	W	
$R_{DSON125}$	R_{DSON} at T_J = 125 °C, and I_{OUT} -150 mA V_{SUP} > 9.0 V	-	-	5.0	W	
$R_{DON125-2}$	R_{DSON} at T_J = 125 °C, and I_{OUT} -120 mA 5.5 V < V_{SUP} < 9.0 V	-	4.0	5.5	W	
I_{LIM}	Output current limitation	160	-	500	mA	
O_{VT}	Overtemperature Shutdown	155	-	190	°C	
I_{LEAK}	Leakage current	-	-	10	µA	
V_{CL}	Output Clamp Voltage at I_{OUT} = -1.0 mA no inductive load drive capability	-1.5	-	-0.3	V	(18)
Input pins (L0 and L1)						
V_{TH0N}	L0 Negative Switching Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	 1.7 2.0 2.0	 2.0 2.4 2.5	 3.0 3.0 3.1	V	
V_{TH0P}	L0 Positive Switching Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	 2.2 2.5 2.5	 2.75 3.4 3.5	 4.0 4.0 4.1	V	
V_{TH1N}	L1 Negative Switching Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	 2.0 2.5 2.7	 2.5 3.0 3.2	 3.0 3.7 3.8	V	
V_{TH1P}	L1 Positive Switching Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18V 18 V < V_{SUP} < 27 V	 2.7 3.0 3.5	 3.3 4.0 4.2	 3.8 4.7 4.8	V	
V_{HYST}	Hysteresis 5.5 V < V_{SUP} < 27 V	0.6	1.0	1.3	V	
I_{IN}	Input current -0.2 V < V_{IN} < 40 V	-10	-	10	µA	

Notes
18. Refer to HS1 negative maximum rating voltage limitation of -0.2 V.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions - V_{SUP} From 5.5 V to 18 V and T_J from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
CAN module specification (TX, RX, CANH, CANL, RTH, and RTL)						
V_{LOGIC}	DC Voltage On Pins TX, RX	-0.3		V_{DD1} + 0.3	V	
$V2_{INT}$	DC voltage at V2 (V2INT)	0.0		5.25	V	
V_{BUS}	DC Voltage On Pins CANH, CANL	-20		+27	V	
V_{CANH}/V_{CANL}	Transient Voltage At Pins CANH, CANL $0.0 < V_{2\text{-}INT} < 5.5$ V; $V_{SUP} \geq 0.0$; T < 500 ms	-40	-	40	V	
V_{TR}	Transient Voltage On Pins CANH, CANL (Coupled Through 1.0 nF Capacitor)	-150	-	100	V	
V_{CANH}	Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode) MC33889B	V_{SUP}/2+3	-	V_{SUP}/2+5	V	
V_{CANH}	Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode) MC33889D	V_{SUP}/2+3	-	V_{SUP}/ 2+4.55	V	
V_{RTL}, V_{RTH}	DC Voltage On Pins RTH, RTL	-0.3	-	+27	V	
V_{RTH}/V_{RTL}	Transient Voltage At Pins RTH, RTL $0.0 < V_{2\text{-}INT} < 5.5$ V; $V_{SUP} \geq 0.0$; T < 500 ms	-0.3	-	40	V	
Transmitter Data Pin (TX)						
V_{IH}	High Level Input Voltage	0.7*V_2	-	V_2+0.3V	V	
V_{IL}	Low Level Input Voltage	-0.3	-	0.3 * V_2	V	
I_{TXH}	TX High Level Input Current (V_I = 4.0 V)	-100	-50	-25	µA	
I_{TXL}	TX Low Level Input Current (V_I = 1.0 V)	-100	-50	-25	µA	
Receive data pin (rX)						
V_{OH}	High Level Output Voltage RX (I_0 = -250 µA)	$V_{2\text{-}INT}$ - 0.9	-	$V_{2\text{-}INT}$	V	
V_{OL}	Low Level Output Voltage (I_0 = 1.5 mA)	0.0	-	0.9	V	
CAN high and can low pins (CANH, CANL)						
V_{DIFF1}	Differential Receiver, Recessive To Dominant Threshold (By Definition, $V_{DIFF} = V_{CANH}$-V_{CANL}) For 33889D For 33889B	 -3.5 -3.2	 -3.0 -2.6	 -2.5 -2.1	V	
V_{DIFF2}	Differential Receiver, Dominant To Recessive Threshold (Bus Failures 1, 2, 5) For 33889D For 33889B	 -3.5 -3.2	 -3.0 -2.6	 -2.5 -2.1	V	
V_{CANH}	CANH Recessive Output Voltage TX = 5.0 V; $R_{(RTH)}$ < 4.0 k	-	-	0.2	V	
V_{CANL}	CANL Recessive Output Voltage TX = 5.0 V; $R_{(RTL)}$ < 4.0 k	$V_{2\text{-}INT}$ - 0.2	-	-	V	

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions - V_{SUP} From 5.5 V to 18 V and T_J from -40 to 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{CANH}	CANH Output Voltage, Dominant TX = 0.0 V; I_{CANH} = -40 mA; Normal Operating Mode	V_2 - 1.4	-	-	V	(19)
V_{CANL}	CANL Output Voltage, Dominant TX = 0.0 V; I_{CANL} = 40 mA; Normal Operating Mode	-	-	1.4	V	(19)
I_{CANH}	CANH Output Current (V_{CANH} = 0; TX = 0.0) For 33889D For 33889B	 50 50	 100 75	 130 110	mA	
I_{CANL}	CANL Output Current (V_{CANL} = 14 V; TX = 0.0) For 33889D For 33889B	 50 50	 140 90	 170 135	mA	
V_{CANH}, V_{CANL}	Detection Threshold For Short-circuit To Battery Voltage (Normal Mode)	7.3	7.9	8.9	V	
VcanH	Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode), MC33889B	Vsup/2+3	-	Vsup/2+5	V	
VcanH	Detection Threshold For Short-circuit To Battery Voltage (Term VBAT Mode), MC33889D	Vsup/2+3	-	Vsup/ 2+4.55	V	
I_{CANH}	CANH Output Current (Term V_{BAT} Mode; V_{CANH} = 12 V, Failure3)	-	5.0	10	µA	
I_{CANL}	CANL Output Current (Term V_{BAT} Mode; V_{CANL} = 0.0 V; V_{BAT} = 12 V, Failure 4)	-	0.0	2.0	µA	
$V_{WAKE,L}$	CANL Wake-up Voltage Threshold	2.5	3.0	3.9	V	
$V_{WAKE,H}$	CANH Wake-up Voltage Threshold	1.2	2.0	2.7	V	
V_{WAKEL}-V_{WAKEH}	Wake-up Threshold Difference (Hysteresis)	0.2	-	-	V	
$V_{SE, CANH}$	CANH Single Ended Receiver Threshold (Failures 4, 6, 7)	1.5	1.85	2.15	V	
$V_{SE, CANL}$	CANL Single Ended Receiver Threshold (Failures 3, 8)	2.8	3.05	3.4	V	
$I_{CANL,PU}$	CANL Pull-up Current (Normal Mode)	45	75	90	µA	
$I_{CANH,PD}$	CANH Pull-down Current (Normal Mode)	45	75	90	µA	
R_{DIFF}	Receiver Differential Input Impedance CANH / CANL	100	-	300	kΩ	
V_{COM}	Differential Receiver Common Mode Voltage Range	-10	-	10	V	(20)
C_{CANH}	CANH To Ground Capacitance	-	-	50	pF	
C_{CANL}	CANL To Ground Capacitance	-	-	50	pF	
DC_{CAN}	C_{CANL} to C_{CANH} Capacitor Difference	-	-	10	pF	
t_{CSD}	CAN Driver Thermal Shutdown	150	160	-	°C	
Bus termination pins (RTH, RTL)						
R_{RTL}	RTL to V2 Switch On Resistance (I_{OUT} < -10 mA; Normal Operating Mode)	10	30	90	W	
R_{RTL}	RTL to BAT Switch Series Resistance (term V_{BAT} Mode)	8.0	12.5	20	kΩ	
R_{RTH}	RTH To Ground Switch On Resistance (I_{OUT} < 10 mA; Normal Operating Mode)	10	30	90	W	

Notes

19. For MC33889B, after 128 pulses on TX and no bus failure.
20. Guaranteed by design

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

V_{SUP} From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and T_J from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Digital interface timing (SCLK, CS, MOSI, MISO)						
FREQ	SPI operation frequency	-	-	4.0	MHz	
t_{PCLK}	SCLK Clock Period	250	-	-	ns	
t_{WSCLKH}	SCLK Clock High Time	125	-	-	ns	
t_{WSCLKL}	SCLK Clock Low Time	125	-	-	ns	
t_{ILEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	100	50	-	ns	
t_{LAG}	Falling Edge of SCLK to Rising Edge of $\overline{CS}$	100	50	-	ns	
t_{SISU}	MOSI to Falling Edge of SCLK	40	25	-	ns	
t_{SIH}	Falling Edge of SCLK to MOSI	40	25	-	ns	
t_{RSO}	MISO Rise Time (CL = 220 pF)	-	25	50	ns	
t_{fSO}	MISO Fall Time (CL = 220 pF)	-	25	50	ns	
t_{SOEN} t_{SODIS}	Time from Falling or Rising Edges of $\overline{CS}$ to: - MISO Low-impedance - MISO High-impedance	 - -	 - -	 50 50	ns	
t_{VALID}	Time from Rising Edge of SCLK to MISO Data Valid 0.2 V1 ≤ SO ≥ 0.8 V1, C_L = 200 pF	-	-	50	ns	
$T_{\overline{CS}\text{-STOP}}$	Delay between $\overline{CS}$ low to high transition (at end of SPI stop command) and Stop or sleep mode activation detected by V2 off	18	-	34	µs	(21)
T_{INT}	Interrupt low level duration SBC in stop mode	7.0	10	13	µs	
$O_{SC\text{-}F1}$	Internal oscillator frequency All modes except Sleep and Stop	-	100	-	kHz	(21)
$O_{SC\text{-}F2}$	Internal low power oscillator frequency Sleep and Stop modes	-	100	-	kHz	(21)
W_{D1}	Watchdog period 1 Normal and standby modes	8.58	9.75	10.92	ms	
W_{D2}	Watchdog period 2 Normal and standby modes	39.6	45	50.4	ms	
W_{D3}	Watchdog period 3 Normal and standby modes	88	100	112	ms	
W_{D4}	Watchdog period 4 Normal and standby modes	308	350	392	ms	
$F1_{ACC}$	Watchdog period accuracy Normal and standby modes	-12	-	12	%	
NR_{TOUT}	Normal request mode timeout Normal request mode	308	350	392	ms	
$WD1_{STOP}$	Watchdog period 1 - stop Stop mode	6.82	9.75	12.7	ms	
$WD2_{STOP}$	Watchdog period 2- stop Stop mode	31.5	45	58.5	ms	

Notes

21. Guaranteed by design

Table 5. Dynamic electrical characteristics (continued)

V_{SUP} From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and T_J from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
$WD3_{STOP}$	Watchdog period 3 - stop Stop mode	70	100	130	ms	
$WD4_{STOP}$	Watchdog period 4 - stop Stop mode	245	350	455	ms	
$F2_{ACC}$	Stop mode watchdog period accuracy Stop mode	-30	-	30	%	
CSFWU1	Cyclic sense/FWU timing 1 Sleep and Stop modes	3.22	4.6	5.98	ms	
CSFWU2	Cyclic sense/FWU timing 2 Sleep and Stop modes	6.47	9.25	12	ms	
CSFWU3	Cyclic sense/FWU timing 3 Sleep and Stop modes	12.9	18.5	24	ms	
CSFWU4	Cyclic sense/FWU timing 4 Sleep and Stop modes	25.9	37	48.1	ms	
CSFWU5	Cyclic sense/FWU timing 5 Sleep and Stop modes	51.8	74	96.2	ms	
CSFWU6	Cyclic sense/FWU timing 6 Sleep and Stop modes	66.8	95.5	124	ms	
CSFWU7	Cyclic sense/FWU timing 7 Sleep and Stop modes	134	191	248	ms	
CSFWU8	Cyclic sense/FWU timing 8 Sleep and Stop modes	271	388	504	ms	
t_{ON}	Cyclic sense On time Sleep and Stop modes	200	300	400	µs	
t_{ACC}	Cyclic sense/FWU timing accuracy Sleep and Stop mode	-30	-	+30	%	
t_{S-HSON}	Delay between SPI command and HS1 turn on Normal or Standby mode, V_{SUP} > 9.0 V	-	-	22	µs	(22)
$t_{S-HSOFF}$	Delay between SPI command and HS1 turn off Normal or Standby mode, V_{SUP} > 9.0 V	-	-	22	µs	(22)
t_{S-V2ON}	Delay between SPI and V2 turn on Standby mode	9.0	-	25	µs	(22)
$t_{S-V2OFF}$	Delay between SPI and V2 turn off Normal modes	9.0	-	25	µs	(22)
t_{S-NR2N}	Delay between Normal Request and Normal mode, after W/D trigger command Normal request mode	15	35	70	µs	

Notes

22. State Machine Timing - Delay starts at rising edge of $\overline{CS}$ (end of SPI command) and start of Turn on or Turn off of HS1 or V2.

Table 5. Dynamic electrical characteristics (continued)

V_{SUP} From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and T_J from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
t_{S-CANN}	Delay between SPI and “CAN normal mode” SBC Normal mode	-	-	10	µs	(23)
t_{S-CANS}	Delay between SPI and “CAN sleep mode” SBC Normal mode	-	-	10	µs	(23)
$t_{W-\overline{CS}}$	Delay between $\overline{CS}$ wake-up ($\overline{CS}$ low to high) and SBC normal request mode (V_{DD1} on & reset high) SBC in Stop mode	15	40	90	µs	
t_{W-SPI}	Delay between $\overline{CS}$ wake-up ($\overline{CS}$ low to high) and first accepted SPI command SBC in Stop mode	90	-	-	µs	
$t_{S-1STSPI}$	Delay between INT pulse and 1st SPI command accepted In Stop mode after wake-up	20	-	-	µs	
$t2_{SPI}$	Delay between two SPI messages addressing the same register For 33889D only	25	-	-	µs	
Input pins (L0 and L1)						
t_{WUF}	Wake-up Filter Time (enable/disable option on L0 input) (If filter enabled)	8.0	20	38	µs	
Pin AC characteristics (canh, canl, rx, tx)						
t_{SLDR}	CANL and CANH Slew Rates (25% to 75% CAN signal). Recessive to Dominant state Dominant to Recessive state	 2.0 2.0	 - -	 8.0 9.0	V/µs	(24)
t_{ONRX}	Propagation Delay TX to RX Low. -40 < T ≤ 25°C. TX to RX Low. 25 < T < 125°C.	 - -	 1.2 1.1	 1.6 1.8	µs	(25)
t_{OFFRX}	Propagation Delay TX to RX High.	-	1.8	2.2	µs	(25)

Notes

23. Guaranteed by design
24. Dominant to recessive slew rate is dependant upon the bus load characteristics.
25. AC Characteristics measured according to schematic Figure 5

Table 5. Dynamic electrical characteristics (continued)

V_{SUP} From 5.5 V to 18 V, V2INT from 4.75 to 5.25 V and T_J from -40 to 150 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
t_{LOOPRD}	Loop time Tx to Rx, no bus failure, MC33889D only (Figure 6) (ISO ICT test series 10) Tx high to low transition (dominant edge) Tx low to high transition (recessive edge)	 - -	 1.15 1.45	 1.5 1.5	µs	(26)
$t_{LOOPRD-F}$	Loop time Tx to Rx, with bus failure, MC33889D only (Figure 7) (ISO ICT test series 10) Tx high to low transition (dominant edge) Tx low to high transition (recessive edge)	 - -	 - -	 1.9 1.9	µs	(26)
$t_{LOOPRD/DR-F+GS}$	Loop time Tx to Rx, with bus failure and ±1.5 V gnd shift, 5 nodes network, MC33889D,(Figure 8, ISO ICT tests series 11)			3.6	µs	(27)
t_{WAKE}	Min. Dominant Time For Wake-up On CANL or CANH (Term V_{BAT}; V_{SUP} = 12 V) Guaranteed by design. MC33889B MC33889D	 - 8.0	 30 16	 - 30	µs	
t_{DF3}	Failure 3 Detection Time (Normal Mode)	10	30	80	µs	
t_{DR3}	Failure 3 Recovery Time (Normal Mode)	-	160	-	µs	
t_{DF6}	Failure 6 Detection Time (Normal Mode)	50	200	500	µs	
t_{DR6}	Failure 6 Recovery Time (Normal Mode)	150	200	1000	µs	
t_{DF47}	Failure 4, 7 Detection Time (Normal Mode)	0.75	1.5	4.0	ms	
t_{DR47}	Failure 4, 7 Recovery Time (Normal Mode)	10	30	60	µs	
t_{DF8}	Failure 3a, 8 Detection Time (Normal Mode)	0.75	1.7	4.0	ms	
tT_{DR8}	Failure 3a, 8 Recovery Time (Normal Mode)	0.75	1.5	4.0	ms	
t_{DR47}	Failure 4, 7 Detection Time, (Term V_{BAT}; V_{SUP} = 12 V)	0.8	1.2	8.0	ms	
t_{DR47}	Failure 4, 7 Recovery Time (Term V_{BAT}; V_{SUP} = 12 V)	-	1.92	-	ms	
t_{DR3}	Failure 3 Detection Time (Term V_{BAT}; V_{SUP} = 12 V)	-	3.84	-	ms	
t_{DR3}	Failure 3 Recovery Time (Term V_{BAT}; V_{SUP} = 12 V)	-	1.92	-	ms	
t_{DR8}	Failure 3a, 8Detection Time (Term V_{BAT}; V_{SUP} = 12 V)	-	2.3	-	ms	
t_{DR8}	Failure 3a, 8 Recovery Time (Term V_{BAT}; V_{SUP} = 12 V)	-	1.2	-	ms	
E_{CDF}	Edge Count Difference Between CANH and CANL for Failures 1, 2, 5 Detection (Failure bit set, Normal Mode)	-	3	-		
E_{CDR}	Edge Count Difference Between CANH And CANL For Failures 1, 2, 5 Recovery (Normal Mode)	-	3	-		
$t_{TX,D}$	TX Permanent Dominant Timer Disable Time (Normal Mode And Failure Mode)	0.75	-	4.0	ms	
$t_{TX,E}$	TX Permanent Dominant Timer Enable Time (Normal Mode And Failure Mode)	10	-	60	µs	

Notes

26. AC characteristic according to ISO11898-3, tested per figure 5 and 6. Guaranteed by design, room temperature only.
27. AC characteristic according to ISO11898-3, tested per figure 7. Max. reported is the typical measurement under the worst condition (gnd shift, dominant/recessive edge, at source or destination node. ref to ISO test specification). Guaranteed by design, room temperature only.

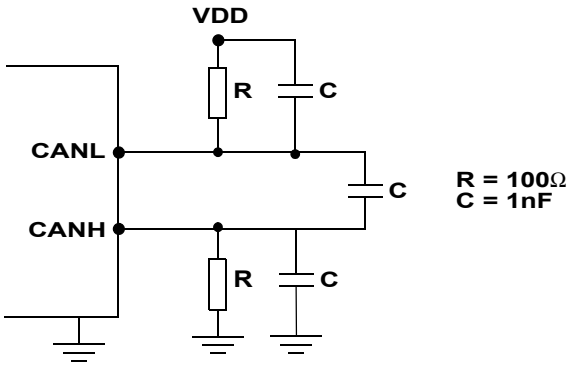
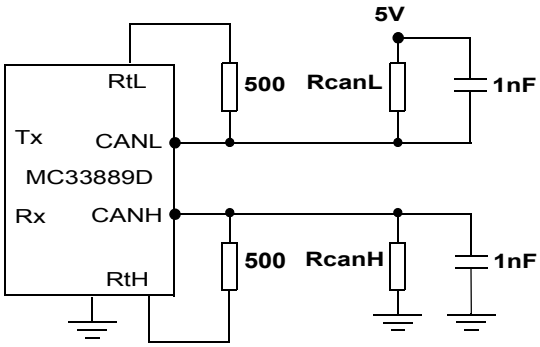
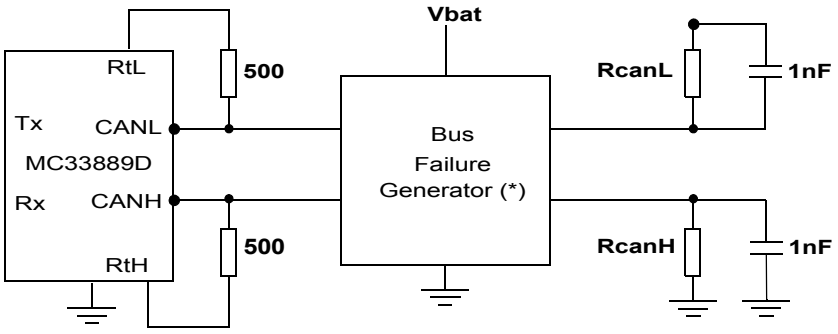


Figure 5. Test circuit for AC characteristics



RcanL = RcanH = 125 Ω

Figure 6. ISO loop time without bus failure



RcanL = RcanH = 125 Ω
except for failure CANH short to CANL
(Rcanl = 1M Ω)

(*) List of failure
CANL short to gnd, Vdd, Vbat
CANHshort to gnd, Vdd, Vbat
CANL short to CANH
CANL and CANH open

Figure 7. ISO loop time with bus failure

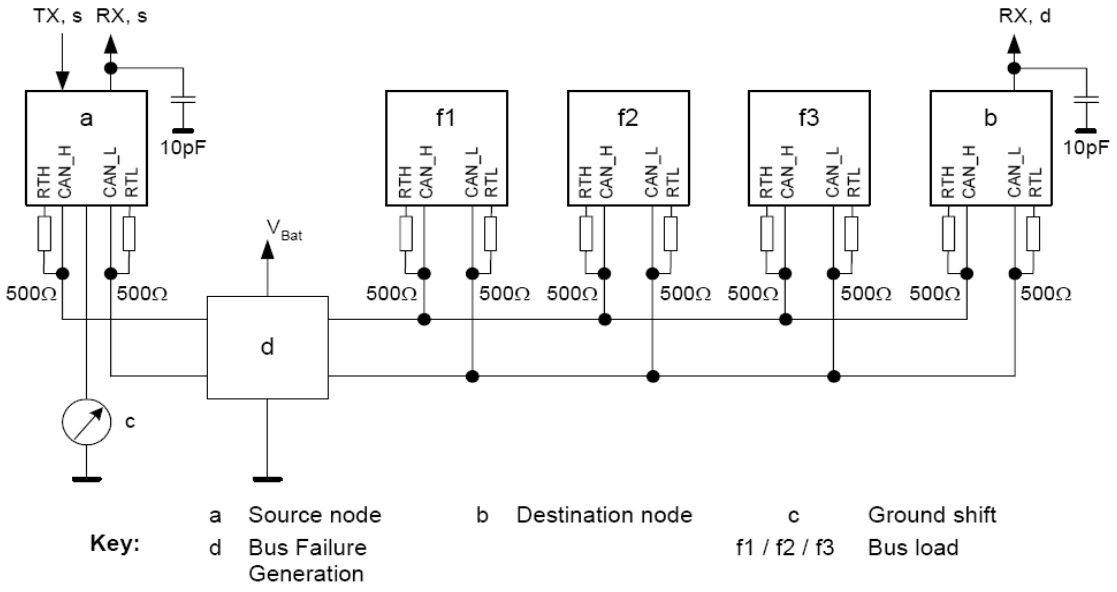


Figure 8. Test set up for propagation delay with GND shift in a 5 node configuration

4.4 Timing diagrams

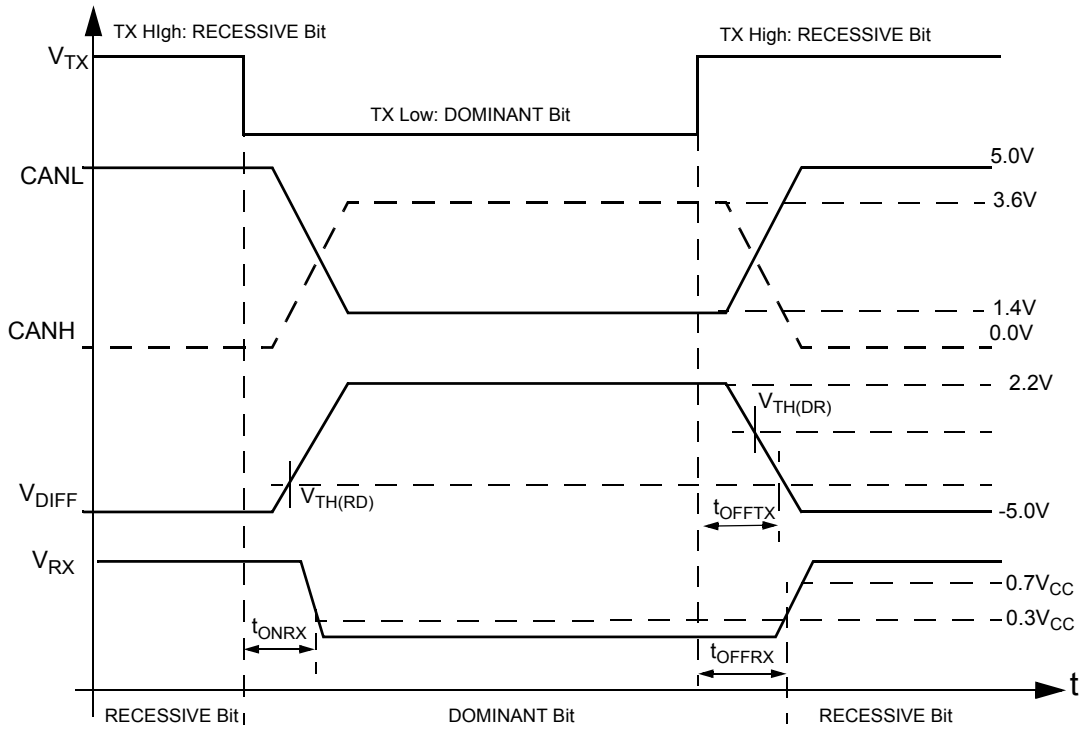


Figure 9. Device signal waveforms

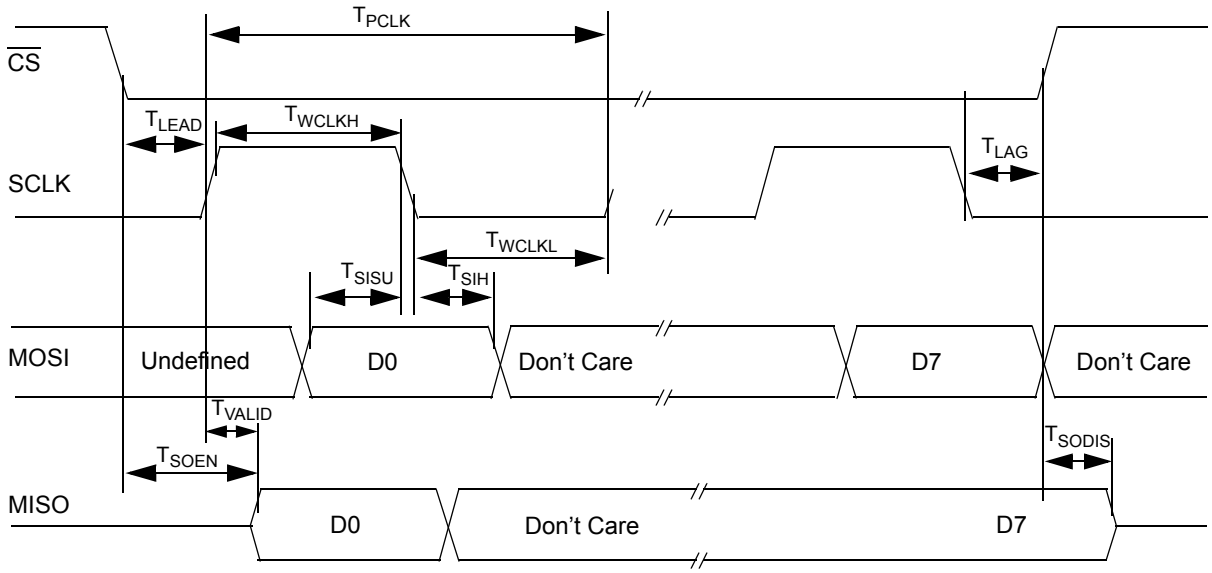


Figure 10. Timing characteristic

5 Functional description

5.1 Introduction

The MC33889 is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 200 mA total output current capability.
- Driver for external path transistor for V2 regulator function.
- Reset, programmable watchdog function
- Four operational modes
- Wake-up capabilities: Forced wake-up, cyclic sense and wake-up inputs, CAN and the SPI
- Can low speed fault tolerant physical interface.

5.2 Functional pin description

5.2.1 Receive and transmit data (RX and TX)

The RX and TX pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TX is an input and controls the CANH and CANL line state (dominant when TX is LOW, recessive when TX is HIGH). RX is an output and reports the bus state (RX LOW when CAN bus is dominant, HIGH when CAN bus is recessive).

5.2.2 Voltage regulator one (VDD1)

The VDD1 pin is the output pin of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against overcurrent and overtemperature. It includes an overtemperature prewarning flag, which is set when the internal regulator temperature exceeds 130 °C typical. When the temperature exceeds the overtemperature shutdown (170 °C typical), the regulator is turned off. VDD1 includes an undervoltage reset circuitry, which sets the $\overline{\text{RST}}$ pin LOW when VDD is below the undervoltage reset threshold.

5.2.3 Reset ($\overline{\text{RST}}$)

The Reset pin $\overline{\text{RST}}$ is an output that is set LOW when the device is in reset mode. The $\overline{\text{RST}}$ pin is set HIGH when the device is not in reset mode. $\overline{\text{RST}}$ includes an internal pull-up current source. When $\overline{\text{RST}}$ is LOW, the sink current capability is limited, allowing $\overline{\text{RST}}$ to be shorted to 5.0 V for software debug or software download purposes.

5.2.4 Interrupt ($\overline{\text{INT}}$)

The Interrupt pin $\overline{\text{INT}}$ is an output that is set LOW when an interrupt occurs. $\overline{\text{INT}}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{\text{INT}}$ stays LOW until the interrupt source is cleared. $\overline{\text{INT}}$ output also reports a wake-up event by a 10 sec. typical pulse when the device is in Stop mode.

5.2.5 Ground (GND)

This pin is the ground of the integrated circuit.

5.2.6 V2CTRL (V2CTRL)

The V2CTRL pin is the output drive pin for the V2 regulator connected to the external series pass transistor.

5.2.7 Voltage supply (VSUP)

The VSUP pin is the battery supply input of the device.

5.2.8 High-side output 1 (HS1)

The HS pin is the internal high-side driver output. It is internally protected against overcurrent and overtemperature.

5.2.9 Level 0-1 inputs (L0: L1)

The L0: L1 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by the SPI. These inputs can be used as wake-up events for the SBC when operating in the Sleep or Stop mode.

5.2.10 Voltage regulator two (V2)

The V2 pin is the input sense for the V2 regulator. It is connected to the external series pass transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the VDD output when no external series pass transistor is used. In this case, the V2CTRL pin must be left open.

5.2.11 RTH (RTH)

Pin for the connection of the bus termination resistor to CANH

5.2.12 RTL (RTL)

Pin for the connection of the bus termination resistor to CANL

5.2.13 CAN high and CAN low outputs (CANH and CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TXD input level, and the state of CANH and CANL is reported through RXD output.

5.2.14 System clock (SCLK)

SCLK is the Serial Data Clock input pin of the serial peripheral interface.

5.2.15 Master in/slave out (MISO

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

5.2.16 Master out/slave in (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

5.2.17 Chip select ($\overline{CS}$)

$\overline{CS}$ is the Chip Select pin of the serial peripheral interface. When this pin is LOW, the SPI port of the device is selected.

5.2.18 Watchdog ($\overline{WDOG}$)

The Watchdog output pin is asserted LOW to flag that the software watchdog has not been properly triggered.

5.3 Functional internal block description

5.3.1 Device supply

The device is supplied from the battery line through the VSUP pin. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5 V and under the jump start condition at 27 V DC. This pin sustains standard automotive voltage conditions such as load dump at 40 V. When V_{SUP} falls below 3.0 V typical, the MC33889 detects it and stores the information in the SPI register, in a bit called “BATFAIL”. This detection is available in all operation modes.

5.3.2 VDD1 voltage regulator

VDD1 Regulator is a 5.0 V output voltage with total current capability of 200 mA. It includes a voltage monitoring circuitry associated with a reset function. The VDD1 regulator is fully protected against overcurrent, short-circuit and has overtemperature detection warning flags and shutdown with hysteresis.

5.3.3 V2 regulator

V2 Regulator circuitry is designed to drive an external path transistor in order to increase output current flexibility. Two pins are used: V2 and V2CTRL. Output voltage is 5.0 V and is realized by a tracking function of the VDD1 regulator. A recommended ballast transistor is the MJD32C. Other transistors might be used, however depending upon the PNP gain, an external resistor capacitor network might be connected between the emitter and base of the PNP. The use of external ballast is optional (refer to simplified typical application). The state of V2 is reported into the IOR register (if V2 is below 4.5 V typical, or in cases of overload or short-circuit).

5.3.4 HS1 VBAT switch output

HS1 output is a 2.0 Ω typical switch from the VSUP pin. It allows the supply of external switches and their associated pull-up or pull-down circuitry, for example, in conjunction with the wake-up input pins. Output current is limited to 200 mA and HS1 is protected against short-circuit and has an over temperature shutdown (reported into the IOR register). The HS1 output is controlled from the internal register and the SPI. It can be activated at regular intervals in sleep mode thanks to an internal timer. It can also be permanently turned on in normal or stand-by modes to drive external loads, such as relays or supply peripheral components. In case of inductive load drive, external clamp circuitry must be added.

5.3.5 SPI

The complete device control as well as the status report is done through an 8 bit SPI interface. Refer to the SPI paragraph.

5.3.6 CAN

The device incorporates a low speed fault tolerant CAN physical interface. The speed rate is up to 125 kBaud.

The state of the CAN interface is programmable through the SPI. Reference the CAN transceiver description on page 28.

5.3.7 Package and thermal consideration

The device is proposed in a standard surface mount SO28 package. In order to improve the thermal performances of the SO28 package, 8 pins are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

6 Functional device operation

6.1 Operational modes

6.1.1 Introduction

The device has four modes of operation, normal, stand-by, sleep and stop modes. All modes are controlled by the SPI. An additional temporary mode called “normal request mode” is automatically accessed by the device (refer to state machine) after wake-up events. Special mode and configurations are possible for software application debug and flash memory programming.

6.1.2 Normal mode

In this mode both regulators are ON, and this corresponds to the normal application operation. All functions are available in this mode (watchdog, wake-up input reading through the SPI, HS1 activation, and CAN communication). The software watchdog is running and must be periodically cleared through the SPI.

6.1.3 Standby mode

Only the Regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2CTRL pin. The CAN cell is not available, as powered from V2. Other functions are available: wake-up input reading through the SPI and HS1 activation. The watchdog is running.

6.1.4 Sleep mode

Regulators 1 and 2 are OFF. In this mode, the MCU is not powered. The device can be awakened internally by cyclic sense via the wake-up input pins and HS1 output, from the forced wake function, the CAN physical interface, and the SPI ($\overline{CS}$ pin).

6.1.5 Stop mode

Regulator 2 is turned OFF by disabling the V2CTRL pin. Regulator 1 is activated in a special low power mode which allows it to deliver 2.0 mA. The objective is to supply the MCU of the application while it is turned into a power saving condition (i.e stop or wait mode).

Stop mode is entered through the SPI. Stop mode is dedicated to powering the Microcontroller when it is in low power mode (stop, pseudo stop, wait etc.). In these modes, the MCU supply current is less than 1.0 mA. The MCU can restart its software application very quickly without the complete power up and reset sequence.

When the application is in stop mode (both MCU and SBC), the application can wake-up from the SBC side (ex cyclic sense, forced wake-up, CAN message, wake-up inputs) or the MCU side (key wake-up etc.).

When Stop mode is selected by the SPI, stop mode becomes active 20 μs after end of the SPI message. The “go to stop” instruction must be the last instruction executed by the MCU before going to low power mode.

In Stop mode, the Software watchdog can be “running” or “not running” depending on the selection by the SPI. Refer to the SPI description, RCR register bit WDSTOP. If the W/D is enabled, the SBC must wake-up before the W/D time has expired, otherwise a reset is generated. In stop mode, the SBC wake-up capability is identical as in sleep mode.

6.1.5.1 Stop mode: wake-up from SBC side, INT pin activation

When an application is in stop mode, it can wake-up from the SBC side. When a wake-up is detected by the SBC (CAN, Wake-up input, forced wake-up, etc.), the SBC turns itself into Normal request mode and activates the VDD1 main regulator. When the main regulator is fully active, then the wake-up is signalled to the MCU through the $\overline{INT}$ pin. The $\overline{INT}$ pin is pulled low for 10 μs and then returns high. Wake-up events can be read through the SPI registers.

6.1.5.2 Stop mode: wake-up from MCU side

When the application is in stop mode, the wake-up event may come to the MCU. In this case, the MCU has to signal to the SBC that it has to go into Normal mode in order for the VDD1 regulator to be able to deliver full current capability. This is done by a low to high transition of the $\overline{CS}$ pin. The $\overline{CS}$ pin low to high activation has to be done as soon as possible after the MCU. The SBC generates a pulse at the $\overline{INT}$ pin. Alternatively the L0 and L1 inputs can also be used as wake-up from the Stop mode.

6.1.5.3 Stop mode current monitoring

If the current in Stop mode exceeds the $I_{DD1S-WU}$ threshold, the SBC jumps into Normal request mode, activates the VDD1 main regulator, and generates an interrupt to the MCU. This interrupt is not maskable and a not bit are set into the $\overline{INT}$ register.

6.1.5.4 Software watchdog in stop mode

If the watchdog is enabled (register MCR, bit WDSTOP set), the MCU has to wake-up independently of the SBC before the end of the SBC watchdog time. In order to do this, the MCU has to signal the wake-up to the SBC through the SPI wake-up ($\overline{CS}$ pin low to high transition to activated the SPI wake-up). Then the SBC wakes up and jumps into the normal request mode. The MCU has to configure the SBC to go to either into normal or standby mode. The MCU can then choose to go back into stop mode.

If no MCU wake-up occurs within the watchdog timing, the SBC will activate the reset pin and jump into the normal request mode. The MCU can then be initialized.

6.1.5.5 Normal request mode

This is a temporary mode automatically accessed by the device after a wake-up event from sleep or stop mode, or after device power up. In this mode, the VDD1 regulator is ON, V2 is off, and the reset pin is high. As soon as the device enters the normal request mode, an internal 350 ms timer is started. During these 350 ms, the microcontroller of the application must address the SBC via the SPI and configure the watchdog register (TIM1 register). This is the condition for the SBC to leave the Normal request Mode and enter the Normal mode, and to set the watchdog timer according to the configuration done during the Normal Request mode.

The “BATFAIL flag” is a bit which is triggered when V_{SUP} falls below 3.0 V. This bit is set into the MCR register. It is reset by the MCR register read.

6.1.6 Internal Clock

This device has an internal clock used to generate all timings (reset, watchdog, cyclic wake-up, filtering time etc...).

6.1.7 Reset Pin

A reset output is available in order to reset the microcontroller. Reset causes are:

- V_{DD1} falling out of range: if V_{DD1} falls below the reset threshold (parameter R_{ST-TH}), the reset pin is pulled low until V_{DD1} returns to the nominal voltage.
- Power on reset: at device power on or at device wake-up from sleep mode, the reset is maintained low until V_{DD1} is within its operation range.
- Watchdog timeout: if the watchdog is not cleared, the SBC will pull the reset pin low for the duration of the reset duration time (parameter: RESET-DUR).

For debug purposes at 25 °C, the reset pin can be shorted to 5.0 V.

6.1.8 Software watchdog (selectable window or timeout watchdog)

The software watchdog is used in the SBC normal and stand-by modes for monitoring the MCU. The watchdog can be either a window or timeout. This is selectable by the SPI (register TIM, bit WDW). Default is the window watchdog. The period of the watchdog is selectable by the SPI from 5.0 to 350 ms (register TIM, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first half of the selected period, and the open window is the second half of the period. The watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. The Watchdog is cleared through the SPI by addressing the TIM register.

Refer to “table for reset pin operations” operation in mode 2.

6.1.9 Wake-up capabilities

Several wake-up capabilities are available for the device when it is in sleep or stop mode. When a wake-up has occurred, the wake-up event is stored into the WUR or CAN registers. The MCU can then access the wake-up source. The wake-up options are selectable through the SPI while the device is in normal or standby mode, and prior to entering low power mode (Sleep or Stop mode).

6.1.10 Wake-up from wake-up inputs (L0, L1) without cyclic sense

The wake-up lines are dedicated to sense external switch states, and when changes occur to wake-up the MCU (In sleep or stop modes). The wake-up pins are able to handle 40 V DC. The internal threshold is 3.0 V typical, and these inputs can be used as an input port expander. The wake-up inputs state can be read through the SPI (register WUR). L0 has a lower threshold than L1 in order to allow a connection and wake-up from a digital output such as a CAN physical interface.

6.1.11 Cyclic sense wake-up (cyclic sense timer and wake-up inputs L0, L1)

The SBC can wake-up from a state change of one of the wake-up input lines (L0, L1), while the external pull-up or pull-down resistor of the switches associated to the wake-up input lines are biased with HS1 VSUP switch. The HS1 switch is activated in sleep or stop mode from an internal timer. Cyclic sense and forced wake-up are exclusive. If Cyclic sense is enabled, the forced wake-up can not be enabled.

6.1.12 Info for cyclic sense + dual edge selection

In case the Cyclic sense and Lx both level sensitive conditions are use together, the initial value for Lx inputs are sampled in two cases:

1) When the register LPC[D3 and D0] are set and

2) At cyclic sense event, that is when device is in sleep or stop mode and HS1 is active.

The consequence is that when the device wake up by Lx transition, the new value is sampled as default, then when the device is set back into low power again, it will automatically wake up.

The user should reset the LPC bits [D3 and D0] to 0 and set them again to the desired value prior to enter sleep or stop mode.

6.1.13 Forced wake-up

The SBC can wake-up automatically after a predetermined time spent in sleep or stop mode. Forced wake-up is enabled by setting bit FWU in the LPC register. Cyclic sense and forced wake-up are exclusive. If forced wake-up is enabled, the Cyclic sense can not be enabled.

6.1.14 CAN wake-up

The device can wake-up from a CAN message. A CAN wake-up cannot be disabled.

6.1.15 SPI wake-up

The device can wake-up by the $\overline{CS}$ pin in sleep or stop mode. Wake-up is detected by the $\overline{CS}$ pin transition from a low to high level. In stop mode this correspond to the condition where the MCU and SBC are both in Stop mode, and when the application wake-up events come through the MCU.

6.1.16 System power up

At power up the device automatically wakes up.

6.1.17 Device power up, SBC wake up

After device or system power up or a wake-up from sleep mode, the SBC enters into “reset mode” then into “normal request mode”.