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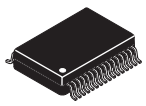
NXP Semiconductors
Data Sheet: Advance Information

Document Number: MC33903_4_5
Rev. 14.0, 2/2018

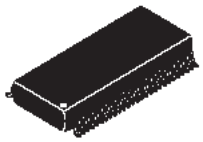
SBC Gen2 with CAN high speed and LIN interface

33903/4/5

SYSTEM BASIS CHIP



EK Suffix (Pb-free)
98ASA10556D
32-PIN SOIC



EK Suffix (Pb-free)
98ASA10506D
54-PIN SOIC

The 33903/4/5 is the second generation family of the System Basis Chip (SBC). It combines several features and enhances present module designs. The device works as an advanced power management unit for the MCU with additional integrated circuits such as sensors and CAN transceivers. It has a built-in enhanced high-speed CAN interface (ISO11898-2 and -5) with local and bus failure diagnostics, protection, and fail-safe operation modes. The SBC may include zero, one or two LIN 2.1 interfaces with LIN output pin switches. It includes up to four wake-up input pins that can also be configured as output drivers for flexibility. This device is powered by SMARTMOS technology.

This device implements multiple Low-power (LP) modes, with very low-current consumption. In addition, the device is part of a family concept where pin compatibility adds versatility to module design.

The 33903/4/5 also implements an innovative and advanced fail-safe state machine and concept solution.

Features

- Voltage regulator for MCU, 5.0 or 3.3 V, part number selectable, with possibility of usage external PNP to extend current capability and share power dissipation
- Voltage, current, and temperature protection
- Extremely low quiescent current in LP modes
- Fully-protected embedded 5.0 V regulator for the CAN driver
- Multiple undervoltage detections to address various MCU specifications and system operation modes (i.e. cranking)
- Auxiliary 5.0 or 3.3 V SPI configurable regulator, for additional ICs, with overcurrent detection and undervoltage protection
- MUX output pin for device internal analog signal monitoring and power supply monitoring
- Advanced SPI, MCU, ECU power supply, and critical pins diagnostics and monitoring.
- Multiple wake-up sources in LP modes: CAN or LIN bus, I/O transition, automatic timer, SPI message, and V_{DD} overcurrent detection.
- ISO11898-5 high-speed CAN interface compatibility for baud rates of 40 kb/s to 1.0 Mb/s
- Scalable product family of devices ranging from 0 to 2 LINs which are compatible to J2602-2 and LIN 2.1

Applications

- Aircraft and marine systems
- Automotive and robotic systems
- Farm equipment
- Industrial actuator controls
- Lamp and inductive load controls
- DC motor control applications requiring diagnostics
- Applications where high-side switch control is required

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Simplified application diagrams

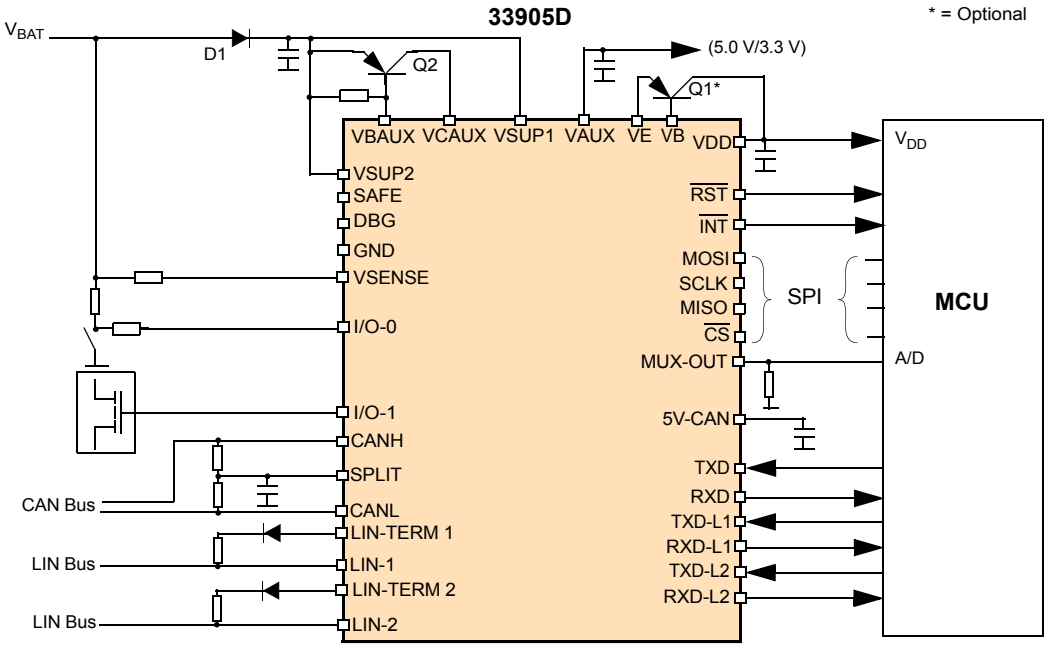


Figure 1. 33905D simplified application diagram

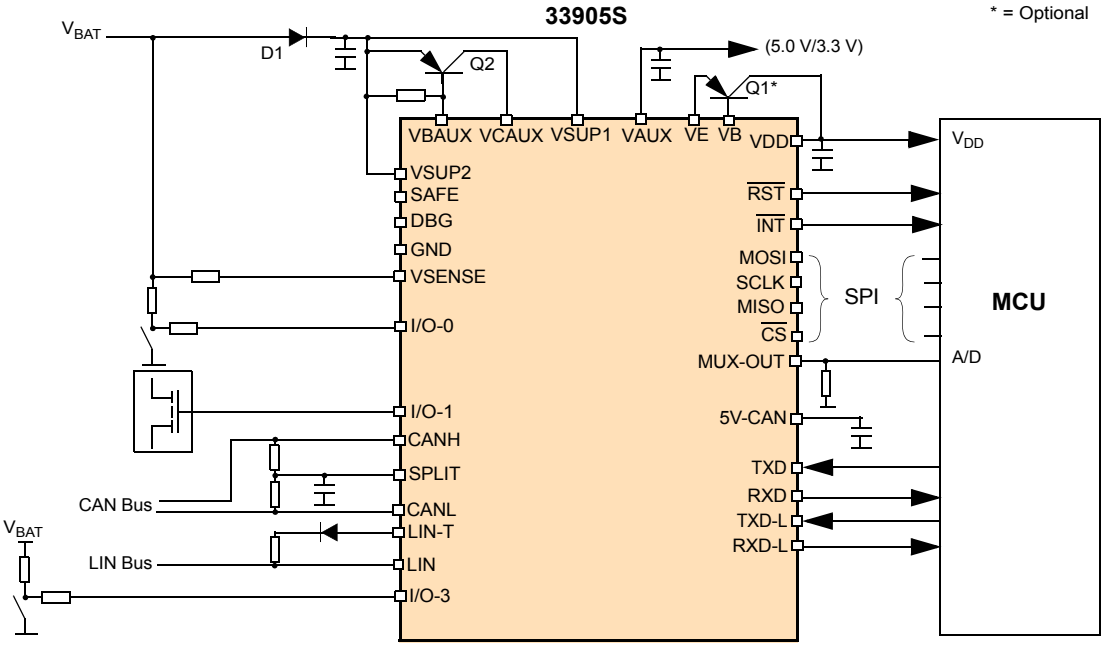


Figure 2. 33905S simplified application diagram

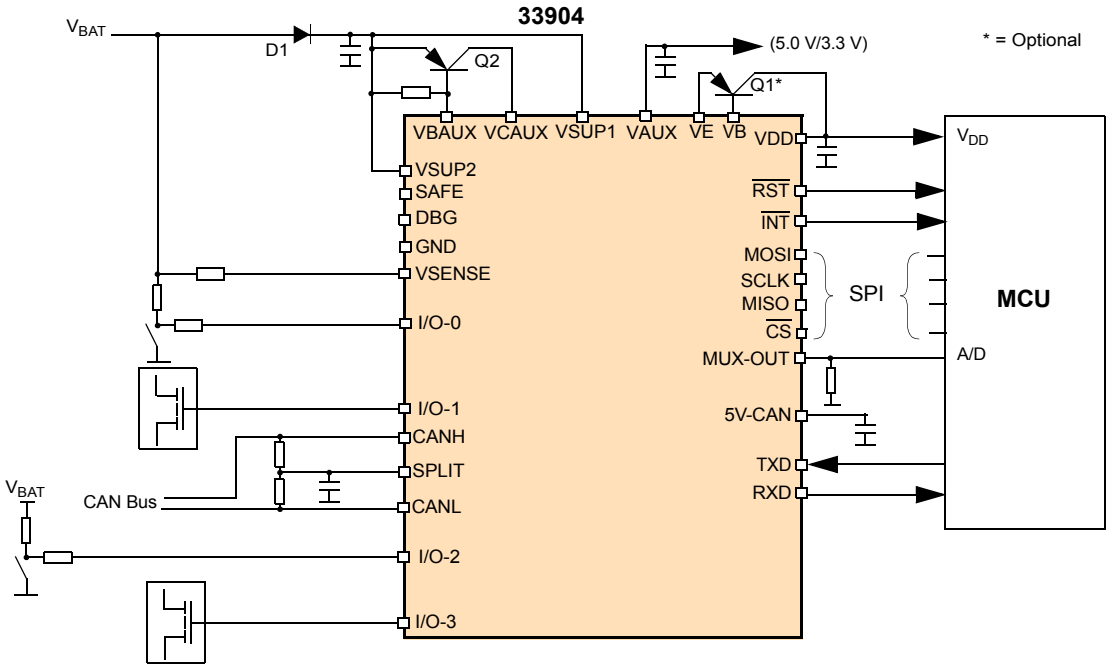


Figure 3. 33904 simplified application diagram

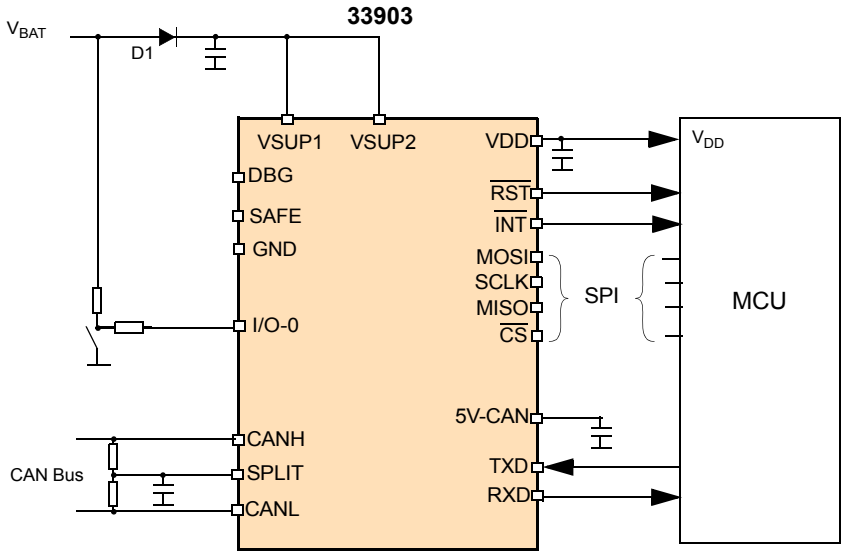


Figure 4. 33903 simplified application diagram

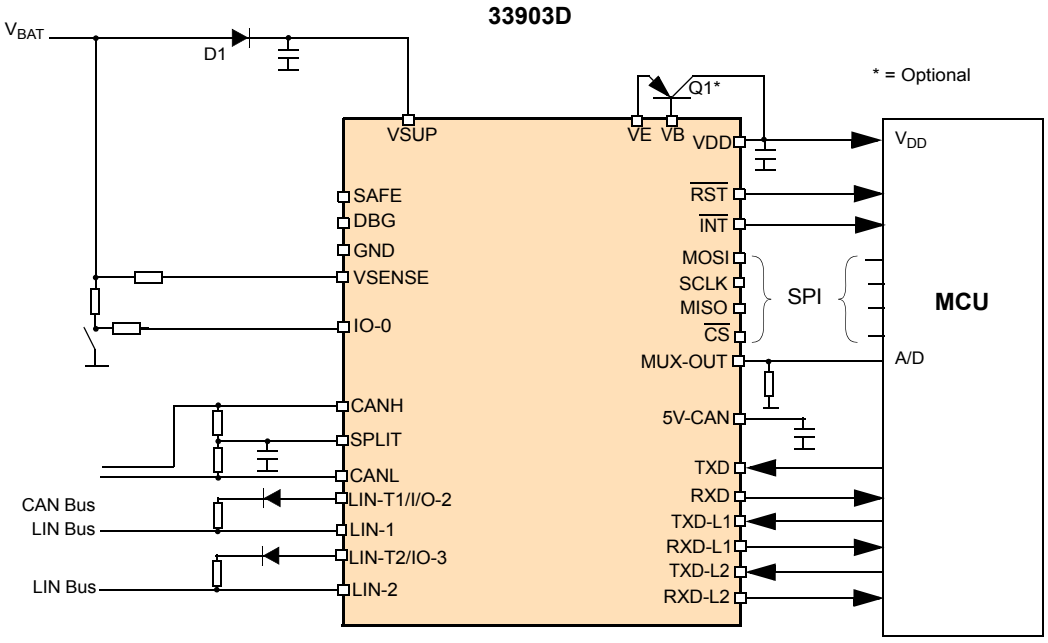


Figure 5. 33903D simplified application diagram

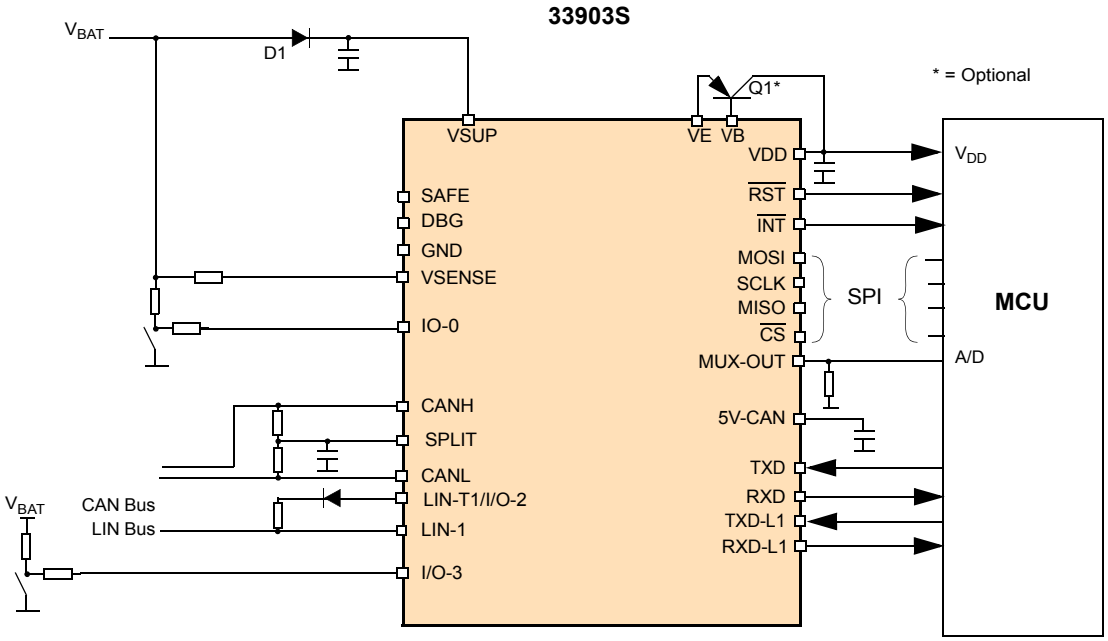


Figure 6. 33903S simplified application diagram

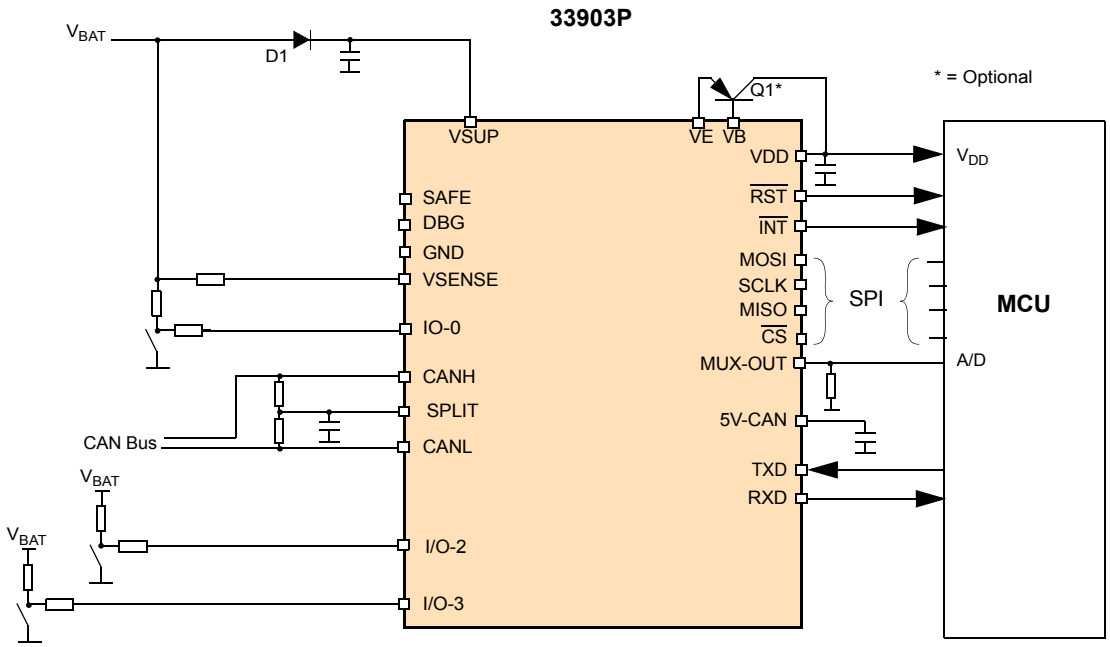


Figure 7. 33903P simplified application diagram

2 Orderable part

Table 1. MC33905 orderable part variations - (all devices rated at T_A = -40 °C TO 125 °C)

NXP part number	Version (1), (2), (3)	V_{DD} output voltage	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
MC33905D (Dual LIN)								
MCZ33905BD3EK/R2	B	3.3 V	2	2 Wake-up + 2 LIN terms or 3 Wake-up + 1 LIN terms or 4 Wake-up + no LIN terms	SOIC 54-pin exposed pad	Yes	Yes	Yes
MCZ33905CD3EK/R2	C							
MCZ33905DD3EK/R2	D							
MCZ33905D5EK/R2		5.0 V						
MCZ33905BD5EK/R2	B							
MCZ33905CD5EK/R2	C							
MCZ33905DD5EK/R2	D							
MC33905S (Single LIN)								
MCZ33905BS3EK/R2	B	3.3 V	1	3 Wake-up + 1 LIN terms or 4 Wake-up + no LIN terms	SOIC 32-pin exposed pad	Yes	Yes	Yes
MCZ33905CS3EK/R2	C							
MCZ33905DS3EK/R2	D							
MCZ33905S5EK/R2		5.0 V						
MCZ33905BS5EK/R2	B							
MCZ33905CS5EK/R2	C							
MCZ33905DS5EK/R2	D							

Notes

1. Design changes in the 'B' version resolved V_{SUP} slow ramp up issues, enhanced device current consumption and improved oscillator stability. 'B' version has an errata linked to the SPI operation.
2. Design changes in the 'C' version resolve the SPI deviation of all prior versions, and does not have the RxD short to ground detection feature.
3. 'C' versions are no longer recommended for new design.
   'D' versions are recommended for new design, and include quality improvement, and has no electrical parameters specification changes.

Table 2. MC33904 orderable part variations - (all devices rated at T_A = -40 °C TO 125 °C)

NXP part number	Version (4), (5), (6)	V_{DD} output voltage	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
MC33904								
MCZ33904B3EK/R2	B	3.3 V	0	4 Wake-up	SOIC 32 pin exposed pad	Yes	Yes	Yes
MCZ33904C3EK/R2	C							
MCZ33904D3EK/R2	D							
MCZ33904A5EK/R2	A	5.0 V						
MCZ33904B5EK/R2	B							
MCZ33904C5EK/R2	C							
MCZ33904D5EK/R2	D							

Notes

4. Design changes in the "B" version resolved V_{SUP} slow ramp up issues, enhanced device current consumption and improved oscillator stability. 'B' version has an errata linked to the SPI operation.
5. Design changes in the "C" version resolve the SPI deviation of all prior versions, and does not have the RxD short to ground detection feature.
6. 'C' versions are no longer recommended for new design.
   'D' versions are recommended for new design, and include quality improvement, and has no electrical parameters specification changes.

Table 3. MC33903 orderable part variations - (all devices rated at T_A = -40 °C TO 125 °C)

NXP part number	Version (8), (9), (10)	V_{DD} output voltage	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
MC33903								
MCZ33903B3EK/R2	B	3.3 V(7)	0	1 Wake-up	SOIC 32 pin exposed pad	No	No	No
MCZ33903C3EK/R2	C							
MCZ33903D3EK/R2	D							
MCZ33903B5EK/R2	B	5.0 V(7)						
MCZ33903C5EK/R2	C							
MCZ33903D5EK/R2	D							
MC33903D (Dual LIN)								
MCZ33903BD3EK/R2	B	3.3 V	2	1 Wake-up + 2 LIN terms or 2 Wake-up + 1 LIN terms or 3 Wake-up + no LIN terms	SOIC 32 pin exposed pad	No	Yes	Yes
MCZ33903CD3EK/R2	C							
MCZ33903DD3EK/R2	D							
MCZ33903BD5EK/R2	B	5.0 V						
MCZ33903CD5EK/R2	C							
MCZ33903DD5EK/R2	D							
MC33903S (Single LIN)								
MCZ33903BS3EK/R2	B	3.3 V	1	2 Wake-up + 1 LIN terms or 3 Wake-up + no LIN terms	SOIC 32 pin exposed pad	No	Yes	Yes
MCZ33903CS3EK/R2	C							
MCZ33903DS3EK/R2	D							
MCZ33903BS5EK/R2	B	5.0 V						
MCZ33903CS5EK/R2	C							
MCZ33903DS5EK/R2	D							
MC33903P								
MCZ33903CP5EK/R2	C	5.0 V	0	3 Wake-up	SOIC 32 pin exposed pad	No	Yes	Yes
MCZ33903DP5EK/R2	D							
MCZ33903CP3EK/R2	C	3.3 V						
MCZ33903DP3EK/R2	D							

Notes

7. V_{DD} does not allow usage of an external PNP on the 33903.
8. Design changes in the ‘B’ version resolved V_{SUP} slow ramp up issues, enhanced device current consumption and improved oscillator stability. ‘B’ version has an errata linked to the SPI operation.
9. Design changes in the “C” version resolve the SPI deviation of all prior versions, and does not have the RxD short to ground detection feature.
10. ’C’ versions are no longer recommended for new design.
’D’ versions are recommended for new design, and include quality improvement, and has no electrical parameters specification changes.

3 Internal block diagrams

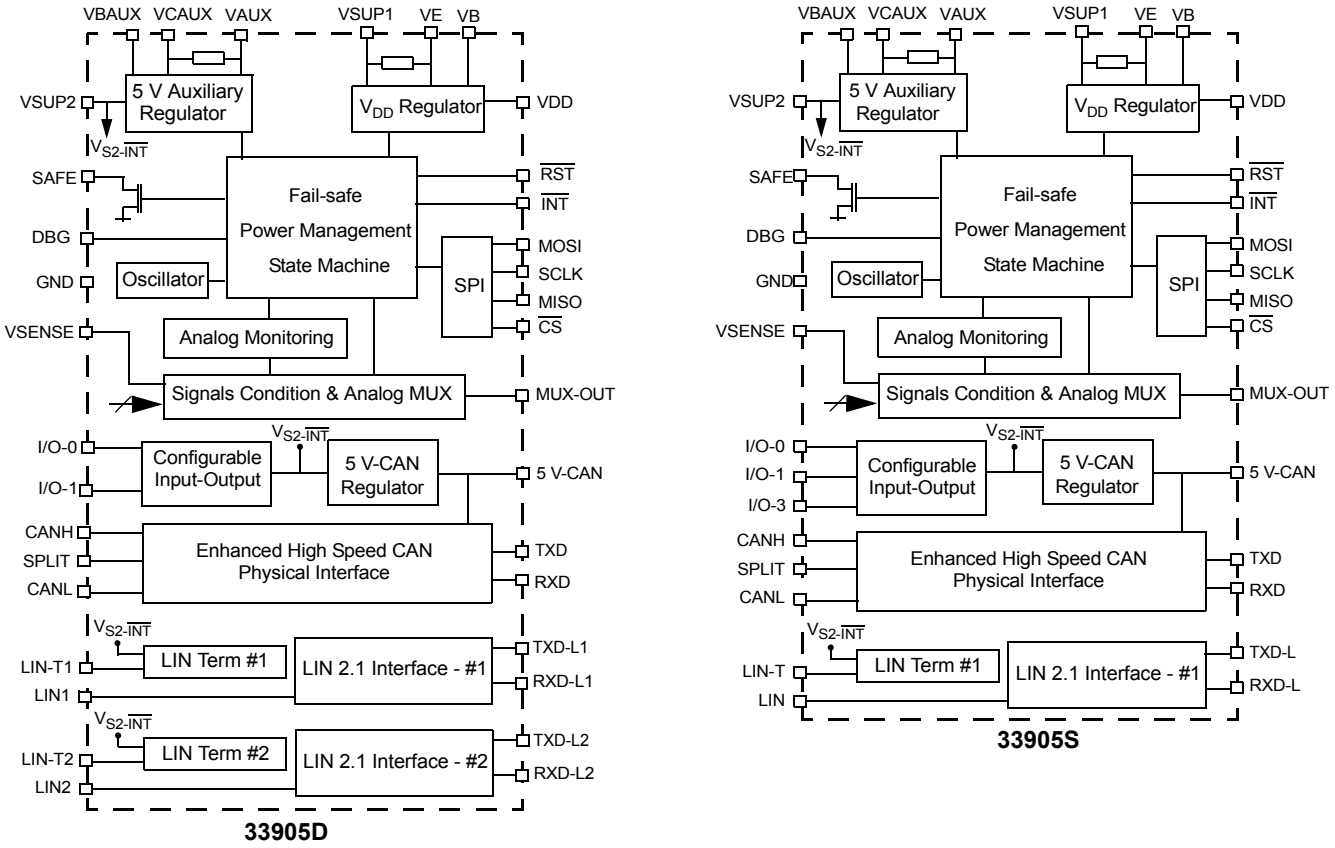


Figure 8. 33905 internal block diagram

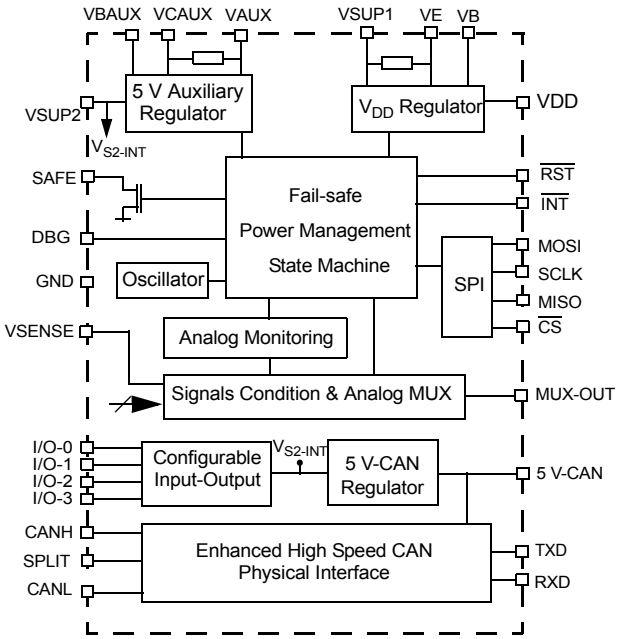


Figure 9. 33904 internal block diagram

33903/4/5

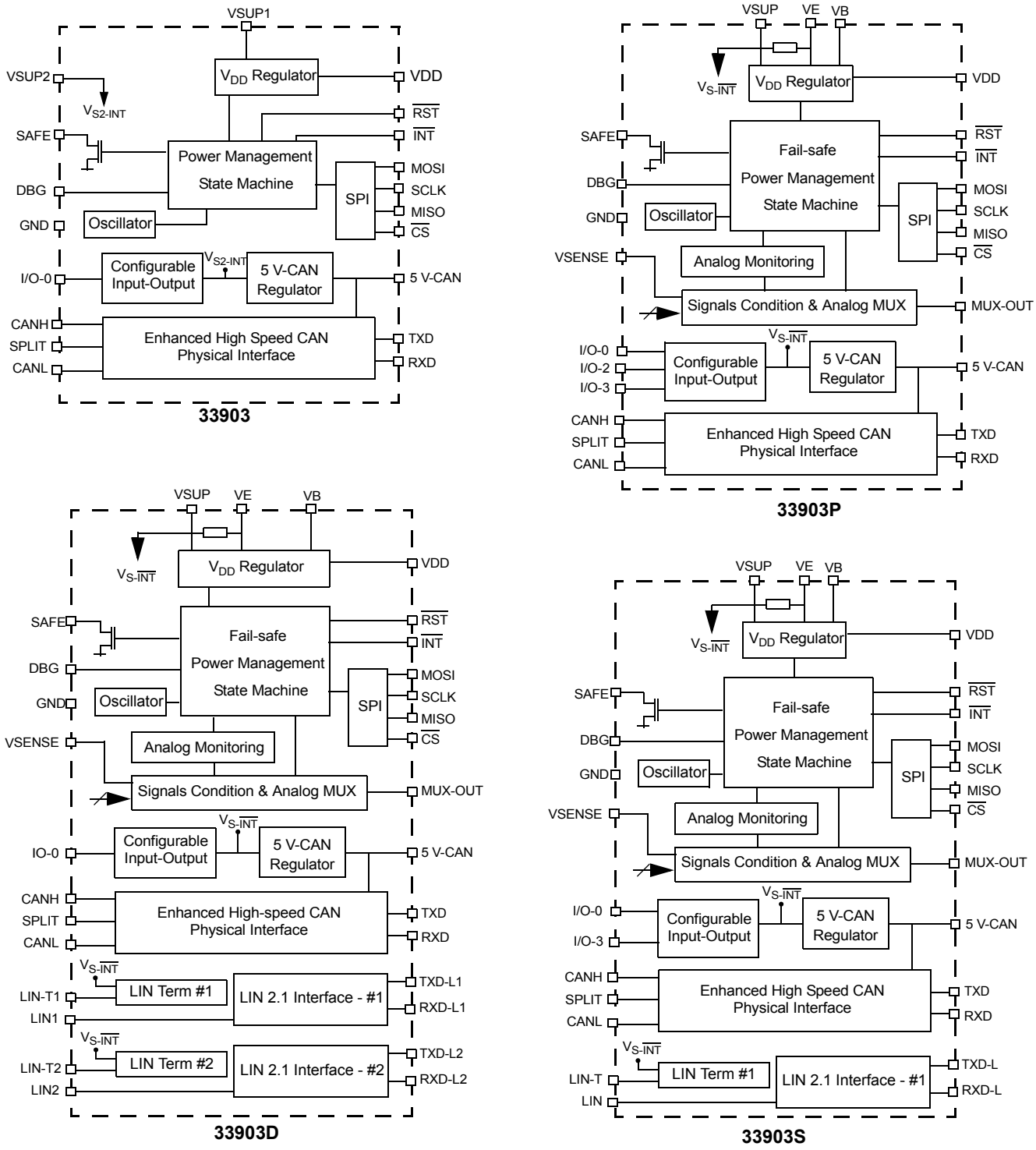
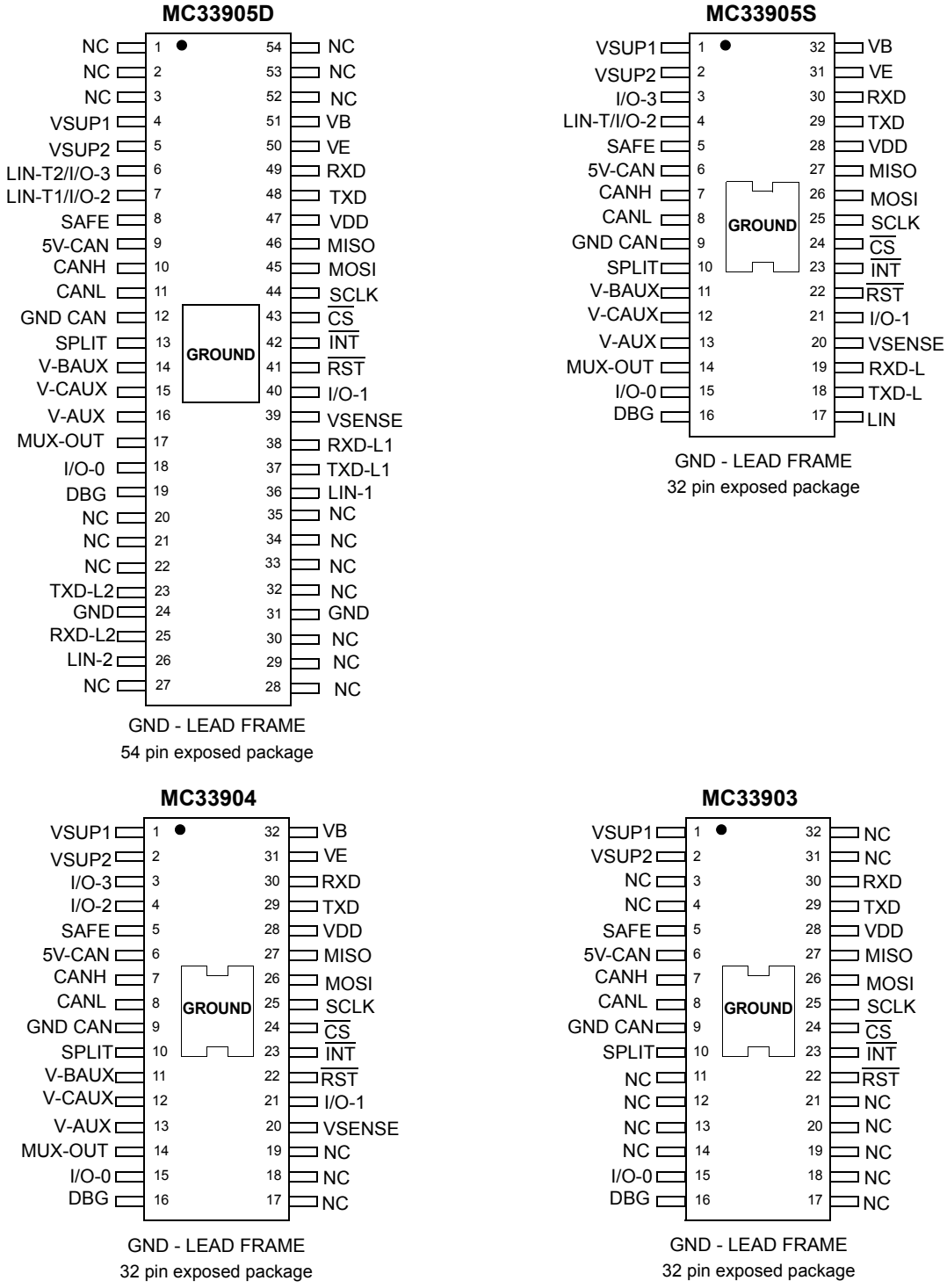


Figure 10. 33903 internal block diagram

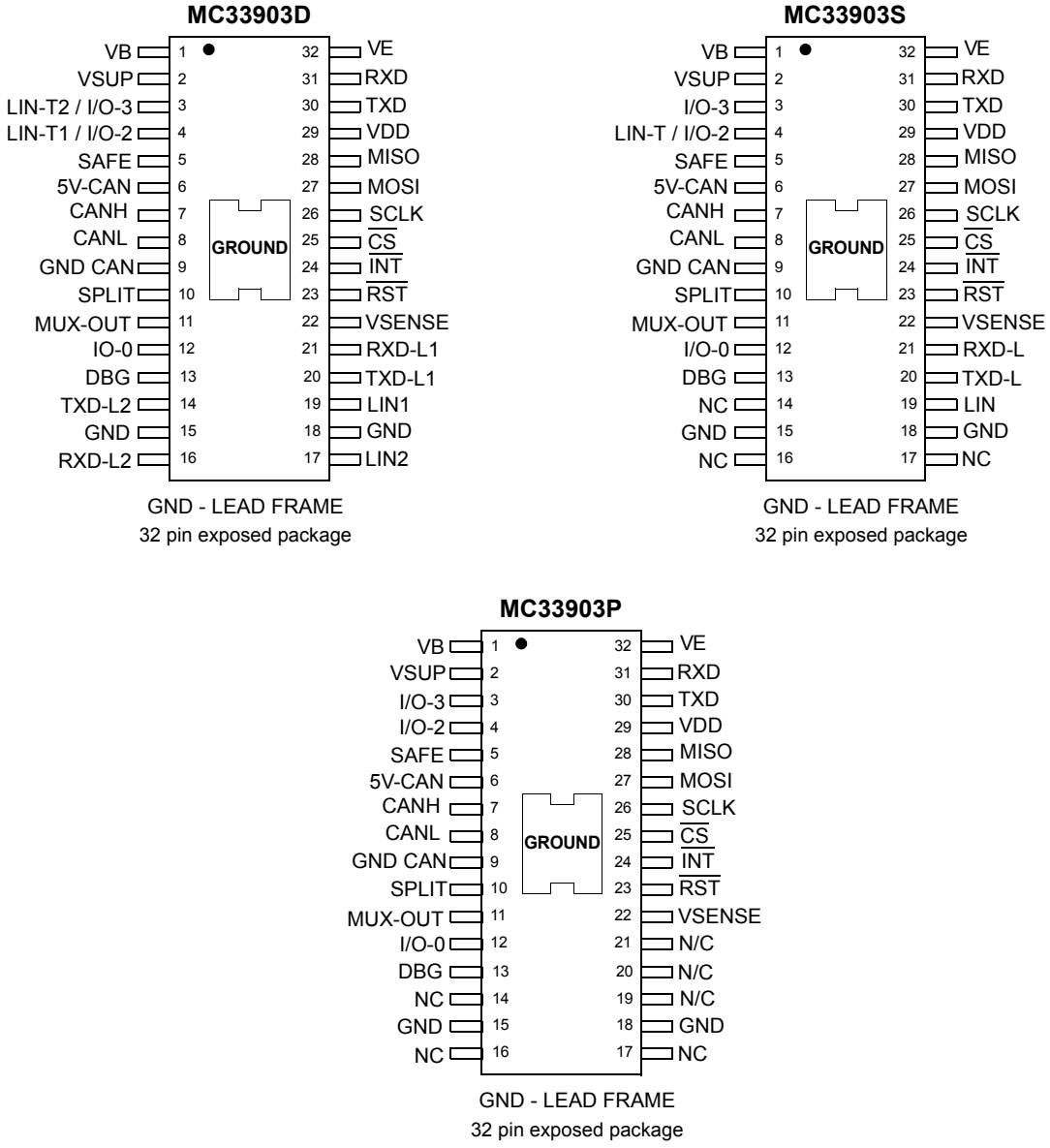
4 Pin Connections

4.1 Pinout diagram



Note: MC33905D, MC33905S, MC33904 and MC33903 are footprint compatible,

Figure 11. 33905D, MC33905S, MC33904 and MC33903 pin connections



Note: MC33903D, MC33903S, and MC33903P are footprint compatible.

Figure 12. 33905D, MC33905S, MC33904 and MC33903 pin connections

4.2 Pin definitions

A functional description of each pin can be found in the Functional pin description section beginning on page 32.

Table 4. 33903/4/5 pin definitions

54 Pin 33905D	32 Pin 33905S	32 Pin 33904	32 Pin 33903	32 Pin 33903D	32 Pin 33903S	32 Pin 33903P	Pin Name	Pin Function	Formal Name	Definition
1-3, 20-22, 27-30, 32-35, 52-54	N/A	17, 18, 19	3-4,11-14, 17-21, 31, 32	N/A	N/A	N/A	N/C	No Connect	-	Connect to GND.
N/A	N/A	N/A	N/A	N/A	14, 16, 17	14, 16, 17, 19-21	N/C	No Connect		**Do NOT connect the N/C pins to GND. Leave these pins Open**.
4	1	1	1	2	2	2	VSUP/1	Power	Battery Voltage Supply 1	Supply input for the device internal supplies, power on reset circuitry and the V_{DD} regulator. VSUP and VSUP1 supplies are internally connected on part number MC33903BDEK and MC33903BSEK
5	2	2	2	N/A	N/A	N/A	VSUP2	Power	Battery Voltage Supply 2	Supply input for 5 V-CAN regulator, V_{AUX} regulator, I/O and LIN pins. VSUP1 and VSUP2 supplies are internally connected on part number MC33903BDEK and MC33903BSEK
6	3	3	N/A	3	3	3	LIN-T2 or I/O-3	Output or Input/ Output	LIN Termination 2 or Input/Output 3	33903D and 33905D - Output pin for the LIN2 master node termination resistor. or 33903P, 33903S, 33903D, 33904, 33905S and 33905D - Configurable pin as an input or HS output, for connection to external circuitry (switched or small load). The input can be used as a programmable Wake-up input in (LP) mode. When used as a HS, no overtemperature protection is implemented. A basic short to GND protection function, based on switch drain-source overvoltage detection, is available.
7	4	4	N/A	4	4	4	LIN-T1 or LIN-T or I/O-2	Output or Input/ Output	LIN Termination 1 or Input/Output 2	33905D - Output pin for the LIN1 master node termination resistor. or 33903P, 33903S, 33903D, 33904, 33905S and 33905D - Configurable pin as an input or HS output, for connection to external circuitry (switched or small load). The input can be used as a programmable Wake-up input in (LP) mode. When used as a HS, no overtemperature protection is implemented. A basic short to GND protection function, based on switch drain-source overvoltage detection, is available.
8	5	5	5	5	5	5	SAFE	Output	Safe Output (Active LOW)	Output of the safe circuitry. The pin is asserted LOW if a fault event occurs (e.g.: software watchdog is not triggered, V_{DD} low, issue on the RST pin, etc.). Open drain structure.
9	6	6	6	6	6	6	5 V-CAN	Output	5V-CAN	Output voltage for the embedded CAN interface. A capacitor must be connected to this pin.
10	7	7	7	7	7	7	CANH	Output	CAN High	CAN high output.
11	8	8	8	8	8	8	CANL	Output	CAN Low	CAN low output.
12	9	9	9	9	9	9	GND-CAN	Ground	GND-CAN	Power GND of the embedded CAN interface
13	10	10	10	10	10	10	SPLIT	Output	SPLIT Output	Output pin for connection to the middle point of the split CAN termination

Table 4. 33903/4/5 pin definitions (continued)

54 Pin 33905D	32 Pin 33905S	32 Pin 33904	32 Pin 33903	32 Pin 33903D	32 Pin 33903S	32 Pin 33903P	Pin Name	Pin Function	Formal Name	Definition
14	11	11	N/A	N/A	N/A	N/A	VBAUX	Output	VB Auxiliary	Output pin for external path PNP transistor base
15	12	12	N/A	N/A	N/A	N/A	VCAUX	Output	VCOLLECTOR Auxiliary	Output pin for external path PNP transistor collector
16	13	13	N/A	N/A	N/A	N/A	VAUX	Output	VOUT Auxiliary	Output pin for the auxiliary voltage.
17	14	14	N/A	11	11	11	MUX-OUT	Output	Multiplex Output	Multiplexed output to be connected to an MCU A/D input. Selection of the analog parameter available at MUX-OUT is done via the SPI. A switchable internal pull-down resistor is integrated for V_{DD} current sense measurements.
18	15	15	15	12	12	12	I/O-0	Input/ Output	Input/Output 0	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable Wake-up input in LP mode. In LP, when used as an output, the High-side (HS) or Low-side (LS) can be activated for a cyclic sense function.
19	16	16	16	13	13	13	DBG	Input	Debug	Input to activate the Debug mode. In Debug mode, no watchdog refresh is necessary. Outside of Debug mode, connection of a resistor between DBG and GND allows the selection of Safe mode functionality.
23	N/A	N/A	N/A	14	N/A	N/A	TXD-L2	Input	LIN Transmit Data 2	LIN bus transmit data input. Includes an internal pull-up resistor to VDD.
24,31	N/A	N/A	N/A	15, 18	15, 18	15, 18	GND	Ground	Ground	Ground of the IC.
25	N/A	N/A	N/A	16	N/A	N/A	RXD-L2	Output	LIN Receive Data	LIN bus receive data output.
26	N/A	N/A	N/A	17	N/A	N/A	LIN2	Input/ Output	LIN bus	LIN bus input output connected to the LIN bus.
36	17	N/A	N/A	19	19	N/A	33903D/5D LIN-1 33903S/5S LIN	Input/ Output	LIN bus	LIN bus input output connected to the LIN bus.
37	18	N/A	N/A	20	20	N/A	33903D/5D TXD-L11 33903S/5S TXD-L	Input	LIN Transmit Data	LIN bus transmit data input. Includes an internal pull-up resistor to VDD.
38	19	N/A	N/A	21	21	N/A	33903D/5D RXD-L1 33903S/5S RXD-L	Output	LIN Receive Data	LIN bus receive data output.
39	20	20	N/A	22	22	22	VSENSE	Input	Sense input	Direct battery voltage input sense. A serial resistor is required to limit the input current during high voltage transients.
40	21	21	N/A	N/A	N/A	N/A	I/O-1	Input/ Output	Input Output 1	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and the MUX output pin. The input can be used as a programmable Wake-up input in (LP) mode. It can be used in association with I/O-0 for a cyclic sense function in (LP) mode.

Table 4. 33903/4/5 pin definitions (continued)

54 Pin 33905D	32 Pin 33905S	32 Pin 33904	32 Pin 33903	32 Pin 33903D	32 Pin 33903S	32 Pin 33903P	Pin Name	Pin Function	Formal Name	Definition
41	22	22	22	23	23	23	$\overline{RST}$	Output	Reset Output (Active LOW)	This is the device reset output whose main function is to reset the MCU. This pin has an internal pull-up to VDD. The reset input voltage is also monitored in order to detect external reset and safe conditions.
42	23	23	23	24	24	24	$\overline{INT}$	Output	Interrupt Output (Active LOW)	This output is asserted low when an enabled interrupt condition occurs. This pin is an open drain structure with an internal pull up resistor to VDD.
43	24	24	24	25	25	25	$\overline{CS}$	Input	Chip Select (Active LOW)	Chip select pin for the SPI. When the $\overline{CS}$ is low, the device is selected. In (LP) mode with V_{DD} ON, a transition on $\overline{CS}$ is a Wake-up condition
44	25	25	25	26	26	26	SCLK	Input	Serial Data Clock	Clock input for the Serial Peripheral Interface (SPI) of the device
45	26	26	26	27	27	27	MOSI	Input	Master Out/ Slave In	SPI data received by the device
46	27	27	27	28	28	28	MISO	Output	Master In/ Slave Out	SPI data sent to the MCU. When the $\overline{CS}$ is high, MISO is high-impedance
47	28	28	28	29	29	29	VDD	Output	Voltage Digital Drain	5.0 or 3.3 V output pin of the main regulator for the Microcontroller supply.
48	29	29	29	30	30	30	TXD	Input	Transmit Data	CAN bus transmit data input. Internal pull-up to VDD
49	30	30	30	31	31	31	RXD	Output	Receive Data	CAN bus receive data output
50	31	31	N/A	32	32	32	VE		Voltage Emitter	Connection to the external PNP path transistor. This is an intermediate current supply source for the V_{DD} regulator
51	32	32	N/A	1	1	1	VB	Output	Voltage Base	Base output pin for connection to the external PNP pass transistor
EX PAD	EX PAD	EX PAD	EX PAD	EX PAD	EX PAD	EX PAD	GND	Ground	Ground	Ground

5 Electrical characteristics

5.1 Maximum ratings

Table 5. Maximum ratings

All voltages are referenced to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings[11]				
$V_{SUP1/2}$ $V_{SUP1/2TR}$	Supply Voltage at VSUP/1 and VSUP2 Normal Operation (DC) Transient Conditions (Load Dump)	 -0.3 to 28 -0.3 to 40	V	
V_{BUSLIN} $V_{BUSLINTR}$	DC voltage on LIN/1 and LIN2 Normal Operation (DC) Transient Conditions (Load Dump)	 -28 to 28 -28 to 40	V	
V_{BUS} V_{BUSTR}	DC voltage on CANL, CANH, SPLIT Normal Operation (DC) Transient Conditions (Load Dump)	 -28 to 28 -32 to 40	V	
V_{SAFE} V_{SAFETR}	DC Voltage at SAFE Normal Operation (DC) Transient Conditions (Load Dump)	 -0.3 to 28 -0.3 to 40	V	
$V_{I/O}$ $V_{I/OTR}$	DC Voltage at I/O-0, I/O-1, I/O-2, I/O-3 (LIN-T Pins) Normal Operation (DC) Transient Conditions (Load Dump)	 -0.3 to 28 -0.3 to 40	V	
V_{DIGLIN}	DC voltage on TXD-L, TXD-L1 TXD-L2, RXD-L, RXD-L1, RXD-L2	-0.3 to V_{DD} +0.3	V	
V_{DIG}	DC voltage on TXD, RXD	-0.3 to V_{DD} +0.3	V	(13)
$V_{\overline{INT}}$	DC Voltage at $\overline{INT}$	-0.3 to 10	V	
$V_{\overline{RST}}$	DC Voltage at $\overline{RST}$	-0.3 to V_{DD} +0.3	V	
$V_{\overline{RST}}$	DC Voltage at MOSI, MSIO, SCLK and $\overline{CS}$	-0.3 to V_{DD} +0.3	V	
V_{MUX}	DC Voltage at MUX-OUT	-0.3 to V_{DD} +0.3	V	
V_{DBG}	DC Voltage at DBG	-0.3 to 10	V	
ILH	Continuous current on CANH and CANL	200	mA	
V_{REG}	DC voltage at VDD, 5V-CAN, VAUX, VCAUX	-0.3 to 5.5	V	
V_{REG}	DC voltage at VBASE and VBAUX	-0.3 to 40	V	(12)
VE	DC voltage at VE	-0.3 to 40	V	(13)
V_{SENSE}	DC voltage at VSENSE	-28 to 40	V	

Notes

11. The voltage on non-VSUP pins should never exceed the V_{SUP} voltage at any time or permanent damage to the device may occur.
12. If the voltage delta between VSUP/1/2 and VBASE is greater than 6.0 V, the external V_{DD} ballast current sharing functionality may be damaged.
13. Potential Electrical Over Stress (EOS) damage may occur if RXD is in contact with VE while the device is ON.

Table 5. Maximum ratings *(continued)*

All voltages are referenced to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
	ESD Capability			
	AECQ100[14]			
	Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
V_{ESD1-1}	CANH and CANL. LIN1 and LIN2, Pins versus all GND pins	±8000		
V_{ESD1-2}	all other Pins including CANH and CANL	±2000		
	Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
V_{ESD2-1}	Corner Pins (Pins 1, 16, 17, and 32)	±750		
V_{ESD2-2}	All other Pins (Pins 2-15, 18-31)	±500		
	Tested per IEC 61000-4-2 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)		V	
V_{ESD3-1}	Device unpowered, CANH and CANL pin without capacitor, versus GND	±15000		
V_{ESD3-2}	Device unpowered, LIN, LIN1 and LIN2 pin, versus GND	±15000		
V_{ESD3-3}	Device unpowered, VS1/VS2 (100 nF to GND), versus GND	±15000		
	Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor on VSUP/1/2 pins (See Typical applications on page 92)			
V_{ESD4-1}	CANH, CANL without bus filter	±9000		
V_{ESD4-2}	LIN, LIN1 and LIN2 with and without bus filter	±12000		
V_{ESD4-3}	I/O with external components (22 k - 10 nF)	±7000		
Thermal ratings				
T_J	Junction temperature	150	°C	
T_A	Ambient temperature	-40 to 125	°C	
T_{ST}	Storage temperature	-50 to 150	°C	
Thermal resistance				
$R_{\theta JA}$	Thermal resistance junction to ambient	50	°C/W	(17)
T_{PPRT}	Peak package reflow temperature during reflow	Note 16	°C	(15), (16)

Notes

14. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Charge Device Model (CDM), and Robotic (C_{ZAP} = 4.0 pF).
15. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
16. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
17. This parameter was measured according to Figure 13:

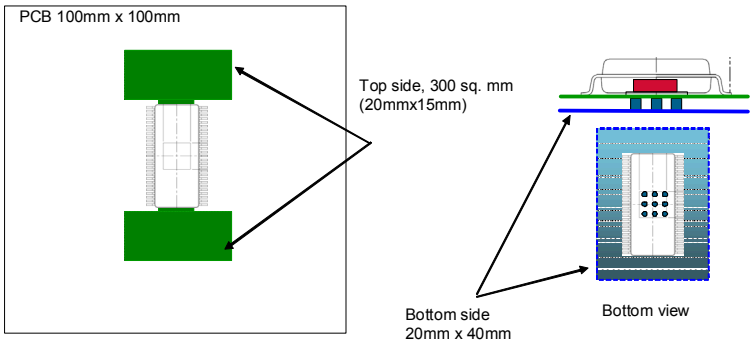


Figure 13. PCB with top and bottom layer dissipation area (dual layer)

5.2 Static electrical characteristics

Table 6. Static electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power input						
V_{SUP1}/V_{SUP2}	Nominal DC Voltage Range	5.5	-	28	V	(18)
V_{SUP1}/V_{SUP2}	Extended DC Low Voltage Range	4.0	-	5.5	V	(19)
V_{S1_LOW}	Undervoltage Detector Thresholds, at the VSUP/1 pin, Low threshold (VSUP/1 ramp down) High threshold (VSUP/1 ramp up) Hysteresis Note: function not active in LP mode	 5.5 - 0.22	 6.0 - 0.35	 6.5 6.6 0.5	V	
V_{S2_LOW}	Undervoltage Detector Thresholds, at the VSUP2 pin: Low threshold (VSUP2 ramp down) High threshold (VSUP2 ramp up) Hysteresis Note: function not active in LP modes	 5.5 - 0.22	 6.0 - 0.35	 6.5 6.6 0.5	V	
V_{S_HIGH}	V_{SUP} Overvoltage Detector Thresholds, at the VSUP/1 pin: Not active in LP modes	16.5	17	18.5	V	
BATFAIL	Battery loss detection threshold, at the VSUP/1 pin.	2.0	2.8	4.0	V	
$V_{SUP-TH1}$	VSUP/1 to turn V_{DD} ON, VSUP/1 rising	-	4.1	4.5	V	
$V_{SUP-TH1HYST}$	VSUP/1 to turn V_{DD} ON, hysteresis (Guaranteed by design)	150	180		mV	
I_{SUP1}	Supply current - from VSUP/1 - from VSUP2, (5V-CAN V_{AUX}, I/O OFF)	 - -	 2.0 0.05	 4.0 0.85	mA	(20), (21)
I_{SUP1+2}	Supply current, I_{SUP1} + I_{SUP2}, Normal mode, V_{DD} ON - 5 V-CAN OFF, V_{AUX} OFF - 5 V-CAN ON, CAN interface in Sleep mode, V_{AUX} OFF - 5 V-CAN OFF, Vaux ON - 5 V-CAN ON, CAN interface in TXD/RXD mode, V_{AUX} OFF, I/O-x disabled	 - - - -	 2.8 - - -	 4.5 5.0 5.5 8.0	mA	
I_{LPM_OFF}	LP mode V_{DD} OFF. Wake-up from CAN, I/O-x inputs V_{SUP} ≤ 18 V, -40 to 25 °C V_{SUP} ≤ 18 V, 125 °C	 - -	 15 -	 35 50	µA	
I_{LPM_ON}	LP mode V_{DD} ON (5.0 V) with V_{DD} undervoltage and V_{DD} overcurrent monitoring, Wake-up from CAN, I/O-x inputs V_{SUP} ≤ 18 V, -40 to 25 °C, I_{DD} = 1.0 µA V_{SUP} ≤ 18 V, -40 to 25 °C, I_{DD} = 100 µA V_{SUP} ≤ 18 V, 125 °C, I_{DD} = 100 µA	 - -	 20 40 -	 - 65 85	µA	
I_{OSC}	LP mode, additional current for oscillator (used for: cyclic sense, forced Wake-up, and in LP V_{DD} ON mode cyclic interruption and watchdog) V_{SUP} ≤ 18 V, -40 to 125 °C	 -	 5.0	 9.0	µA	
V_{DBG}	Debug mode DBG voltage range	8.0	-	10	V	

Notes

18. All parameters in spec (ex: V_{DD} regulator tolerance).
19. Device functional, some parameters could be out of spec. V_{DD} is active, device is not in Reset mode if the lowest V_{DD} undervoltage reset threshold is selected (approx. 3.4 V). CAN and I/Os are not operational.
20. In Run mode, CAN interface in Sleep mode, 5 V-CAN and V_{AUX} turned OFF. I_{OUT} at V_{DD} < 50 mA. Ballast: turned OFF or not connected.
21. VSUP1 and VSUP2 supplies are internally connected on part number MC33903BDEK and MC33903BSEK. Therefore, I_{SUP1} and I_{SUP2} cannot be measured individually.

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V_{DD} Voltage regulator, VDD pin						
$V_{OUT-5.0}$ $V_{OUT-5.0-EMC}$ $V_{OUT-3.3}$	Output Voltage V_{DD} = 5.0 V, V_{SUP} 5.5 to 28 V, I_{OUT} 0 to 150 mA V_{DD} = 5.0 V, under EMC immunity test condition V_{DD} = 3.3 V, V_{SUP} 5.5 to 28 V, I_{OUT} 0 to 150 mA	 4.9 4.9 3.234	 5.0 5.0 3.3	 5.1 5.15 3.4	V	(22)
V_{DROP}	Drop voltage without external PNP pass transistor V_{DD} = 5.0 V, I_{OUT} = 100 mA V_{DD} = 5.0 V, I_{OUT} = 150 mA	 - -	 330 -	 450 500	mV	(23)
V_{DROP-B}	Drop voltage with external transistor I_{OUT} = 200 mA ($I\__{BALLAST}$ + $I\__{INTERNAL}$)	-	350	500	mV	(23)
$V_{SUP1-3.3}$	VSUP/1 to maintain V_{DD} within $V_{OUT-3.3}$ specified voltage range V_{DD} = 3.3 V, I_{OUT} = 150 mA V_{DD} = 3.3 V, I_{OUT} = 200 mA, external transistor implemented	 4.0 4.0	 - -	 - -	V	
K	External ballast versus internal current ratio ($I\__{BALLAST}$ = K x Internal current)	1.5	2.0	2.5		
I_{LIM}	Output Current limitation, without external transistor	150	350	550	mA	
T_{PW}	Temperature pre-warning (Guaranteed by design)	-	140	-	°C	
T_{SD}	Thermal shutdown (Guaranteed by design)	160	-	-	°C	
C_{EXT}	Range of decoupling capacitor (Guaranteed by design)	4.7	-	100	µF	(24)
V_{DDLP}	LP mode V_{DD} ON, I_{OUT} ≤ 50 mA (time limited) V_{DD} = 5.0 V, 5.6 V ≤ V_{SUP} ≤ 28 V V_{DD} = 3.3 V, 5.6 V ≤ V_{SUP} ≤ 28 V	 4.75 3.135	 5.0 3.3	 5.25 3.465	V	
$L_{P-IOUTDC}$	LP mode V_{DD} ON, dynamic output current capability (Limited duration. Ref. to device description).	-	-	50	mA	
L_{P-ITH}	LP V_{DD} ON mode: Overcurrent Wake-up threshold. Hysteresis	 1.0 0.1	 3.0 1.0	 - -	mA	
$L_{P-VDROP}$	LP mode V_{DD} ON, drop voltage, at I_{OUT} = 30 mA (Limited duration. Ref. to device description)	-	200	400	mV	(23)
$L_{P-MINVS}$	LP mode V_{DD} ON, min V_{SUP} operation (Below this value, a V_{DD}, undervoltage reset may occur)	5.5	-	-	V	
V_{DD_OFF}	V_{DD} when V_{SUP} < $V_{SUP-TH1}$, at I_V_{DD} ≤ 10 µA (Guaranteed by design)	-	-	0.3	V	
$V_{DD\_START\ UP}$	V_{DD} when V_{SUP} ≥ $V_{SUP-TH1}$, at I_V_{DD} ≤ 40 mA (Guaranteed with parameter $V_{SUP-TH1}$	3.0	-	-	V	

Notes

22. Guaranteed by design. During immunity tests, according to IEC62132-4, with RF injection applied to CAN or LIN pins. No filter components on CAN or LIN pins. When immunity tests are performed with a CAN filter component (common mode choke) or LIN filter component (capacitor), the V_{DD} specification is 5.0 V ±2%.
23. For 3.3 V V_{DD} devices, the drop-out voltage test condition leads to a V_{SUP} below the min V_{SUP} threshold (4.0 V). As a result, the dropout voltage parameter cannot be specified.
24. The regulator is stable without an external capacitor. Usage of an external capacitor is recommended for AC performance.

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Voltage regulator for CAN interface supply, 5.0 V-CAN pin						
$5V_{-C\ OUT}$	Output voltage, $V_{SUP/2}$ = 5.5 to 40 V I_{OUT} 0 to 160 mA	4.75	5.0	5.25	V	
$5V_{-C\ ILIM}$	Output Current limitation	160	280	-	mA	(25)
$5V_{-C\ UV}$	Undervoltage threshold	4.1	4.5	4.7	V	
$5V_{-CTS}$	Thermal shutdown (Guaranteed by design)	160	-	-	°C	
$C_{EXT-CAN}$	External capacitance (Guaranteed by design)	1.0	-	100	µF	
V auxiliary output, 5.0 and 3.3 V selectable pin VB-Aux, VC-Aux, Vaux						
V_{AUX}	VAUX output voltage V_{AUX} = 5.0 V, V_{SUP} = V_{SUP2} 5.5 to 40 V, I_{OUT} 0 to 150 mA V_{AUX} = 3.3 V, V_{SUP} = V_{SUP2} 5.5 to 40 V, I_{OUT} 0 to 150 mA	 4.75 3.135	 5.0 3.3	 5.25 3.465	V	
$V_{AUX-UVTH}$	VAUX undervoltage detector (VAUX configured to 5.0 V) Low Threshold Hysteresis VAUX undervoltage detector (VAUX configured to 3.3 V, default value)	 4.2 0.06 2.75	 4.5 - 3.0	 4.70 0.12 3.135	V	
$V_{AUX-ILIM}$	VAUX overcurrent threshold detector V_{AUX} set to 3.3 V V_{AUX} set to 5.0 V	 250 230	 360 330	 450 430	mA	
$V_{AUX\ CAP}$	External capacitance (Guaranteed by design)	2.2	-	100	µF	
Undervoltage reset and reset function, $\overline{RST}$ pin						
$V_{RST-TH1}$	V_{DD} undervoltage threshold down - 90% V_{DD} (V_{DD} 5.0 V) V_{DD} undervoltage threshold up - 90% V_{DD} (V_{DD} 5.0 V) V_{DD} undervoltage threshold down - 90% V_{DD} (V_{DD} 3.3 V) V_{DD} undervoltage threshold up - 90% V_{DD} (V_{DD} 3.3 V)	4.5 - 2.75 -	4.65 - 3.0 -	4.85 4.90 3.135 3.135	V	(26), (28) (26), (28)
$V_{RST-TH2-5}$	V_{DD} undervoltage reset threshold down - 70% V_{DD} (V_{DD} 5.0 V)	2.95	3.2	3.45	V	(27), (28)
$V_{RST-HYST}$	Hysteresis for threshold 90% V_{DD}, 5.0 V device for threshold 70% V_{DD}, 5.0 V device Hysteresis 3.3 V V_{DD} for threshold 90% V_{DD}, 3.3 V device	 20 10 10	 - - -	 150 150 150	mV	
V_{RST-LP}	V_{DD} undervoltage reset threshold down - LP V_{DD} ON mode (Note: device change to Normal Request mode). V_{DD} 5.0 V (Note: device change to Normal Request mode). V_{DD} 3.3 V	 4.0 2.75	 4.5 3.0	 4.85 3.135	V	
V_{OL}	Reset V_{OL} @ 1.5 mA, V_{SUP} 5.5 to 28 V	-	300	500	mV	
$I_{RESET\ LOW}$	Current limitation, Reset activated, V_{RESET} = 0.9 x V_{DD}	2.5	7.0	10	mA	
$R_{PULL-UP}$	Pull-up resistor (to VDD pin)	8.0	11	15	kΩ	

Notes

25. Current limitation will be reported by setting a flag.
26. Generate a Reset or an $\overline{INT}$. SPI programmable
27. Generate a Reset
28. In Non-LP modes

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Undervoltage reset and reset function, RST PIN (continued)						
$V_{SUP-RSTL}$	V_{SUP} to guaranteed reset low level	2.5	-	-	V	(29)
$V_{RST-VTH}$	Reset input threshold Low threshold, V_{DD} = 5.0 V High threshold, V_{DD} = 5.0 V Low threshold, V_{DD} = 3.3 V High threshold, V_{DD} = 3.3 V	 1.5 - 0.99 -	 - - - -	 - 3.5 - 2.31	V	
V_{HYST}	Reset input hysteresis	0.5	1.0	1.5	V	
I/O pins when function selected is output						
$V_{I/O-0\ HSDRP}$	I/O-0 HS switch drop @ I = -12 mA, V_{SUP} = 10.5 V	-	0.5	1.4	V	
$V_{I/O-2-3\ HSDRP}$	I/O-2 and I/O-3 HS switch drop @ I = -20 mA, V_{SUP} = 10.5 V	-	0.5	1.4	V	
$V_{I/O-1\ HSDRP}$	I/O-1, HS switch drop @ I = -400 µA, V_{SUP} = 10.5 V	-	0.4	1.4	V	
$V_{I/O-01\ LSDRP}$	I/O-0, I/O-1 LS switch drop @ I = 400 µA, V_{SUP} = 10.5 V	-	0.4	1.4	V	
I_{I/O_LEAK}	Leakage current, I/O-x ≤ V_{SUP}	-	0.1	3.0	µA	
I/O pins when function selected is input						
V_{I/O_NTH}	Negative threshold	1.4	2.0	2.9	V	
V_{I/O_PTH}	Positive threshold	2.1	3.0	3.8	V	
V_{I/O_HYST}	Hysteresis	0.2	1.0	1.4	V	
I_{I/O_IN}	Input current, I/O ≤ VSUP/2	-5.0	1.0	5.0	µA	
$R_{I/O-X}$	I/O-0 and I/O-1 input resistor. I/O-0 (or I/O-1) selected in register, 2.0 V < $V_{I/O-X}$ <16 V (Guaranteed by design).	-	100	-	kΩ	
VSENSE input						
V_{SENSE_TH}	VSENSE undervoltage threshold (Not active in LP modes) Low Threshold High threshold Hysteresis	 8.1 - 0.1	 8.6 - 0.25	 9.0 9.1 0.5	V	
R_{VSENSE}	Input resistor to GND. In all modes except in LP modes. (Guaranteed by design).	-	125	-	kΩ	

Notes

29. Reset must be kept low

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Analog MUX output						
V_{OUT_MAX}	Output Voltage Range, with external resistor to GND >2.0 kΩ	0.0	-	V_{DD} - 0.5	V	
R_{MI}	Internal pull-down resistor for regulator output current sense	0.8	1.9	2.8	kΩ	
C_{MUX}	External capacitor at MUX OUTPUT (Guaranteed by design)	-	-	1.0	nF	(30)
$TEMP_{-COEFF}$	Chip temperature sensor coefficient (Guaranteed by design and device characterization) V_{DD} = 5.0 V V_{DD} = 3.3 V	 20 13.2	 21 13.9	 22 14.6	mv/°C	
V_{TEMP}	Chip temperature: MUX-OUT voltage V_{DD} = 5.0 V, T_A = 125 °C V_{DD} = 3.3 V, T_A = 125 °C	 3.6 2.45	 3.75 2.58	 3.9 2.65	V	
$V_{TEMP(GD)}$	Chip temperature: MUX-OUT voltage (guaranteed by design and characterization) T_A = -40 °C, V_{DD} = 5.0 V T_A = 25 °C, V_{DD} = 5.0 V T_A = -40 °C, V_{DD} = 3.3 V T_A = 25 °C, V_{DD} = 3.3 V	 0.12 1.5 0.07 1.08	 0.30 1.65 0.19 1.14	 0.48 1.8 0.3 1.2	V	
V_{SENSE} GAIN	Gain for V_{SENSE}, with external 1.0 k 1% resistor V_{DD} = 5.0 V V_{DD} = 3.3 V	 5.42 8.1	 5.48 8.2	 5.54 8.3		
V_{SENSE} OFFSET	Offset for V_{SENSE}, with external 1.0 k 1% resistor	-20	-	20	mV	
$V_{SUP/1}$ RATIO	Divider ratio for $V_{SUP/1}$ V_{DD} = 5.0 V V_{DD} = 3.3 V	 5.335 7.95	 5.5 8.18	 5.665 8.45		
VI/O RATIO	Attenuation/Gain ratio for I/O-0 and I/O-1 actual voltage: V_{DD} = 5.0 V, I/O = 16 V (Attenuation, MUX-OUT register bit 3 set to 1) V_{DD} = 5.0 V, (Gain, MUX-OUT register bit 3 set to 0) V_{DD} = 3.3 V, I/O = 16 V (Attenuation, MUX-OUT register bit 3 set to 1) V_{DD} = 3.3 V, (Gain, MUX-OUT register bit 3 set to 0)	 3.8 - 5.6 -	 4.0 2.0 5.8 1.3	 4.2 - 6.2 -		
V_{REF}	Internal reference voltage V_{DD} = 5.0 V V_{DD} = 3.3 V	 2.45 1.64	 2.5 1.67	 2.55 1.7	V	
I_{DD_RATIO}	Current ratio between VDD output & I_{OUT} at MUX-OUT (I_{OUT} at MUX-OUT = I_{DD} out / I_{DD_RATIO}) At I_{OUT} = 50 mA $I_{\_OUT}$ from 25 to 150 mA	 80 62.5	 97 97	 115 117		
SAFE output						
V_{OL}	SAFE low level, at I = 500 µA	0.0	0.2	1.0	V	
$I_{SAFE-IN}$	Safe leakage current (V_{DD} low, or device unpowered). V_{SAFE} 0 to 28 V.	-	0.0	1.0	µA	

Notes

30. When C is higher than CMUX, a serial resistor must be inserted

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Interrupt						
V_{OL}	Output low voltage, I_{OUT} = 1.5 mA	-	0.2	1.0	V	
R_{PU}	Pull-up resistor	6.5	10	14	kΩ	
$V_{OH-LPVDDON}$	Output high level in LP V_{DD} ON mode (Guaranteed by design)	3.9	4.3		V	
V_{MAX}	Leakage current $\overline{INT}$ voltage = 10 V (to allow high-voltage on MCU $\overline{INT}$ pin)	-	35	100	µA	
I_{SINK}	Sink current, $V_{\overline{INT}}$ > 5.0 V, $\overline{INT}$ low state	2.5	6.0	10	mA	
MISO, MOSI, SCLK, $\overline{CS}$ pins						
V_{OL}	Output low voltage, I_{OUT} = 1.5 mA (MISO)	-	-	1.0	V	
V_{OH}	Output high voltage, I_{OUT} = -0.25 mA (MISO)	V_{DD} -0.9	-		V	
V_{IL}	Input low voltage (MOSI, SCLK,$\overline{CS}$)	-	-	0.3 x V_{DD}	V	
V_{IH}	Input high voltage (MOSI, SCLK,$\overline{CS}$)	0.7 x V_{DD}	-	-	V	
I_{HZ}	Tri-state leakage current (MISO)	-2.0	-	2.0	µA	
I_{PU}	Pull-up current ($\overline{CS}$)	200	370	500	µA	
CAN logic input pins (TXD)						
V_{IH}	High Level Input Voltage	0.7 x V_{DD}	-	V_{DD} + 0.3	V	
V_{IL}	Low Level Input Voltage	-0.3	-	0.3 x V_{DD}	V	
I_{PDWN}	Pull-up Current, TXD, V_{IN} = 0 V V_{DD} = 5.0 V V_{DD} = 3.3 V	 -850 -500	 -650 -250	 -200 -175	µA	
CAN data output pins (RXD)						
$VOUT_{LOW}$	Low Level Output Voltage I_{RXD} = 5.0 mA	0.0	-	0.3 x V_{DD}	V	
$VOUT_{HIGH}$	High Level Output Voltage I_{RX} = -3.0 mA	0.7 x V_{DD}	-	V_{DD}	V	
$IOUT_{HIGH}$	High Level Output Current V_{RXD} = V_{DD} - 0.4 V	2.5	5.0	9.0	mA	
$IOUT_{LOW}$	Low Level Input Current V_{RXD} = 0.4 V	2.5	5.0	9.0	mA	

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
CAN output pins (CANH, CANL)						
V_{COM}	Bus pins common mode voltage for full functionality	-12	-	12	V	
$V_{CANH-VCANL}$	Differential input voltage threshold	500	-	900	mV	
$V_{DIFF-HYST}$	Differential input hysteresis	50	-	-	mV	
R_{IN}	Input resistance	5.0	-	50	kΩ	
$R_{IN-DIFF}$	Differential input resistance	10	-	100	kΩ	
$R_{IN-MATCH}$	Input resistance matching	-3.0	0.0	3.0	%	
V_{CANH}	CANH output voltage (45 Ω < R_{BUS} < 65 Ω) TXD dominant state TXD recessive state	 2.75 2.0	 3.5 2.5	 4.5 3.0	V	
V_{CANL}	CANL output voltage (45 Ω < R_{BUS} < 65 Ω) TXD dominant state TXD recessive state	 0.5 2.0	 1.5 2.5	 2.25 3.0	V	
V_{OH}-V_{OL}	Differential output voltage (45 Ω < R_{BUS} < 65 Ω) TXD dominant state TXD recessive state	 1.5 -0.5	 2.0 0.0	 3.0 0.05	V	
I_{CANH}	CAN H output current capability - Dominant state	-	-	-30	mA	
I_{CANL}	CAN L output current capability - Dominant state	30	-	-	mA	
$I_{CANL-OC}$	CANL overcurrent detection - Error reported in register	75	120	195	mA	
$I_{CANH-OC}$	CANH overcurrent detection - Error reported in register	-195	-120	-75	mA	
$R_{INSLEEP}$	CANH, CANL input resistance to GND, device supplied, CAN in Sleep mode, V_CANH, V_CANL from 0 to 5.0 V	5.0	-	50	kΩ	
V_{CANLP}	CANL, CANH output voltage in LP V_{DD} OFF and LP V_{DD} ON modes	-0.1	0.0	0.1	V	
I_{CAN-UN_SUP1}	CANH, CANL input current, VCANH, VCANL = 0 to 5.0 V, device unpowered (VSUP, VDD, 5V-CAN: open).	-	3.0	10	µA	(31)
I_{CAN-UN_SUP2}	CANH, CANL input current, VCANH, VCANL = -2.0 to 7.0 V, device unpowered (VSUP, VDD, 5V-CAN: open).	-	-	250	µA	(31)
$V_{DIFF-R-LP}$	Differential voltage for recessive bit detection in LP mode	-	-	0.4	V	(32)
$V_{DIFF-D-LP}$	Differential voltage for dominant bit detection in LP mode	1.15	-	-	V	(32)
CANH and CANL diagnostic information						
V_{LG}	CANL to GND detection threshold	1.6	1.75	2.0	V	
V_{HG}	CANH to GND detection threshold	1.6	1.75	2.0	V	
V_{LVB}	CANL to VBAT detection threshold, $V_{SUP/1}$ and V_{SUP2} > 8.0 V	-	V_{SUP} -2.0	-	V	
V_{HVB}	CANH to VBAT detection threshold, $V_{SUP/1}$ and V_{SUP2} > 8.0 V	-	V_{SUP} -2.0	-	V	
V_{L5}	CANL to VDD detection threshold	4.0	V_{DD} -0.43	-	V	
V_{H5}	CANH to VDD detection threshold	4.0	V_{DD} -0.43	-	V	

Notes

31. VSUP, VDD, 5V-CAN: shorted to GND, or connected to GND via a 47 k resistor instances are guaranteed by design and device characterization.
32. Guaranteed by design and device characterization.

Table 6. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPLIT						
V_{SPLIT}	Output voltage Loaded condition I_{SPLIT} = ±500 µA Unloaded condition Rmeasure > 1.0 MΩ	 0.3 x V_{DD} 0.45 x V_{DD}	 0.5 x V_{DD} 0.5 x V_{DD}	 0.7 x V_{DD} 0.55 x V_{DD}	V	
I_{LSPLIT}	Leakage current -12 V < V_{SPLIT} < +12 V -22 to -12 V < V_{SPLIT} < +12 to +35 V	 - -	 0.0 -	 5.0 200	µA	
LIN terminals (LIN-T/1, LIN-T2)						
V_{LT_HSDRP}	LIN-T1, LIN-T2, HS switch drop @ I = -20 mA, V_{SUP} > 10.5 V	-	1.0	1.4	V	
LIN1 & LIN2 33903D/5D pin - LIN 33903S/5S pin (parameters guaranteed for $V_{SUP/1}$, V_{SUP2} 7.0 V ≤ V_{SUP} ≤ 18 V)						
V_{BAT}	Operating Voltage Range	8.0	-	18	V	
V_{SUP}	Supply Voltage Range	7.0	-	18	V	
I_{BUS_LIM}	Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	40	90	200	mA	
$I_{BUS\_PAS\_DOM}$	Input Leakage Current at the receiver Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	-1.0	-	-	mA	
$I_{BUS\_PAS\_REC}$	Leakage Output Current to GND Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	-	-	20	µA	
$I_{BUS\_NO\_GND}$	Control unit disconnected from ground (Loss of local ground must not affect communication in the residual network) GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V (Guaranteed by design)	-1.0	-	1.0	mA	
I_{BUSNO_BAT}	V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V (Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition). (Guaranteed by design)	-	-	100	µA	
V_{BUSDOM}	Receiver Dominant State	-	-	0.4	V_{SUP}	
V_{BUSREC}	Receiver Recessive State	0.6	-	-	V_{SUP}	
V_{BUS_CNT}	Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	0.475	0.5	0.525	V_{SUP}	
V_{HYS}	Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	-	-	0.175	V_{SUP}	
V_{BUSWU}	LIN Wake-up threshold from LP V_{DD} ON or LP V_{DD} OFF mode	-	5.3	5.8	V	
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	30	60	kΩ	
T_{LINSD}	Overtemperature Shutdown (Guaranteed by design)	140	160	180	°C	
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis (Guaranteed by design)	-	10	-	°C	