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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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RoHS

Three-Phase Field Effect Transistor Pre-Driver

33927

FET PRE-DRIVER

EK SUFFIX (Pb-FREE)
98ASA99334D
54-PIN SOICW-EP

The 33927 is a Field Effect Transistor (FET) pre-driver designed for three-phase motor control and similar applications. The integrated circuit (IC) uses *SMARTMOS™* technology.

The IC contains three high-side FET pre-drivers and three low-side FET pre-drivers.Three external bootstrap capacitors provide gate charge to the high side FETs.

The IC interfaces to a MCU via six direct input control signals, a SPI port for device setup and asynchronous reset, enable and interrupt signals. Both 5.0V and 3.0V logic level inputs are accepted and 5.0V logic level outputs are provided.

Features

- Fully specified from 8.0V to 40V covers 12V and 24V automotive systems
- Extended operating range from 6.0V to 58V covers 12V and 42V systems
- 1.0A gate drive capability with protection
- Protection against reverse charge injection from CGD and CGS of external FETs
- Includes a charge pump to support full FET drive at low battery voltages
- Deadtime is programmable via the SPI port
- Simultaneous output capability enabled via safe SPI command
- Pb-Free Packaging Designated by Suffix Code EK

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MCZ33927EK/R2	-40°C to 125°C	54 SOICW-EP

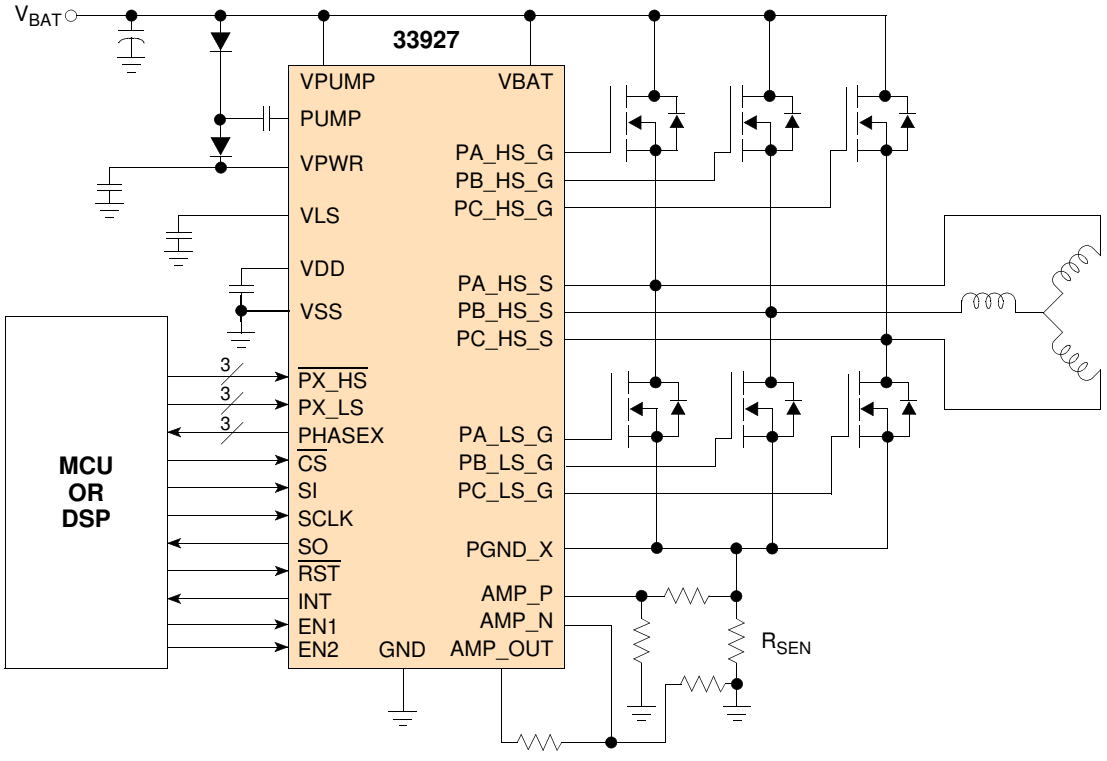

Figure 1. 33927 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

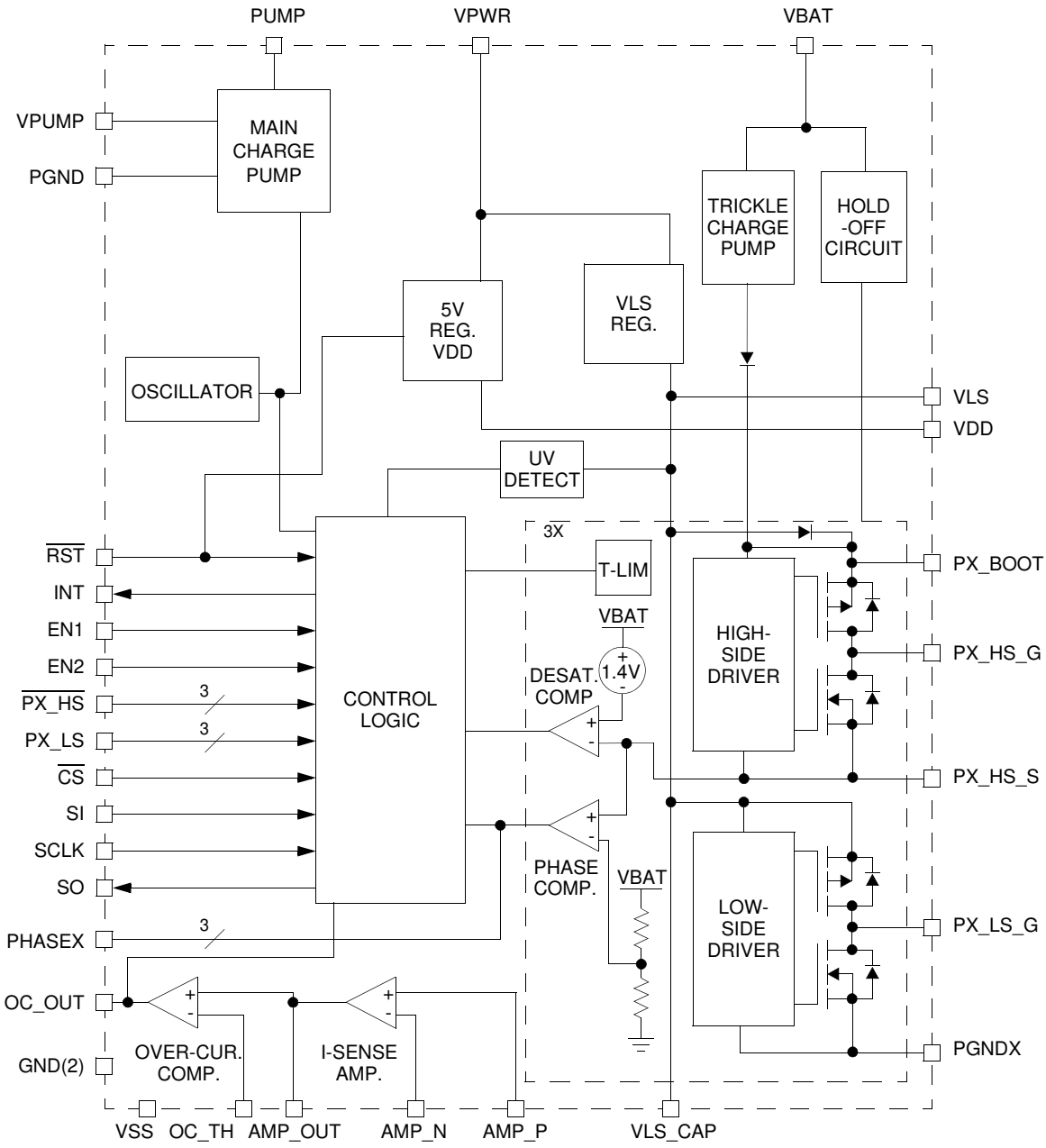

Figure 2. 33927 Simplified Internal Block Diagram

PIN CONNECTIONS

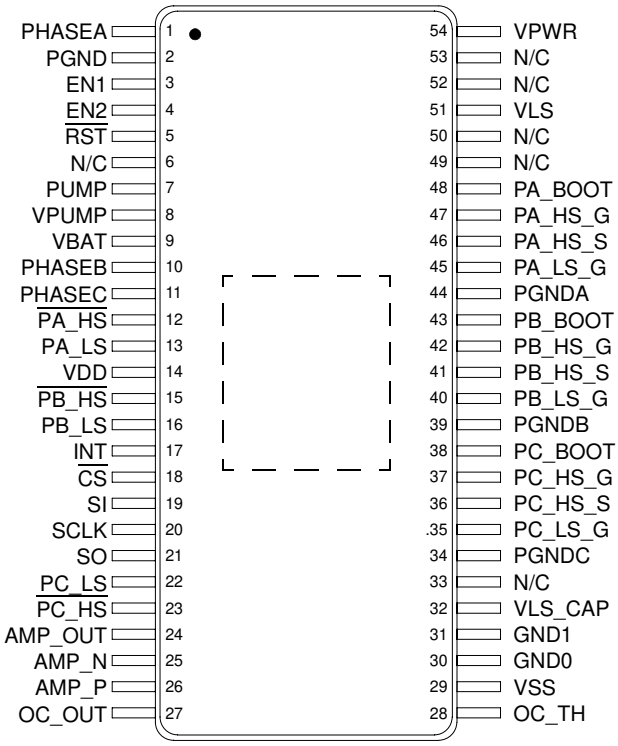

Figure 3. 33927 Pin Connections

Table 1. 33927 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin	Pin Name	Pin Function	Formal Name	Definition
1	PHASEA	Digital Output	Phase A	Totem Pole output of Phase A comparator. This output is low when the voltage on PA_HS_S (Source of High-Side FET) is less than 50% of VBAT
2	PGND	Ground	Power Ground	Power ground for charge pump
3	EN1	Digital Input	Enable 1	Logic signal input must be high (ANDed with EN2) to enable any gate drive output.
4	EN2	Digital Input	Enable 2	Logic signal input must be high (ANDed with EN1) to enable any gate drive output
5	$\overline{\text{RST}}$	Digital Input	Reset	Reset input
6, 33, 49, 50, 52, 53	N/C	–	No Connect	These pins do not connect
7	PUMP	Power Drive Out	Pump	Charge pump output
8	VPUMP	Power Input	Voltage Pump	Charge pump supply
9	VBAT	Digital Input	Voltage Battery	Battery supply
10	PHASEB	Digital Output	Phase B	Totem Pole output of Phase B comparator. This output is low when the voltage on PB_HS_S (Source of High-Side FET) is less than 50% of VBAT
11	PHASEC	Digital Output	Phase C	Totem Pole output of Phase C comparator. This output is low when the voltage on PC_HS_S (Source of High-Side FET) is less than 50% of VBAT

Table 1. 33927 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin	Pin Name	Pin Function	Formal Name	Definition
12	$\overline{\text{PA\_HS}}$	Digital Input	Phase A High-Side	Active low input logic signal enables the High-Side Driver for Phase A
13	PA_LS	Digital Input	Phase A Low-Side	Active high input logic signal enables the Low-Side Driver for Phase A
14	VDD	Analog Output	VDD Regulator	VDD regulator output. Internally generated 5V supply
15	$\overline{\text{PB\_HS}}$	Digital Input	Phase B High-Side	Active low input logic signal enables the High-Side Driver for Phase B
16	PB_LS	Digital Input	Phase B Low-Side	Active high input logic signal enables the Low-Side Driver for Phase B
17	INT	Digital Output	Interrupt	Interrupt pin output
18	$\overline{\text{CS}}$	Digital Input	Chip Select	Chip Select input. It frames SPI commands and enables SPI port
19	SI	Digital Input	Serial In	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
20	SCLK	Digital Input	Serial Clock	Clock for SPI port and typically is 3.0 MHz
21	SO	Digital Output	Serial Out	Output data for SPI port. Tri-state until $\overline{\text{CS}}$ becomes low
22	PC_LS	Digital Input	Phase C Low-Side	Active high input logic signal enables the Low-Side Driver for Phase C
23	$\overline{\text{PC\_HS}}$	Digital Input	Phase C High-Side	Active low input logic signal enables the High-Side Driver for Phase C
24	AMP_OUT	Analog Output	Amplifier Output	Output of the current-sensing amplifier
25	AMP_N	Analog Input	Amplifier Invert	Inverting input of the current-sensing amplifier
26	AMP_P	Analog Input	Amplifier Non-Invert	Non-inverting input of the current-sensing amplifier
27	OC_OUT	Digital Output	Overcurrent Out	Totem pole digital output of the Over-current Comparator
28	OC_TH	Analog Input	Overcurrent Threshold	Threshold of the overcurrent detector
29	VSS	Ground	Voltage Source Supply	Ground reference for logic interface and power supplies
30, 31	GND	Ground	Ground	Substrate and ESD reference, connect to VSS
32	VLS_CAP	Analog Output	VLS Regulator Output Capacitor	VLS Regulator connection for additional output capacitor, providing low impedance supply source for Low-Side Gate Drive
34	PGNDC	Power Input	Phase C Return	Gate current return for the Low-Side FETs for Phase C gate current
35	PC_LS_G	Power Output	Phase C Low-Side Gate Drive	Gate drive output for Phase C Low-Side
36	PC_HS_S	Power Input	Phase C High-Side Source	Source connection for Phase C High-Side FET
37	PC_HS_G	Power Output	Phase C High-Side Gate Drive	Gate Drive for output Phase C High-Side FET
38	PC_BOOT	Analog Input	Phase C Bootstrap	Bootstrap capacitor for Phase C
39	PGNDB	Power Input	Phase B Return	Gate current return for the Low-Side FETs for Phase B
40	PB_LS_G	Power Output	Phase B Low-Side Gate Drive	Gate Drive for output Phase B Low-Side
41	PB_HS_S	Power Input	Phase B High-side Source	Source connection for Phase B High-Side FET
42	PB_HS_G	Power Output	Phase B High-Side Gate Drive	Gate Drive for output Phase B High-Side
43	PB_BOOT	Analog Input	Phase B Bootstrap	Bootstrap capacitor for Phase B
44	PGNDA	Power Input	Phase A Return	Gate current return for the Low-Side FETs for Phase A
45	PA_LS_G	Power Output	Phase A Low-Side Gate Drive	Gate Drive for output Phase A Low-Side

Table 1. 33927 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Pin	Pin Name	Pin Function	Formal Name	Definition
46	PA_HS_S	Power Input	Phase A High-Side Source	Source connection for Phase A High-Side FET
47	PA_HS_G	Power Output	Phase A High-Side Gate Drive	Gate Drive for output Phase A High-Side
48	PA_BOOT	Analog Input	Phase A Bootstrap	Bootstrap capacitor for Phase A
51	VLS	Analog Output	VLS Regulator	VLS regulator output. Power supply for the gate drives
54	VPWR	Power Input	Voltage Power	Power supply input for gate drives
	EP	Ground	Exposed Pad	Device will perform as specified with the Exposed Pad un-terminated (floating) however, it is recommended that the Exposed Pad be terminated to pin 29 (VSS) and system ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
VBAT Supply Voltage Normal Operation (Steady-State) Transient Survival(1)	V_{BAT}	 58 -1.5 to 80	V
VPWR Supply Voltage Normal Operation (Steady-State) Transient Survival(1)	V_{PWR}	 58 -1.5 to 80	V
Charge Pump (PUMP, VPUMP)	V_{PUMP}	-0.3 to 40	V
VLS Regulator Outputs (VLS, VLS_CAP)	V_{LS}	-0.3 to 18	V
Logic Supply Voltage	V_{DD}	-0.3 to 7.0	V
Logic Output (INT, SO, PHASEA, PHASEB, PHASEC, OC_OUT)(2)	V_{OUT}	-0.3 to 7.0	V
Logic Input Pin Voltage (EN1, EN2, $\overline{Px\_HS}$, Px_LS, SI, SCLK, $\overline{CS}$, $\overline{RST}$) 10mA	V_{IN}	-0.3 to 7.0	V
Amplifier Input Voltage (Both Inputs-GND), (AMP_P - GND) or (AMP_N - GND) 6mA source or sink	V_{IN_A}	 -7.0 to 10.0	V
Over-current comparator threshold 10mA	V_{OC}	-0.3 to 7.0	V
Driver Output Voltage(3) High-Side bootstrap (PA_BOOT, PB_BOOT, PC_BOOT) High-Side (PA_HS_G, PB_HS_G, PC_HS_G) Low-Side (PA_LS_G, PB_LS_G, PC_LS_G)	 V_{BOOT} V_{HS_G} V_{LS_G}	 75 75 16	V
Driver Voltage Transient Survival High-Side (PA_HS_G, PB_HS_G, PC_HS_G, PA_HS_S, PB_HS_S, PC_HS_S) Low-Side (PA_LS_G, PB_LS_G, PC_LS_G, PGNDA, PGNDB, PGNDC)	 V_{HS_G} V_{HS_S} V_{LS_G} V_{PGND}	 -7.0 -7.0 -7.0 -7.0	V
Continuous Output Current	I_{GATE}	-0.1 to 0.1	A
ESD Voltage(4) Human Body Model - HBM (All pins except for the pins listed below) Pins: PA_Boot, PA_HS_S, PA_HS_G, PB_Boot, PB_HS_S, PB_HS_G, PC_Boot, PC_HS_S, PC_HS_G, VPWR Charge Device Model - CDM	V_{ESD}	 ±2000 ±1000 ±750	V

Notes

1. The device will withstand load dump transient as defined by ISO7637 with peak voltage of 80V.
2. Short-circuit proof, the device will not be damaged or induce unexpected behavior due to shorts to external sources within this range.
3. This voltage should not be applied without also taking voltage at HS_S and voltage at PGND_x into account.
4. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100pF, R_{ZAP} = 1500Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Thermal Resistance[5] Junction-to-Case	$R_{\theta JC}$	3.0	°C/W
Soldering Temperature[6]	T_{SOLDER}	Note 7	°C

Notes

5. Case is considered EP - pin 55 under the body of the device. The actual power dissipation of the device is dependent on the operating mode, the heat transfer characteristics of the board and layout and the operating voltage. See Figure 19 and Figure 20 for examples of power dissipation profiles of two common configurations. Operation above the maximum operating junction temperature will result in a reduction in reliability leading to malfunction or permanent damage to the device.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS					
VBAT Supply Voltage Startup Threshold[8]	V_{BAT_ST}	–	6.0	8.0	V
VBAT Supply Current, V_{PWR} = V_{BAT} = 40V $\overline{RST}$ and ENABLE = 5.0V No output loads on Gate Drive Pins, No PWM No output loads on Gate Drive Pins, 20kHz, 50% Duty Cycle	I_{BAT}	 – –	 1.0 –	 – 10	mA
VPWR Supply Current, V_{PWR} = V_{BAT} = 40V $\overline{RST}$ and ENABLE = 5.0V No output loads on Gate Drive Pins, No PWM Output Loads = 620nC per FET, 20kHz PWM[9]	I_{PWR_ON}	 – –	 11 –	 20 95	mA
Sleep State Supply Current, $\overline{RST}$ = 0V V_{BAT} = 40V V_{PWR} = 40V	 I_{BAT} I_{PWR}	 – –	 14 56	 30 100	µA
Sleep State Output Gate Voltage IG < 100µA	V_{GATESS}	–	–	1.3	V
Trickle Charge Pump (Bootstrap Voltage) V_{BAT} = 14V	V_{Boot}	22	28	32	V
Bootstrap Diode Forward Voltage at 10mA	V_F	–	–	1.2	V
VDD V INTERNAL REGULATOR					
V_{DD} Output Voltage, V_{PWR} = 8V to 40V, C = 0.47µF[10] External Load I_{DD_EXT} = 0 to 1.0mA	V_{DD}	4.5	–	5.5	V
Internal V_{DD} Supply Current, V_{DD} = 5.5V, No External Load	I_{DD}	–	–	12	mA
VLS REGULATOR					
Peak Output Current, V_{PWR} = 16V, V_{LS} = 10V	I_{PEAK}	350	600	800	mA
Linear Regulator Output Voltage, I_{VLS} = 0 to 60mA[11]	V_{LS}	13.5	15	17	V
VLS Disable Threshold[12]	V_{THVLS}	7.5	8.0	8.5	V

Notes

8. When minimum system voltage could be less than 14V operation with the Charge Pump is recommended. V_{BAT} must exceed this threshold in order for the Charge Pump and V_{DD} regulator to startup and drive V_{PWR} to > 8.0V. Once V_{PWR} exceeds 8.0V, the circuits will continue to operate even if V_{BAT} drops below 6.0V.
9. This parameter is guaranteed by design. It is not production tested.
10. Minimum external capacitor for stable V_{DD} operation is 0.47µF.
11. Recommended external capacitor for the V_{LS} regulator is 2.2µF low ESR at each pin VLS and VLS_CAP.
12. When V_{LS} is less than this value, the outputs are disabled and HOLDOFF circuits are active.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHARGE PUMP					
Charge Pump					
High-Side Switch On-Resistance	$R_{DS(on)\_HS}$	–	6.0	10	Ω
Low-Side Switch On-Resistance	$R_{DS(on)\_LS}$	–	5.0	9.4	Ω
Regulation Threshold Difference[13][15]	V_{THREG}	250	500	900	mV
Charge Pump Output Voltage[14], [15]	V_{CP}				V
I_{OUT} = 40mA, 6.0V < V_{BAT} < 8.0V		8.5	9.5	–	
I_{OUT} = 40mA, V_{BAT} > = 8.0V		12	–	–	
GATE DRIVE					
High-Side Driver On-Resistance (Sourcing)	$R_{DS(on)\_H\_SRC}$				Ω
V_{PWR} = V_{BAT} = 16V, -40°C ≤ T_A ≤ 25°C		–	–	6.0	
V_{PWR} = V_{BAT} = 16V, 25°C < T_A ≤ 125°C		–	–	8.5	
High-Side Driver On-Resistance (Sinking)	$R_{DS(on)\_H\_SINK}$				Ω
V_{PWR} = V_{BAT} = 16V		–	–	3.0	
High-Side Current Injection Allowed Without Malfunction[15], [16]	I_{HS_INJ}	–	–	0.5	A
Low-Side Driver On-Resistance (Sourcing)	$R_{DS(on)\_L\_SRC}$				Ω
V_{PWR} = V_{BAT} = 16V, -40°C ≤ T_A ≤ 25°C		–	–	6.0	
V_{PWR} = V_{BAT} = 16V, 25°C < T_A ≤ 125°C		–	–	8.5	
Low-Side Driver On-Resistance (Sinking)	$R_{DS(on)\_L\_SINK}$	–	–	3.0	Ω
V_{PWR} = V_{BAT} = 16 V					
Low-Side Current Injection Allowed Without Malfunction[15], [16]	I_{LS_INJ}	–	–	0.5	A
Gate Source Voltage, V_{PWR} = V_{BAT} = 40V					V
High-Side, I_{GATE} = 0[17]	V_{GS_H}	13	14.8	16.5	
Low-Side, I_{GATE} = 0	V_{GS_L}	13	15.4	17	
High-Side Gate Drive Output Leakage Current, Per Output[18]	I_{HS_LEAK}	–	–	18	µA

Notes

13. When VLS is this amount below the normal VLS linear regulation threshold, the pump is enabled.
14. With recommended external components (1.0µF, MUR 120 diode). The Charge Pump is designed to supply the gate currents of a system with 100A FETs in a 12V application.
15. This parameter is a design characteristic, not production tested.
16. Current injection only occurs during output switch transitions. The IC is immune to specified injected currents for a duration of approximately 1 µs after an output switch transition. 1 µs is sufficient for all intended applications of this IC.
17. If a slightly higher gate voltage is required, larger bootstrap capacitors are required. At high duty cycles, the bootstrap voltage may not recover completely, leading to a higher output on-resistance. This effect can be minimized by using low ESR capacitors for the bootstrap and the VLS capacitors.
18. A small internal charge pump will supply up to 30 µA nominal to compensate for leakage on the high-side FET gate output and maintain voltages after bootstrap events. It is not intended for external components to be connected to the High-Side FET gate, but small amounts of additional leakage can be accommodated.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVERCURRENT COMPARATOR					
Common Mode Input Range	V_{CM}	2.0	–	V_{DD}-0.02	V
Input Offset Voltage	V_{OS_OC}	-50	–	50	mV
Overcurrent Comparator Threshold Hysteresis[19]	V_{OC_HYST}	50		300	mV
Output Voltage High-Level at I_{OH} = -500µA Low-Level at I_{OL} = 500µA	 V_{OH} V_{OL}	 0.85 V_{DD} –	 – –	 V_{DD} 0.5	V
HOLD OFF CIRCUIT					
V_{DD} Threshold (V_{DD} Falling) $\overline{RST}$ pin High	V_{DD_TH}	1.5	–	4.0	V
Hold Off Current (At Each GATE Pin) 3.0V < V_{BAT} < 40V[20]	I_{HOLD}	10	–	300	µA
PHASE COMPARATOR					
High-Level Input Voltage Threshold	V_{IH_TH}	0.5 V_{BAT}	–	0.65 V_{BAT}	V
Low-Level Input Voltage Threshold	V_{IL_TH}	0.3 V_{BAT}	–	0.45 V_{BAT}	V
High-Level Output Voltage at I_{OH} = -500µA	V_{OH}	0.85 V_{DD}	–	V_{DD}	V
Low-Level Output Voltage at I_{OL} = 500µA	V_{OL}	–	–	0.5	V
High-Side Source Input Resistance[19], [23]	R_{IN}	–	50	–	kΩ
DESATURATION DETECTOR					
Desaturation Detector Threshold[21]	V_{DES_TH}	1.2	1.4	1.6	V
CURRENT SENSE AMPLIFIER					
Recommended External Series Resistor (See Figure 9)	R_S	–	1.0	–	kΩ
Recommended External Feedback Resistor (See Figure 9) Limited by the Output Voltage Dynamic Range	R_{FB}	5.0	–	15	kΩ
Maximum Input Differential Voltage (See Figure 9) V_{ID} = V_{AMP_P} - V_{AMP_N}	V_{ID}	-800	–	+800	mV
Input Common Mode Range[19], [22]	V_{CM}	0	–	3.0	V
Input Offset Voltage R_S = 1kΩ, V_{CM} = 0.0V	V_{OS}	-15	–	+15	mV
Input Offset Voltage Drift[19]	$\delta V_{OS}/\delta T$	–	-10	–	µV/°C
Input Bias Current V_{CM} = 2.0V	I_b	-200	–	+200	nA

Notes

19. This parameter is a design characteristic, not production tested.
20. The hold off circuit is designed to operate over the full operating range of V_{BAT}. The specification indicates the conditions used in production test.
21. Desaturation is measured as the voltage drop below V_{BAT}, thus the threshold is compared to the drain-source voltage of the external high-side FET. See Figure 5.
22. As long as one input is within V_{CM} the output is guaranteed to have the correct phase. Exceeding the common mode rails will not cause a phase inversion on the output.
23. Input resistance is impedance from high-side source and is referenced to ground. Approximate tolerance is ±20%.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER (CONTINUED)					
Input Offset Current I_{OS} = I_{AMP_P} - I_{AMP_N}	I_{OS}	-80	–	+80	nA
Input Offset Current Drift (24)	$\delta I_{OS}/\delta T$	–	40	–	pA/°C
Output Voltage High-Level with R_{LOAD} = 10 kΩ to V_{SS} Low-Level with R_{LOAD} = 10 kΩ to V_{DD}	 V_{OH} V_{OL}	 V_{DD}-0.2 –	 – –	 V_{DD} 0.2	V
Differential Input Resistance	R_I	1.0	–	–	MΩ
Output Short Circuit Current	I_{SC}	5.0	–	–	mA
Common-Mode Input Capacitance at 10 kHz (24)(25)	C_I	–	–	10	pF
Common-Mode Rejection Ratio at DC CMRR = 20*Log ((V_{OUT_diff}/V_{IN_diff}) * (V_{IN_CM}/V_{OUT_CM}))	CMRR	60	80	–	dB
Large Signal Open Loop Voltage Gain (DC) (24)(25)	A_{OL}	–	60	–	dB
Gain Margin at Gain = 5.0 (24)(25)	A_M	–	5.0	–	dB
Nonlinearity (24)(25) RL = 1kΩ, C_L = 500pF, 0.3 < V_O < 4.8V, Gain = 5.0 to 15	NL	-1.0	–	+1.0	%

Notes

24. This parameter is a design characteristic, not production tested.
25. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPERVISORY AND CONTROL CIRCUITS					
Logic Inputs (Px_LS, $\overline{Px\_HS}$, EN1, EN2) [27]					V
High-Level Input Voltage Threshold	V_{IH}	–	–	2.1	
Low-Level Input Voltage Threshold	V_{IL}	0.9	–	–	
Logic Inputs (SI, SCLK, $\overline{CS}$) [26], [27]					V
High-Level Input Voltage Threshold	V_{IH}	–	–	2.1	
Low-Level Input Voltage Threshold	V_{IL}	0.9	–	–	
Input Logic Threshold Hysteresis [26] Inputs Px_LS, SI, SCLK, $\overline{CS}$, $\overline{Px\_HS}$, EN1, EN2	V_{IHYS}	100	250	450	mV
Input Pull-Down Current, (Px_LS, SI, SCLK, EN1, EN2) 0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}	I_{INPD}	8.0	–	18	µA
Input Pull-Up Current, ($\overline{CS}$, $\overline{Px\_HS}$) [28] 0 ≤ V_{IN} ≤ 0.7 V_{DD}	I_{INPU}	10	–	25	µA
Input Capacitance [26] 0.0 ≤ V_{IN} ≤ 5.5V	C_{IN}	–	15	–	pF
$\overline{RST}$ Threshold [29]	$V_{TH\_\overline{RST}}$	1.0	–	2.1	V
$\overline{RST}$ Pull-Down Resistance 0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}	$R_{\overline{RST}}$	40	60	85	kΩ
Power-ON $\overline{RST}$ Threshold, (V_{DD} Falling)	$V_{TH\overline{RST}}$	3.4	4.0	4.5	V
SO High-Level Output Voltage I_{OH} = 1.0mA	V_{SOH}	0.9 V_{DD}	–	–	V
SO Low-Level Output Voltage I_{OL} = 1.0mA	V_{SOL}	–	–	0.1 V_{DD}	V
SO Tri-State Leakage Current $\overline{CS}$ = 0.7 V_{DD}, 0.3 V_{DD} = V_{SO} = 0.7 V_{DD}	$I_{SO\_LEAK\_T}$	-1.0	–	1.0	µA
SO Tri-State Capacitance [26], [30] 0.0 ≤ V_{IN} ≤ 5.5V	C_{SO_T}	–	15	–	pF
INT High-Level Output Voltage I_{OH} = -500µA	V_{OH}	0.85 V_{DD}	–	V_{DD}	% VDD
INT Low-Level Output Voltage I_{OL} = 500µA	V_{OL}	–	–	0.5	V
THERMAL WARNING					
Thermal Warning Temperature [26], [31]	T_{WARN}	150	170	185	°C
Thermal Hysteresis [26]	T_{HYST}	8	10	12	°C

Notes

26. This parameter is guaranteed by design, not production tested.
27. Logic threshold voltages derived relative to a 3.3V 10% system.
28. Pull-Up circuits will not allow back biasing of V_{DD}.
29. There are two elements in the $\overline{RST}$ circuit: 1) one generally lower threshold enables the internal regulator; 2) the second removes the reset from the internal logic.
30. This parameter applies to the OFF state (tri-stated) condition of SO is guaranteed by design but is not production tested.
31. The Thermal Warning circuit does not force IC shutdown above this temperature. It is possible to set a bit in the MASK register to generate an interrupt when overtemperature is detected, and the status bits will always read back the state of the three individual Thermal Warning circuits in the IC.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INTERNAL REGULATORS					
V_{DD} Power-Up Time (Until INT High) 8.0V ≤ V_{PWR} (32)	t_{PU_VDD}	–	–	2.0	ms
VLS Power-Up Time 16V ≤ V_{PWR} (33)	t_{PU_VDD}	–	–	2.0	ms
CHARGE PUMP					
Charge Pump Oscillator Frequency	F_{OSC}	90	125	190	kHz
Charge Pump Slew Rate(34)	SR_{CP}	–	100	–	V/µs
GATE DRIVE					
High-Side Turn-On Time Transition Time from 1.0 to 10V, Load: C = 500pF, Rg = 0, (Figure 7)	t_{ONH}	–	20	35	ns
High-Side Turn-On Delay(35) Delay from Command to 1.0V, (Figure 7)	t_{D_ONH}	130	265	386	ns
High-Side Turn-Off Time Transition Time from 10 to 1.0V, Load: C = 500pF, Rg = 0, (Figure 8)	t_{OFFH}	–	20	35	ns
High-Side Turn-Off Delay(35) Delay from Command to 10V, (Figure 8)	t_{D_OFFH}	130	265	386	ns
Low-Side Turn-On Time Transition Time from 1.0 to 10V, Load: C = 500pF, Rg = 0, (Figure 7)	t_{ONL}	–	20	35	ns
Low-Side Turn-On Delay(35) Delay from Command to 1.0V, (Figure 7)	t_{D_ONL}	130	265	386	ns
Low-Side Turn-Off Time Transition Time from 10 to 1.0V, Load: C = 500pF, Rg = 0, (Figure 8)	t_{OFFL}	–	20	35	ns
Low-Side Turn-Off Delay(35) Delay from Command to 10V, (Figure 8)	t_{D_OFFL}	130	265	386	ns
Same Phase Command Delay Match(36)	t_{D_DIFF}	-20	0	+20	ns
Thermal Filter Duration (37)	t_{DUR}	8.0	–	30	µs

Notes

32. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitor on V_{DD}.
33. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitor on VLS. This delay includes the expected time for V_{DD} to rise.
34. The charge pump operating at 12V V_{bat}, 1µF pump capacitor, MUR120 diodes and 47µF filter capacitor.
35. These delays include all logic delays except deadtime. All internal logic is synchronous with the internal clock. The total delay includes one clock period for state machine decision block, an additional clock period for FULLON mux logic, input synchronization time and output driver propagation delay. Subtract one clock period for operation in FULLON mode which bypasses the state machine decision block. Synchronization time accounts for up to one clock period of variation. See Figure 6.
36. This is the maximum separation or overlap of the High and Low side gate drives due to propagation delays when commanding one ON and the other OFF simultaneously.
37. The output of the overtemperature comparator goes through a digital filter before generating a warning or interrupt.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GATE DRIVE (CONTINUED)					
Duty Cycle (38), (39)	t_{DC}	0.0	–	96	%
100% Duty Cycle Duration (38), (39)	t_{DC}	–	–	Unlimited	s
Maximum Programmable Deadtime (40)	t_{MAX}	10.2	15	19.6	µs
OVERCURRENT COMPARATOR					
Overcurrent Protection Filter Time	t_{OC}	0.9	–	3.5	µs
Rise Time (OC_OUT) 10% - 90% C_L = 100 pF	t_{ROC}	10	–	240	ns
Fall Time (OC_OUT) 90% - 10% C_L = 100 pF	t_{FOC}	10	–	200	ns
PHASE COMPARATOR					
Propagation Delay Time to 50% of V_{DD}; C_L ≤ 100 pF					ns
Rising Edge Delay	t_R	–	–	200	
Falling Edge Delay	t_F	–	–	350	
Match Conversion Time (Prop Delay Mismatch of Three Phases) C_L = 100 pF (38)	t_{MATCH}	–	–	100	ns
DESATURATION DETECTOR					
Desaturation and Phase Error Blanking Time	t_{BLANK}	4.0	–	8.1	µs
Filter Time (38)	t_{FILT}				ns
Fault Must be Present for This Time to Trigger		560	1000	1230	
CURRENT SENSE AMPLIFIER					
Output Settle Time to 99% (38), (41) RL = 1kΩ, C_L = 500pF 0.3 < V_O < 4.8V Gain = 5 to 15	t_{SETTLE}	–	1.0	2.0	µs

Notes

38. This parameter is guaranteed by design, not production tested.
39. Maximum duty cycle is actually 100% because there is an internal charge pump to maintain the gate voltage in the 100% on condition. However, in high duty cycle cases, there may not be sufficient time to recharge the bootstrap capacitors during the off time. Large bootstrap capacitors will allow high duty cycles to be obtained for a short time. For applications needing closer to 100% duty cycle, external diodes may optionally be used to provide high peak current charging capability to the bootstrap capacitors. These diodes would be connected between VLS and the Px_BOOTSTRAP pins. In applications with lower gate charge requirements, the maximum duty cycle can also be increased.
40. A Minimum Deadtime of 0.0 can be set via a SPI command. When Deadtime is set via a DEADTIME command, a minimum of 1 clock cycle duration and a maximum of 255 clock cycles is set using the internal time base clock as a reference. Commands exceeding this value limits at this value.
41. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER (CONTINUED)					
Output Rise Time to 90% (43) RL = 1kΩ, C_L = 500 pF 0.3 < V_O < 4.8V Gain = 5 to 15	t_{IS_RISE}	–	–	1.0	µs
Output Fall Time to 10% (43) RL = 1kΩ C_L = 500pF 0.3 < V_O < 4.8V Gain = 5 to 15	t_{IS_FALL}	–	–	1.0	µs
Slew Rate at Gain = 5.0(42) RL = 1 κΩ, C_L = 20pF	SR(5)	5.0	–	–	V/µs
Phase Margin at Gain = 5.0(42)	f_M	–	30	–	°
Unity Gain Bandwidth (42) RL = 1 κΩ, C_L = 100pF	G_{BW}	–	20	–	MHz
Bandwidth at Gain = 15 (42) R_L = 1 κΩ, C_L = 50pF	BW_G	2.0	–	–	MHz
Common Mode Rejection (CMR) (42) with V_{IN} V_{IN_CM} = 400mV*sin(2*π*freq*t) V_{IN_DIF} = 0.0V, RS = 1kΩ R_{FB} = 15 kΩ, V_{REFIN} = 0.0V CMR = 20*Log(V_{OUT}/V_{IN_CM}) Freq = 100kHz Freq = 1.0MHz Freq = 10MHz	CMR	 50 40 30	 – – –	 – – –	dB
SUPERVISORY AND CONTROL CIRCUITS					
EN1 and EN2 Propagation Delay	t_{PROP}	–	–	280	ns
INT Rise Time CL = 100 pF	t_{RINT}	10	–	250	ns
INT Fall Time CL = 100 pF	t_{FINT}	10	–	200	ns
INT Propagation Time	$t_{PROPINT}$	–	–	250	ns

Notes

42. This parameter is guaranteed by design, not production tested.
43. Rise and fall times are measured from the transition of a step function on the input to 90% of the change in output voltage.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 8.0V ≤ V_{PWR} = V_{BAT} ≤ 40V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING					
Maximum Frequency of SPI Operation	f_{OP}	–		5.0	MHz
Internal Time Base	f_{TB}	13	17	25	MHz
Internal Time Base drift from value at 25°C (44)	TC_{TB}	-5	–	5	%
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (44)	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (44)	t_{LAG}	100	–	–	ns
SI to Falling Edge of SCLK (Required Setup Time) (44)	t_{SISU}	25	–	–	ns
Falling Edge of SCLK to SI (Required Setup Time) (44)	t_{SIHOLD}	25	–	–	ns
SI, $\overline{CS}$, SCLK Signal Rise Time (44), (45)	t_{RSI}	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time (44), (45)	t_{FSI}	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (44), (46)	t_{SOEN}	–	55	100	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (44), (47)	t_{SODIS}	–	100	125	ns
Time from Rising Edge of SCLK to SO Data Valid (44), (48)	t_{VALID}	–	55	100	ns
Time from Rising Edge of $\overline{CS}$ to Falling Edge of the next $\overline{CS}$ (44)	t_{DT}	200	–	–	ns

Notes

44. This parameter is guaranteed by design, not production tested.
45. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
46. Time required for valid output status data to be available on SO pin.
47. Time required for output states data to be terminated at SO pin.
48. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

TIMING DIAGRAMS

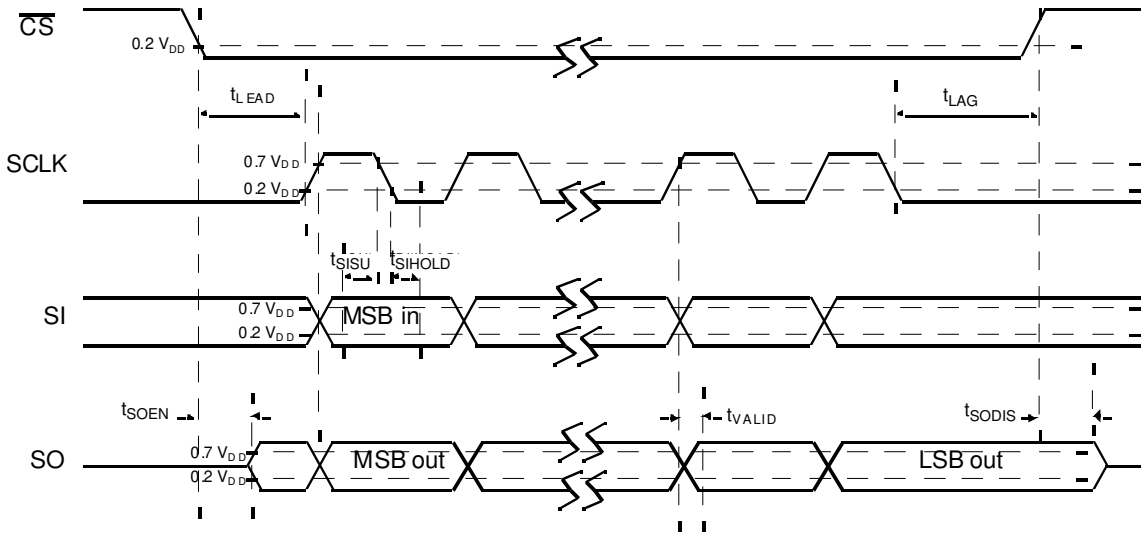

Figure 4. SPI Interface Timing

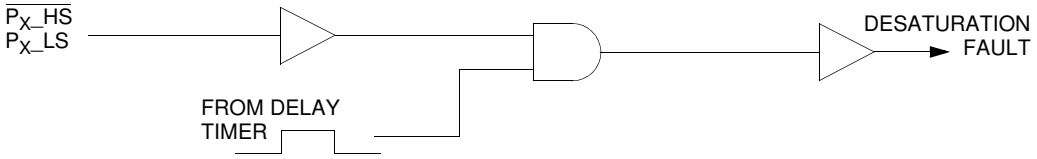

Figure 5. Desaturation Blanking and Filtering Detail

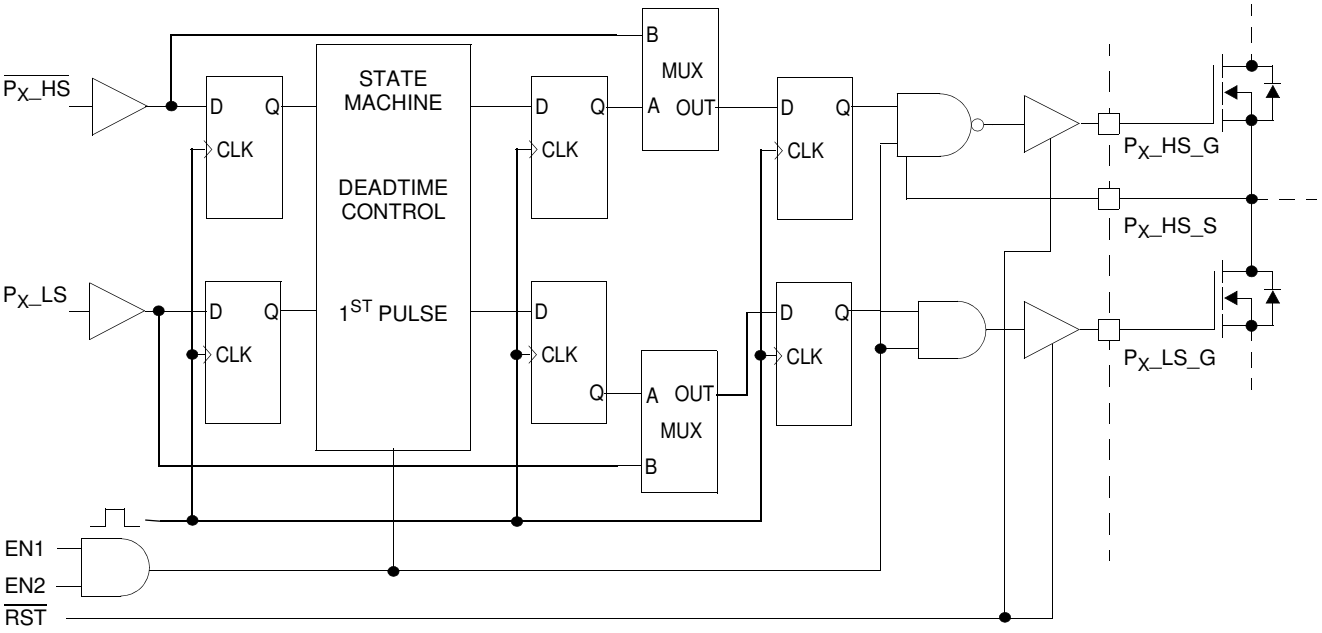

Figure 6. Deadtime Control Delays

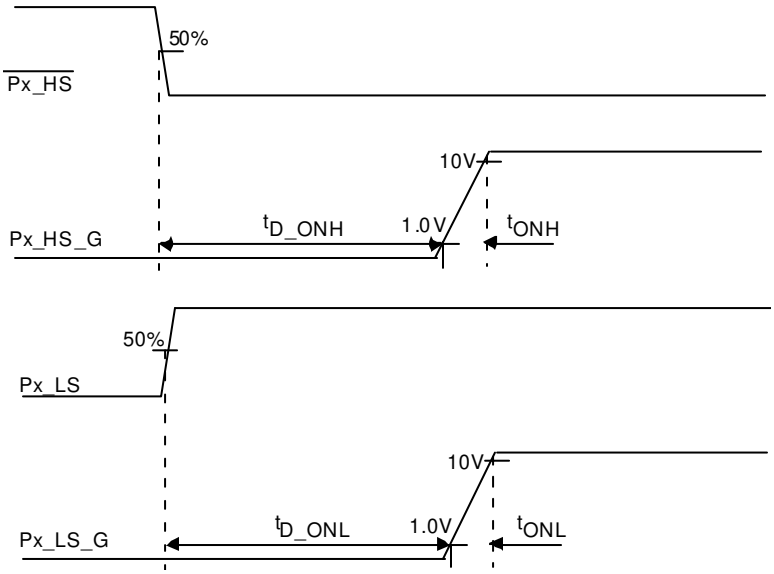

Figure 7. Driver Turn-On Time and Turn-On Delay

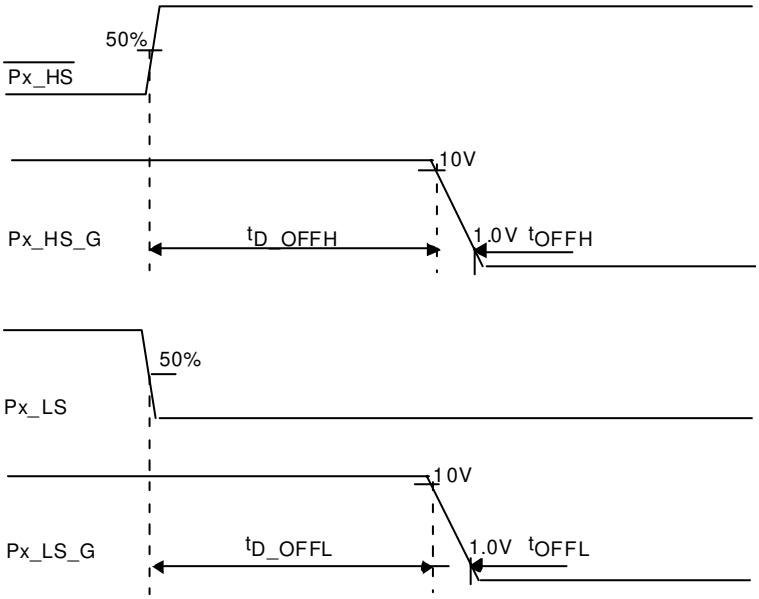

Figure 8. Driver Turn-Off Time and Turn-Off Delay

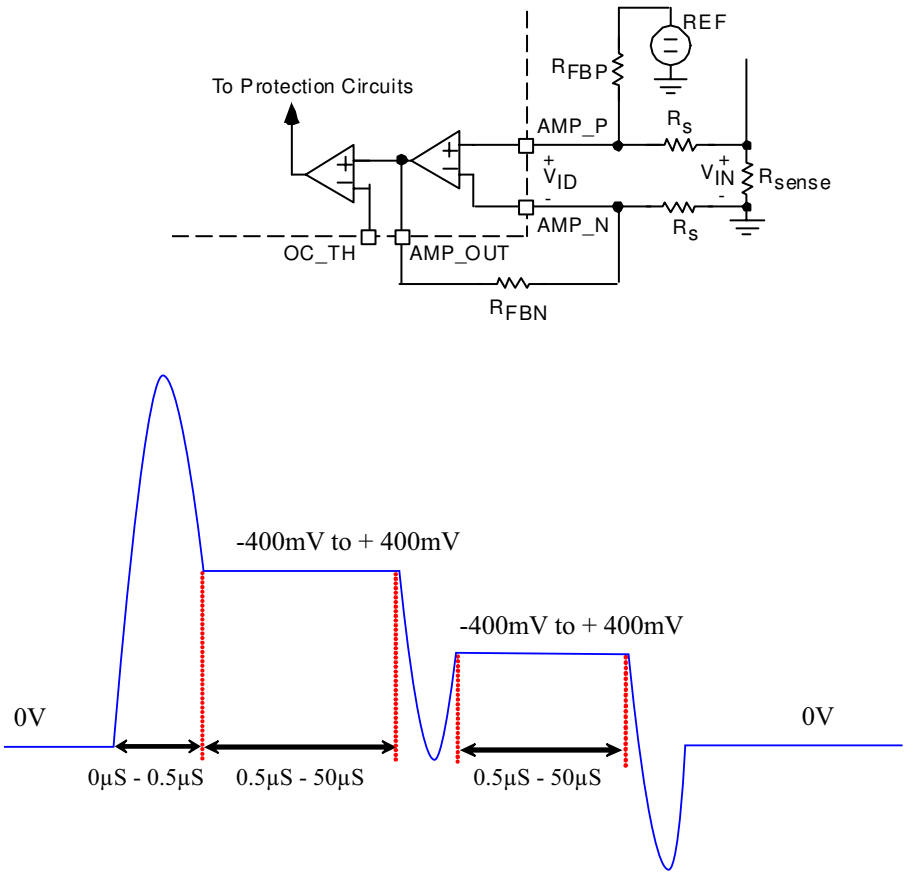

Figure 9. Current Amplifier and Input Waveform (V_{IN} Voltage Across R_{SENSE})

FUNCTIONAL DESCRIPTIONS

INTRODUCTION

The 33927 provides an interface between an MCU and the large FETs used to drive three-phase loads. A typical load FET may have an on-resistance of 4.0mΩ or less and could require a gate charge of over 400 nC to fully turn on. The IC can operate in automotive 12V to 42V environments.

Because there are so many methods of controlling three-phase systems, the IC enforces few constraints on driving the FETs. It does provide deadtime (cross-over) blanking and logic, both of which can be overridden, ensuring both FETs in a phase are not simultaneously enabled.

A SPI port is used to configure the IC modes.

FUNCTIONAL PIN DESCRIPTION

PHASE A (PHASEA)

This pin is the totem pole output of the Phase A comparator. This output is low when the voltage on Phase A high-side source (source of the High-Side load FET) is less than 50 percent of VBAT.

POWER GROUND (PGND)

This pin is power ground for the charge pump. It should be connected to VSS, however routing to a single point ground on the PCB may help to isolate charge pump noise.

NOTE: This is NOT the same as the Phase Grounds for each of the Phases.

ENABLE 1 AND ENABLE 2 (EN1, EN2)

Both of these logic signal inputs must be high to enable any gate drive output. When either or both are low, the internal logic (SPI port, etc.) still functions normally, but all gate drives are forced off (external power FET gates pulled low). The signal is asynchronous.

When EN1 and EN2 return high to enable the outputs, each LS driver must be pulsed on before the corresponding HS driver can be commanded on. This ensures that the bootstrap capacitors are charged.

RESET ($\overline{\text{RST}}$)

When the reset pin is low the integrated circuit (IC) is in a low power state. In this mode all outputs are disabled, internal bias circuits are turned off, and a small pull down current is applied to the output gate drives. The internal logic will be reset within 77ns of RESET going low. When $\overline{\text{RST}}$ is low, the IC will consume minimal current.

This input should not be driven above the VDD voltage.

CHARGE PUMP OUT (PUMP)

This pin is the switching node of the charge pump circuit. The output of the internal charge pump support circuit. When the charge pump is used, it is connected to the external pumping capacitor. This pin may be left floating if the charge pump is not required.

CHARGE PUMP INPUT (VPUMP)

This pin is the input supply for the charge pump circuit. When the charge pump is required, this pin should be connected to a polarity protected supply. Typical applications would connect it to VBAT. This input should never be connected to a supply greater than 40V.

If the charge pump is not required this pin may be left floating.

VBAT INPUT (VBAT)

This pin should be connected to the system battery voltage. It is used to provide power to the internal steady state trickle charge pump and to energize the hold-off circuit. It is also the reference bias for the Phase Comparators and Desaturation Comparator.

PHASE B (PHASEB)

This pin is the totem pole output of the Phase B comparator. This output is low when the voltage on Phase B high-side source (source of the High-Side load FET) is less than 50 percent of VBAT.

PHASE C (PHASEC)

This pin is the totem pole output of the Phase C comparator. This output is low when the voltage on Phase C high-side source (source of the High-Side load FET) is less than 50 percent of VBAT.

PHASE A HIGH-SIDE INPUT ($\overline{\text{PA\_HS}}$)

This input logic signal pin enables the High-Side Driver for Phase A. The signal is active low, and is pulled up by an internal current source.

PHASE A LOW-SIDE INPUT (PA_LS)

This input logic signal pin enables the Low-Side Driver for Phase A. The signal is active high, and is pulled down by an internal current sink.

VDD VOLTAGE REGULATOR (VDD)

This pin is an internally generated 5V supply. The internal regulator provides continuous power to the IC and is a supply

reference for the SPI port. A 0.47µF (min) decoupling capacitor must be connected to this pin.

This regulator is intended for internal IC use and can supply only a small (1mA) external load current.

A power-on-reset (POR) circuit monitors this pin and until the voltage rises above the threshold, the internal logic will be reset; driver outputs will be tri-stated and SPI communication disabled.

The VDD regulator can be disabled by asserting the $\overline{\text{RST}}$ signal low. The VDD regulator is powered from the VPWR pin.

PHASE B HIGH-SIDE CONTROL INPUT ($\overline{\text{PB\_HS}}$)

This pin is the input logic signal, enabling the High-Side driver for Phase B. The signal is active low, and is pulled up by an internal current source.

PHASE B LOW-SIDE INPUT (PB_LS)

This pin is the input logic signal, enabling the Low-Side driver for Phase B. The signal is active high, and is pulled down by an internal current sink.

INTERRUPT (INT)

The Interrupt pin is a totem pole logic output. When a fault is detected, this pin will pull high until it is cleared by executing the Clear Interrupt command via the SPI port. The faults capable of causing an interrupt can be masked via the MASK0 and MASK1 SPI registers to customize the response.

CHIP SELECT ($\overline{\text{CS}}$)

Chip select is a logic input that frames the SPI commands and enables the SPI port. This signal is active low, and is pulled up by an internal current source.

SERIAL IN (SI)

The Serial In pin is used to input data to the SPI port. Clocked on the falling edge of SCLK, it is the most significant bit (MSB) first. This pin is pulled down by an internal current sink.

SERIAL CLOCK (SCLK)

This logic input is the clock is used for the SPI port. The SCLK typically runs at 3 MHz (up to 5 MHz) and is pulled down by an internal current sink.

SERIAL OUT (SO)

Output data for the SPI port streams from this pin. It is tri-stated until $\overline{\text{CS}}$ is low. New data appears on rising edges of SCLK in preparation for latching by the falling edge of SCLK on the master.

PHASE C LOW-SIDE INPUT (PC_LS)

This input logic pin enables the Low-Side Driver for Phase C. This pin is an active high, and is pulled down by an internal current sink.

PHASE C HIGH-SIDE INPUT ($\overline{\text{PC\_HS}}$)

This input logic pin enables the High-Side Driver for Phase C. This signal is active low, and is pulled up by an internal current source.

AMPLIFIER OUTPUT (AMP_OUT)

This pin is the output for the current sensing amplifier. It is also the sense input to the overcurrent comparator.

AMPLIFIER INVERTING INPUT (AMP_N)

The inverting input to the current sensing amplifier.

AMPLIFIER NON-INVERTING INPUT (AMP_P)

The non-inverting input to the current sensing amplifier.

OVERCURRENT COMPARATOR OUTPUT (OC_OUT)

The overcurrent comparator output is a totem pole logic level output. A logic high indicates an overcurrent condition.

OVERCURRENT COMPARATOR THRESHOLD (OC_TH)

This input sets the threshold level of the overcurrent comparator.

VOLTAGE SOURCE SUPPLY (VSS)

VSS is the ground reference for the logic interface and power supplies.

GROUND (GND0,GND1)

These two pins are connected internally to VSS by a 1.0 Ω resistor. They provide device substrate connections and also the primary return path for ESD protection.

VLS REGULATOR CAPACITOR (VLS_CAP)

This connection is for a capacitor which will provide a low impedance for switching currents on the gate drive. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents must be connected between this pin and VSS.

This is the same DC node as VLS, but it is physically placed on the opposite end of the IC to minimize the source impedance to the gate drive circuits.

PHASE C GROUND (PGNDC)

The phase C power ground is the pin used to return the gate currents from the low side FET. Best performance is normally realized by connecting this node directly to the source of the low side FET for phase C.

PHASE C LOW-SIDE GATE (PC_LS_G)

This is the gate drive for the phase C low side output FET. It provides a high current with a low impedance to turn on and off the low side FET. A low impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has been designed to resist the influence of negative currents also.

PHASE C HIGH-SIDE SOURCE (PC_HS_S)

The source connection for the phase C high side output FET is the reference voltage for the gate drive on the high side FET and also the low voltage end of the bootstrap capacitor.

PHASE C HIGH-SIDE GATE (PC_HS_G)

This is the gate drive for the phase C high side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15V above the FET source voltage. A low impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has been designed to resist the influence of negative currents also.

PHASE C BOOTSTRAP (PC_BOOT)

This is the bootstrap capacitor connection for phase C. A capacitor (typically 0.1µF) connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. The voltage across this capacitor is limited to about 15V.

PHASE B GROUND (PGNDB)

The phase B power ground is the pin used to return the gate currents from the low side FET. Best performance is normally realized by connecting this node directly to the source of the low side FET for phase B.

PHASE B LOW-SIDE GATE (PC_LS_G)

This is the gate drive for the phase B low side output FET. It provides a high current with a low impedance to turn on and off the low side FET. A low impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has been designed to resist the influence of negative currents also.

PHASE B HIGH-SIDE SOURCE (PB_HS_S)

The source connection for the phase B high side output FET is the reference voltage for the gate drive on the high side FET and also the low voltage end of the bootstrap capacitor.

PHASE B HIGH-SIDE GATE (PB_HS_G)

This is the gate drive for the phase B high side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15V above the FET source voltage. A low impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has been designed to resist the influence of negative currents also.

PHASE B BOOTSTRAP (PB_BOOT)

This is the bootstrap capacitor connection for phase B. A capacitor (typically 0.1µF) connected between PB_HS_S and this pin provides the gate voltage and current to drive the external FET gate. The voltage across this capacitor is limited to about 15V.

PHASE A GROUND (PGNDA)

The phase A power ground is the pin used to return the gate currents from the low side FET. Best performance is normally realized by connecting this node directly to the source of the low side FET for phase A.

PHASE A LOW-SIDE GATE (PA_LS_G)

This is the gate drive for the phase A low side output FET. It provides a high current with a low impedance to turn on and off the low side FET. A low impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has been designed to resist the influence of negative currents also.

PHASE A HIGH-SIDE SOURCE (PA_HS_S)

The source connection for the phase A high side output FET is the reference voltage for the gate drive on the high side FET and also the low voltage end of the bootstrap capacitor.

PHASE A HIGH-SIDE GATE (PA_HS_G)

This is the gate drive for the phase A high side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15V above the FET source voltage. A low impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has been designed to resist the influence of negative currents also.

PHASE A BOOTSTRAP (PA_BOOT)

This is the bootstrap capacitor connection for phase A. A capacitor (typically 0.1µF) connected between PA_HS_S and this pin provides the gate voltage and current to drive the external FET gate. The voltage across this capacitor is limited to about 15V.

VLS REGULATOR (VLS)

VLS is the gate drive power supply regulated at approximately 15V. This is an internally generated supply from VPWR. It is the source for the low side gate drive voltage, and also the high side bootstrap source. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents, must be connected between this pin and VSS or PGND.

VPWR INPUT (VPWR)

VPWR is the power supply input for VLS and VDD. Current flowing into this input recharges the bootstrap capacitors as well as supplying power to the low-side gate drivers and the VDD regulator. An internal regulator regulates the actual gate voltages. This pin can be connected to system battery voltage if power dissipation is not a concern.

EXPOSED PAD (EP)

The primary function of the Exposed Pad is to conduct heat out of the device. This pad may be connected electrically to the substrate of the device.The device will perform as specified with the Exposed Pad un-terminated (floating). However, it is recommended that the Exposed Pad be terminated to pin 29 (VSS) and the system ground.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

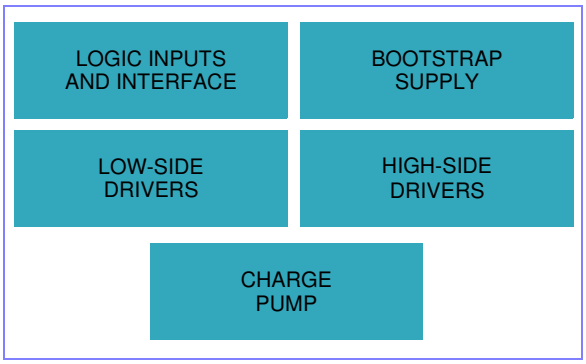

Figure 10. Functional Internal Block Description

All functions of the IC can be described as the following five major functional blocks:

- Logic Inputs and Interface
- Bootstrap Supply
- Low-Side Drivers
- High-Side Drivers
- Charge Pump

LOGIC INPUTS AND INTERFACE

This section contains the SPI port, control logic, and shoot-through timers.

The IC logic inputs have Schmitt trigger inputs with hysteresis. Logic inputs are 3V compatible. The logic outputs are driven from the internal supply of approximately 5.0V. When the internal supply is not enabled, the SO pin should not be externally driven high.

The SPI registers and functionality is described completely in the LOGIC COMMANDS AND REGISTERS section of this document. SPI functionality includes the following:

- **Programming of deadtime delay**—This delay is adjustable in approximately 50 ns steps from 0 ns to 12 µs. Calibration of the delay, because of internal IC variations, is performed via the SPI.
- **Enabling of simultaneous operation of high-side and low-side FETs**—Normally, both FETs would not be enabled simultaneously. However, for certain applications where the load is connected between the high-side and low-side FETs, this could be advantageous. If this mode is enabled, the blanking time delay will be disabled. A sequence of commands may be required to enable this function to prevent inadvertent enabling. In addition, this command can only be executed once after reset to enable or disable simultaneous turn-on.
- **Setting of various operating modes** of the IC and enabling of interrupt sources.
  The 33927 allows different operating modes to be set and locked by a SPI command (FULLON, Desaturation Fault, Zero-Deadtime). SPI commands can also determine how the various faults are (or are not) reported.
- **Read back of internal registers**.
  The status of the 33927 Status Registers can be read back by the Master (DSP or MCU).

The $\overline{\text{Px\_HS}}$ and Px_LS logic inputs are edge sensitive. This means the leading edge on an input will cause the complementary output to immediately turn off and the selected one to turn on after the deadtime delay as illustrated in Figure 11. The deadtime delay timer starts when the corresponding FET was commanded off (see Figure 6 and Figure 11).

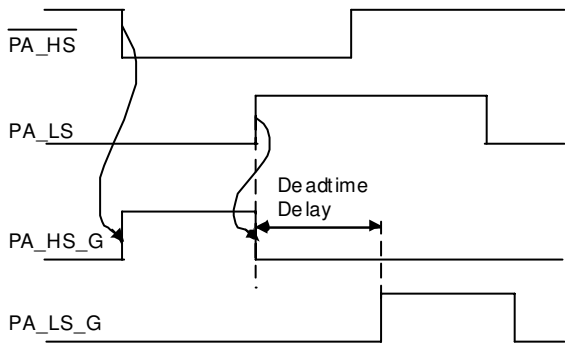

Figure 11. Edge Sensitive Logic Inputs (Phase A)

BOOTSTRAP SUPPLY (VPWR)

This is the portion of the IC providing current to recharge the bootstrap capacitors. It also supplies the peak currents required for the low-side gate drivers.

The power for the gate drive circuits is provided through the VPWR pin. This pin can be connected to VBAT and is capable of withstanding up to the full load dump voltage of the system. However, the IC only requires a low-voltage supply

on this pin, typically 15V. Higher voltages on the pin increases the IC power dissipation.

In 12V systems the supply voltage can fall as low as 6.0V. This limits the gate voltage capable of being applied to the FETs and reduces system performance due to the higher FET on-resistance. To allow a higher gate voltage to be supplied, the IC also incorporates a charge pump. The switches and control circuitry are internal; the capacitors and diodes are external (see Figure 17).

LOW SIDE DRIVERS

These three drivers turn on and off the external low side FETs. The circuits provide a low impedance drive to the gate, ensuring the FETs remain off in the presence of high dV/dt transients on their drains. Additionally, these output drivers isolate the other portions of the IC from currents capable of being injected into the substrate due to rapid dV/dt transients on the FET drains.

Low-side drivers switch power from VLS to the gates of the low-side FETs. The low-side drivers are capable of providing a typical peak current of 2.0A. This gate drive current may be limited by external resistors in order to achieve a good trade-off between the efficiency and EMC (Electro-Magnetic Compatibility) compliance of the application. the low side driver uses high side PMOS for turn on and low side isolated LDMOS for turn off. The circuit ensures the impedance of the driver remains low, even during periods of reduced current. Current limit is blanked immediately after subsequent input state change in order to ensure device stays off during dV/dt transients.

HIGH SIDE DRIVERS

These three drivers switch the voltage across the bootstrap capacitor to the external high side FETs. The circuits provide a low-impedance drive to the gate, ensuring the FETs remain off in the presence of high dV/dt transients on their sources. Further, these output drivers isolate the other portions of the IC from currents capable of being injected into the substrate due to rapid dV/dt transients on the FETs.

The high-side drivers deliver power from their bootstrap capacitor to the gate of the external high-side FET, thus turning the high-side FET on. The high-side driver uses a level shifter, which allows the gate of the external high-side FET to be turned off by switching to the high-side FET source.

Because the gate supply voltage for the high-side drivers is obtained from the bootstrap supply, a short time is required after the application of power to the IC to charge the bootstrap capacitors. To ensure this occurrence, the internal control logic will not allow a high-side switch to be turned on after entering the ENABLE state until the corresponding low side switch is enabled at least once. Caution must be exercised after a long period of inactivity of the low-side switches, to verify the bootstrap capacitor is not discharged. It can be recharged by activating the low-side switches for a brief period, or by attaching external bleed resistors to the HS_S pins to GND.

In order to achieve a 100% duty cycle operation of the high-side external FETs, a fully integrated trickle charge pump provides the charge necessary to fully enhance the external FET gates.

The slew rate of the external output FET is limited by the driver output impedance, overall (external and internal) gate resistance and the load capacitance. To ensure the low-side FET is not turned on by a large positive dV/dt on the drain of the low side FET, the turn-on slew rate of the high-side should be limited. If the slew rate of the high side is limited by the gate-drain capacitance of the high side FET, then the displacement current injected into the low-side gate drive output will be approximately the same value. Therefore, to ensure the low side drivers can be held off, the voltage drop across the low side gate driver must be lower than the threshold voltage of the low side FET (see Figure 12).

Similarly, during large negative dV/dt, the high side FET will be able to remain off if its gate drive low side switch, develops a voltage drop less than the threshold voltage of the high side FET. The gate drive low side switch discharges the gate to the source.

Additionally, during negative dV/dt the low side gate drive could be forced below ground. The low side FETs must not inject detrimental substrate currents in this condition.

The occurrence of these cases depends on the polarity of the load current during switching.

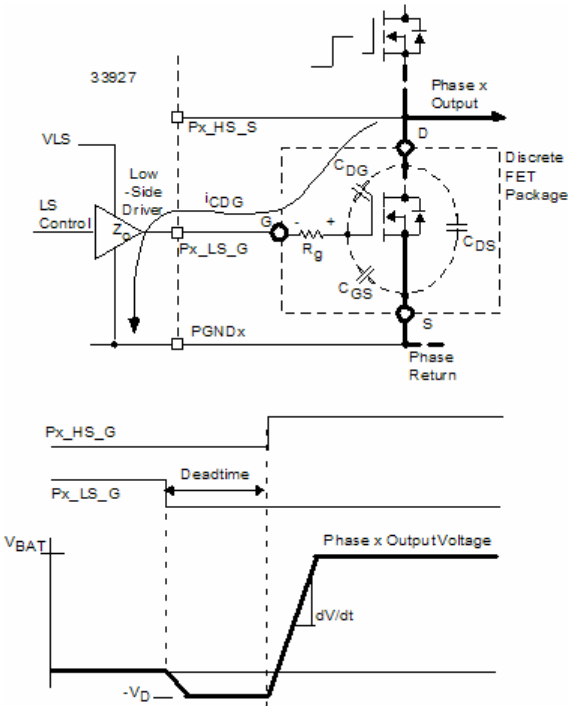

Figure 12. Positive DV/dt Transient