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NXP Semiconductors
Technical Data

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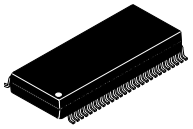
Three phase field effect transistor pre-driver

33937A

THREE PHASE PRE-DRIVER



EK SUFFIX (Pb-FREE)
98ASA99334D
54-PIN SOICW-EP

The 33937A is a field effect transistor (FET) pre-drivers designed for three phase motor control and similar applications. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

The IC contains three high-side FET pre-drivers and three low-side FET pre-drivers. Three external bootstrap capacitors provide gate charge to the high-side FETs.

The IC interfaces to a MCU via six direct input control signals, an SPI port for device setup and asynchronous reset, enable and interrupt signals. Both 5.0 and 3.0 V logic level inputs are accepted and 5.0 V logic level outputs are provided. The integrated circuit (IC) uses SMARTMOS technology.

Features

- Extended operating range from 6.0 V to 58 V covers 12 V and 42 V systems
- Gate drive capability of 1.0 A to 2.5 A
- Fully specified from 8.0 V to 40 V covers 12 and 24 V automotive systems
- Protection against reverse charge injection from CGD and CGS of external FETs
- Includes a charge pump to support full FET drive at low battery voltages
- Dead time is programmable via the SPI port
- Simultaneous output capability enabled via safe SPI command
- AEC-Q100 grade 1 qualified

Applications

Automotive systems

- Cooling fan
- Water pump
- Actuator controls
- Fuel pump
- Electro-hydraulic and electric power steering
- Engine control
- Motor control

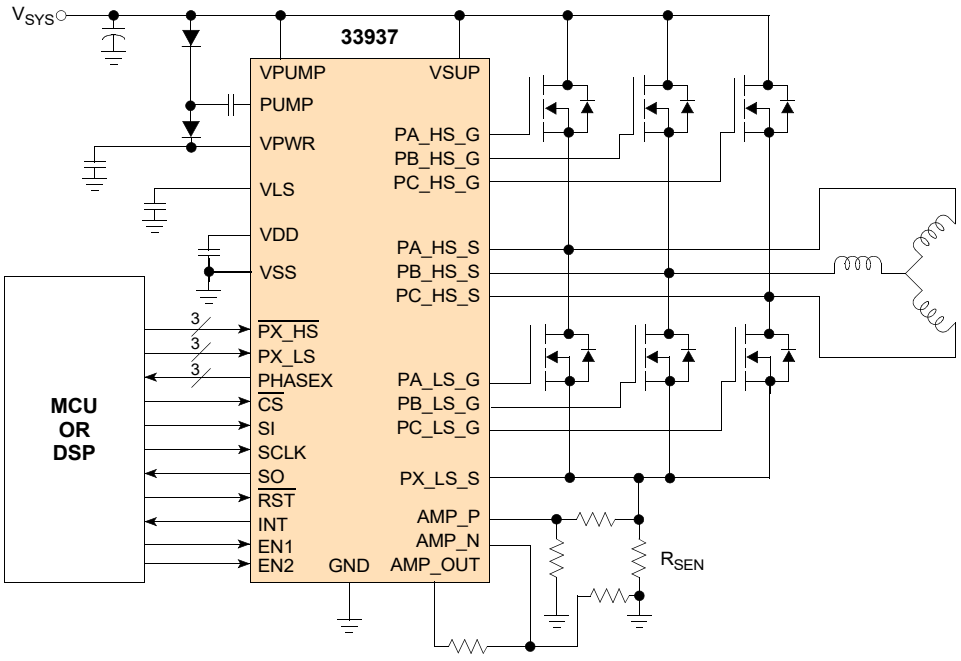


Figure 1. 33937A simplified application diagram

1 Orderable parts

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package
MC33937APEK	-40 °C to 135 °C	54 SOICW-EP

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

2 Internal block diagram

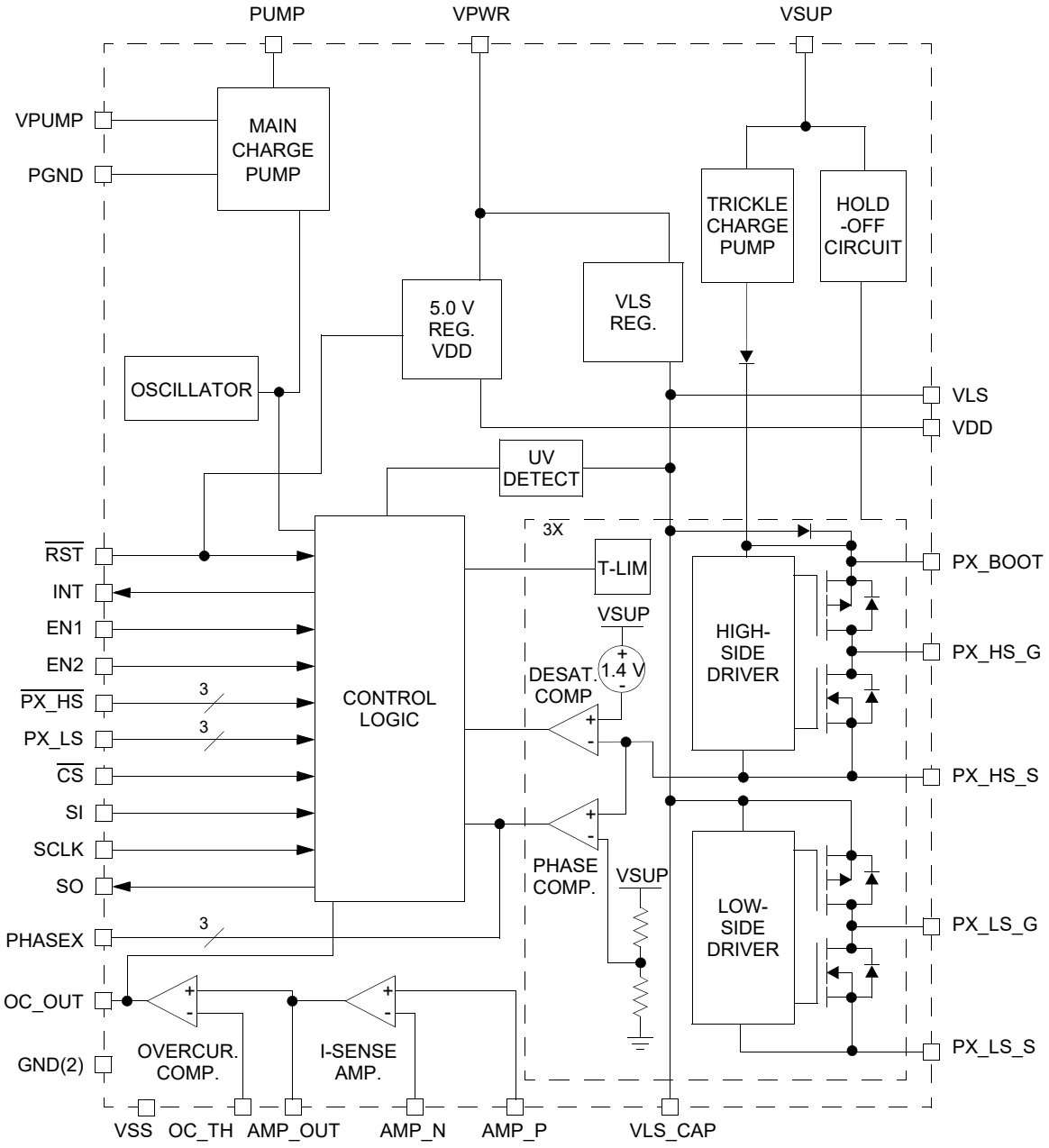


Figure 2. 33937A simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

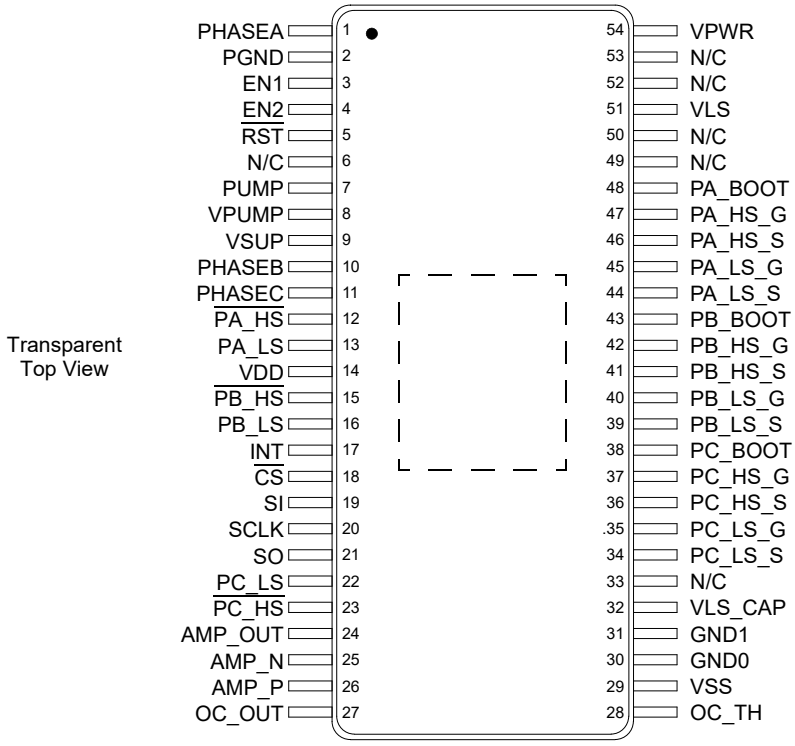


Figure 3. 33937A pin connections

3.2 Pin definitions

A functional description of each pin can be found in the Functional pin description section beginning on page 21.

Table 2. 33937A pin definitions

Pin	Pin name	Pin function	Formal name	Definition
1	PHASEA	Digital Output	Phase A	Totem Pole output of Phase A comparator. This output is low when the voltage on PA_HS_S (Source of High-side FET) is less than 50% of V_{SUP}
2	PGND	Ground	Power Ground	Power ground for charge pump
3	EN1	Digital Input	Enable 1	Logic signal input must be high (ANDed with EN2) to enable any gate drive output.
4	EN2	Digital Input	Enable 2	Logic signal input must be high (ANDed with EN1) to enable any gate drive output
5	$\overline{\text{RST}}$	Digital Input	Reset	Reset input
6, 33, 49, 50, 52, 53	N/C	–	No Connect	Do not connect these pins
7	PUMP	Power Drive Out	Pump	Charge pump output
8	VPUMP	Power Input	Voltage Pump	Charge pump supply
9	VSUP	Analog Input	Supply Voltage	Supply voltage to the load. This pin is to be connected to the common Drains of the external high-side FETs

Table 2. 33937A pin definitions (continued)

Pin	Pin name	Pin function	Formal name	Definition
10	PHASEB	Digital Output	Phase B	Totem Pole output of Phase B comparator. This output is low when the voltage on PB_HS_S (Source of high-side FET) is less than 50% of V_{SUP}
11	PHASEC	Digital Output	Phase C	Totem Pole output of Phase C comparator. This output is low when the voltage on PC_HS_S (Source of high-side FET) is less than 50% of V_{SUP}
12	PA_HS	Digital Input	Phase A High-side	Active low input logic signal enables the high-side driver for Phase A
13	PA_LS	Digital Input	Phase A Low-side	Active high input logic signal enables the low-side driver for Phase A
14	VDD	Analog Output	VDD Regulator	VDD regulator output capacitor connection.
15	PB_HS	Digital Input	Phase B High-side	Active low input logic signal enables the high-side driver for Phase B
16	PB_LS	Digital Input	Phase B Low-side	Active high input logic signal enables the low-side driver for Phase B
17	INT	Digital Output	Interrupt	Interrupt pin output
18	CS	Digital Input	Chip Select	Chip Select input. It frames SPI commands and enables SPI port
19	SI	Digital Input	Serial In	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
20	SCLK	Digital Input	Serial Clock	Clock for SPI port and typically is 3.0 MHz
21	SO	Digital Output	Serial Out	Output data for SPI port. Tri-state until $\overline{CS}$ becomes low
22	PC_LS	Digital Input	Phase C Low-side	Active high input logic signal enables the low-side driver for Phase C
23	PC_HS	Digital Input	Phase C High-side	Active low input logic signal enables the high-side driver for Phase C
24	AMP_OUT	Analog Output	Amplifier Output	Output of the current-sensing amplifier
25	AMP_N	Analog Input	Amplifier Invert	Inverting input of the current-sensing amplifier
26	AMP_P	Analog Input	Amplifier Non-Invert	Non-inverting input of the current-sensing amplifier
27	OC_OUT	Digital Output	Overcurrent Out	Totem pole digital output of the overcurrent comparator
28	OC_TH	Analog Input	Overcurrent Threshold	Threshold of the overcurrent detector
29	VSS	Ground	Voltage Source Supply	Ground reference for logic interface and power supplies
30, 31	GND	Ground	Ground	Substrate and ESD reference, connect to VSS
32	VLS_CAP	Analog Output	VLS Regulator Output Capacitor	VLS Regulator connection for additional output capacitor, providing low-impedance supply source for low-side gate drive
34	PC_LS_S	Power Input	Phase C Low-side Source	Source connection for Phase C low-side FET
35	PC_LS_G	Power Output	Phase C Low-side Gate Drive	Gate drive output for Phase C low-side
36	PC_HS_S	Power Input	Phase C High-side Source	Source connection for Phase C high-side FET
37	PC_HS_G	Power Output	Phase C High-side Gate Drive	Gate Drive for output Phase C high-side FET
38	PC_BOOT	Analog Input	Phase C Bootstrap	Bootstrap capacitor for Phase C
39	PB_LS_S	Power Input	Phase B Low-side Source	Source connection for Phase B low-side FET
40	PB_LS_G	Power Output	Phase B Low-side Gate Drive	Gate Drive for output Phase B low-side
41	PB_HS_S	Power Input	Phase B High-side Source	Source connection for Phase B high-side FET
42	PB_HS_G	Power Output	Phase B High-side Gate Drive	Gate Drive for output Phase B high-side
43	PB_BOOT	Analog Input	Phase B Bootstrap	Bootstrap capacitor for Phase B
44	PA_LS_S	Power Input	Phase A Low-side Source	Source connection for Phase A low-side FET

Table 2. 33937A pin definitions (continued)

Pin	Pin name	Pin function	Formal name	Definition
45	PA_LS_G	Power Output	Phase A Low-side Gate Drive	Gate Drive for output Phase A low-side
46	PA_HS_S	Power Input	Phase A High-side Source	Source connection for Phase A high-side FET
47	PA_HS_G	Power Output	Phase A High-side Gate Drive	Gate Drive for output Phase A high-side
48	PA_BOOT	Analog Input	Phase A Bootstrap	Bootstrap capacitor for Phase A
51	VLS	Analog Output	VLS Regulator	VLS regulator output. Power supply for the gate drives
54	VPWR	Power Input	Voltage Power	Power supply input for gate drives
	EP	Ground	Exposed Pad	Device will perform as specified with the exposed pad un-terminated (floating) however, it is recommended that the exposed pad be terminated to pin 29 (VSS) and system ground

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V_{SUP}	VSUP Supply Voltage • Normal Operation (Steady-state) • Transient Survival	 58 -1.5 to 80	V	(2)
V_{PWR}	VPWR Supply Voltage • Normal Operation (Steady-state) • Transient Survival	 58 -1.5 to 80	V	(2)
V_{PUMP}	Charge Pump (PUMP, VPUMP)	-0.3 to 40	V	
V_{LS}	VLS Regulator Outputs (VLS, VLS_CAP)	-0.3 to 18	V	
V_{DD}	Logic Supply Voltage	-0.3 to 7.0	V	
V_{OUT}	Logic Output (INT, SO, PHASEA, PHASEB, PHASEC, OC_OUT)	-0.3 to 7.0	V	(3)
V_{IN}	Logic Input Pin Voltage (EN1, EN2, $\overline{Px\_HS}$, Px_LS, SI, SCLK, $\overline{CS}$, $\overline{RST}$) 10 mA	-0.3 to 7.0	V	
V_{IN_A}	Amplifier Input Voltage • (Both Inputs-GND), (AMP_P - GND) or (AMP_N - GND) 6.0 mA source or sink	-7.0 to 7.0	V	
V_{OC}	Overcurrent comparator threshold 10 mA	-0.3 to 7.0	V	
V_{BOOT} V_{HS_G} V_{LS_G}	Driver Output Voltage • High-side bootstrap (PA_BOOT, PB_BOOT, PC_BOOT) • High-side (PA_HS_G, PB_HS_G, PC_HS_G) • Low-side (PA_LS_G, PB_LS_G, PC_LS_G)	 75 75 16	V	(4)
V_{HS_G} V_{HS_S} V_{LS_G} V_{LS_S}	Driver Voltage Transient Survival • High-side (PA_HS_G, PB_HS_G, PC_HS_G, PA_HS_S, PB_HS_S, PC_HS_S) • Low-side (PA_LS_G, PB_LS_G, PC_LS_G, PA_LS_S, PB_LS_S, PC_LS_S)	 -7.0 to 75.0 -7.0 to 75.0 -7.0 to 18.0 -7.0 to 7.0	V	(5)
V_{ESD}	ESD Voltage • Human Body Model - HBM (All pins except for the pins listed below) Pins: PA_Boot, PA_HS_S, PA_HS_G, PB_Boot, PB_HS_S, PB_HS_G, PC_Boot, PC_HS_S, PC_HS_G, VPWR • Charge Device Model - CDM • Corner pins • All other pins	 ±2000 ±1000 ±750 ±300	V	(6)

Notes

2. The device will withstand load dump transient as defined by ISO7637 with peak voltage of 80 V.
3. Short-circuit proof, the device will not be damaged or induce unexpected behavior due to shorts to external sources within this range.
4. This voltage should not be applied without also taking voltage at HS_S and voltage at PX_LS_S into account.
5. Actual operational limitations may differ from survivability limits. The V_{LS} - V_{LS_S} differential and the V_{BOOT} - V_{HS_S} differential must be greater than 3.0 V to insure the output gate drive will maintain a commanded OFF condition on the output.
6. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 3. Maximum ratings (continued)

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal ratings				
T_{STG}	Storage Temperature	-55 to +150	°C	
T_J	Operating Junction Temperature	-40 to +150	°C	
$R_{\theta JC}$	Thermal Resistance • Junction-to-Case	3.0	°C/W	(7)
T_{SOLDER}	Soldering Temperature	Note 9	°C	(8)

Notes

7. Case is considered EP - pin 55 under the body of the device. The actual power dissipation of the device is dependent on the operating mode, the heat transfer characteristics of the board and layout and the operating voltage. See Figure 24 and Figure 25 for examples of power dissipation profiles of two common configurations. Operation above the maximum operating junction temperature will result in a reduction in reliability leading to malfunction or permanent damage to the device.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes and enter the core ID) to view all orderable parts, and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power inputs						
V_{PWR_ST}	VPWR Supply Voltage Startup Threshold	–	6.0	8.0	V	(10)
I_{SUP}	VSUP Supply Current, V_{PWR} = V_{SUP} = 40 V, $\overline{RST}$ and ENABLE = 5.0 V • No output loads on Gate Drive Pins, No PWM • No output loads on Gate Drive Pins, 20 kHz, 50% Duty Cycle	 – –	 1.0 –	 – 10	mA	
I_{PWR_ON}	VPWR Supply Current, V_{PWR} = V_{SUP} = 40 V, $\overline{RST}$ and ENABLE = 5.0 V • No output loads on Gate Drive Pins, No PWM, Outputs initialized • Output Loads = 620 nC per FET, 20 kHz PWM	 – –	 11 –	 20 95	mA	 (11)
I_{SUP} I_{PWR}	Sleep State Supply Current, $\overline{RST}$ = 0 V • V_{SUP} = 40 V • V_{PWR} = 40 V	 – –	 14 56	 30 100	µA	
V_{GATESS}	Sleep State Output Gate Voltage • IG < 100 µA	–	–	1.3	V	
V_{Boot}	Trickle Charge Pump (Bootstrap Voltage) • V_{SUP} = 14 V	22	28	32	V	(15)
V_F	Bootstrap Diode Forward Voltage at 10 mA	–	–	1.2	V	
VDD internal regulator						
V_{DD}	V_{DD} Output Voltage, V_{PWR} = 8 to 40 V, C = 0.47 µF • External Load I_{DD_EXT} = 0 to 1.0 mA	4.5	–	5.5	V	(12)
I_{DD}	Internal V_{DD} Supply Current, V_{DD} = 5.5 V, No External Load	–	–	12	mA	
VLS regulator						
I_{PEAK}	Peak Output Current, V_{PWR} = 16 V, V_{LS} = 10 V	350	600	800	mA	
V_{LS}	Linear Regulator Output Voltage, I_{VLS} = 0 to 60 mA, V_{PWR} > V_{LS} + 2.0 V	13.5	15	17	V	(13)
V_{THVLS}	VLS Disable Threshold	7.5	8.0	8.5	V	(14)

Notes

10. Operation with the Charge Pump is recommended when minimum system voltage could be less than 14 V. V_{PWR} must exceed this threshold in order for the Charge Pump and V_{DD} regulator to startup and drive V_{PWR} to > 8.0 V. Once V_{PWR} exceeds 8.0 V, the circuits will continue to operate even if system voltage drops below 6.0 V.
11. This parameter is guaranteed by design. It is not production tested.
12. Minimum external capacitor for stable V_{DD} operation is 0.47 µF.
13. Recommended external capacitor for the V_{LS} regulator is 2.2 µF low ESR at each pin VLS and VLS_CAP.
14. When V_{LS} is less than this value, the outputs are disabled and HOLDOFF circuits are active. Recovery requires initialization when V_{LS} rises above this threshold again. A filter delay of approximately 700 ns on the comparator output eliminates responses to spurious transients on V_{LS}.
15. See Figure 11 for typical capability to maintain gate voltage with a 5.0 µA load.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Charge pump						
$R_{DS(on)\_HS}$ $R_{DS(on)\_LS}$ V_{THREG}	Charge Pump • High-side Switch On Resistance • Low-side Switch On Resistance • Regulation Threshold Difference	 – – 250	 6.0 5.0 500	 10 9.4 900	 Ω Ω mV	(16), (18)
V_{CP}	Charge Pump Output Voltage • I_{OUT} = 40 mA, 6.0 V < V_{SYS} < 8.0 V • I_{OUT} = 40 mA, V_{SYS} > = 8.0 V	 8.5 12	 9.5 –	 – –	 V	(17), (18)
Gate drive						
$R_{DS(on)\_H\_SRC}$	High-side Driver On Resistance (Sourcing) • V_{PWR} = V_{SUP} = 16 V, -40 °C ≤ T_A ≤ 25 °C • V_{PWR} = V_{SUP} = 16 V, 25 °C < T_A ≤ 135 °C	 – –	 – –	 6.0 8.5	 Ω	
$R_{DS(on)\_H\_SINK}$	High-side Driver On Resistance (Sinking) • V_{PWR} = V_{SUP} = 16 V	–	–	3.0	Ω	
I_{HS_INJ}	High-side Current Injection Allowed Without Malfunction	–	–	0.5	A	(18), (19)
$R_{DS(on)\_L\_SRC}$	Low-side Driver On Resistance (Sourcing) • V_{PWR} = V_{SUP} = 16 V, -40 °C ≤ T_A ≤ 25 °C • V_{PWR} = V_{SUP} = 16 V, 25 °C < T_A ≤ 135 °C	 – –	 – –	 6.0 8.5	 Ω	
$R_{DS(on)\_L\_SINK}$	Low-side Driver On-Resistance (Sinking) • V_{PWR} = V_{SUP} = 16 V	–	–	3.0	Ω	
I_{LS_INJ}	Low-side Current Injection Allowed Without Malfunction	–	–	0.5	A	(18), (19)
V_{GS_H} V_{GS_L}	Gate Source Voltage, V_{PWR} = V_{SUP} = 40 V • High-side, I_{GATE} = 0 • Low-side, I_{GATE} = 0	 13 13	 14.8 15.4	 16.5 17	 V	(20)
$V_{HS\_G\_HOLD}$	Reverse High-side Gate Holding Voltage Gate Output Holding Current = 2.0 µA Gate Output Holding Current = 5.0 µA, V_{SUP}<26 V Gate Output Holding Current = 5.0 µA, V_{SUP}<40 V	 – – –	 10 10 –	 15 15 15	 V	(21)

Notes

16. When VLS is this amount below the normal VLS linear regulation threshold, the charge pump is enabled.
17. V_{SYS} is the system voltage on the input to the charge pump. Recommended external components: 1.0 µF MLC, MUR 120 diode.
18. This parameter is a design characteristic, not production tested.
19. Current injection only occurs during output switch transitions. The IC is immune to specified injected currents for a duration of approximately 1.0 µs after an output switch transition. 1.0 µs is sufficient for all intended applications of this IC.
20. If a slightly higher gate voltage is required, larger bootstrap capacitors are required. At high duty cycles, the bootstrap voltage may not recover completely, leading to a higher output on-resistance. This effect can be minimized by using low ESR capacitors for the bootstrap and the VLS capacitors.
21. High-side Gate Holding voltage is the voltage between the Gate and Source of the high-side FET when held in an on condition. The trickle charge pump supplies bias and holding current for the High-side FET gate driver and output to maintain voltages after bootstrap events. See Figure 11 for typical 100% high-side gate voltage with a 5.0 µA load. This parameter is a design characteristic, not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Overcurrent comparator						
V_{CM}	Common Mode Input Range	2.0	–	V_{DD}-0.02	V	(23)
V_{OS_OC}	Input Offset Voltage	-50	–	50	mV	
V_{OC_HYST}	Overcurrent Comparator Threshold Hysteresis	50		300	mV	(22)
V_{OH} V_{OL}	Output Voltage • High Level at I_{OH} = -500 µA • Low Level at I_{OL} = 500 µA	0.85 V_{DD} –	– –	V_{DD} 0.5	V	
Hold off circuit						
I_{HOLD}	Hold Off Current (At Each GATE Pin) • 3.0 V < V_{SUP} < 40 V, V_{GATE} = 1.0 V	10	–	300	µA	(24)
Phase comparator						
V_{IH_TH}	High Level Input Voltage Threshold	0.5 V_{SUP}	–	0.65 V_{SUP}	V	
V_{IL_TH}	Low Level Input Voltage Threshold	0.3 V_{SUP}	–	0.45 V_{SUP}	V	
V_{OH}	High Level Output Voltage at I_{OH} = -500 µA	0.85 V_{DD}	–	V_{DD}	V	
V_{OL}	Low Level Output Voltage at I_{OL} = 500 µA	–	–	0.5	V	
R_{IN}	High-side Source Input Resistance	–	40	–	kΩ	(22), (27)
Desaturation detector						
V_{DES_TH}	Desaturation Detector Threshold	1.2	1.4	1.6	V	(25)
Current sense amplifier						
R_S	Recommended External Series Resistor (See Figure 9)	–	1.0	–	kW	
R_{FB}	Recommended External Feedback Resistor (See Figure 9) • Limited by the Output Voltage Dynamic Range	5.0	–	15	kW	(28)
V_{ID}	Maximum Input Differential Voltage (See Figure 9) • V_{ID} = V_{AMP_P} - V_{AMP_N}	-800	–	+800	mV	
V_{CM}	Input Common Mode Range	-0.5	–	3.0	V	(22), (26)
V_{OS}	Input Offset Voltage • R_S = 1.0 kΩ, V_{CM} = 0.0 V	-15	–	+15	mV	
$\delta V_{OS}/\delta T$	Input Offset Voltage Drift	–	-10	–	µV/°C	(22)
I_b	Input Bias Current • V_{CM} = 2.0 V	-200	–	+200	nA	

Notes

22. This parameter is a design characteristic, not production tested.
23. As long as one input is in the common mode range there is no phase inversion on the output.
24. The hold off circuit is designed to operate over the full operating range of V_{SUP}. The specification indicates the conditions used in production test. Hold off is activated at V_{POR} or V_{THVLS}.
25. Desaturation is measured as the voltage drop below V_{SUP}, thus the threshold is compared to the drain-source voltage of the external High-side FET. See Figure 5.
26. As long as one input is within V_{CM} the output is guaranteed to have the correct phase. Exceeding the common mode rails on one input will not cause a phase inversion on the output.
27. Input resistance is impedance from the high-side source and is referenced to V_{SS}. Approximate tolerance is ±20%.
28. The current sense amplifier is unity gain stable with a phase margin of approximately 45°. See Figure 10.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense amplifier (continued)						
I_{OS}	Input Offset Current • I_{OS} = I_{AMP_P} - I_{AMP_N}	-80	–	+80	nA	
$\delta I_{OS}/\delta T$	Input Offset Current Drift	–	40	–	pA/°C	(29)
V_{OH} V_{OL}	Output Voltage • High Level with R_{LOAD} = 10 kΩ to V_{SS} • Low Level with R_{LOAD} = 10 kΩ to V_{DD}	V_{DD}-0.2 –	– –	V_{DD} 0.2	V	
R_I	Differential Input Resistance	1.0	–	–	MΩ	
I_{SC}	Output Short-circuit Current	5.0	–	–	mA	
C_I	Common Mode Input Capacitance at 10 kHz	–	–	10	pF	(29), (30)
CMRR	Common Mode Rejection Ratio at DC • CMRR = 20*Log ((V_{OUT_DIFF}/V_{IN_DIFF}) * (V_{IN_CM}/V_{OUT_CM}))	60	80	–	dB	
A_{OL}	Large Signal Open Loop Voltage Gain (DC)	–	78	–	dB	(29), (30)
NL	Nonlinearity • RL = 1.0 kΩ, C_L = 500 pF, 0.3 < V_O < 4.8 V, Gain = 5.0 to 15	-1.0	–	+1.0	%	(29), (30)

Notes

29. This parameter is a design characteristic, not production tested.
30. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supervisory and control circuits						
V_{IH} V_{IL}	Logic Inputs (Px_LS, $\overline{Px\_HS}$, EN1, EN2) • High Level Input Voltage Threshold • Low Level Input Voltage Threshold	2.1 –	– –	– 0.9	V	(32)
V_{IH} V_{IL}	Logic Inputs (SI, SCLK, $\overline{CS}$) • High Level Input Voltage Threshold • Low Level Input Voltage Threshold	2.1 –	– –	– 0.9	V	(31), (32)
V_{IHYS}	Input Logic Threshold Hysteresis • Inputs Px_LS, SI, SCLK, $\overline{CS}$, $\overline{Px\_HS}$, EN1, EN2	100	250	450	mV	(31)
I_{INPD}	Input Pull-down Current, (Px_LS, SI, SCLK, EN1, EN2) • 0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}	8.0	–	18	µA	
I_{INPU}	Input Pull-up Current, ($\overline{CS}$, $\overline{Px\_HS}$) • 0 ≤ V_{IN} ≤ 0.7 V_{DD}	10	–	25	µA	(33)
C_{IN}	Input Capacitance • 0.0 V ≤ V_{IN} ≤ 5.5 V	–	15	–	pF	(31)
$V_{TH\_\overline{RST}}$	$\overline{RST}$ Threshold	1.0	–	2.1	V	(34)
$R_{\overline{RST}}$	$\overline{RST}$ Pull-down Resistance • 0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}	40	60	85	kW	
V_{POR}	Power-OFF $\overline{RST}$ Threshold, (V_{DD} Falling)	3.4	4.0	4.5	V	
V_{SOH}	SO High Level Output Voltage • I_{OH} = 1.0 mA	0.9 V_{DD}	–	–	V	
V_{SOL}	SO Low Level Output Voltage • I_{OL} = 1.0 mA	–	–	0.1 V_{DD}	V	
$I_{SO\_LEAK\_T}$	SO Tri-state Leakage Current • $\overline{CS}$ = 0.7 V_{DD}, 0.3 V_{DD} ≤ V_{SO} ≤ 0.7 V_{DD}	-1.0	–	1.0	µA	
C_{SO_T}	SO Tri-state Capacitance • 0.0 V ≤ V_{IN} ≤ 5.5 V	–	15	–	pF	(31), (35)
V_{OH}	INT High Level Output Voltage • I_{OH} = -500 µA	0.85 V_{DD}	–	V_{DD}	V	
V_{OL}	INT Low Level Output Voltage • I_{OL} = 500 µA	–	–	0.5	V	
Thermal warning						
T_{WARN}	Thermal Warning Temperature	150	170	185	°C	(31), (36)
T_{HYST}	Thermal Hysteresis	8.0	10	12	°C	(31)

Notes

31. This parameter is guaranteed by design, not production tested.
32. Logic threshold voltages derived relative to a 3.3 V 10% system.
33. Pull-up circuits will not allow back biasing of V_{DD}.
34. There are two elements in the $\overline{RST}$ circuit: 1) one generally lower threshold enables the internal regulator; 2) the second removes the reset from the internal logic.
35. This parameter applies to the OFF state (tri-stated) condition of SO is guaranteed by design but is not production tested.
36. The Thermal Warning circuit does not force IC shutdown above this temperature. It is possible to set a bit in the MASK register to generate an interrupt when overtemperature is detected, and the status bit will always indicate if any of the three individual Thermal Warning circuits in the IC sense a fault.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Internal regulators						
t_{PU_VDD}	V_{DD} Power-up Time (Until INT High) • 8.0 V ≤ V_{PWR}	–	–	2.0	ms	(37), (39)
t_{PU_VLS}	VLS Power-up Time • 16 V ≤ V_{PWR}	–	–	2.0	ms	(38), (39)
Charge pump						
F_{OSC}	Charge Pump Oscillator Frequency	90	125	190	kHz	
SR_{CP}	Charge Pump Slew Rate	–	100	–	V/µs	(40)
Gate drive						
t_{ONH}	High-side Turn On Time • Transition Time from 1.0 V to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	–	20	35	ns	(41)
t_{D_ONH}	High-side Turn On Delay • Delay from Command to 1.0 V, (Figure 7)	130	265	386	ns	(42)
t_{OFFH}	High-side Turn Off Time • Transition Time from 10 V to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	–	20	35	ns	(41)
t_{D_OFFH}	High-side Turn Off Delay • Delay from Command to 10 V, (Figure 8)	130	265	386	ns	(42)
t_{ONL}	Low-side Turn On Time • Transition Time from 1.0 V to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	–	20	35	ns	(41)
t_{D_ONL}	Low-side Turn On Delay • Delay from Command to 1.0 V, (Figure 7)	130	265	386	ns	(42)
t_{OFFL}	Low-side Turn Off Time • Transition Time from 10 V to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	–	20	35	ns	(41)
t_{D_OFFL}	Low-side Turn Off Delay • Delay from Command to 10 V, (Figure 8)	130	265	386	ns	(42)

Notes

37. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitor on V_{DD}.
38. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitors on VLS and VLS_CAP. This delay includes the expected time for V_{DD} to rise.
39. This specification is based on capacitance of 0.47 µF on VDD, 2.2 µF on VLS and 2.2 µF on VLS_CAP.
40. The charge pump operating at 12 V V_{SYS}, 1.0 µF pump capacitor, MUR120 diodes and 47 µF filter capacitor.
41. This parameter is guaranteed by characterization, not production tested.
42. These delays include all logic delays except deadtime. All internal logic is synchronous with the internal clock. The total delay includes one clock period for state machine decision block, an additional clock period for FULLON mux logic, input synchronization time and output driver propagation delay. Subtract one clock period for operation in FULLON mode which bypasses the state machine decision block. Synchronization time accounts for up to one clock period of variation. See Figure 6.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Gate drive (continued)						
t_{D_DIFF}	Same Phase Command Delay Match	-20	0.0	+20	ns	(43)
t_{DUR}	Thermal Filter Duration	8.0	–	30	µs	(44)
t_{DC}	Duty Cycle	0.0	–	96	%	(45), (46)
t_{DC}	100% Duty Cycle Duration	–	–	Unlimited	s	(45), (46)
t_{MAX}	Maximum Programmable Deadtime	10.2	15	19.6	µs	(47)
Overcurrent comparator						
t_{OC}	Overcurrent Protection Filter Time	0.9	–	3.5	µs	
t_{ROC}	Rise Time (OC_OUT) • 10% - 90% • C_L = 100 pF	10	–	240	ns	
t_{FOC}	Fall Time (OC_OUT) • 90% - 10% • C_L = 100 pF	10	–	200	ns	
Desaturation detector and phase comparator						
t_R t_F	Phase Comparator Propagation Delay Time to 50% of V_{DD}; C_L ≤ 100 pF • Rising Edge Delay • Falling Edge Delay	– –	– –	200 350	ns	
t_{MATCH}	Phase Comparator Match (Prop Delay Mismatch of Three Phases) • C_L = 100 pF	–	–	100	ns	(45)
t_{BLANK}	Desaturation and Phase Error Blanking Time	4.7	7.1	9.1	µs	(48)
t_{FILT}	Desaturation Filter Time (Filter Time is digital) • Fault Must be Present for This Time to Trigger	640	937	1231	ns	(45)
Current sense amplifier						
t_{SETTLE}	Output Settle Time to 99% • RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5 to 15	–	1.0	2.0	µs	(45), (49)

Notes

43. The maximum separation or overlap of the High and Low-side gate drives, due to propagation delays when commanding one ON and the other OFF simultaneously, is guaranteed by design.
44. The output of the overtemperature comparator goes through a digital filter before generating a warning or interrupt.
45. This parameter is guaranteed by design, not production tested.
46. As duty cycle approaches the limit of 100% or 0% there is a maximum and minimum which is not achievable due to deadtime, propagation delays, switching times and charge time of the bootstrap capacitor (for the High-side FET). 0% is available by definition (FET always OFF) and unlimited ON (100%) is possible as long as gate charge maintenance current is within the trickle charge pump capacity.
47. A Minimum Deadtime of 0.0 can be set via an SPI command. When Deadtime is set via a DEADTIME command, a minimum of 1 clock cycle duration and a maximum of 255 clock cycles is set using the internal time base clock as a reference. Commands exceeding this value limits at this value.
48. Blanking time, t_{BLANK}, is applied to all phases simultaneously when switching ON any output FET. This precludes false errors due to system noise during the switching event.
49. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense amplifier (continued)						
t_{IS_RISE}	Output Rise Time to 90% • RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5.0 to 15	–	–	1.0	µs	(51)
t_{IS_FALL}	Output Fall Time to 10% • RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5.0 to 15	–	–	1.0	µs	(51)
SR(5)	Slew Rate at Gain = 5.0 • RL = 1.0 kΩ, C_L = 20 pF	5.0	–	–	V/µs	(50)
f_M	Phase Margin at Gain = 5.0	–	30	–	°	(50)
G_{BW}	Unity Gain Bandwidth • RL = 1.0 kΩ, C_L = 100 pF	–	20	–	MHz	(50)
BW_G	Bandwidth at Gain = 15 • R_L = 1.0 kΩ, C_L = 50 pF	2.0	–	–	MHz	(50)
CMR	Common Mode Rejection (CMR) with V_{IN} • V_{IN_CM} = 400 mV*sin(2*π*freq*t) • V_{IN_DIF} = 0.0 V, RS = 1.0 kΩ • R_{FB} = 15 kΩ, V_{REFIN} = 0.0 V CMR = 20*Log(V_{OUT}/V_{IN_CM}) • Freq = 100 kHz • Freq = 1.0 MHz • Freq = 10 MHz	 50 40 30	 – – –	 – – –	dB	(50)
Supervisory and control circuits						
t_{PROP}	EN1 and EN2 Propagation Delay	–	–	280	ns	
t_{RINT}	INT Rise Time CL = 100 pF	10	–	250	ns	
t_{FINT}	INT Fall Time CL = 100 pF	10	–	200	ns	
$t_{PROPINT}$	INT Propagation Time	–	–	250	ns	
t_{TRRST}	$\overline{RST}$ Transition Time (Rise and Fall)	–	–	1.25	µs	(50),(52)

Notes

50. This parameter is guaranteed by design, not production tested.
51. Rise and fall times are measured from the transition of a step function on the input to 90% of the change in output voltage.
52. t_{TRRST} is given as a design guideline. The bounds for this specification are VPWR ≤ 58 V, total capacitance on VLS > 1.0 µF.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing						
f_{OP}	Maximum Frequency of SPI Operation	–		4.0	MHz	
f_{TB}	Internal Time Base	13	17	25	MHz	
TC_{TB}	Internal Time Base drift from value at 25 °C	-5.0	–	5.0	%	(53)
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)	100	–	–	ns	(53)
t_{LAG}	Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)	100	–	–	ns	(53)
t_{SISU}	SI to Falling Edge of SCLK (Required Setup Time)	25	–	–	ns	(53)
t_{SIHOLD}	Falling Edge of SCLK to SI (Required Setup Time)	25	–	–	ns	(53)
t_{RSI}	SI, $\overline{CS}$, SCLK Signal Rise Time	–	5.0	–	ns	(53), (54)
t_{FSI}	SI, $\overline{CS}$, SCLK Signal Fall Time	–	5.0	–	ns	(53), (54)
t_{SOEN}	Time from Falling Edge of $\overline{CS}$ to SO Low-impedance	–	55	100	ns	(53), (55)
t_{SODIS}	Time from Rising Edge of $\overline{CS}$ to SO High-impedance	–	100	125	ns	(53), (56)
t_{VALID}	Time from Rising Edge of SCLK to SO Data Valid	–	80	125	ns	(53), (57)
t_{DT}	Time from Rising Edge of $\overline{CS}$ to Falling Edge of the next $\overline{CS}$	200	–	–	ns	(53)

Notes

53. This parameter is guaranteed by design, not production tested.
54. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
55. Time required for valid output status data to be available on SO pin.
56. Time required for output states data to be terminated at SO pin.
57. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

4.4 Timing diagrams

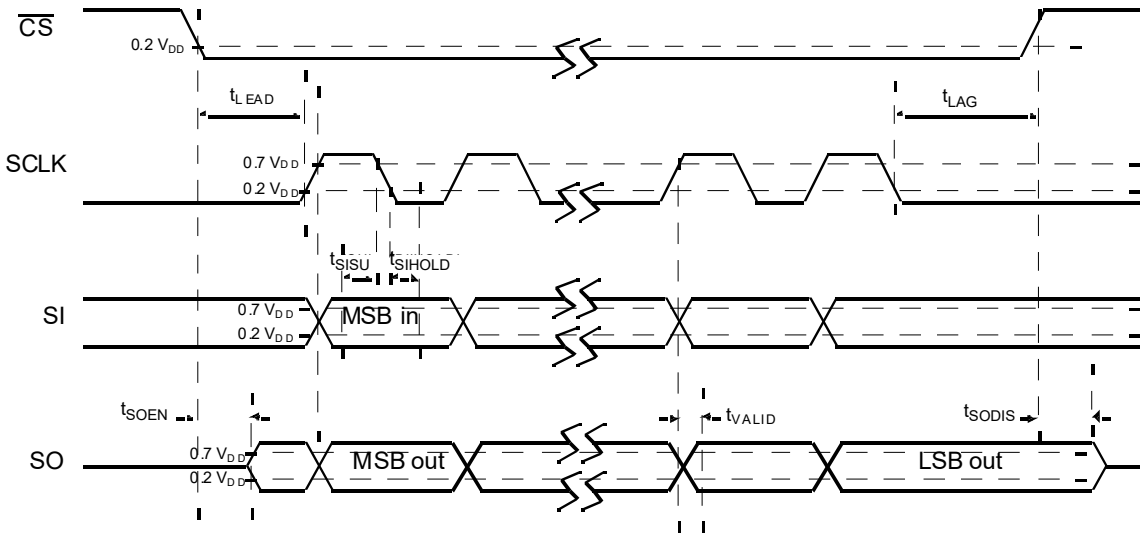


Figure 4. SPI interface timing

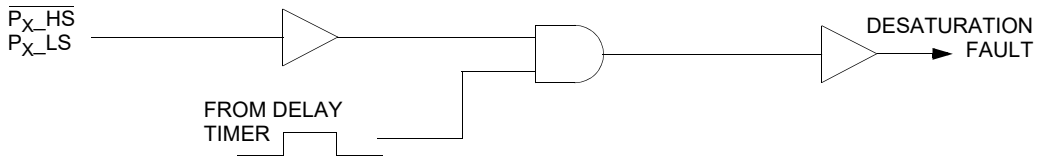


Figure 5. Desaturation blanking and filtering detail

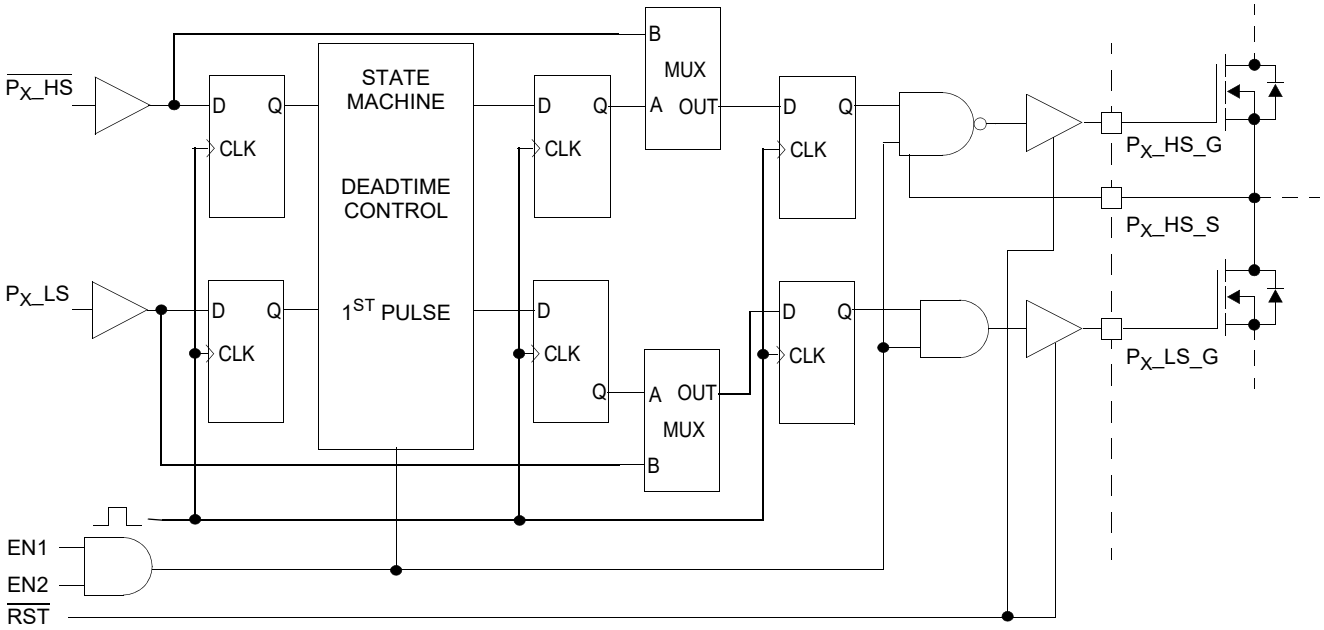


Figure 6. Deadtime control delays

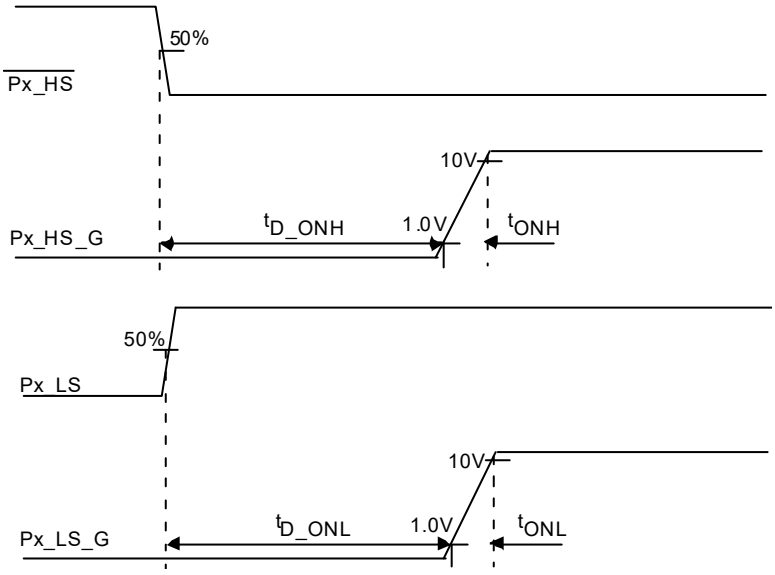


Figure 7. Driver turn-on time and turn-on delay

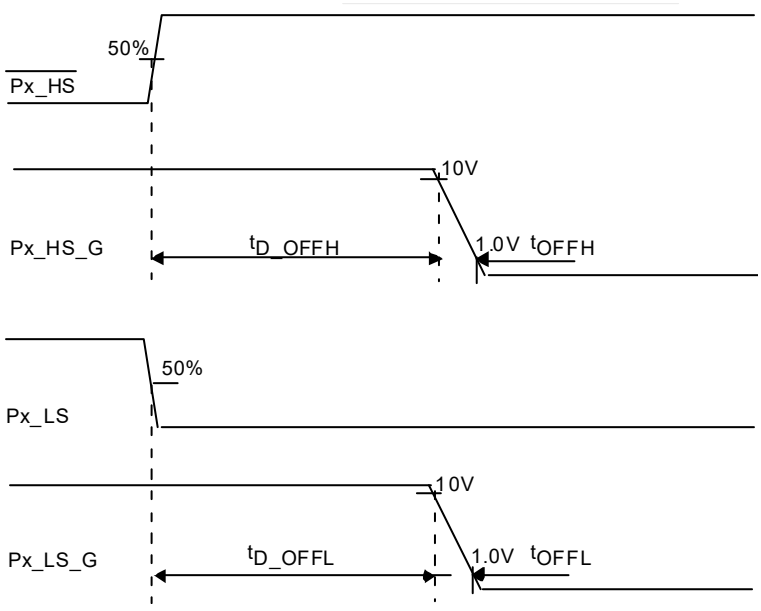


Figure 8. Driver turn-off time and turn-off delay

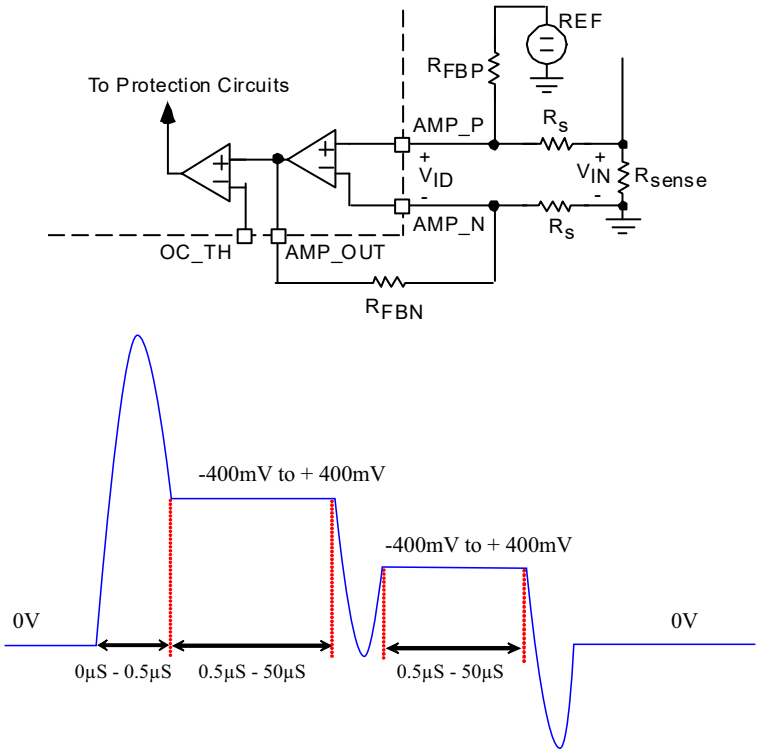


Figure 9. Current amplifier and input waveform (V_{IN} voltage across R_{SENSE})

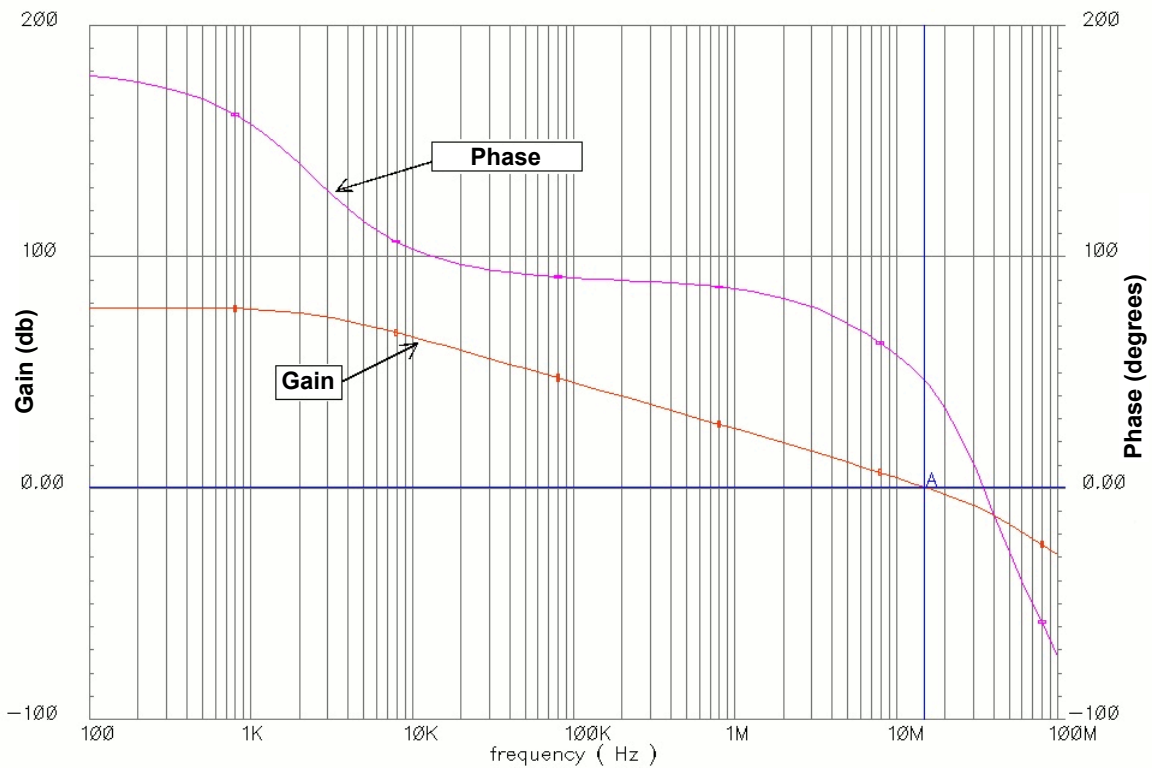


Figure 10. Typical amplifier open-loop gain and phase vs. frequency

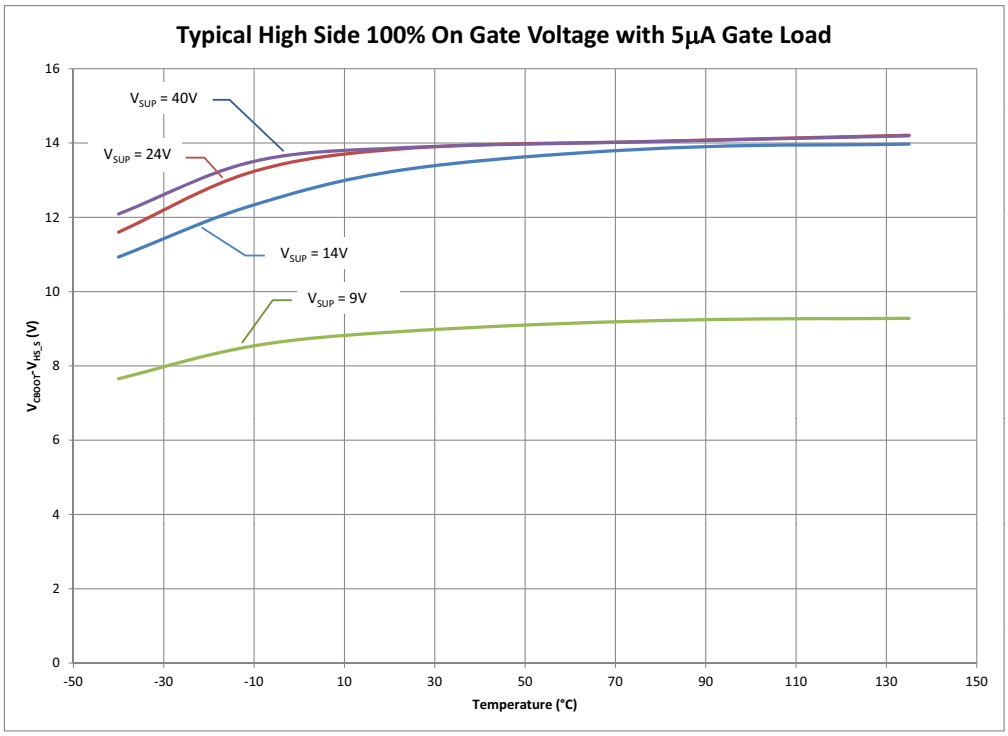


Figure 11. Typical high-side 100% on gate voltage with 5.0 µA gate load

5 Functional descriptions

5.1 Introduction

The 33937A provides an interface between an MCU and the large FETs used to drive three phase loads. A typical load FET may have an on resistance of 4.0 mΩ or less and could require a gate charge of over 400 nC to fully turn on. The IC can operate in automotive 12 V to 42 V environments.

Because there are so many methods of controlling three phase systems, the IC enforces few constraints on driving the FETs. It does provide deadtime (cross-over) blanking and logic, both of which can be overridden, ensuring both FETs in a phase are not simultaneously enabled. A SPI port is used to configure the IC modes.

5.2 Functional pin description

5.2.1 Phase A (PHASEA)

This pin is the totem pole output of the Phase A comparator. This output is low when the voltage on Phase A high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP}.

5.2.2 Power ground (PGND)

This pin is power ground for the charge pump. It should be connected to VSS, however routing to a single point ground on the PCB may help to isolate charge pump noise.

5.2.3 Enable 1 and enable 2 (EN1, EN2)

Both of these logic signal inputs must be high to enable any gate drive output. When either or both are low, the internal logic (SPI port, etc.) still functions normally, but all gate drives are forced off (external power FET gates pulled low). The signal is asynchronous.

When EN1 and EN2 return high to enable the outputs, each LS driver must be pulsed ON before the corresponding HS driver can be commanded ON. This ensures that the bootstrap capacitors are charged. See 7.3, Initialization requirements on page 41.

5.2.4 Reset ($\overline{\text{RST}}$)

When the reset pin is low the integrated circuit (IC) is in a low power state. In this mode, all outputs are disabled, internal bias circuits are turned off, and a small pull-down current is applied to the output gate drives. The internal logic will be reset within 77 ns of RESET going low. When $\overline{\text{RST}}$ is low, the IC consumes minimal current.

5.2.5 Charge pump out (PUMP)

This pin is the switching node of the charge pump circuit. The output of the internal charge pump support circuit. When the charge pump is used, it is connected to the external pumping capacitor. This pin may be left floating if the charge pump is not required.

5.2.6 Charge pump input (VPUMP)

This pin is the input supply for the charge pump circuit. When the charge pump is required, this pin should be connected to a polarity protected supply. This input should never be connected to a supply greater than 40 V. If the charge pump is not required this pin may be left floating.

5.2.7 VSUP input (VSUP)

The supply voltage pin should be connected to the common connection of the high-side FETs. It is the reference bias for the Phase Comparators and Desaturation Comparator. It is also used to provide power to the internal steady state trickle charge pump and to energize the hold off circuit.

5.2.8 Phase B (PHASEB)

This pin is the totem pole output of the Phase B comparator. This output is low when the voltage on Phase B high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP}.

5.2.9 Phase C (PHASEC)

This pin is the totem pole output of the Phase C comparator. This output is low when the voltage on Phase C high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP}.

5.2.10 Phase A high-side input ($\overline{\text{PA\_HS}}$)

This input logic signal pin enables the high-side driver for Phase A. The signal is active low, and is pulled up by an internal current source.

5.2.11 Phase A low-side input (PA_LS)

This input logic signal pin enables the low-side driver for Phase A. The signal is active high, and is pulled down by an internal current sink.

5.2.12 VDD Voltage Regulator (VDD)

VDD is an internally generated 5.0 V supply. The internal regulator provides continuous power to the IC and is a supply reference for the SPI port. A 0.47 µF (min) decoupling capacitor must be connected to this pin. This regulator is intended for internal IC use and can supply only a small (1.0 mA) external load current. A power-on-reset (POR) circuit monitors this pin and until the voltage rises above the threshold, the internal logic will be reset; driver outputs are tri-stated and SPI communication is disabled. The VDD regulator can be disabled by asserting the $\overline{\text{RST}}$ signal low. The VDD regulator is powered from the VPWR pin.

5.2.13 Phase B high-side control input ($\overline{\text{PB\_HS}}$)

This pin is the input logic signal, enabling the high-side driver for Phase B. The signal is active low, and is pulled up by an internal current source.

5.2.14 Phase B low-side input (PB_LS)

This pin is the input logic signal, enabling the low-side driver for Phase B. The signal is active high, and is pulled down by an internal current sink.

5.2.15 Interrupt (INT)

The Interrupt pin is a totem pole logic output. When a fault is detected, this pin pulls high until it is cleared by executing the Clear Interrupt command via the SPI port. The faults capable of causing an interrupt can be masked via the MASK0 and MASK1 SPI registers to customize the response.

5.2.16 Chip select ($\overline{\text{CS}}$)

Chip select is a logic input that frames the SPI commands and enables the SPI port. This signal is active low, and is pulled up by an internal current source.

5.2.17 Serial in (SI)

The Serial In pin is used to input data to the SPI port. Clocked on the falling edge of SCLK, it is the most significant bit (MSB) first. This pin is pulled down by an internal current sink.

5.2.18 Serial clock (SCLK)

This logic input is the clock is used for the SPI port. The SCLK typically runs at 3.0 MHz (up to 5.0 MHz) and is pulled down by an internal current sink.

5.2.19 Serial out (SO)

Output data for the SPI port streams from this pin. It is tri-stated until $\overline{CS}$ is low. New data appears on rising edges of SCLK in preparation for latching by the falling edge of SCLK on the master.

5.2.20 Phase C low-side input (PC_LS)

This input logic pin enables the low-side driver for Phase C. This pin is an active high, and is pulled down by an internal current sink.

5.2.21 Phase C high-side input ($\overline{PC\_HS}$)

This input logic pin enables the high-side driver for Phase C. This signal is active low, and is pulled up by an internal current source.

5.2.22 Amplifier output (AMP_OUT)

This pin is the output for the current sensing amplifier. It is also the sense input to the overcurrent comparator.

5.2.23 Amplifier inverting input (AMP_N)

The inverting input to the current sensing amplifier.

5.2.24 Amplifier non-inverting input (AMP_P)

The non-inverting input to the current sensing amplifier.

5.2.25 Overcurrent comparator output (OC_OUT)

The overcurrent comparator output is a totem pole logic level output. A logic high indicates an overcurrent condition.

5.2.26 Overcurrent comparator threshold (OC_TH)

This input sets the threshold level of the overcurrent comparator.

5.2.27 Voltage source supply (VSS)

VSS is the ground reference for the logic interface and power supplies.

5.2.28 Ground (GND0, GND1)

These two pins are connected internally to VSS by a 1.0 Ω resistor. They provide device substrate connections and also the primary return path for ESD protection.

5.2.29 VLS regulator capacitor (VLS_CAP)

This connection is for a capacitor which provides a low-impedance for switching currents on the gate drive. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents must be connected between this pin and VSS. This is the same DC node as VLS, but it is physically placed on the opposite end of the IC to minimize the source impedance to the gate drive circuits.

5.2.30 Phase C low-side source (PC_LS_S)

The phase C low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for phase C.

5.2.31 Phase C low-side gate (PC_LS_G)

This is the gate drive for the Phase C low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.32 Phase C high-side source (PC_HS_S)

The source connection for the Phase C high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.33 Phase C high-side gate (PC_HS_G)

This is the gate drive for the Phase C high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.34 Phase C bootstrap (PC_BOOT)

This is the bootstrap capacitor connection for Phase C. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.35 Phase B low-side source (PB_LS_S)

The Phase B low-side source is the pin used to return the gate currents from the Low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for Phase B.

5.2.36 Phase B low-side gate (PC_LS_G)

This is the gate drive for the Phase B low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.37 Phase B high-side source (PB_HS_S)

The source connection for the Phase B high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.38 Phase B high-side gate (PB_HS_G)

This is the gate drive for the Phase B high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.39 Phase B bootstrap (PB_BOOT)

This is the bootstrap capacitor connection for phase B. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.40 PHASE A low-side source (PA_LS_S)

The Phase A low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for phase A.

5.2.41 Phase A low-side gate (PA_LS_G)

This is the gate drive for the Phase A low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.42 Phase A high-side source (PA_HS_S)

The source connection for the Phase A high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.43 Phase A high-side gate (PA_HS_G)

This is the gate drive for the Phase A high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.44 Phase A bootstrap (PA_BOOT)

This is the bootstrap capacitor connection for phase A. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.45 VLS regulator (VLS)

VLS is the gate drive power supply regulated at approximately 15 V. This is an internally generated supply from VPWR. It is the source for the low-side gate drive voltage, and also the high-side bootstrap source. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents, must be connected between this pin and VSS.

5.2.46 VPWR input (VPWR)

VPWR is the power supply input for VLS and VDD. Current flowing into this input recharges the bootstrap capacitors as well as supplying power to the low-side gate drivers and the VDD regulator. An internal regulator regulates the actual gate voltages. This pin can be connected to system battery voltage if power dissipation is not a concern.

5.2.47 Exposed pad (EP)

The primary function of the exposed pad is to conduct heat out of the device. This pad may be connected electrically to the substrate of the device.The device performs as specified with the exposed pad un-terminated (floating). However, it is recommended the exposed pad be terminated to pin 29 (VSS) and the system ground.