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Document Number: MC33989
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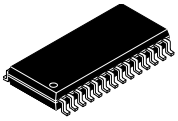
System Basis Chip with High Speed CAN Transceiver

33989

SYSTEM BASIS CHIP WITH HIGH SPEED CAN



EG SUFFIX (PB-FREE)
98ASB42345B
28-PIN SOICW

The 33989 is a monolithic integrated circuit combining many functions used by microcontrollers (MCU) found in automotive Engine Control Units (ECUs). The device incorporates functions such as: two voltage regulators, four high-voltage (wake-up) inputs, a 1.0 Mbaud capable CAN physical interface, an SPI interface to the MCU and VSUP monitoring and fault detection circuitry. The 33989 also provides reset control in conjunction with VSUP monitoring and the watchdog timer features. Also, an Interrupt can be generated, for the MCU, based on CAN bus activity as well as mode changes.

Features

- V_{DD1}: Low drop voltage regulator, current limitation, overtemperature detection, monitoring, and reset function
- V_{DD1}: Total current capability 200 mA
- V2: Tracking function of V_{DD1} regulator. Control circuitry for external bipolar ballast transistor for high flexibility in choice of peripheral voltage and current supply
- Low stand-by current consumption in Stop and Sleep modes
- High speed 1.0 MBaud CAN physical interface
- Four external high voltage wake-up inputs associated with HS1 V_{BAT} switch
- 150 mA output current capability for HS1 V_{BAT} switch allowing drive of external switches pull-up resistors or relays
- V_{SUP} failure detection
- 40 V maximum transient voltage

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33989PEG/R2	-40 to 125 °C	28 SOICW

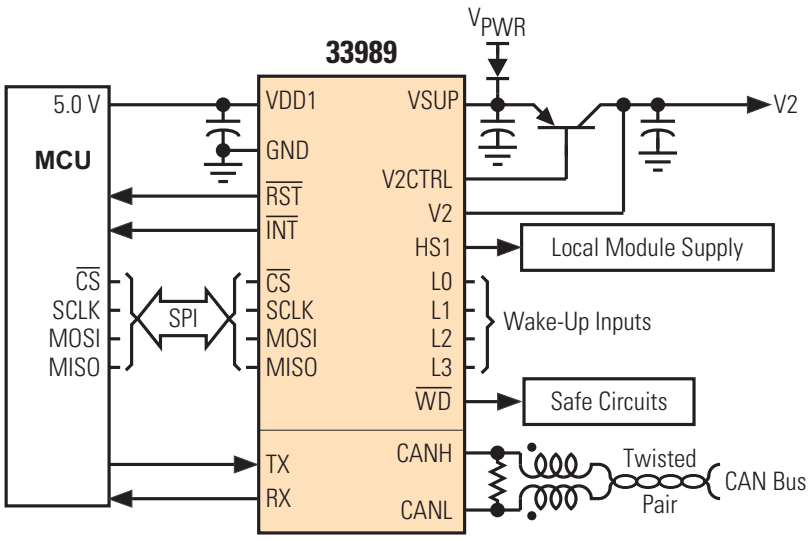


Figure 1. MC33989 Simplified Application Diagram

*This document contains certain information on a product under development.
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INTERNAL BLOCK DIAGRAM

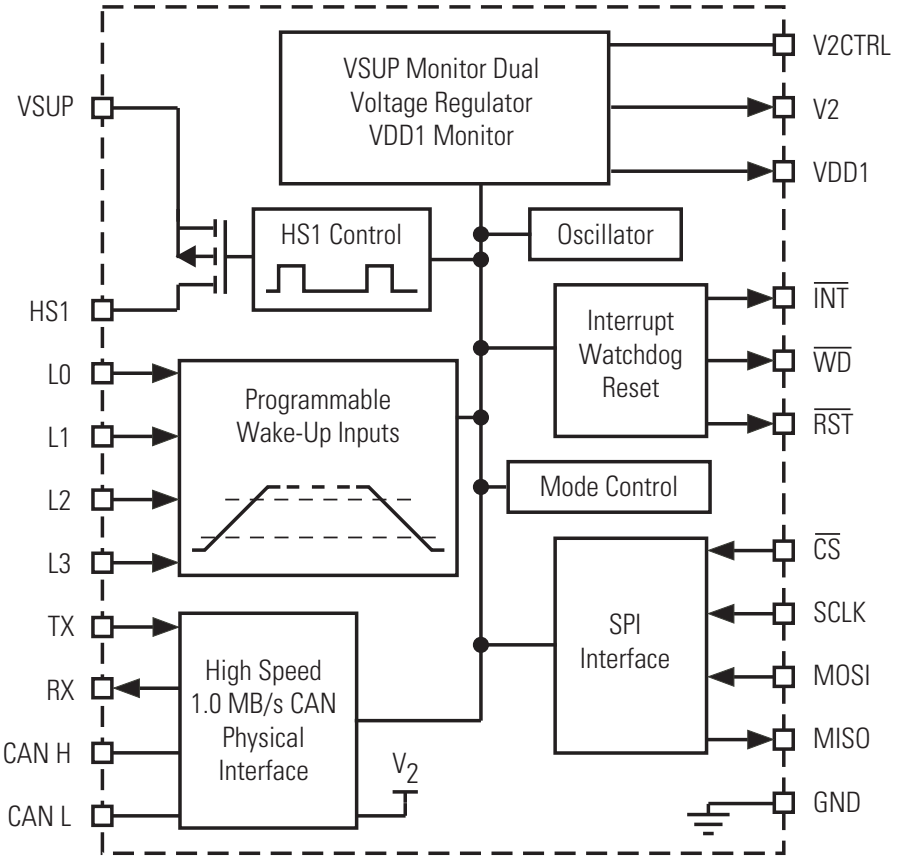


Figure 2. 33989 Simplified Internal Block Diagram

PIN CONNECTIONS

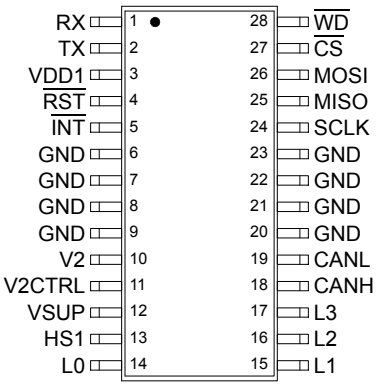


Figure 3. 33989 Pin Connections

Table 1. 33989 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 18.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	RX	Output	Receive Data	CAN bus receive data output pin.
2	TX	Input	Transmit Data	CAN bus transmit data input pin.
3	VDD1	Power Output	Voltage Digital Drain One	5.0 V regulator output pin. Supply pin for the MCU.
4	$\overline{\text{RST}}$	Output	Reset	This is the device reset output pin whose main function is to reset the MCU. This pin has an internal pullup current source to VDD.
5	$\overline{\text{INT}}$	Output	Interrupt	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
6–9 20–23	GND	Ground	Ground	These device ground pins are internally connected to the package lead frame to provide a 33989-to-PCB thermal path.
10	V2	Input	Voltage Source Two	Sense input for the V2 regulator using an external series pass transistor. V2 is also the internal supply for the CAN transceiver.
11	V2CTRL	Power Output	Voltage Control	Output drive source for the V2 regulator connected to the external series pass transistor.
12	VSUP	Power	Voltage Supply	Supply input pin for the 33989.
13	HS1	Output	High Side One	Output of the internal high side switch. The output current is internally limited to 150 mA.
14–17	L0:L3	Input	Level 0: 3	Inputs from external switches or from logic circuitry.
22	CANH	Output	CAN High	CAN high output pin.
23	CANL	Output	CAN Low	CAN low output pin.
24	SCLK	Input	System Clock	Clock input pin for the serial peripheral interface (SPI).
25	MISO	Output	Master In/Slave Out	SPI data sent to the MCU by the 33989. When $\overline{\text{CS}}$ is HIGH, the pin is in the high-impedance state.
26	MOSI	Input	Master Out/Slave In	SPI data received by the 33989.
27	$\overline{\text{CS}}$	Input	Chip Select	The $\overline{\text{CS}}$ input pin is used with the SPI bus to select the 33989.
28	$\overline{\text{WD}}$	Output	Watch Dog	The $\overline{\text{WD}}$ output pin is asserted LOW if the software watchdog is not correctly triggered.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage at VSUP			V
Continuous (Steady-state)	V_{SUP}	-0.3 to 27	
Transient Voltage (Load Dump)	V_{SUP}	-0.3 to 40	
Logic Signals (RX, TX, MOSI, MISO, $\overline{CS}$, SCLK, $\overline{RST}$, $\overline{WD}$, and $\overline{INT}$)	V_{LOG}	-0.3 to V_{DD1} + 0.3	V
Output Current VDD1	I	Internally Limited	A
HS1			
Voltage	V	-0.3 to V_{SUP} + 0.3	V
Output Current	I	Internally Limited	A
ESD Voltage, Human Body Model (1)			kV
HS1, L0, L1, L2, L3	V_{ESDH}	- 4.0 to 4.0	
All Other Pins		-2.0 to 2.0	
ESD Voltage Machine Model	V_{ESDM}		V
All Pins Except CANH and CANL		±200	
L0, L1, L2, L3	V_{WUDC}		
DC Input Voltage		-0.3 to 40	V
DC Input Current		-2.0 to 2.0	mA
Transient Input Voltage with External Component (2)		-100 to 100	V
CANL and CANH Continuous Voltage	$V_{CANH/L}$	-27 to 40	V
CANL and CANH Continuous Current	$I_{CANH/L}$	200	mA
CANH and CANL Transient Voltage (Load Dump) (4)	$V_{TRH/L}$	40	V
CANH and CANL Transient Voltage (5)	$V_{TRH/L}$	-40 to 40	V
Logic Inputs (TX and RX)	V	-0.5 to 6.0	V
ESD Voltage (HBM 100 pF, 1.5 k) CANL, CANH	V_{ESDCH}	-4.0 to 4.0	KV
ESD Voltage Machine Model	V_{ESDCM}		V
CANH and CANL		-200 to 200	

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, 1.5 k), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
2. According to ISO 7637 specification. See **Table 6**, page 24.
3. Load Dump test according to ISO 7637 part 1.
4. Transient test according to ISO 7637 part 1, pulses 1, 2, 3a, and 3b according to schematic in **Table 17**, page 37.

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Operating Junction Temperature	T_J	-40 to 150	°C
Storage Temperature	T_S	-55 to 165	°C
Ambient Temperature	T_A	-40 to 125	°C
Thermal Resistance Junction to GND Pins (5)	$R_{\theta J/P}$	20	°C/W
Peak Package Reflow Temperature During Reflow (6), (7)	T_{PPRT}	Note 7.	°C

Notes

5. Ground pins 6, 7, 8, 9, 20, 21, 22, and 23
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VSUP)					
Nominal DC Supply Voltage Range	V_{SUP}	5.5	—	18	V
Extended DC Voltage Range 1 Reduced Functionality (8)	V_{SUPEX1}	4.5	—	5.5	V
Extended DC Voltage Range 2 (9)	V_{SUPEX2}	18	—	27	V
Input Voltage During Load Dump Load Dump Situation	V_{SUPLD}	—	—	40	V
Input Voltage During Jump Start Jump Start Situation	V_{SUPJS}	—	—	27	V
Supply Current in Standby Mode (10) (11) I_{OUT} at V_{DD1} = 40 mA CAN recessive or Sleep-Disable State	$I_{SUP(STDBY)}$	—	42	45	mA
Supply Current in Normal Mode (10) I_{OUT} at V_{DD1} = 40 mA CAN recessive or Sleep-Disable State	$I_{SUP(NORM)}$	—	42.5	45	mA
Supply Current in Sleep Mode (10) (11) V_{DD1} and V2 OFF, V_{SUP} < 12 V, Oscillator Running (12) CAN in Sleep-Disable State	$I_{SUP(SLEEP1)}$	—	72	105	µA
Supply Current in Sleep Mode (10) (11) V_{DD1} and V2 OFF, V_{SUP} < 12 V, Oscillator Not Running (12) CAN in Sleep-Disable State	$I_{SUP(SLEEP2)}$	—	57	90	µA
Supply Current in Sleep Mode (10) (11) V_{DD1} and V2 OFF, V_{SUP} > 12 V, Oscillator Running (12) CAN in Sleep-Disable State	$I_{SUP(SLEEP3)}$	—	100	150	µA
Supply Current in Stop Mode I_{OUT} V_{DD1} < 2.0 mA (10) (11) V_{DD1} ON, V_{SUP} < 12 V, Oscillator Running (12) CAN in Sleep-Disable State	$I_{SUP(STOP1)}$	—	135	210	µA
Supply Current in Stop Mode I_{OUT} V_{DD1} < 2.0 mA (11) V_{DD1} ON, V_{SUP} < 12 V, Oscillator Not Running (12) CAN in Sleep-Disable State	$I_{SUP(STOP2)}$	—	130	210	µA
Supply Current in Stop Mode I_{OUT} V_{DD1} < 2.0 mA (10) (11) V_{DD1} ON, V_{SUP} > 12 V, Oscillator Running (12) CAN in Sleep-Disable State	$I_{SUP(STOP3)}$	—	160	230	µA
BATFAIL Flag Internal Threshold	VBF	1.5	3.0	4.0	V

Notes

8. V_{DD1} > 4.0 V, Reset high, logic pin high level reduced, device is functional.
9. Device is fully functional. All functions are operating. All modes available and operating. Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0:L3 inputs operating, SPI read/write operation. Overtemperature may occur.
10. Current measured at the VSUP pin.
11. With CAN cell in Sleep-Disable state. If CAN cell is Sleep-Enabled for wake-up, an additional 60 µA must be added to specified value.
12. Oscillator running means Forced Wake-up or Cyclic Sense of Software Watchdog is Stop mode are not activated.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BATFAIL Flag Hysteresis (13)	$VBF_{(HYS)}$	—	1.0	—	V
Battery Fall Early Warning Threshold In Normal and Standby Mode	BF_{EW}	5.3	5.8	6.3	V
Battery Fall Early Warning Hysteresis In Normal and Standby Mode (13)	BF_{EWH}	0.1	0.2	0.3	V
POWER OUTPUT (VDD1) (14)					
VDD1 Output Voltage I_{DD1} from 2.0 to 200 mA T_{AMB} -40 to 125 °C, 5.5 V < V_{SUP} < 27 V	V_{DD1OUT}	4.9	5.0	5.1	V
VDD1 Output Voltage I_{DD1} from 2.0 to 200 mA, 4.5 V < V_{SUP} < 5.5 V	$V_{DD1OUT2}$	4.0	—	—	V
Dropout Voltage I_{DD1} = 200 mA	V_{DD1DRP}	—	0.2	0.5	V
Dropout Voltage, Limited Output Current I_{DD1} = 50 mA, 4.5 V < V_{SUP}	$V_{DD1DRP2}$	—	0.1	0.25	V
I_{DD1} Output Current Internally Limited	I_{DD1}	200	285	350	mA
Junction Thermal Shutdown Normal or Standby Modes	T_{SD}	160	—	200	°C
Junction Overtemperature Pre-warning V_{DDTEMP} Bit Set	T_{PW}	125	—	160	°C
Temperature Threshold Difference	T_{SD} - T_{PW}	20	—	40	°C
Reset Threshold 1 Selectable by SPI. Default Value After Reset.	RST_{TH1}	4.5	4.6	4.7	V
Reset Threshold 2 Selectable by SPI	RST_{TH2}	4.1	4.2	4.3	V
V_{DD1} Range for Reset Active	V_{DDR}	1.0	—	—	V
Reset Delay Time Measured at 50% of Reset Signal	t_D	4.0	—	30	µs
Line Regulation (C at V_{DD1} = 47 µF Tantal) 9.0 V V_{SUP} < 18, I_{DD} = 10 mA	LR1	—	5.0	25	mV
Line Regulation (C at V_{DD1} = 47 µF Tantal) 5.5 < V_{SUP} < 27 V, I_{DD} = 10 mA	LR2	—	10	25	mV
Load Regulation (C at V_{DD1} = 47 µF Tantal) 1.0 mA < I_{IDD} < 200 mA	LD	—	25	75	mV
Thermal Stability V_{SUP} = 13.5 V, 1 = -100 mA Not Tested (15)	$THERM_S$	—	30	50	mV

Notes

13. With CAN cell in Sleep-Disable state. If CAN cell is Sleep-Enabled for wake-up, an additional 60 µA must be added to specified value.
14. I_{DD1} is the total regulator output current. V_{DD} specification with external capacitor. Stability requirement: C > 47 µF ESR < 1.3 Ω (tantalum capacitor). In reset, normal request, normal and standby modes. Measure with C = 47 µF Tantalum.
15. Guaranteed by design; however, it is not production tested.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (VDD1) IN STOP MODE (16)					
VDD1 Output Voltage I_{DD1} < = 2.0 mA	V_{DDSTOP}	4.75	5.00	5.25	V
VDD1 Output Voltage I_{DD1} < = 10 mA	$V_{DDSTOP2}$	4.75	5.00	5.25	V
I_{DD1} Stop Output Current to Wake-up SBC	I_{DD1SWU}	10	17	25	mA
I_{DD1} Overcurrent to Wake-up Deglitcher Time (17)	$I_{DD1DGLT}$	40	55	75	µs
Reset Threshold	RST_{STOP1}	4.5	4.6	4.7	V
Reset Threshold	RST_{STOP2}	4.1	4.2	4.3	V
Line Regulation (C at V_{DD1} = 47 µF Tantal) 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	LR_S	—	5.0	25	mV
Load Regulation (C at V_{DD1} = 47 µF Tantal) 1.0 mA < I_{DD} < 10 mA	LD_S	—	15	75	mV
Max Decoupling Capacitor at VDD1 Pin, in Stop Mode(18)	$V_{DDst-cap}$	—	—	200	µF
TRACKING VOLTAGE REGULATOR (V2) (19)					
V2 Output Voltage (C at V2 = 10 µF Tantal) I2 from 2.0 to 200 mA, 5.5 V < V_{SUP} < 27 V	V2	0.99	1.0	1.01	V_{DD1}
I2 Output Current (for information only) Depending Upon External Ballast Transistor	I2	200	—	—	mA
V2 Control Drive Current Capability Worst Case at T_J = 125 °C	12_{CTRL}	0.0	—	10	mA
V2LOW Flag Threshold	$V2L_{TH}$	3.75	4.0	4.25	V
LOGIC OUTPUT PIN (MISO) (20)					
Low Level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	—	1.0	V
High Level Output Voltage I_{OUT} = 250 µA	V_{OH}	$V_{DD1-0.9}$	—	V_{DD1}	V
Tri-Stated MISO Leakage Current 0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	—	2.0	µA

Notes

16. If stop mode is used, the capacitor connected at VDD pin should not exceed the maximum specified by the "$V_{DDST-CAP}$" parameter. If capacitor value is exceeded, upon entering stop mode, VDD output current may exceed the I_{DDSWU} and prevent the device to stay in stop mode.
17. Guaranteed by design; however, it is not production tested.
18. Guaranteed by design.
19. V2 specification with external capacitor
    - Stability requirement: C > 42 µF and ESR < 1.3 Ω (Tantalum capacitor), external resistor between base and emitter required
    - Measurement conditions: Ballast transistor MJD32C, C = 10 µF Tantalum, 2.2 k resistor between base and emitter of ballast transistor
20. Push/Pull structure with tri-state condition $\overline{CS}$ high.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT PINS (MOSI, SCLK, $\overline{CS}$)					
High Level Input Voltage	V_{IH}	0.7 V_{DD1}	—	V_{DD1} + 0.3	V
Low Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD1}	V
High Level Input Current on $\overline{CS}$	L_{IH}	-100	—	-20	µA
Low Level Input Current on $\overline{CS}$	L_{IL}	-100	—	-20	µA
MOSI and SCLK Input Current	L_N	-10	—	10	µA
RESET PIN ($\overline{RST}$) (21)					
High Level Output Current 0 < V_{OUT} < 0.7 V_{DD}	I_{OH}	-300	-250	-150	µA
Low Level Output Voltage (I_0 = 1.5 mA) 5.5 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
Low Level Output Voltage (I_0 = 0 µA 1.0 V < V_{SUP} < 5.5 V	V_{OL}	0.0	—	0.9	V
Reset Pull-down Current V > 0.9 V	I_{PDW}	2.3	—	5.0	mA
Reset Duration After V_{DD1} High	RST_{DUR}	3.0	3.4	4.0	ms
WATCHDOG OUTPUT PIN ($\overline{WD}$) (22)					
Low Level Output Voltage (I_0 = 1.5 mA) 1.0 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
High Level Output Voltage (I_0 = 250 µA)	V_{OH}	V_{DD1}-0.9	—	V_{DD1}	V
INTERRUPT PIN ($\overline{INT}$) (22)					
Low Level Output Voltage (I_0 = 1.5 mA)	V_{OL}	0.0	—	0.9	V
High Level Output Voltage (I_0 = 250 µA)	V_{OH}	V_{DD1}-0.9	—	V_{DD1}	V
HIGH SIDE OUTPUT PIN (HS1)					
R_{DSON} at T_J = 25 °C, and I_{OUT} - 150 mA V_{SUP} > 9.0 V	RON_{25}	—	2.0	2.5	Ω
R_{DSON} at T_A = 125 °C, and I_{OUT} - 150 mA V_{SUP} > 9.0 V	RON_{125}	—	—	4.5	Ω
R_{DSON} at T_A = 125 °C, and I_{OUT} - 120 mA 5.5 < V_{SUP} < 9.0 V	RON_{125-2}	—	3.5	5.5	Ω
Output Current Limitation	L_{LIM}	160	—	500	mA
HS1 Overtemperature Shutdown	O_{VT}	155	—	190	°C
HS1 Leakage Current	L_{LEAK}	—	—	10	µA
Output Clamp Voltage at I_{OUT} = -10 mA No Inductive Load Drive Capability	V_{CL}	-1.5	—	-0.3	V

Notes
21. Push/Pull structure with tri-state condition $\overline{CS}$ high.
22. Output pin only. Supply from VDD1. Structure switch to ground with pull-up current source.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS (L0:L3)					
Negative Switching Threshold	V_{THN}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.6	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
Positive Switching Threshold	V_{THP}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.6	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.6	—	1.3	
Input Current	L_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	—	10	
CAN SUPPLY (V2)					
Supply Current Cell	I_{RES}				mA
Recessive State		—	1.5	3.0	
Supply Current Cell	I_{DOM}				mA
Dominant State without Bus Load		—	2.0	6.0	
Supply Current Cell, CAN in Sleep State Wake-up Enable	I_{SLEEP}				µA
V2 Regulator OFF		—	55	70	
Supply Current Cell, CAN in Sleep State Wake-up Disable	I_{DIS}				µA
V2 Regulator OFF (23)		—	—	1.0	

Notes
23. Push/Pull structure.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CANH AND CANL					
Bus Pins Common Mode Voltage	V_{CM}	-27	—	40	V
Differential Input Voltage (Common Mode Between -3.0 and 7.0 V)	V_{CANH}-V_{CANL}				mV
Recessive State at RXD		—	—	500	
Dominant State at RXD		900	—	—	
Differential Input Hysteresis (RXD)	V_{HYS}	100	—	—	mV
Input Resistance	R_{IN}	5.0	—	100	KΩ
Differential Input Resistance	R_{IND}	10	—	100	KΩ
Unpowered Node Input Current	I_{CANUP}	—	—	1.5	mA
CANH Output Voltage					V
TXD Dominant State	V_{CANHD}	2.75	—	4.5	
TXD Recessive State	V_{CANHR}	—	—	3.0	
CANL Output Voltage					V
TXD Dominant State	V_{CANLD}	0.5	—	2.25	
TXD Recessive State	V_{CANLR}	2.0	—	—	
Differential Output Voltage					
TXD Dominant State	V_{DIFFD}	1.5	—	3.0	V
TXD Recessive State	V_{DIFFR}	—	—	100	mV
CANH AND CANL					
Output Current Capability (Dominant State)					mA
CANH	I_{CANH}	—	—	-35	
CANL	I_{CANL}	35			
Overtemperature Shutdown	T_{SHUT}	160	180°C	—	°C
CANL Overcurrent Detection	$I_{CANL/OC}$				mA
Error Reported in CANR		60	—	200	
CANH Overcurrent Detection	$I_{CANH/OC}$				mA
Error Reported in CANR		-200	—	-60	
TX AND RX					
TX Input High Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} + 0.4	V
TX Input Low Voltage	V_{ILP}	-0.4	—	0.3 V_{DD}	V
TX High Level Input Current, VTX = V_{DD}	L_{IH}	-10	—	10	µA
TX Low Level Input Current, VTX = 0 V	L_{IL}	-100	-50	-20	µA
RX Output Voltage High, IRX = 250 µA	V_{OH}	VDD-1	—	—	V
RX Output Voltage Low, IRX = 1.0 mA	V_{OL}	—	—	0.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING (SCLK, $\overline{CS}$, MOSI, MISO)					
SPI Operation Frequency	F_{REQ}	0.25	—	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	—	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	—	N/A	ns
SCLK Clock Low Time	t_{WSCLKH}	125	—	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	—	N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	100	—	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	40	—	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	40	—	N/A	ns
MISO Rise Time (C_L = 220 pF)	t_{RSO}	—	25	50	ns
MISO Fall Time (C_L = 220 pF)	t_{FSO}	—	25	50	ns
Time from Falling or Rising Edges of $\overline{CS}$ to: MISO Low-impedance MISO High-impedance	t_{SOEN} t_{SODIS}	 — —	 — —	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid 0.2 V1 = <MISO> = 0.8 V1, C_L = 200 pF	t_{VALID}	—	—	50	ns
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WD}$, $\overline{INT}$)					
Delay Between $\overline{CS}$ Low to High Transition (End of SPI Stop Command) and Stop Mode Activation Detected by V2 OFF (24)	$t_{\overline{CS}STOP}$	18	—	34	µs
Interrupt Low Level Duration SBC in Stop Mode	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency All Modes Except Sleep and Stop (24)	O_{SCF1}	—	100	—	kHz
Internal Low Power Oscillator Frequency Sleep and Stop Modes (24)	O_{SCF2}	—	100	—	kHz
Watchdog Period 1 Normal and Standby Modes	WD_1	8.58	9.75	10.92	ms
Watchdog Period 2 Normal and Standby Modes	WD_2	39.6	45	50.4	ms
Watchdog Period 3 Normal and Standby Modes	WD_3	88	100	112	ms
Watchdog Period 4 Normal and Standby Modes	WD_4	308	350	392	ms
Watchdog Period Accuracy Normal and Standby Modes	f_{1ACC}	-12	—	12	%

Notes

24. Guaranteed by design; however it is not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Normal Request Mode Timeout Normal Request Modes	NR_{TOUT}	308	350	392	ms
Watchdog Period 1 - Stop Stop Mode	WD_{1STOP}	6.82	9.75	12.7	ms
Watchdog Period 2 - Stop Stop Mode	WD_{2STOP}	31.5	45	58.5	ms
Watchdog Period 3 - Stop Stop Mode	WD_{3STOP}	70	100	130	ms
Watchdog Period 4 - Stop Stop Mode	WD_{4STOP}	245	350	455	ms
Stop Mode Watchdog Period Accuracy Stop Mode	f_{2ACC}	-30	—	30	%
Cyclic Sense/FWU Timing 1 Sleep and Stop Modes	CS_{FWU1}	3.22	4.6	5.98	ms
Cyclic Sense/FWU Timing 2 Sleep and Stop Modes	CS_{FWU2}	6.47	9.25	12	ms
Cyclic Sense/FWU Timing 3 Sleep and Stop Modes	CS_{FWU3}	12.9	18.5	24	ms
Cyclic Sense/FWU Timing 4 Sleep and Stop Modes	CS_{FWU4}	25.9	37	48.1	ms
Cyclic Sense/FWU Timing 5 Sleep and Stop Modes	CS_{FWU5}	51.8	74	96.2	ms
Cyclic Sense/FWU Timing 6 Sleep and Stop Modes	CS_{FWU6}	66.8	95.5	124	ms
Cyclic Sense/FWU Timing 7 Sleep and Stop Modes	CS_{FWU7}	134	191	248	ms
Cyclic Sense/FWU Timing 8 Sleep and Stop Modes	CS_{FWU8}	271	388	504	ms
Cyclic Sense ON Time Sleep and Stop Modes Threshold and Condition to be Added	t_{ON}	200	350	500	µs
Cyclic Sense/FWU Timing Accuracy Sleep and Stop Modes	t_{ACC}	-30	—	30	%
Delay Between SPI Command and HS1 Turn ON (25)	t_{SHSON}	—	—	22	µs
Delay Between SPI Command and HS1 Turn OFF (25)	t_{SHSOFF}	—	—	22	µs
Delay Between SPI and V2 Turn ON (25) Standby Mode	tS_{V2ON}	9.0	—	22	µs
Delay Between SPI and V2 Turn OFF (25) Normal Mode	tS_{V2OFF}	9.0	—	22	µs

Notes

25. Delay starts at falling edge of clock cycle #8 of the SPI command and start of *Turn ON* or *Turn OFF* of HS1 or V2.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Delay Between Normal Request and Normal Mode After $\overline{WD}$ Trigger Command Normal Request Mode	tS_{NR2N}	 15	 35	 70	µs
Delay Between SPI and CAN Normal Mode SBC Normal Mode (26)	tS_{CANN}	 —	 —	 10	µs
Delay Between SPI and CAN Normal Mode SBC Normal Mode (26)	tS_{CANS}	 —	 —	 10	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ Low to High) and SBC Normal Request Mode (V_{DD1} on and Reset High) SBC in Stop Mode	$tW_{\overline{CS}}$	 15	 40	 90	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ Low to High) and First Accepted API Command SBC in Stop Mode	tW_{SPI}	 90	 —	 N/A	µs
Delay Between $\overline{INT}$ Pulse and First SPI Command Accepted In Stop Mode After Wake-up	tS_{1STSPI}	20	—	 N/A	µs
INPUT TERMINNALS (L0, L1, L2, AND L3)					
Wake-up Filter Time	t_{WUF}	8.0	20	38	µs
CAN MODULE-SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL)					
Dominant State Timeout	t_{DOUT}	200	360	520	µs
Propagation Loop Delay TX to RX, Recessive to Dominant Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LRD}	 70 80 100 110	 140 155 180 220	 210 225 255 310	ns
Propagation Delay TX to CAN Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TRD}	 20 40 60 100	 65 80 120 160	 110 150 200 300	ns
Propagation Delay CAN to RX, Recessive to Dominant	t_{RRD}	30	80	140	ns
Propagation Loop Delay TX to RX, Dominant to Recessive Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LDR}	 70 90 100 130	 120 135 160 200	 170 180 220 260	ns
Propagation Delay TX to CAN Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TDR}	 60 65 75 90	 110 120 150 190	 130 150 200 300	ns
Propagation Delay CAN to RX, Dominant to Recessive	t_{RDR}	20	40	60	

Notes

26. Guaranteed by design; however, it is not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Non Differential Slew Rate (CANL or CANH)					V/µs
Slew Rate 3	t_{SL3}	4.0	19	40	
Slew Rate 2	t_{SL2}	3.0	13.5	20	
Slew Rate 1	t_{SL1}	2.0	8.0	15	
Slew Rate 0	t_{SL0}	1.0	5.0	10	

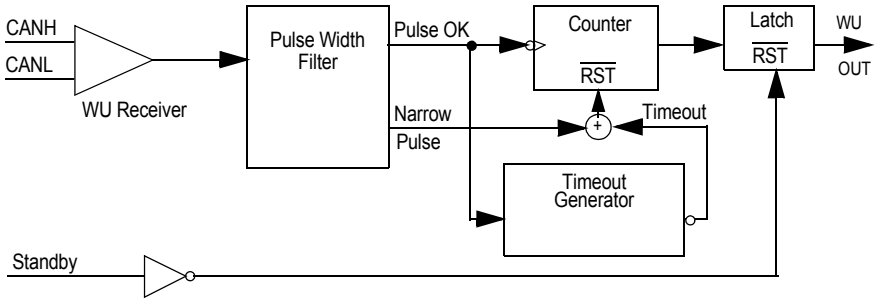
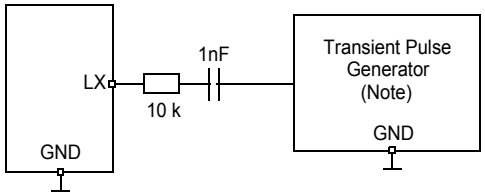


Figure 4. Wake-up Block Diagram

The block diagram in Figure 4 illustrates how the wake-up signal is generated. First the CAN signal is detected by a low consumption receiver (WU receiver). Then the signal passes through a pulse width filter, which discards the undesired pulses. The pulse must have a width bigger than 0.5 µs and smaller than 500 µs to be accepted. When a pulse is discarded the pulse counter is reset and no wake signal is generated, otherwise when a pulse is accepted the pulse counter is incremental and after three pulses the wake signal is asserted.

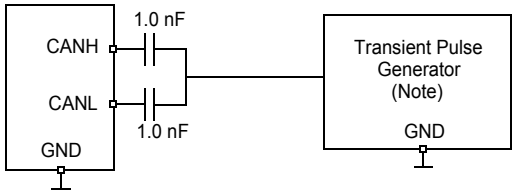


Note: Waveform in accordance to
ISO 7637 part1, test pulses 1, 2, 3a and 3b.

Figure 5. Transient Test Pulse for L0:L3 Inputs

Each one of the pulses must be spaced by no more than 500 µs. In that case, the pulse counter is reset and no wake signal is generated. This is accomplished by the wake timeout generator. The wake-up cycle is completed (and the wake flag reset) when the CAN interface is brought to *CAN Normal* mode.

The wake-up capability of the CAN can be disabled, refer to SPI interface and register section, CAN register.



Note: Waveform in accordance to
ISO 7637 part1, test pulses 1, 2, 3a and 3b.

Figure 6. Transient Test Pulses for CANH/CANL

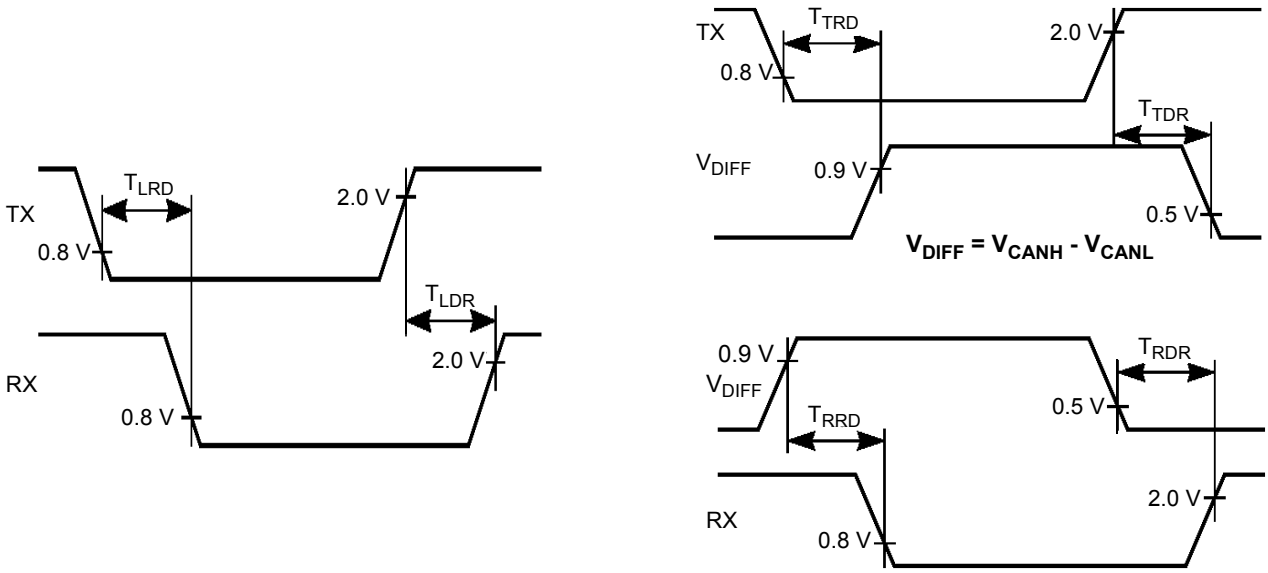
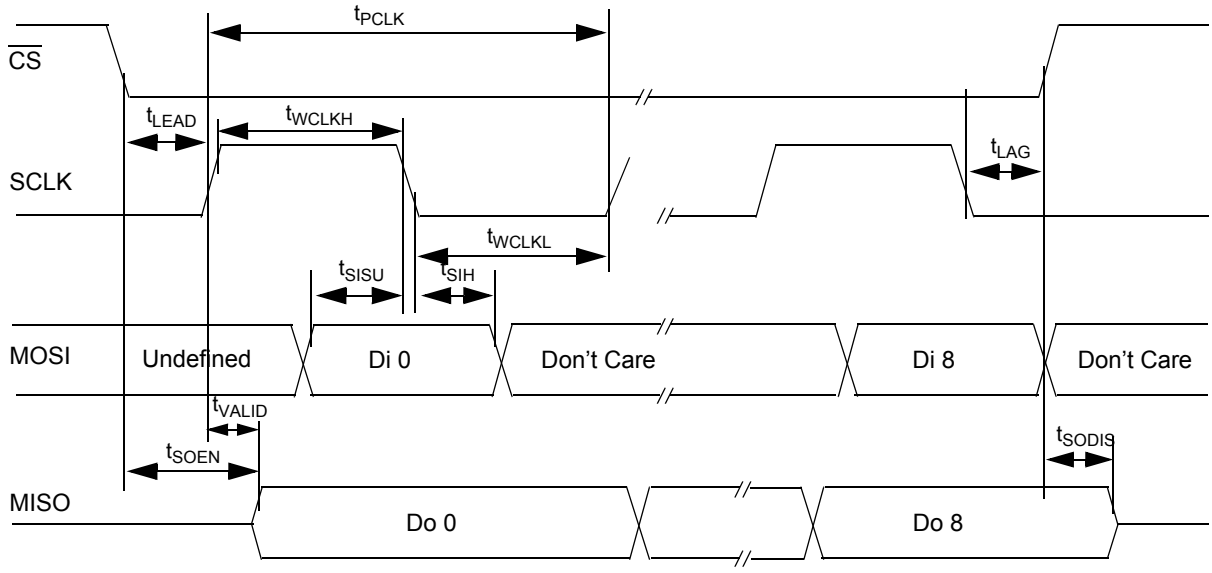


Figure 7. Transceiver AC Characteristics

TIMING DIAGRAMS



Notes:
Incoming data at MOSI pin is sampled by the SBC at SCLK falling edge.
Outgoing data at MISO pin is set by the SBC at SCLK rising edge (after t_{VALID} delay time).

Figure 8. SPI Timing Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33989 is an integrated circuit dedicated to automotive applications. Its functions include:

- One full protected voltage regulator with 200 mA total output current capability available at the VDD1 external pin
- Driver for an external path transistor for the V2 regulator function
- Reset, programmable watchdog function, interrupt, and four operational modes
- Programmable wake-up input and Cyclic Sense wake-up
- CAN high speed physical interface

FUNCTIONAL PIN DESCRIPTION

RECEIVE AND TRANSMIT DATA (RXD AND TXD)

The RX and TX pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TXD is an input and controls the CANH and CANL line state (dominant when TXD is LOW, recessive when TXD is HIGH). RXD is an output and reports the bus state (RXD LOW when CAN bus is dominant, HIGH when CAN bus is recessive).

VOLTAGE DIGITAL DRAIN ONE (VDD1)

The VDD1 pin is the output pin of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against overcurrent and overtemperature. It includes an overtemperature pre-warning flag, which is set when the internal regulator temperature exceeds 130 °C typical. When the temperature exceeds the overtemperature shutdown (170 °C typical), the regulator is turned off.

VDD1 includes an undervoltage reset circuitry, which sets the $\overline{RST}$ pin LOW when V_{DD1} is below the undervoltage reset threshold.

RESET ($\overline{RST}$)

The Reset pin $\overline{RST}$ is an output that is set LOW when the device is in reset mode. The $\overline{RST}$ pin is set HIGH when the device is not in reset mode. $\overline{RST}$ includes an internal pull-up current source. When $\overline{RST}$ is LOW, the sink current capability is limited, allowing $\overline{RST}$ to be shorted to 5.0 V for software debug or software download purposes.

INTERRUPT ($\overline{INT}$)

The Interrupt pin $\overline{INT}$ is an output that is set LOW when an interrupt occurs. $\overline{INT}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{INT}$ stays LOW until the interrupt source is cleared.

$\overline{INT}$ output also reports a wake-up event by a 10 μs typical pulse when the device is in Stop mode.

VOLTAGE SOURCE TWO (V2)

The V2 pin is the input sense for the V2 regulator. It is connected to the external series pass transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the VDD1 output when no external series pass transistor is used. In this case, the V2CTRL pin must be left open.

VOLTAGE SOURCE 2 CONTROL (V2CTRL)

The V2CTRL pin is the output drive pin for the V2 regulator connected to the external series pass transistor.

VOLTAGE SUPPLY (VSUP)

The VSUP pin is the battery supply input of the device.

HIGH-SIDE ONE (HS1)

The HS1 pin is the internal high side driver output. It is internally protected against overcurrent and overtemperature.

LEVEL 0-3 INPUTS (L0:L3)

The L0:L3 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by SPI. These inputs can be used as wake-up events for the SBC when operating in the Sleep or Stop mode.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TX input level, and the state of CANH and CANL is reported through RX output. A 60 Ω termination resistor is connected between CANH and CANL pins.

SYSTEM CLOCK (SCLK)

SCLK is the System Clock input pin of the serial peripheral interface.

MASTER IN SLAVE OUT (MISO)

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

MASTER OUT SLAVE IN (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ is the Chip Select pin of the serial peripheral interface. When this pin is LOW, the SPI port of the device is selected.

WATCHDOG ($\overline{\text{WD}}$)

The Watchdog output pin is asserted LOW to flag that the software watchdog has not been properly triggered.

FUNCTIONAL DEVICE OPERATION

DEVICE SUPPLY

The device is supplied from the battery line through the VSUP pin. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5 V and under the jump start condition at 27 Vdc. This pin sustains standard automotive voltage conditions such as load dump at 40 V. When V_{SUP} falls below 3.0 V typical the 33989 detects it and stores the information into the SPI register in a bit called *BATFAIL*. This detection is available in all operation modes.

The device incorporates a battery early warning function, providing a maskable interrupt when the V_{SUP} voltage is below 6.0 V typical. A hysteresis is included. Operation is only in Normal and Standby modes. V_{SUP} low is reported in the Input/Output Register (IOR).

VDD1 VOLTAGE REGULATOR

The VDD1 Regulator is a 5.0 V output voltage with output current capability up to 200 mA. It includes a voltage monitoring circuitry associated with a reset function. The VDD1 regulator is fully protected against overcurrent and short-circuit. It has over temperature detection warning flags (bit V_{DDTEMP} in MCR and interrupt registers), and overtemperature shutdown with hysteresis.

V2 REGULATOR

V2 Regulator circuitry is designed to drive an external path transistor increasing output current flexibility. Two pins are used to achieve the flexibility. Those pins are V2 and V2 control. The output voltage is 5.0 V and is realized by a tracking function of the VDD1 regulator. The recommended ballast transistor is MJD32C. Other transistors can be used; however, depending upon the PNP gain an external resistor-capacitor network might be connected. The V2 is the supply input for the CAN cell. The state of V2 is reported in the IOR (bit V2LOW set to 1 if V2 is below 4.5 V typical).

HS1 VBAT SWITCH OUTPUT

The HS1 output is a 2.0 Ω typical switch from the VSUP pin. It allows the supply of external switches and their associated pull-up or pull-down circuitry, in conjunction with the wake-up input pins, for example. Output current is limited to 200 mA and HS1 is protected against short-circuit and has an overtemperature shutdown (bit HS1OT in IOR and bit HS1OT-V2LOW in $\overline{\text{INT}}$ register). The HS1 output is controlled from the internal register and the SPI. Because of an internal timer, it can be activated at regular intervals in Sleep and Stop modes. It can also be permanently turned on in Normal or Standby modes to drive loads or supply peripheral components. No internal clamping protection circuit is implemented, thus a dedicated external protection circuit is required in case of inductive load drive.

BATTERY FALL EARLY WARNING

Refer to the discussion under the heading: Device Supply.

INTERNAL CLOCK

The device has an internal clock used to generate all timings (Reset, Watchdog, Cyclic Wake-up, Filtering Time, etc.). Two oscillators are implemented. A high accuracy (±12 percent) used in Normal Request, Normal and Standby modes, and a low accuracy (±30 percent) used in Sleep and Stop modes.

OPERATIONAL MODES

FUNCTIONAL MODES

The device has four primary operation modes:

1. Standby mode
2. Normal mode
3. Stop mode
4. Sleep mode

All modes are controlled by the SPI. An additional temporary mode called Normal Request mode is automatically accessed by the device after reset or wake-up from Stop mode. A Reset ($\overline{\text{RST}}$) mode is also implemented. Special modes and configuration are possible for debug and program MCU flash memory.

STANDBY MODE

Only regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2 control pin. Only the wake-up capability of the CAN interface is available. Other functions available are wake-up input reading through SPI and HS1 activation. The Watchdog is running.

NORMAL MODE

In this mode, both regulators are ON. This corresponds to the normal application operation. All functions are available in this mode (Watchdog, wake-up input reading through SPI, HS1 activation, CAN communication). The software Watchdog is running and must be periodically cleared through SPI.

STOP MODE

Regulator 2 is turned OFF by disabling the V2 control pin. The regulator 1 is activated in a special low power mode, allowing to deliver few mA. The objective is to maintain the MCU of the application supplied while it is turned into power saving condition (i.e Stop or Wait modes). In Stop mode the device supply current from V_{BAT} is very low.

When the application is in Stop mode (both MCU and SBC), the application can wake-up from the SBC side (for example: cyclic sense, forced wake-up, CAN message, wake-up inputs and overcurrent on VDD1), or the MCU side (key wake-up, etc.).

Stop mode is always selected by the SPI. In Stop mode the software Watchdog can be *running* or *idle* depending upon selection by the SPI (RCR, bit WDSTOP). To clear the watchdog, the SBC must be awakened by a $\overline{CS}$ pin (SPI wake-up). In Stop mode, SBC wake-up capability are identical as in Sleep mode. Please refer to Table 5.

SLEEP MODE

Regulators 1 and 2 are OFF. The current from VSUP pin is reduced. In this mode, the device can be awakened internally by cyclic sense via the wake-up inputs pins and HS1 output, from the *forced wake-up* function and from the CAN physical interface. When a wake-up occurs the SBC goes first into reset mode before entering Normal Request mode.

RESET MODE

In this mode, the Reset ($\overline{RST}$) pin is low and a timer is running for a time $\overline{RST}_{DUR}$. After this time is elapsed, the SBC enters Normal Request mode. Reset mode is entered if a reset condition occurs (V_{DD1} low, watchdog timeout or watchdog trigger in a closed window).

NORMAL REQUEST MODE

This is a temporary mode automatically accessed by the device after the reset mode, or after the SBC wake-up from Stop mode. After wake-up from the Sleep mode or after the device power-up, the SBC enters the Reset mode before entering the Normal Request mode. After a wake-up from the Stop mode, the SBC enters Normal Request mode directly.

In Normal Request mode the VDD1 regulator is ON, V2 is OFF, the reset pin is high. As soon as the device enters the Normal Request mode an internal 350 ms timer is started. During these 350 ms the microcontroller of the application must address the SBC via the SPI, configuring the Watchdog register. This is the condition for the SBC to stop the 350 ms timer and to go into the Normal or Standby mode and to set the watchdog timer according to configuration.

NORMAL REQUEST ENTERED AND NO $\overline{WD}$ CONFIGURATION OCCURS

In case the Normal Request mode is entered after SBC power-up, or after a wake-up from Stop mode, and if no $\overline{WD}$ configuration occurs while the SBC is in Normal Request mode, the SBC goes to Reset mode after the 350 ms time period is expired before again going into Normal Request mode. If no $\overline{WD}$ configuration is achieved, the SBC alternatively goes from Normal Request into reset, then Normal Request modes etc.

In case the Normal Request mode is entered after a wake-up from Sleep mode, and if no $\overline{WD}$ configuration occurs while the SBC is in Normal Request mode, the SBC goes back to Sleep mode.

APPLICATION WAKE-UP FROM SBC SIDE

When an application is in Stop mode, it can wake-up from the SBC side. When a wake-up is detected by the SBC (for example, CAN, Wake-up input, etc.) the SBC turns itself into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ pin.

APPLICATION WAKE-UP FROM MCU SIDE

When application is in Stop mode, the wake-up event may come from the MCU side. In this case the MCU signals to the SBC by a low to high transition on the $\overline{CS}$ pin. Then the SBC goes into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ pin.

STOP MODE CURRENT MONITOR

If the VDD1 output current exceed an internal threshold (I_{DD1SWU}), the SBC goes automatically into Normal Request mode and generates an interrupt at the $\overline{INT}$ pin. The interrupt is not maskable and the interrupt register will has no flag set.

INTERRUPT GENERATION WHEN WAKE-UP FROM STOP MODE

When the SBC wakes up from Stop mode, it first enters the Normal Request mode before generating a pulse (10 µs typical) on the $\overline{INT}$ pin. These interrupts are not maskable, and the wake-up event can be read through the SPI registers (CANWU bit in Reset Control Register (RCR) and LCTRx bit in Wake-up Register (WUR). In case of wake-up from Stop mode over current or from forced wake-up, no bit is set. After the $\overline{INT}$ pulse the SBC accept SPI command after a time delay ($t_{S1STSPI}$ parameter).

SOFTWARE WATCHDOG IN STOP MODE

If Watchdog is enabled, the MCU has to wake-up independently of the SBC before the end of the SBC watchdog time. In order to do this, the MCU must signal the wake-up to the SBC through the SPI wake-up ($\overline{CS}$ activation). The SBC then wakes up and jumps into the Normal Request mode. MCU has to configured the SBC to go to either Normal or Standby mode. The MCU can then decide to go back again to Stop mode.

When there is no MCU wake-up occurring within the watchdog timing, the SBC activates the Reset pin, jumping into the Normal Request mode. The MCU can then be initialized.

STOP MODE ENTER COMMAND

Stop mode is entered at the end of the SPI message, and at the rising edge of the $\overline{CS}$. Please refer to the $t_{\overline{CS}STOP}$ data in the Dynamic Electrical Characteristics.

Once Stop mode is entered the SBC could wake-up from the V1 regulator overcurrent detection. In order to allow time for the MCU to complete the last CPU instruction, allowing the MCU to enter its low power mode, a deglitcher time of typical 40 µs is implemented.

Figure 9 indicates the operation to enter Stop mode.

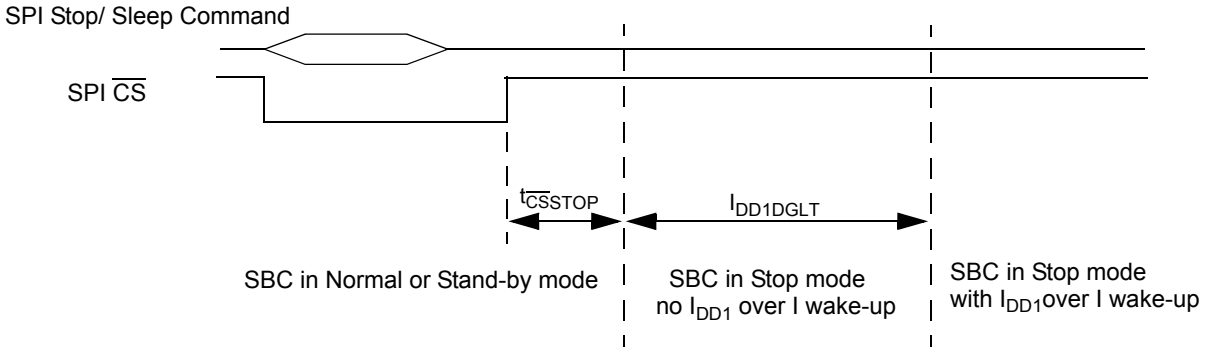


Figure 9. Operation Entering Stop Mode

RESET AND WATCHDOG PINS, SOFTWARE WATCHDOG OPERATIONS

SOFTWARE WATCHDOG (SELECTABLE WINDOW OR TIMEOUT WATCHDOG)

Software watchdog uses in the SBC Normal and Standby modes is to monitor MCU. The Watchdog can be either window or timeout. This is selectable by SPI (register TIM1, bit WDW). Default is window watchdog. The period for the watchdog is selectable from the SPI from 10 ms to 350 ms (register TIM1, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first part of the selected period, and the open window is the second part of the period. Refer to the SPI

TIM register description. Watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. Watchdog is cleared through SPI by addressing the TIM1 register.

RESET PIN DESCRIPTION

A reset output is necessary and available to reset the microcontroller. Modes 1 and 2 are available for the reset pin (please refer to Table 5 for reset pin operation).

Reset causes when SBC is in mode 1:

- V_{DD1} falling out of range — If V_{DD1} falls below the reset threshold (parameter R_{STTH}), the RST pin is pulled low until V_{DD1} returns to the normal voltage.
- Power-on reset — At device power-on or at device wake-up from Sleep mode, the reset is maintained low until V_{DD1} is within its operation range.

Watchdog timeout — If watchdog is not cleared, the SBC will pull the reset pin low for the duration of the reset time (parameter $\overline{RST}_{DUR}$).

Table 5. Reset and Watchdog Output Operation

Events	Mode	$\overline{WD}$ Output	Reset Output
Devices Power-up	1 or 2 (Safe Mode)	Low to High	Low to High
V_{DD1} Normal Watchdog Properly Triggered	1	High	High
V_{DD1} < RST_{TH}	1	High	Low
Watchdog Timeout Reached	1	Low (Note)	Low
V_{DD1} Normal Watchdog Properly Triggered	2 (Safe Mode)	High	High
V_{DD1} < RST_{TH}	2 (Safe Mode)	High	Low
Watchdog Timeout Reached	2 (Safe Mode)	Low (Note)	High

Notes
27. $\overline{WD}$ stays low until the Watchdog register is properly addressed through SPI.

In Mode 2, the reset pin is not activated in case of Watchdog timeout. Please refer to Table 6 for more detail.

For debug purposes at 25 °C, the Reset pin can be shorted to 5.0 V because of its internal limited current drive capability.

RESET AND WATCHDOG OPERATION: MODES1 AND 2

Watchdog and Reset functions have two modes of operation:

1. Mode 1
2. Mode 2 (also called Safe mode)

These modes are independent of the SBC modes (Normal, Standby, Sleep, and Stop). Modes 1 and 2 selection is achieved through the SPI (register MCR, bit SAFE). Default mode after reset is Mode 1.

Table 5 provides Reset and Watchdog output mode of operation. Two modes (modes 1 and 2) are available and can be selected through the SPI Safe bit. Default operation, after reset or power-up, is Mode 1.

In both modes reset is active at device power-up and wake-up.

- In mode 1–Reset is activated in case of V_{DD1} fall or watchdog not triggered. $\overline{WD}$ output is active low as soon as reset goes low. It remains low as long as the watchdog is not properly re-activated by the SPI.
- In mode 2–(Safe mode) Reset is not activated in case of watchdog fault. $\overline{WD}$ output has the same behavior as in mode 1–The Watchdog output pin is a push-pull structure driving external components of the application for signal instance of an MCU wrong operation.

Table 6. Table of Operation

Mode	Voltage Regulator HS1 Switch	Wake-up Capabilities (if enabled)	Reset Pin	$\overline{INT}$	Software Watchdog	CAN Cell
Normal Request	V_{DD1}:ON V2:OFF HS1:OFF	—	Low for Reset-DUR Time, then High	—	—	—
Normal	V_{DD1}:ON V2:ON HS1:Controllable	—	Normally High Active Low if $\overline{WD}$ or V_{DD1} undervoltage occurs (and mode 1 selected)	If Enabled, Signal Failure (V_{DD1} Pre-Warning Temp, CAN, HS1)	Running	Tx/Rx
Standby	V_{DD1}:ON V2:OFF HS1:Controllable	—	Same as Normal Mode	Same as Normal Mode	Running	Low Power
Stop	V_{DD1}:ON (Limited Current Capability) V2:OFF HS1:OFF or Cyclic	CAN SPI L0:L3 Cyclic Sense Forced Wake-up I_{DD1} Over Current (28)	Normally High Active Low if $\overline{WD}$ (29) or V_{DD1} Undervoltage Occurs	Signal SBC Wake-up and IDD > $I_{DD1S/WU}$ (Not Maskable)	Running if Enabled Not Running if Disabled	Low Power Wake-up Capability if Enabled
Sleep	V_{DD1}:OFF V2:OFF HS1:OFF or Cyclic	CAN SPI L0:L3 Cyclic Sense Forced Wake-up	Low	Not Active	Not Running	Low Power Wake-up Capability if Enabled
Debug Normal	Same as Normal	—	Normally High Active Low if V_{DD1} Undervoltage Occurs	Same as Normal	Not Running	Same as Normal
Debug Standby	Same as Standby	—	Normally High Active Low if V_{DD1} Undervoltage Occurs	Same as Standby	Not Running	Same as Standby
Stop Debug	Same as Stop	Same as Stop	Normally High Active Low if V_{DD1} Undervoltage Occurs	Same as Stop	Not Running	Same as Stop
Flash Programming	Forced Externally	—	Not Operating	Not Operating	Not Operating	Not Operating

Notes
28. Always enable.
29. If enabled.

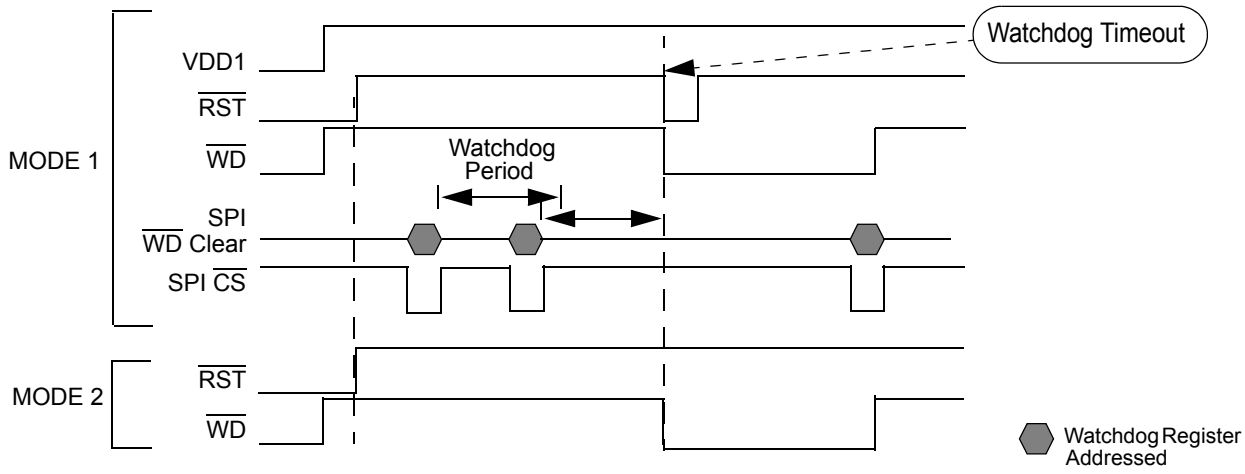


Figure 10. Reset and Watchdog Functions Diagram in Modes 1 and 2

WAKE-UP CAPABILITIES

Several wake-up capabilities are available for the device when it is in Sleep, or Stop modes. When a wake-up has occurred, the wake-up event is stored into the WUR or CAN registers. The MCU can then access to the wake-up source. The wake-up options are able to be selected through the SPI while the device is in Normal or Standby mode and prior to entering low power mode (Sleep or Stop mode). When a wake-up occurs from sleep mode the device activates V_{DD1}. It generates an interrupt if wake-up occurs from Stop mode.

WAKE-UP FROM WAKE-UP INPUTS (L0:L3) WITHOUT CYCLIC SENSE

The wake-up lines are dedicated to sense external switch states and if changes occur to wake-up the MCU (in Sleep or Stop modes). The wake-up pins are able to handle 40 V DC. The internal threshold is 3.0 V typical and these inputs can be used as an input port expander. The wake-up inputs state are read through SPI (register WUR).

In order to select and activate direct wake-up from the LX inputs, the WUR register must be configured with the appropriate level sensitivity. Additionally, the LPC register must be configured with 0x0 data (bits LX2HS1and HS1AUTO are set at 0).

Level sensitivity is selected by WUR register. Level sensitivity is configured by a pair of Lx inputs: L0 and L1 level sensitivity are configured together while L2 and L3 are configured together.

CYCLIC SENSE WAKE-UP (CYCLIC SENSE TIMER AND WAKE-UP INPUTS L0, L1, L2, L3)

The SBC can wake-up upon state change of one of the four wake-up input lines (L0, L1, L2 and L3) while the external pull-up or pull down resistor of the switches associated to the wake-up input lines are biased with HS1 VSUP switch. The HS1 switch is activated in Sleep or Stop modes from an internal timer. Cyclic Sense and Forced Wake-up are exclusive. If Cyclic Sense is enabled the forced wake-up can not be enabled.

In order to select and activate the cyclic sense wake-up from the Lx inputs the WUR register must be configured with the appropriate level sensitivity, and the LPC register must be configured with 1xx1 data (bit LX2HS1 set at 1 and bit HS1AUTO set at 1). The wake-up mode selection (direct or cyclic sense) is valid for all 4 wake-up inputs.

FORCED WAKE-UP

The SBC can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and Forced wake-up are exclusive. If Forced wake-up is enabled (FWU bit set to 1 in LPC register) the Cyclic Sense can not be enabled.

CAN INTERFACE WAKE-UP

The device incorporates a high-speed 1MBaud CAN physical interface. Its electrical parameters for the CANL, CANH, RX and TX pins are compatible with ISO 11898 specification (IS0 11898: 1993(E)). The control of the CAN physical interface operation is accomplished through the SPI. CAN modes are independent of the SBC operation modes.

The device can wake-up from a CAN message if the CAN wake-up is enabled. Please refer to the CAN module description for detail of wake-up detection.