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MD1730

8-Channel Ultra-Low Phase Noise Continuous Waveform Transmitter with Beamformer

Features

- 8-Channel Ultrasound Continuous Waveform (CW) Transmitter with Integrated Beamformer
- CW Output ±1V to ±6Vp-p with Low R_{ON}
- -160 dbc/Hz Ultra-Low Phase Noise at 1 kHz Offset and 5 MHz
- 8-Bit Programmable Per-Channel Beamforming Phase Delay
- 8-Bit Programmable Dividers for CW Frequency with Input Clock Frequency up to 250 Mhz
- Input Clock Compatible with LVDS/SSTL or Single-Ended LVCMOS
- LVCMOS 2.5V Logic for the Control I/O pins
- Fast SPI Interface Supports up to 200 MHz
- SPI Interface Supports Daisy Chaining and Broadcasting Mode

Applications

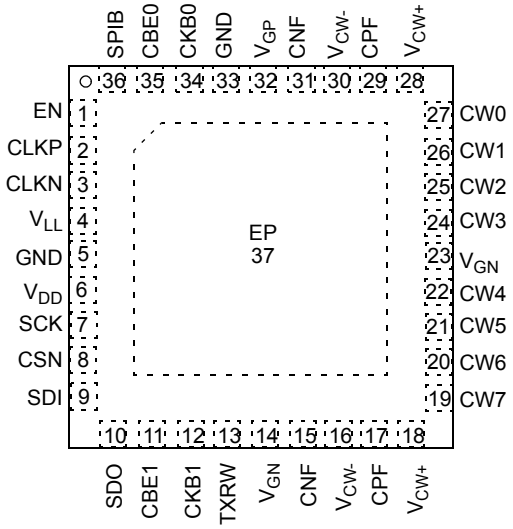
- Medical Ultrasound Imaging System for Cardiovascular Application
- Ultrasound Fetal Heart Monitoring Device
- Ultrasound Flow Meter
- Programmable Array Pattern Generator

General Description

The MD1730 is an 8-channel ultra-low phase noise CW transmitter with integrated beamformer. It is designed for medical ultrasound imaging systems requiring high-performance CW Doppler mode. The MD1730 has a dedicated signal path designed to minimize phase noise to the output. In addition, it has a high-speed SPI interface that enables CW beamforming features. The outputs of the MD1730 can swing up to ±6V and each output has a separate programmable phase delay. Additionally, by programming the internal frequency divider register, the MD1730 can output different CW frequencies from a single clock source. For instance, when the input clock frequency is 160 MHz and the frequency divider is set to 16, an output CW frequency of 5 MHz can be obtained with a phase delay step size of 6.25 ns, which translates to an angular resolution of 11.25 degrees.

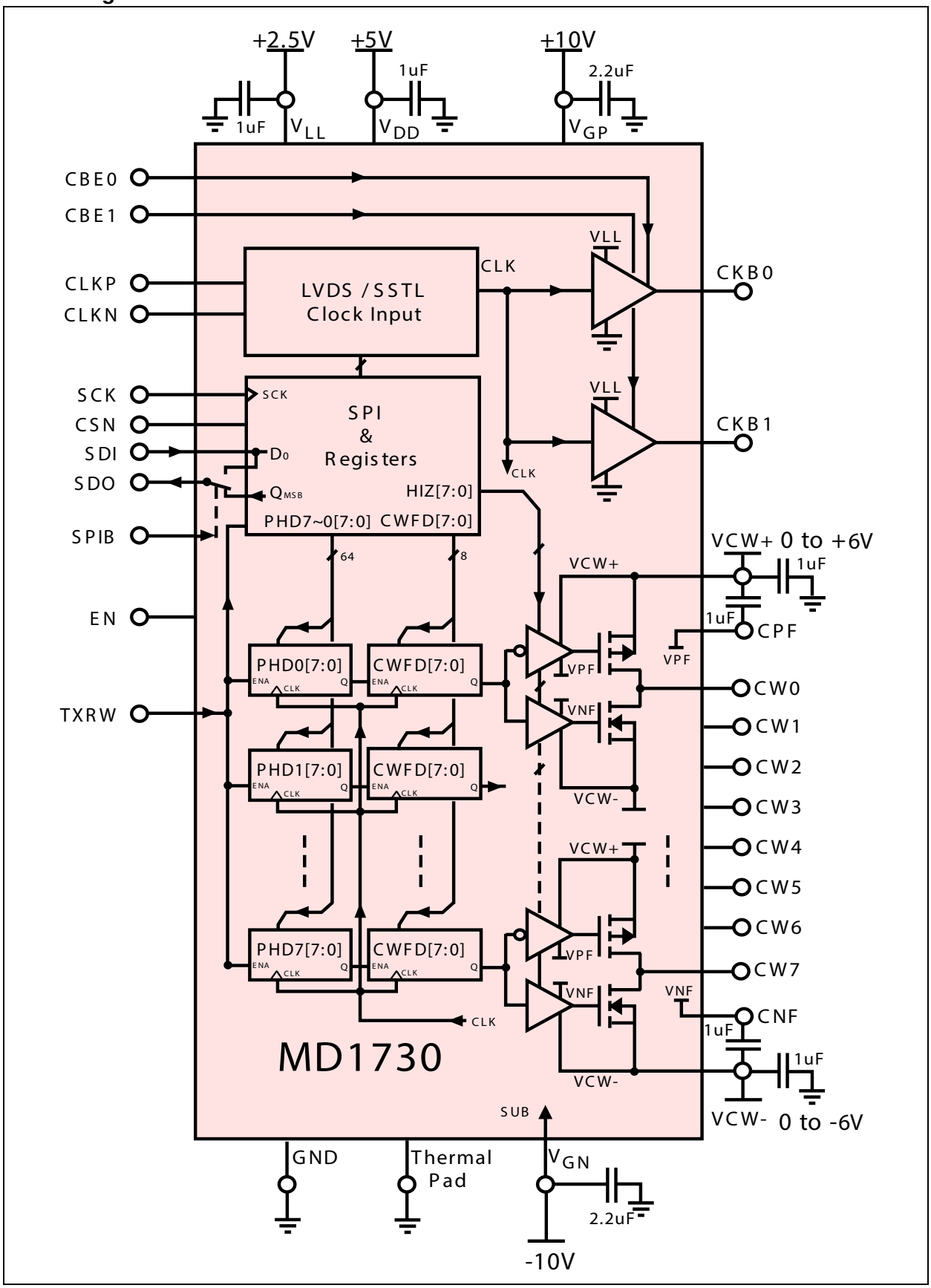
Package Type

MD1730
6x6x0.9 mm 36-lead VQFN*

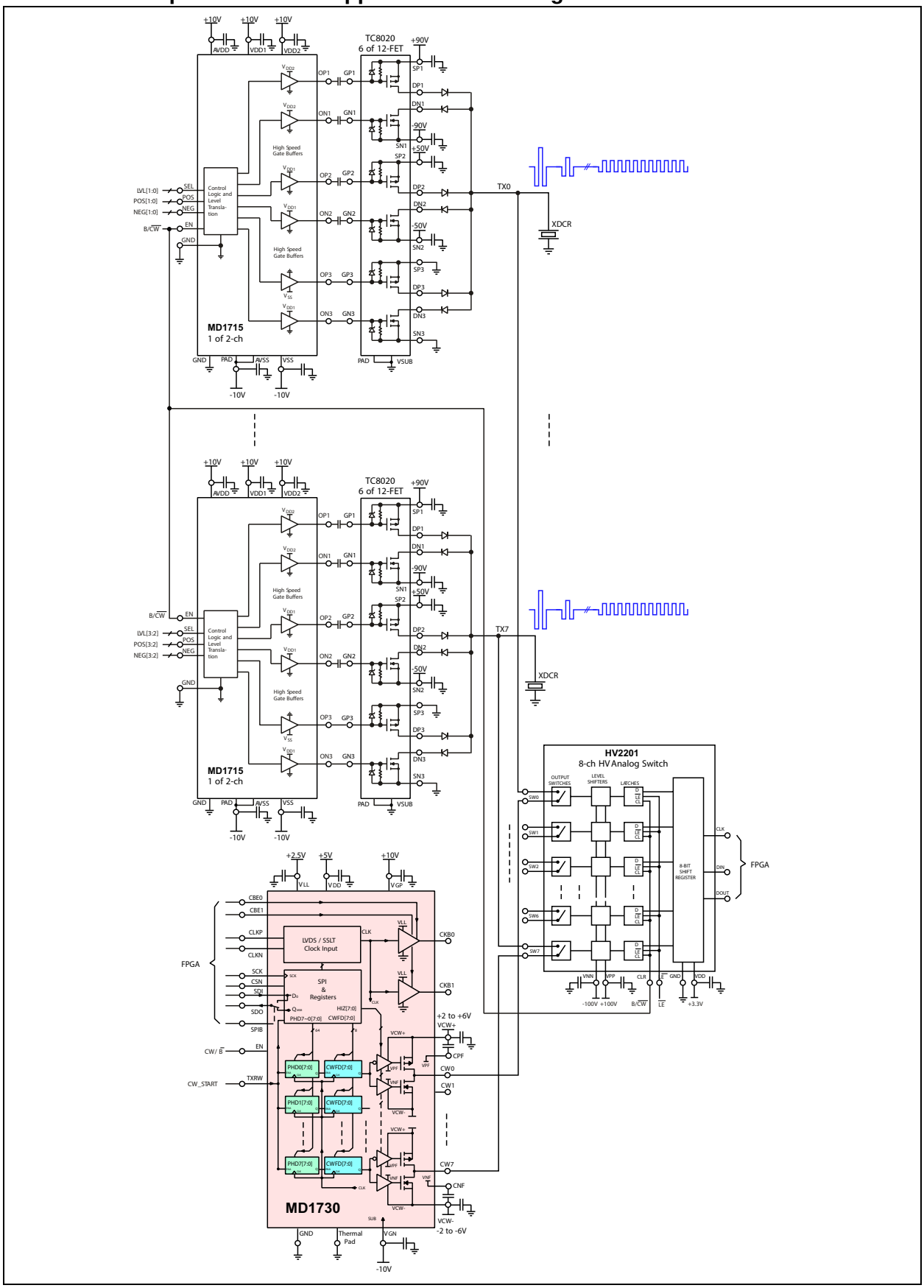


* Includes Exposed Thermal Pad (EP); see Table 3-1.

Block Diagram



MD1730 CW Output via HV2201 Application Block Diagram



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Positive Logic Supply (V_{LL}) ..... -0.5V to +3.0V
Positive Supply Voltage (V_{DD}) ..... -0.5V to +6.0V
Positive Supply Voltage (V_{GP}) ..... -0.5V to +13.5V
Negative Supply Voltage (V_{GN}) ..... +0.5V to -13.5V
CW Output Positive Supply Voltage (V_{CW+}) ..... -0.5V to +12V
CW Output Negative Supply Voltage (V_{CW-}) ..... +0.5V to -12V
All Digital Inputs (V_{IN}) ..... -0.5V to +3.0V
CW Outputs (V_{OUT}) ..... -12V to +12V

Operating Ambient Temperature ..... 0°C to +85°C
Maximum Junction Temperature ..... 0°C to +85°C
Storage Temperature ..... +125°C

Thermal Resistance Junction to Ambient (Θ_{JA}, JESD51-5) ..... 25°C/W
Thermal Resistance Junction to Bottom Cu Pad (Θ_{JB}, JESD51-5) ..... 6.4°C/W
Thermal Resistance Junction to Package Top (Θ_{JC}, JESD51-5) ..... 13.5°C/W
ESD Rating All Pins ..... ±1.0 kV

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: INPUT/OUTPUT PIN DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Supply						
Logic Supply Voltage	V_{LL}	2.35	2.50	2.65	V	$(V_{GP}+\|V_{CW-}\|) \geq 10V$ $(V_{GN}+\|V_{CW+}\|) \geq 10V$ T_A= 0 to +85°C, **Note 2**
VDD Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
Positive Supply Voltage	V_{GP}	8.0	10	12	V	
Negative Supply Voltage	V_{GN}	-12	-10	-8.0	V	
CW Output Positive Supply	V_{CW+}	1.0	—	6.0	V	
CW Output Negative Supply	V_{CW-}	-6.0	—	-1.0	V	
V_{LL} Quiescent Current	I_{LLQ}	—	0.02	0.1	mA	EN = 0, $f_{CLK} = f_{SCK} = 0$ All logic input no transit
V_{DD} Quiescent Current	I_{DDQ}	—	0.15	0.2	mA	
V_{GP} Quiescent Current	I_{GPQ}	—	1.0	2.0	µA	
V_{GN} Quiescent Current	I_{GNQ}	—	33	45	µA	
V_{CW+} Quiescent Current	I_{CW+Q}	—	26	45	µA	
V_{CW-} Quiescent Current	I_{CW-Q}	—	6	10	µA	
V_{LL} Enabled Current	I_{LLEN}	—	6.0	9.0	mA	EN = 1, f_{SCK} = 120 MHz TXRW = 0, SDI = 0, SDO no load.
V_{DD} Enabled Current	I_{DDEN}	—	0.2	0.3	mA	
V_{GP} Enabled Current	I_{GPEN}	—	2.0	3.0	mA	
V_{GN} Enabled Current	I_{GNEN}	—	2.0	3.0	mA	
V_{CW+} Enabled Current	I_{CW+EN}	—	2.0	3.0	mA	
V_{CW-} Enabled Current	I_{CW-EN}	—	2.0	3.0	mA	

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-1: INPUT/OUTPUT PIN DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
V_{LL} Current at CW 5MHz	I_{LL5}	—	2.5	3.0	mA	EN = 1, f_{CLK} = 80 MHz, TXRW = 1, CW 5 MHz, no load 8-channel
V_{DD} Current at CW 5MHz	I_{DD5}	—	1.0	2.0	mA	
V_{GP} Current at CW 5MHz	I_{GP5}	—	6.0	10	mA	
V_{GN} Current at CW 5MHz	I_{GN5}	—	12	18	mA	
V_{CW+} Current at CW 5MHz	I_{CW+5}	—	26	35	mA	
V_{CW-} Current at CW 5MHz	I_{CW-5}	—	21	30	mA	
SPI & Logic						
Input Logic High Voltage	V_{IH}	0.8 V_{LL}	—	V_{LL}	V	2.5V LVCMOS
Input Logic Low Voltage	V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Current	I_{IH}	—	—	1.0	µA	
Input Logic Low Current	I_{IL}		—	—	µA	
SPI and Logic Input Capacitance	C_{IN}	—	4.5	—	pF	**Note 1**
Output Logic High Current	I_{OH}		—	—	mA	2.5V LVCMOS
Output Logic Low Current	I_{OL}		—	—	mA	
SDO Output Logic High Voltage	V_{OH}		—	—	V	with 5 pF load
SDO Output Logic Low Voltage	V_{OL}	—	—	0.35	V	

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-2: SPI AND LOGIC AC ELECTRICAL SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Rise Time	t_r	—	0.65	—	ns	1.5 pF load, **Note 1**
Output Fall Time	t_f	—	0.65	—		
Output Rise Propagation Delay	t_{dr}	—	2.8	—	ns	CLK rise 50% to output 50%, after latency. **Note 1**
Output Fall Propagation Delay	t_{df}	—	3.0	—		
Delay Time Matching	t_{dm}	—	±0.5	±1.0	ns	Channel to channel, **Note 1**, f_{CLK} = 80 MHz
SDI Valid to SCK, Setup Time	t_1	0.6	1.0	—	ns	**Note 1**
SCK To SDI Data Hold Time	t_2	2.0	—	—	ns	
SCK High Time % of 1/f_{CLK}	t_3	45	—	55	%	**Note 2**
SCK Low Time % of 1/f_{CLK}	t_4	45	—	55	%	
CSN Hi-Time	t_5	2-cycle	—	—	SCK	**Note 2**
SCK Rise to CSN Rise	t_6	—	2.0	—	ns	**Note 1**
CSN Low to SCK Rise	t_7	—	0.8	—	ns	
SDO Valid from SCK Rise	t_8	—	3.1	4.0	ns	SPIB = 0, 1.5 pF Load, **Note 1**
CSN Rise to SCK Rise	t_9	—	2.0	—	ns	**Note 1**
CSN Rise to TXRW or SPIB Rise	t_{10}	9-cycle			SCK	**Note 2**
TXRW or SPIB Fall to CSN Fall	t_{11}	1-cycle				

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-2: SPI AND LOGIC AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
SDO to SDI Valid Delay	t_{12}	—	2.3	3.0	ns	SPIB = 1, 1.5 pF Load, **Note 1**
TXRW Rise to CLKP Rise	t_{13}	—	2.5	—	ns	**Note 1**
Latency to CW Wave Rise	t_{14}	2-cycle			CLK	After TXRW = 1, PHD=0, **Note 2**
Latency CSN Rise to TXRW Fall	t_{15}	2-cycle	—	—	CLK	**Note 2**
SCK Clock Frequency	f_{SCK}	—	—	200	MHz	**Note 1**
EN Off Time	t_{EN-Off}	—	20	30	ns	**Note 2**
EN On Time	t_{EN-On}	—	150	300	µs	2.0 µF on CPF/CNF, **Note 2**

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-3: CLOCK BUFFER OUTPUTS AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Clock Output Frequency Range	f_{CKB}	40	160	250	MHz	**Note 1**
Clock Output Duty Cycle	D%	45	—	55	%	**Note 2**
CKB0,1 Rise Time	t_{rb}	—	0.6	1.0	ns	f_{CLK} = 80 Mhz, 1.5 pF load, **Note 1**
CKB0,1 Fall Time	t_{fb}	—	0.5	1.0		
Output Rise Propagation Delay	t_{drb}	—	2.0	3.0	ns	CLK rise to CKB, 50%, **Note 1**
Output Fall Propagation Delay	t_{dfb}	—	2.0	3.0		
CBE Enable Time	t_{cbe}	—	2.1	3.0		CBE to CLK rise, 50%, **Note 1**
CKB0,1 Output logic high	V_{OHCKB}	—	V_{LL}	—	V	**Note 2**
CKB0,1 Output Logic low	V_{OLCKB}	—	GND	—	V	**Note 2**

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-4: CW OUTPUTS DC/AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
CW Output Peak to Peak Voltage	V_{CWOUT}	-6.0	-	+6.0	V	
CW Output Rise Propagation Delay	t_{drCW}	—	4.0	6.0	ns	TxCLK 50% to CWx 10%, after latency, **Note 1**
CW Output Fall Propagation Delay	t_{dfCW}	—	4.0	6.0		
CW Output Maximum Current	$I_{CW\pm}$	±250	±300	—	mA	$V_{CW\pm}$ = ±5.0V, 0.1Ω load, **Note 1**

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-4: CW OUTPUTS DC/AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Static Output Resistance PFET	R_{ONCW}	—	7.5	12	Ω	RON at $V_{CW±}$ = ±5.0V, $I_{CW±}$ = ±100 mA load, **Note 1**
Static Output Resistance NFET		—	6.5	11		
Change in $R_{DS(ON)}$ with Temperature	ΔR_{ONCW}	—	—	1.0	%/C	$V_{CW±}$ = ±5.0V, **Note 2**
CW Phase Resolution	RE_{Phase}	—	1	—	CLK	**Note 2**
CW Phase Noise	N_{Phase}	—	-160	—	dBC/ Hz	CW 5 MHz, 1 kHz Offset, **Note 1**

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

TABLE 1-5: LVDS / SSTL CLOCK INPUTS AC / DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{LL} = +2.5V, V_{GP} = +10V, V_{GN} = -10V, V_{CW+} = +6.0V, V_{CW-} = -6.0V, V_{DD} = +5V, T_A = 25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CLKP/CLKN Clock Frequency	f_{CLK}	40	160	250	MHz	**Note 1**
Clock Input Slew Rate	t_{CSR}	1.0	—	—	V/ns	**Note 2**
Control/Data Input Slew Rate	t_{DSR}	1.0	—	—	V/ns	
Single Ended Clock Input						
SSTL Reference Voltage	V_{REFS}	1.13	1.25	1.38	V	**Note 1**
DC Input Logic High	$V_{IH(DC)}$	V_{REFS} +0.15	—	V_{LL} +0.3	V	**Note 1**
DC Input Logic Low	$V_{IL(DC)}$	-0.3	—	V_{REFS} -0.15	V	**Note 1**
AC Input Logic High	$V_{IH(AC)}$	V_{REFS} +0.31	—	—	V	V_{REF} = 0.5V_{LL}, Slew rate 1.0 V/ns, **Note 1**
AC Input Logic Low	$V_{IL(AC)}$	-	—	V_{REFS} -0.31	V	
Differential Clock Input						
AC Differential Cross Point	$V_{X(AC)}$	0.5V_{LL} -0.2	—	0.5V_{LL}+0.2	V	CLK and $\overline{CLK}$, **Note 1**
DC Input Max Swing Voltage	$V_{SWING(DC)}$	0.3	—	V_{LL} +0.6	V	**Note 1**
AC Differential Input Voltage	$V_{SWING(AC)}$	0.62	—	V_{LL} +0.6	V	**Note 1**
DC Input Signal Voltage	$V_{IN(DC)}$	-0.3	—	V_{LL} +0.3	V	**Note 1**
CLKP/CLKN Slew Rate	SLEW	1.0	—	—	V/ns	**Note 2**

Note 1: Characterized only; not 100% tested in production.
2: Design Guidance Only (DGO).

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

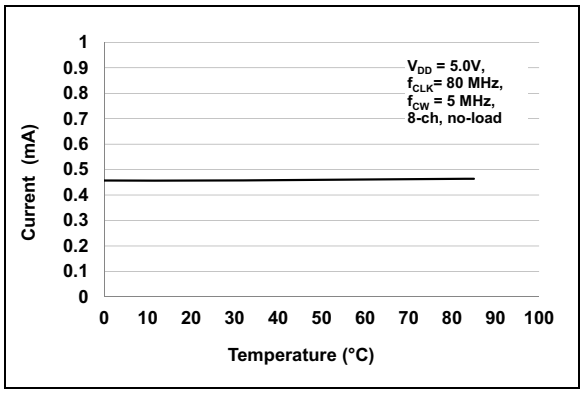


FIGURE 2-1: *I_{DD} vs. Temperature.*

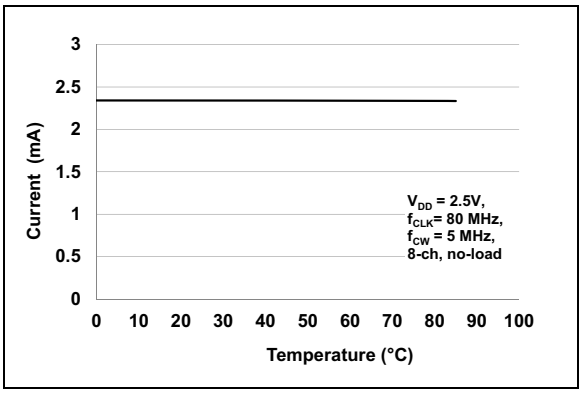


FIGURE 2-4: *I_{VLL} vs. Temperature.*

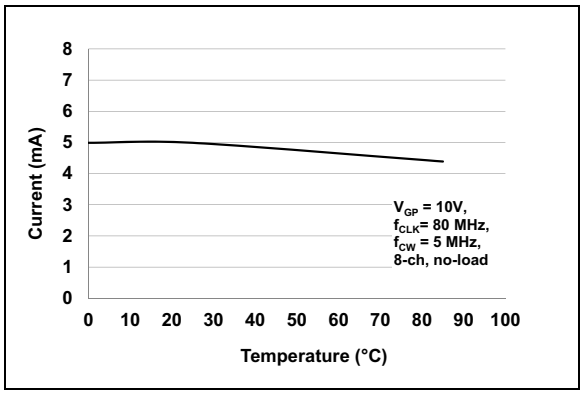


FIGURE 2-2: *I_{VGP} vs. Temperature.*

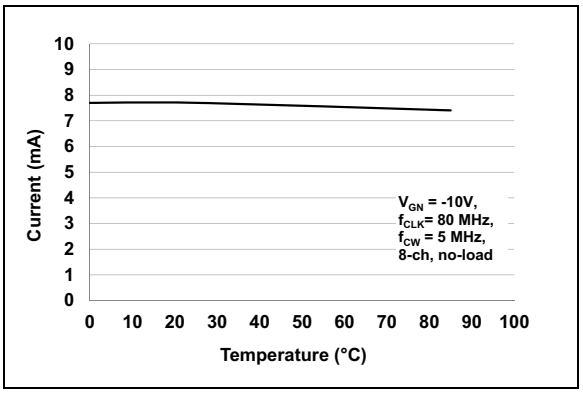


FIGURE 2-5: *I_{VGN} vs. Temperature.*

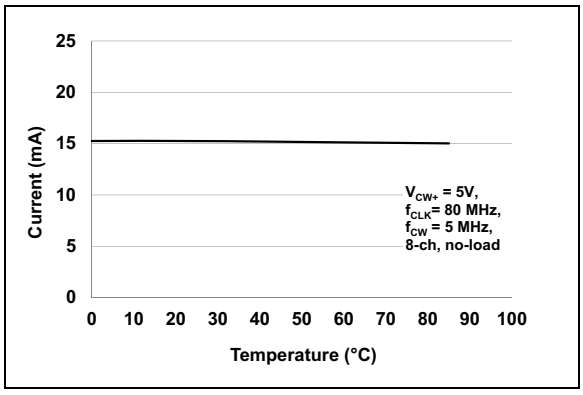


FIGURE 2-3: *I_{VCW+} vs. Temperature.*

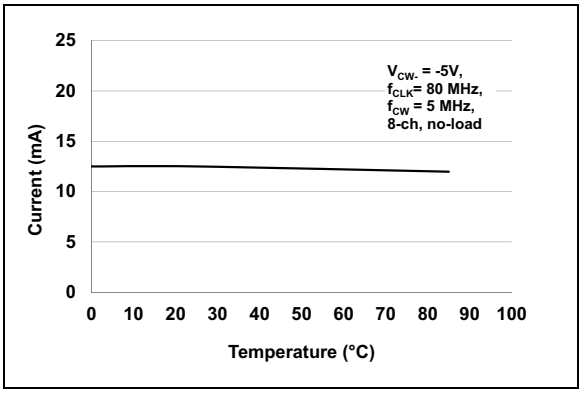


FIGURE 2-6: *I_{VCW-} vs. Temperature.*

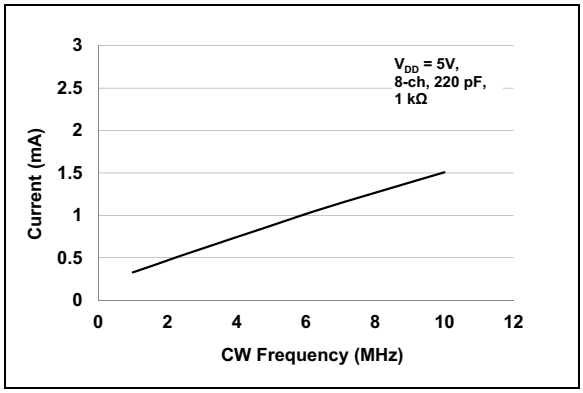


FIGURE 2-7: *I_{VDD} vs. CW Output Frequency.*

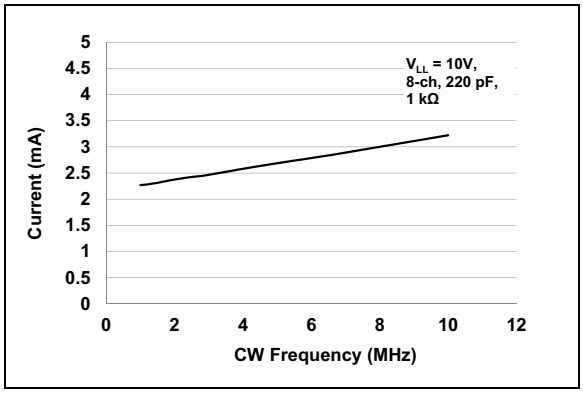


FIGURE 2-10: *I_{VLL} vs. CW Output Frequency.*

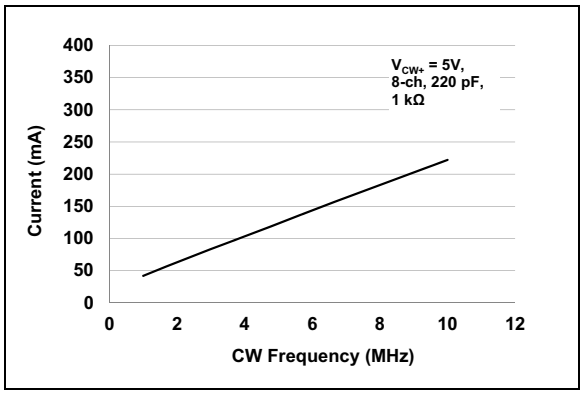


FIGURE 2-8: *I_{VCW+} vs. CW Output Frequency.*

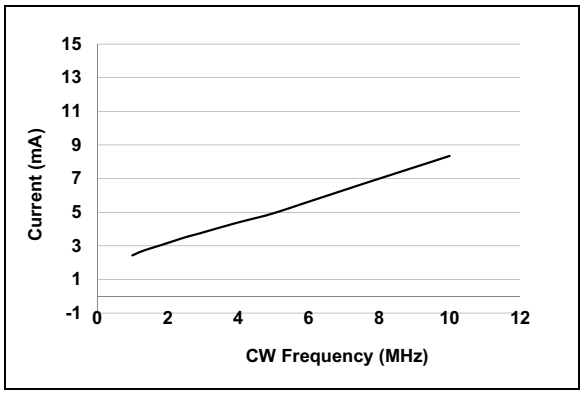


FIGURE 2-11: *I_{VGN} vs. CW Output Frequency.*

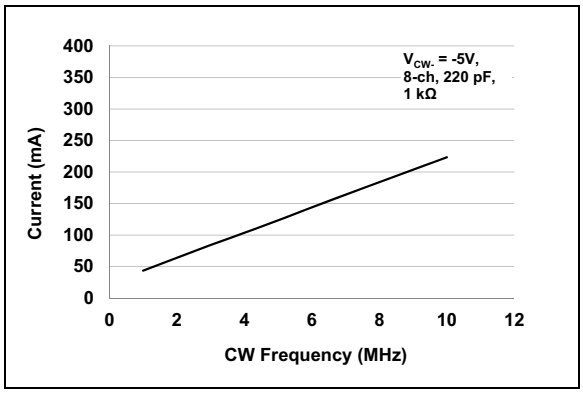


FIGURE 2-9: *I_{VCW-} vs. CW Output Frequency.*

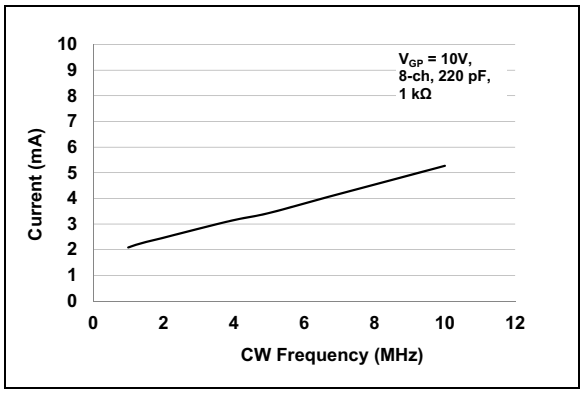


FIGURE 2-12: *I_{VGP} vs. CW Output Frequency.*

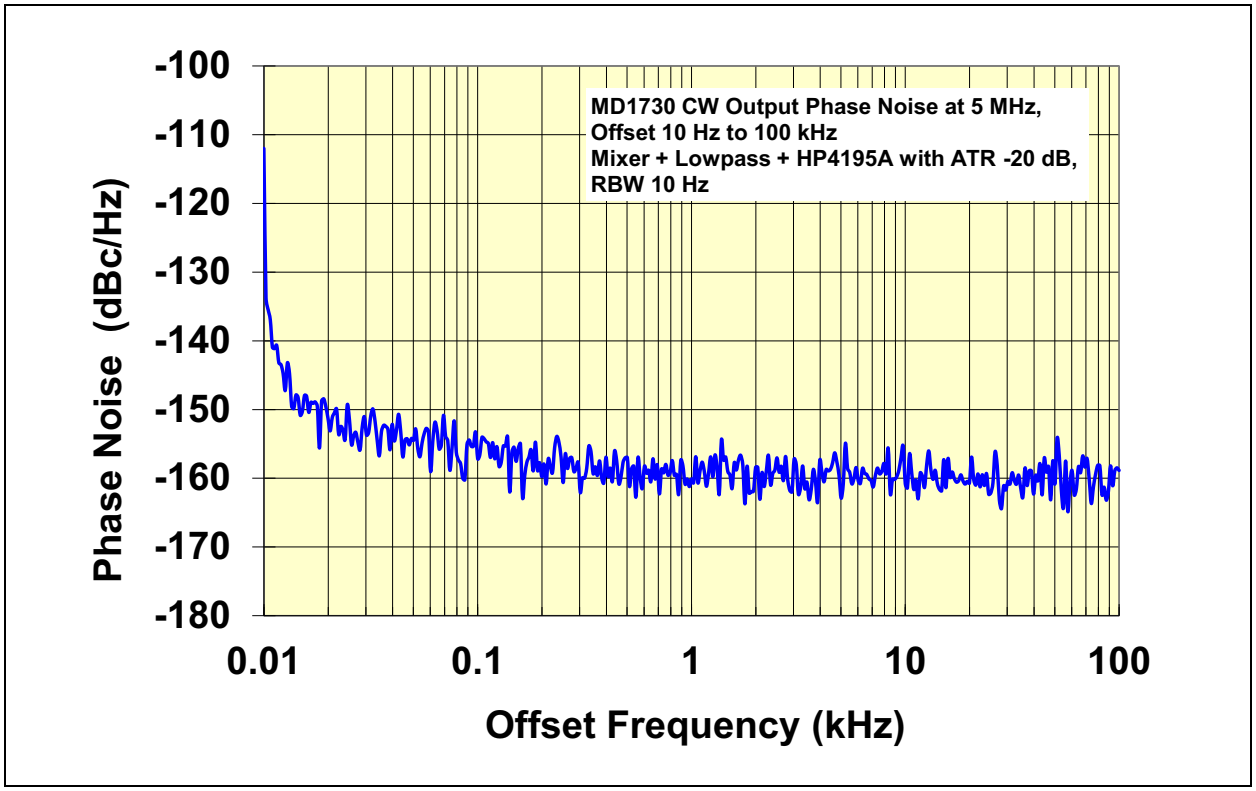


FIGURE 2-13: *Typical CW Output Phase Noise Curves.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

6x6 VQFN	Symbol	Pin Function
1	EN	Device Enable Input. When EN = 0, the SPI and the internal regulator are disabled. The device is enabled when EN = 1. Note that the EN pin has no control over the clock buffers, as the clock buffers have their dedicated enable pins.
2	CLKP	Positive Input of the Internal System Clock and is compatible with LVDS/SSTL. For LVCMOS 2.5V input refer to Figure 4-8.
3	CLKN	Negative Input of the Internal System Clock and is compatible with LVDS/SSTL. For LVCMOS 2.5V input refer to Figure 4-8.
4	V_{LL}	+2.5V Positive Voltage Power Supply, it requires a 1.0 µF decoupling capacitor to GND
5, 33	GND	Ground, 0V
6	V_{DD}	+5V Positive Voltage Power Supply, it requires a 1.0 µF decoupling capacitor to GND
7	SCK	Serial Peripheral Interface (SPI) clock input
8	CSN	Serial Peripheral Interface (SPI) chip-select. CSN is an active-low signal.
9	SDI	Serial Peripheral Interface (SPI) data input
10	SDO	Serial Peripheral Interface (SPI) data output
11, 35	CBE0-1	The clock buffer enable pin. When CBEn = 0, the corresponding clock buffer is disabled. The clock buffer is enabled otherwise.
12, 34	CKB0-1	2.5V Single-ended Clock Buffer output pins
13	TXRW	CW Transmission Control pin. When TXRW = 0, the SPI is enabled for read/write. When TXRW = 1, the SPI is disabled and the CW transmission is started.
14, 23	V_{GN}	-10V Negative Voltage Power Supply, it requires a 2.2 µF capacitor to GND. The V_{GN} supply is also the substrate and should be the most negative supply to the chip.
15, 31	CNF	Negative Floating Supply Bypass Capacitor pin. Connects 1 µF/10V capacitor between this pin and the V_{CW-} pin.
16, 30	V_{CW-}	-1V to -6V Negative Voltage Power Supply for the CW output, it requires a 1.0 µF decoupling capacitor per pin to GND
17, 29	CPF	Positive Floating Supply Bypass Capacitor pin. Connects 1 µF/10V capacitor between this pin and the V_{CW+} pin.
18, 28	V_{CW+}	+1V to +6V Positive Voltage Power Supply for the CW output. It requires a 1.0 µF decoupling capacitor per pin to GND.
19, 20, 21, 22, 24, 25, 26, 27	CW0-7	Channel 0-7 CW Waveform Output
32	V_{GP}	+10V Positive Voltage Power Supply, it requires a 2.2 µF decoupling capacitor to GND
36	SPIB	SPI Broadcasting Mode pin. When SPIB = 1, the broadcast mode is enabled.
37	EP	Exposed Thermal Pad (EP); must be connected to GND

NOTES:

4.0 DEVICE DESCRIPTION

4.1 Operation Description

The MD1730 is an 8-channel ultra-low phase noise monolithic CW transmitter. It consists of an SPI interface to program internal phase delay registers and frequency dividers to facilitate CW beamforming. It supports differential LVDS/SSTL and single-ended 2.5V LVCMOS clock inputs. The MD1730's output path is designed to provide ultra-low phase noise and can swing up to ±6V. The following sections provide a detailed overview of MD1730's feature set and operation.

4.2 Using The Built-in Clock Buffers

The MD1730 has two built-in single ended clock output buffers. The MD1730 can accept LVDS, SSTL25 and LVCMOS 2.5V clock at its input and provide a single-ended output buffered clock. The clock buffers are independent of the chip's main EN pin and each output clock buffer can be enabled or disabled separately using the CBE0 or CBE1 pin. The maximum clock frequency of the buffers is 250 MHz. The output timing diagram for the clock buffers is shown in Figure 4-5. As shown in the diagram CKB0 and CKB1, clock outputs are only dependent on CBE0 and CBE1 respectively. This feature makes it convenient to drive the TX pulser retiming clock input, such as the HV7321. Using the built in clock buffers will save the cost of additional buffers, reduce PCB area, simplify the system clock distribution design and improve power savings as well.

4.3 SPI Registers Description

REGISTER 4-1: SPI CONTROL REGISTER DESCRIPTION

Data Bits	Description
W/R	The W/R is the read write control bit. When W/R = `1`, the SPI writes the data provided at the addressed register. When W/R = `0`, the SPI reads the data stored from the appropriate register. The read operation is disabled when SPIB = `1`.
CWFD<7:0>	The CWFD<7:0> register stores the divisor value for setting the CW output frequency. The CW output frequency is set by using the equation ($f_{CW} = f_{CLK}/(2*CWFD)$) except CWFD = `0`. For CWFD = `0` the CW output frequency is $f_{CW} = f_{CLK}/2*512$. The CW output frequency ranges from ($f_{CLK}/512$) ≤ f_{CW} ≤ ($f_{CLK}/2$). The register's initial value is `0`.
PHD_{CH}<7:0>	PHD_{CH}<7:0> sets the phase delay for each individual channel. The equation for the output delay time is PHD<7:0>/f_{CLK} + 2/f_{CLK} once TXRW goes high. The register initial value is `0`. Refer to Figure 4-4 for further details.
HIZ_{CH}	HIZ_{CH} bit enables the channel output when the corresponding bit is `0`. The channel is disabled and its' output becomes high Z when the corresponding bit is `1`. The default register value is `0`.

Note: CH denotes channel number 0 to 7.

REGISTER 4-2: SPI REGISTER ADDRESS AND CONTROL BITS

W/R	SPI Register ADD<3:0>				Write or Read Data <7:0>							
D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 = Write 0 = Read MSB first. (See Section 4.3 and Section 4.4)	0	0	0	0	Channel 0 phase delay PHD0<7:0>							
	0	0	0	1	Channel 1 phase delay PHD1<7:0>							
	0	0	1	0	Channel 2 phase delay PHD2<7:0>							
	0	0	1	1	Channel 3 phase delay PHD3<7:0>							
	0	1	0	0	Channel 4 phase delay PHD4<7:0>							
	0	1	0	1	Channel 5 phase delay PHD5<7:0>							
	0	1	1	0	Channel 6 phase delay PHD6<7:0>							
	0	1	1	1	Channel 7 phase delay PHD7<7:0>							
	1	0	0	0	HIZ7	HIZ6	HIZ5	HIZ4	HIZ3	HIZ2	HIZ1	HIZ0
	1	0	0	1	CW frequency divisor number CWFD<7:0>							

Note: Power-On or EN = 0 sets all the registers to 0.

TABLE 4-1: PHD<7:0> PHASE DELAY TIME REGISTER DESCRIPTION

PHD<7:0>	Delay Time to Start Transmitting
00000000	$0/f_{CLK}$ (Power-on default)
00000001	$1/f_{CLK}$
00000010	$2/f_{CLK}$
. . . . .	.....
11111110	$254/f_{CLK}$
11111111	$255/f_{CLK}$

TABLE 4-2: CWFD<7:0> CW FREQUENCY DIVIDER REGISTER DESCRIPTION

CWFD[7:0]	Transmit CW Frequency f_{CW}
00000000	$f_{CLK}/512$ (Power-on default)
00000001	$f_{CLK}/2$
00000010	$f_{CLK}/4$
00000011	$f_{CLK}/6$
. . . . .	.....
11111110	$f_{CLK}/508$
11111111	$f_{CLK}/510$

Note: The selected CW frequency is same for all the CW0~7 outputs: $f_{CW} = f_{CLK}/2*CWFD$. The CW frequency applies to all channels.

4.4 Serial Peripheral Interface (SPI)

The MD1730's SPI is used to program the phase delay and frequency divider registers. The SPI supports writing at speed up to 200 MHz and the MSB is shifted in first. SPI interface supports two operating modes: daisy chain mode and broadcasting mode.

When SPIB = 0, the MD1730 is in daisy chain mode. In this mode, it supports both read and write operations.

When SPIB = 1 the chip enters the "Broadcasting" mode. In this mode, the SDI data shifts into the shift register as well as to the SDO output. In this mode, the user can write the same register of different daisy chained chips with the same value in a single write transaction. However, when SPIB = 1 the read operation is disabled. To verify the written data for each chip, the user can revert SPIB = 0 and perform a normal read operation.

4.4.1 SPI WRITE OPERATION EXAMPLES

The following is a 1-byte writing example for the register at ADD = 0011b with the data D<7:0> = 01010101 when SPIB = TXRW = 0.

1. The Write operation starts with setting CSN to low.
2. The SCK clock is used to shift in the following SDI data:

D12 = 1, W/R bit set equal to high for write operation.

ADD<11:8> = 0011b, address for channel-3's phase delay register.

D<7:0> = 01010101b, data to be written into channel-3's phase delay register.

The SDI data is shifted in at the rising edge of SCK.

3. Once the complete data has been shifted in, the CSN should be taken high to finish the writing operation. The SDI data is latched into channel-3's phase delay register on the rising edge of the CSN signal. CSN has to be kept high for a minimum of 2-SCK cycles for the data to be written into the appropriate register.

In the case of eight chips daisy chained together as shown in Figure 4-3, there should be 13 x 8 = 104 cycles of SCK before the CSN is taken high.

The MD1730 can also be used in the Broadcasting mode to write several daisy chained chips with the same data. The Broadcasting mode can be used to reduce the time required to write the SPI if several MD1730 chips need the same data. The following is a 1-byte writing example for the register at the address location ADD = 0011b with data D<7:0> =01010101b while the MD1730 is set to broadcasting mode.

1. The write operation starts with setting CSN to low with TXRW = 0 and SPIB = 1.
2. The SCK clock is used to shift in the following SDI data to the first MD1730 chip:

   D12 = 1, W/R bit set equal to high for write operation.

   ADD<11:8> = 0011b, address for the channel-3's phase delay register.

   D<7:0> = 01010101, data to be written into the channel-3's phase delay register.

   The SDI data is shifted in at the rising edge of SCK.

   In Broadcasting mode, the same set of data shifted into the first chip's SDI is sent to all the MD1730 chips along the daisy chain. As shown is Figure 4-3 when SPIB = 1 an internal switch connects the SDI and SDO directly.
3. Once the complete data has been shifted in, the CSN should be taken high to finish the writing operation. The SDI data is latched into each chip's channel-3 phase delay register on the rising edge of the CSN signal. CSN has to be kept high for a minimum of 2-SCK cycles for the data to be written into the appropriate register.

4.4.2 SPI READ OPERATION EXAMPLES

The following is a 2-byte reading example from the register at ADD = 0011b (Channel-3's phase delay register) when SPIB = TXRW = 0.

1. The read operation starts with setting CSN to low.
2. The SCK clock is used to shift in the following SDI data:

   D12 = 0, W/R bit set equal to high for read operation.

   ADD<11:8> = 0011b, address for channel-3's phase delay register.

   D<7:0> = X, for a Read operation the data field is don't' care.

   The SDI data is shifted in at the rising edge of SCK.
3. Once the complete data has been shifted into the SPI the CSN is taken high. While CSN is high the MD1730 fetches the data located at ADD<11:9> = 0011b and places it in its internal shift register.
4. Once the complete data has been shifted in, the CSN should be taken high to finish the reading operation. While CSN is high the MD1730 fetches the data located at ADD<11:9> = 0011b and places it in its internal shift register. CSN has to be kept high for a minimum of 2-SCK cycles for the data to be fetched and placed into the internal shift register.
5. The CSN is taken low and during the next 13 SCK clock cycles, the fetched data in the internal shift register is clocked out on the rising edge of SCK from the SDO of the MD1730.

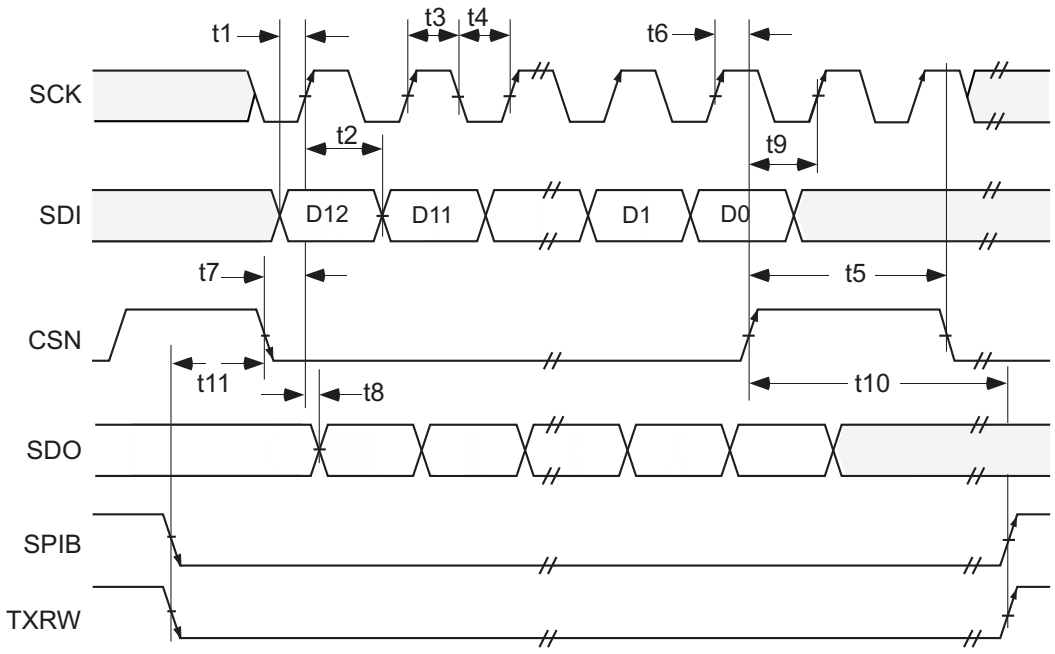


FIGURE 4-1: *SPI Register Read/Write Timing with SPIB = 0, TXRW = 0.*

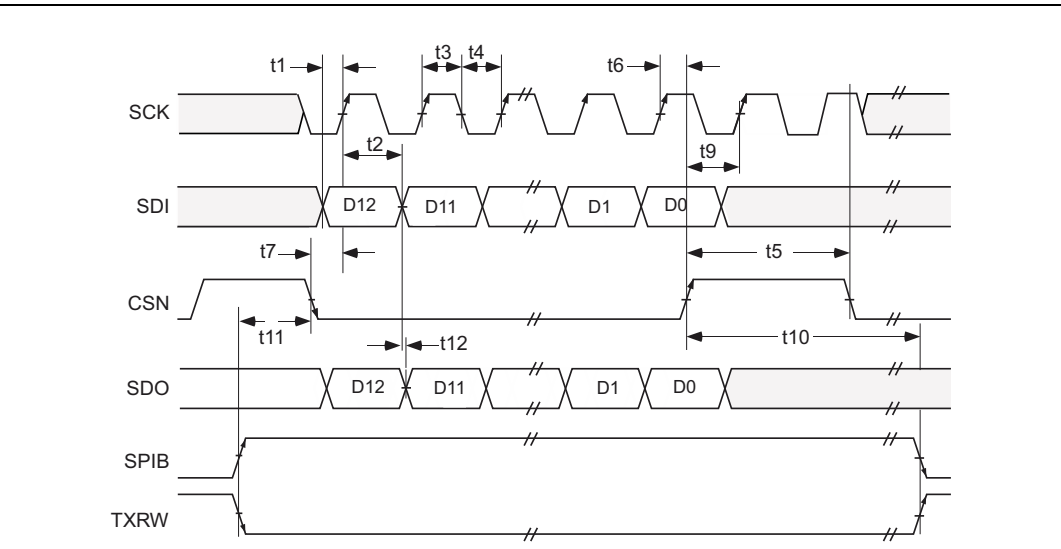


FIGURE 4-2: *SPI Register Broadcasting Write Timing with SPIB = 1, TXRW = 0.*

Note:	When in SPIB = 1 mode, the SPI register READ operations are not available.

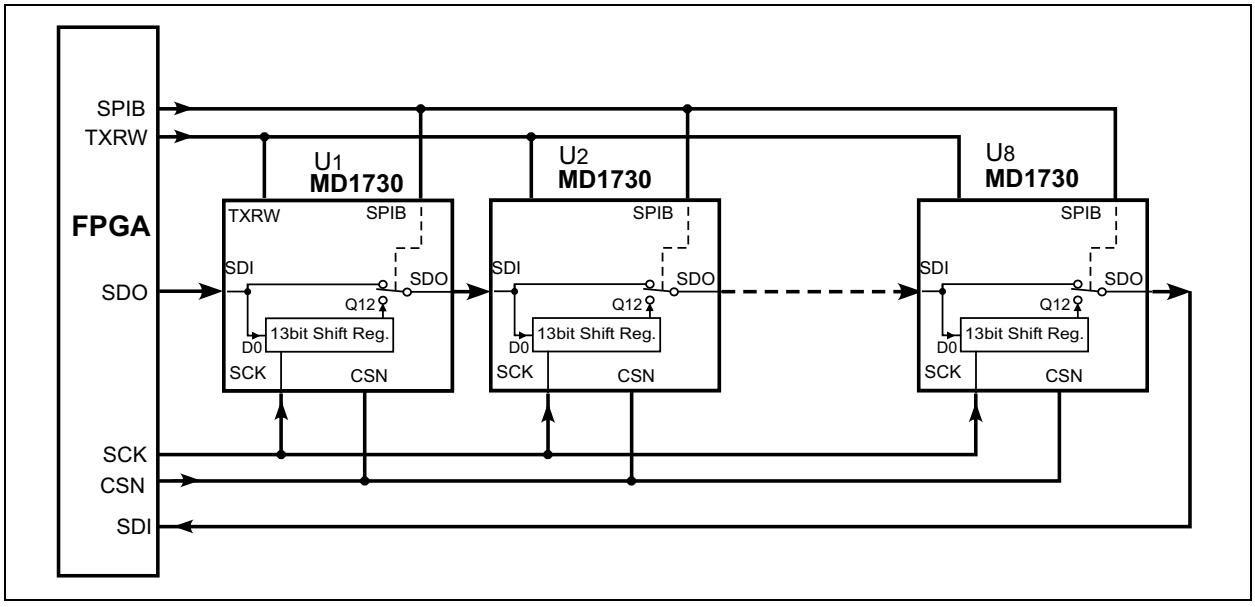


FIGURE 4-3: *Multiple MD1730 Devices SPI Daisy Chain Connections.*

4.5 CW0~7 Output Timing

The CW output waveform transmission timing is crucial to an ultrasound imaging system. Any small timing variations on the output can degrade the phase noise performance. The MD1730's internal circuitry is designed to ensure ultra-low phase noise. Figure 4-4 shows an example of the output waveform timing diagram. The chip is enabled by taking the EN pin high. Then using the SPI, channel-0's and channel-1's phase delay registers (PHD0<7:0> and PHD1<7:0>) are programmed with delays of 2 and 3 respectively. The rest of the channels are set to a high impedance state by programming the HIZ<7:0> register with data `11111100b`. Furthermore, the frequency divider register (CWFD<7:0>) is set to 4. After completing the SPI operation the transmission starts by asserting TXRW high. The phase delay counter starts counting down after a two CLK cycle latency. This is illustrated in Figure 4-4 for channel 0 and channel 1. In channel 0's case, the phase delay starts counting down from 2 to 0 after the latency and once the delay reaches 0 on the next rising edge of CLK, the positive output appears on the pin CW0. Based on the value of the CWFD<7:0> register, after 4-CLK cycles the CW0 output toggles to the negative supply rail. Subsequently, after 4-CLK cycles at the negative rail, the output switches back again to the positive supply rail, completing one full CW output wave cycle. This process continues until the TXRW pin deasserts low, which shuts the transmission off and forces the channel into a high impedance state. This same procedure applies to channel 1, which is also depicted in Figure 4-4.

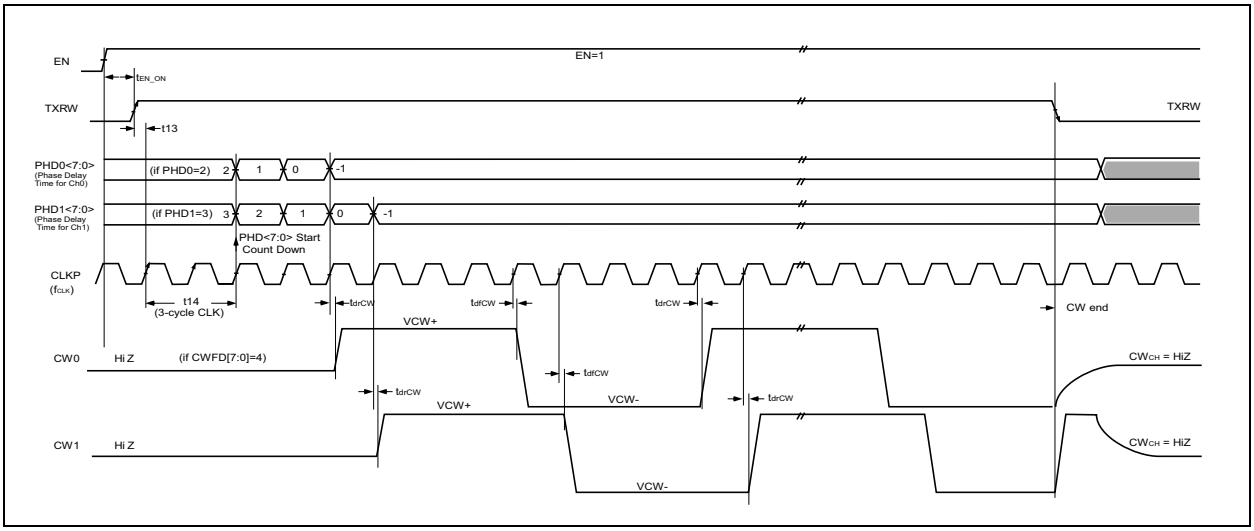


FIGURE 4-4: *CW0~7 Output Timing Diagram.*

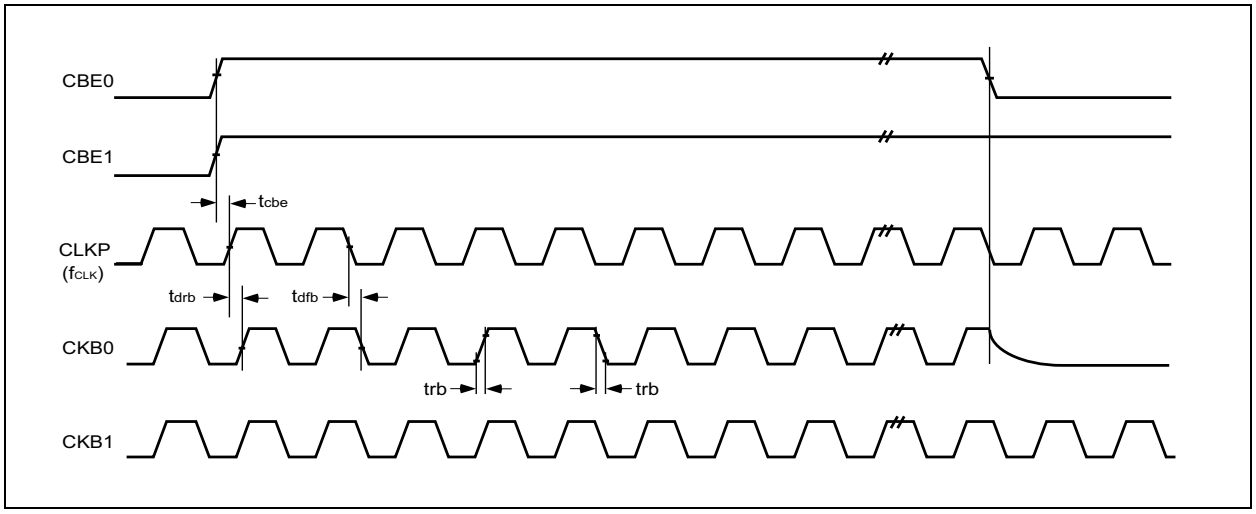


FIGURE 4-5: *Clock Buffers CKB0/1 Output Timing Diagram.*

4.6 MD1730 Working with Two HV7321

The diagrams shown in Figure 4-6 and Figure 4-7 illustrate the MD1730 driving two HV7321s.

When the HV7321 is operated in the specific mode, CW MODE = 1, along with the MD1730, the following steps should be taken to ensure the combination settings work correctly:

6. Apply all power supply rails to both chips and set HV7321's OEN = REN = PWS = `1` along with MD1730's EN = `1` to enable both chips. Set all other control logic pins to zero.
7. Adjust the VCW+ and VCW- power supplies to the required peak-to-peak voltage levels for CW output transmission. Please note that a higher peak-to-peak transmission voltage will result in the MD1730 dissipating more power. The power dissipation on the MD1730 is proportional to the square of the peak-to-peak voltage.
8. Assert HV7321's MODE pin high.
9. Program the MD1730 with the desired CW frequency divider and delay settings for CW transmission.
10. To place a channel in receive mode, set the corresponding pins SEL, NEG, POS = `011b` on the HV7321. To place a channel to CW Transmit mode, set the corresponding pins SEL, NEG, POS to any other combination other than `011b` on HV7321. This will put that channel of the HV7321 high voltage Tx output in High Z mode, but turn the channel's CWSW on.

In the case user wants a channel not in High Z or CW Transmit mode, then similarly, to set the channel of HV7321 to High Z and also set the MD1730's corresponding bit in the HIZ register to `1`.

11. Once the system is ready to perform CW Doppler measurement, assert TXRW high to start the CW transmission on the selected channels.

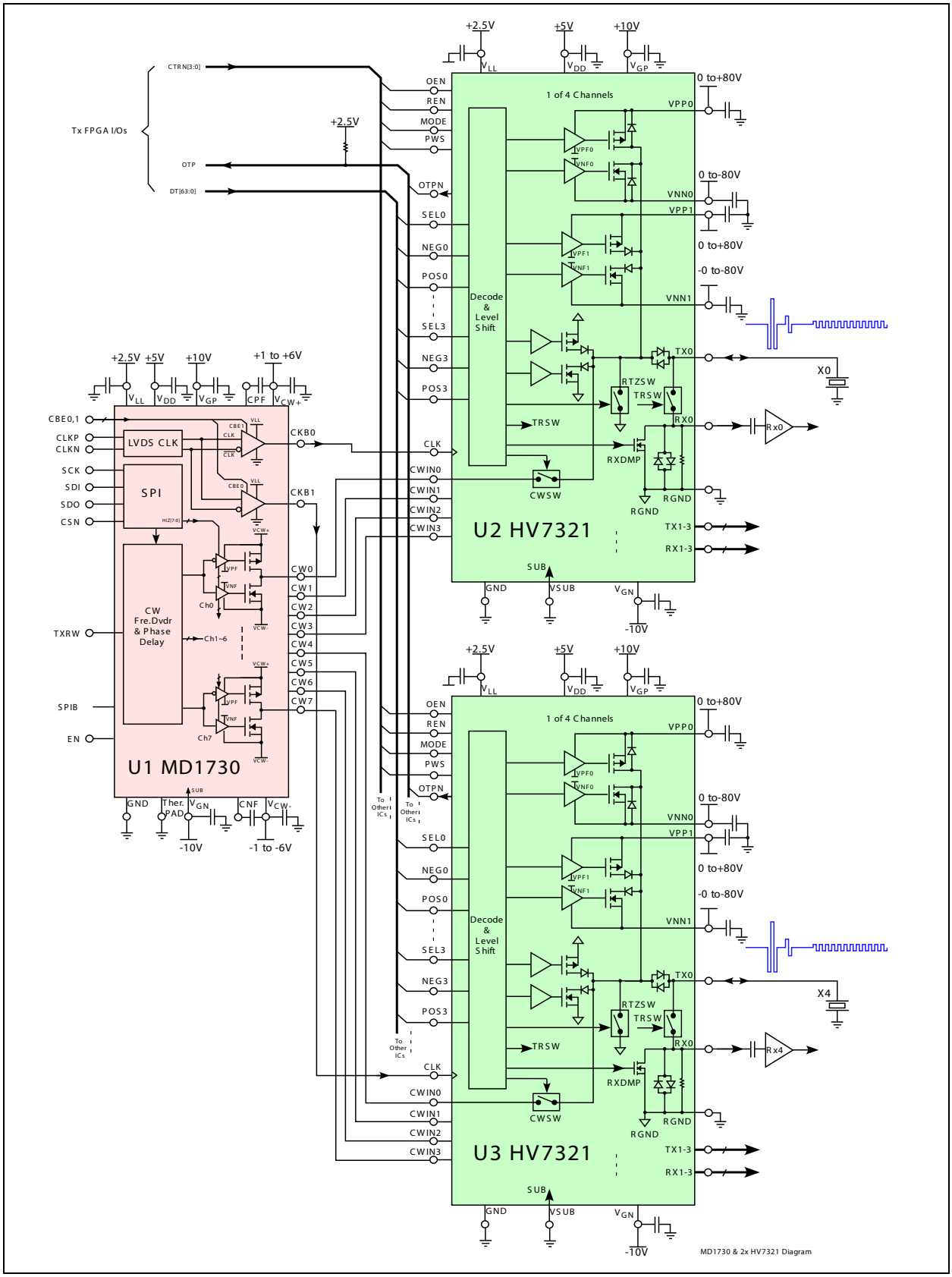


FIGURE 4-6: *MD1730 Works with Two HV7321 4-Channel ±80V 2.6A 5-Level Ultrasound Pulsers.*

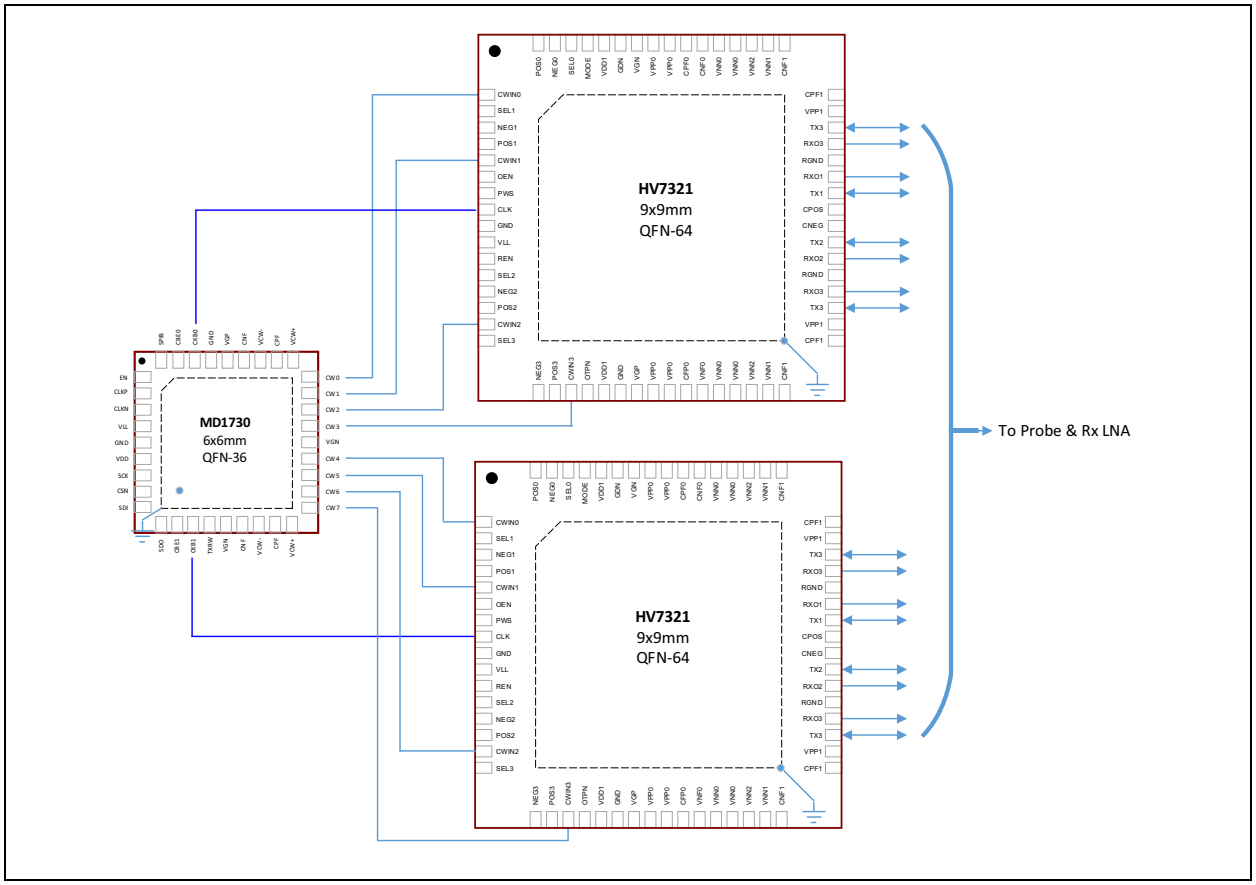


FIGURE 4-7: *MD1730 Working with Two HV7321 Pulsers Pinout and Package.*

4.7 CW Transmission Clock

The input clock of the MD1730, used for CW transmission, can be connected either differentially or single-ended. Figure 4-8 shows the LVDS differential implementation for the transmission clock. Here the CLKP and the CLKN pins are directly driven by a LVDS clock buffer. It is highly recommended that a multiple-output LVDS clock buffer IC is used, such as the SY89832U, and that a 100Ω termination resistor is placed very close to the CLKP and CLKN pins. For successful transmission of the LVDS signal over differential traces, the following guidelines should be followed while laying out the PCB board:

- To ensure minimal reflections and to maintain the receiver's common-mode noise rejection, keep the differential traces as short as possible between the clock buffer IC and the CLKP/CLKN pins of the MD1730.
- To reduce skew, the electrical lengths between differential LVDS traces should be identical. The arrival of one differential signal before the other will create a phase difference between the signal pairs, which would create clock skew and impair the system performance.
- Minimize the number of vias or other discontinuities in the signal path. To avoid discontinuities, arcs or 45-degree traces are recommended instead of 90-degree turns.
- Any parasitic loading, such as capacitance, must be present in equal amounts on each differential line.

Figure 4-9 illustrates the two cases for the MD1730 used in a single-ended configuration. In these cases, one of the clock input pins, CLKP or CLKN, is connected to the $V_{LL}/2$ voltage level and bypassed to ground with a 0.1 uF bypass capacitor. Each bypass capacitor must be placed very close to the MD1730. The other clock input pin connects to the main clock line. The PCB traces on the clock line must be designed for a 50Ω impedance with respect to the PCB ground place. Also, the clock pin must be terminated with a small 50Ω SMT resistor.

Generally, the LVCMOS input configuration provides better CW phase noise performance due to its higher amplitude swing as compared to the LVDS configuration. However, if the user needs a very high frequency clock transmission, such as 160 MHz-240 MHz range for a higher phase delay resolution, then LVDS should be used because it provides a better PCB clock trace distribution.

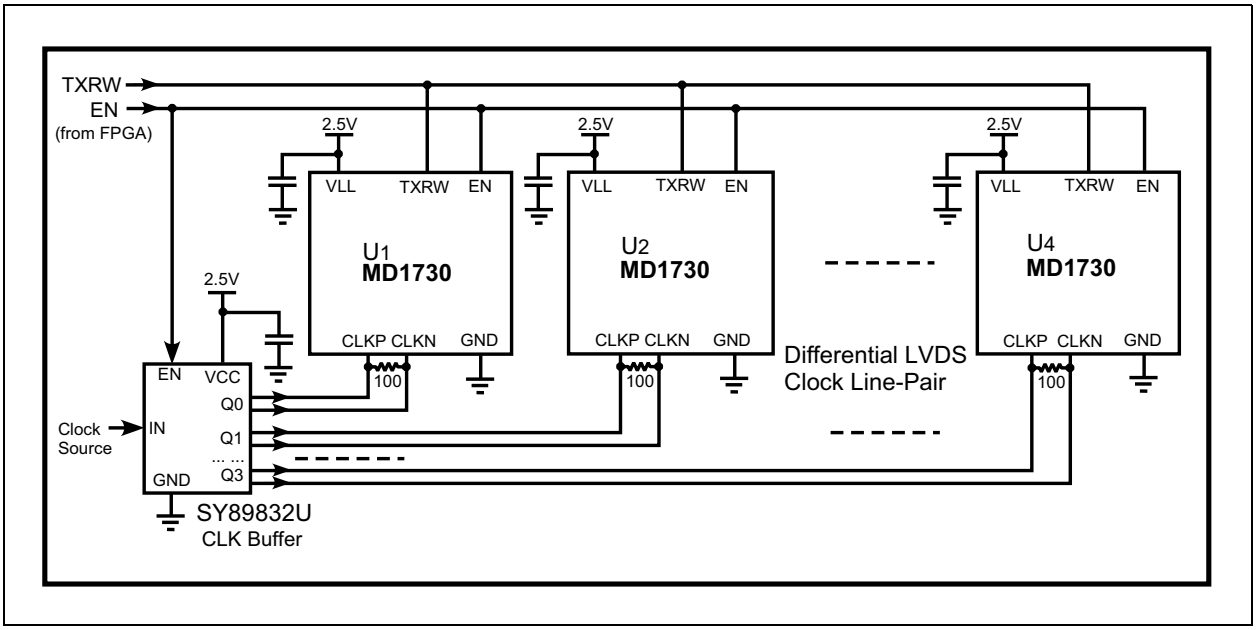


FIGURE 4-8: *LVDS Differential Transmission Clock.*

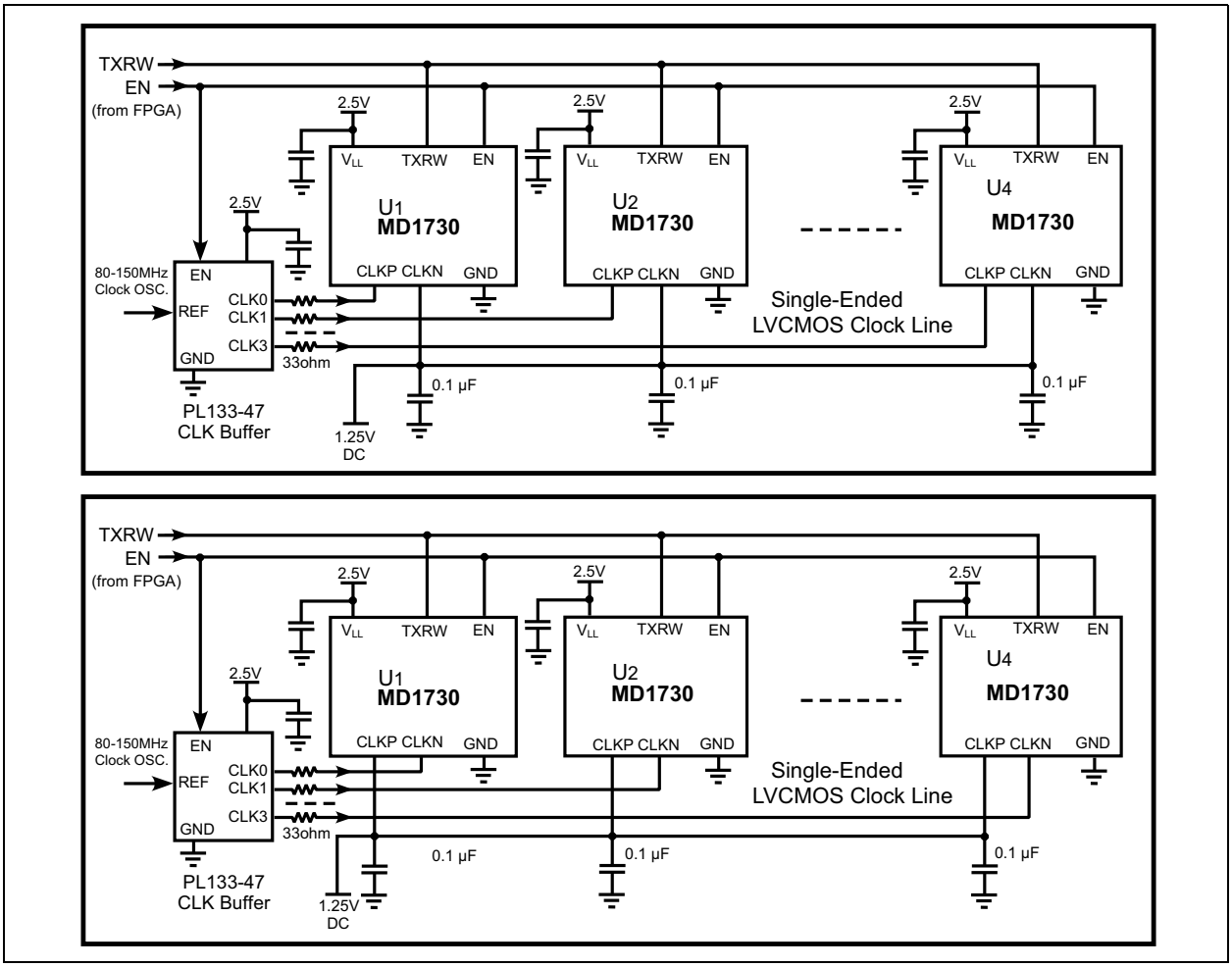


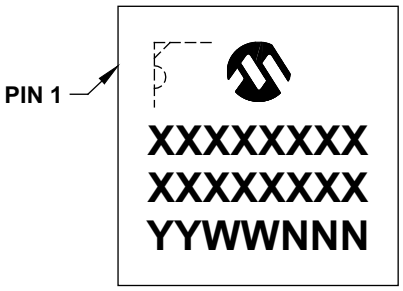
FIGURE 4-9: *LVCMOS Single-Ended Transmission Clock.*

NOTES:

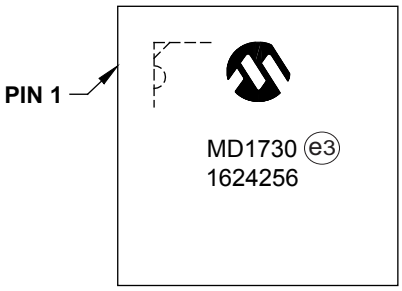
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

36-Lead VQFN (6x6x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.