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MD56V62160M-xxTA

4-Bank×1,048,576-Word×16-Bit SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The MD56V62160M-xxTA is a 4-Bank × 1,048,576-word × 16-bit Synchronous dynamic RAM. The device operates at 3.3V. The inputs and outputs are LVTTL compatible.

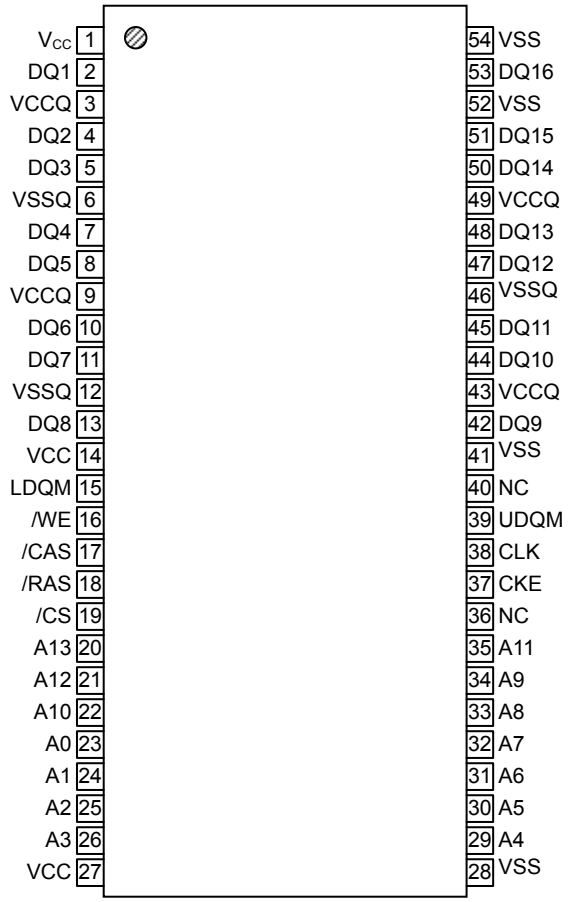
FEATURES

Product Name	MD56V62160M-XXTA
Organization	4Bank x 1,048,576Word x 16Bit
Address Size	4,096Row x 256Column
Power Supply VCC (Core)	3.3V±0.3V
Power Supply VCCQ (I/O)	3.3V±0.3V
Interface	LVTTL compatible
Operating Frequency	Max. 143MHz (Speed Rank 7)
Operating Temperature	0 to +70°C
/CAS Latency	2, 3
Burst Length	1, 2, 4, 8, Full page
Burst Type	Sequential, Interleave
Write Mode	Burst, Single
Refresh	Auto-Refresh, 4,096cycle/64ms, Self-Refresh

PRODUCT FAMILY

VCC	Family	Max. Frequency	Access Time (Max.)	
			tAC2	tAC3
3.0V～3.6V	MD56V62160M -7TA	143MHz	5.4ns	5.4ns
	MD56V62160M -75TA	133MHz	5.4ns	5.4ns
	MD56V62160M -8TA	125MHz	6ns	6ns
	MD56V62160M -10TA	100MHz	6ns	6ns

PIN CONFIGURATION (TOP VIEW)



54-Pin Plastic TSOP(II)
(K Type)

Pin Name	Function	Pin Name	Function
CLK	System Clock	UDQM, LDQM	Data Input / Output Mask
/CS	Chip Select	DQi	Data Input / Output
CKE	Clock Enable	VCC	Power Supply (3.3V)
A0 – A11	Address	VSS	Ground (0V)
A12,A13	Bank Select Address	VCCQ	Data Output Power Supply (3.3V)
/RAS	Row Address Strobe	VSSQ	Data Output Ground (0V)
/CAS	Column Address Strobe	NC	No Connection
/WE	Write Enable		

Note : The same power supply voltage must be provided to every VCC pin .

The same power supply voltage must be provided to every VCCQ pin.

The same GND voltage level must be provided to every VSS pin and VSSQ pin.

PIN DESCRIPTION

CLK	Clock (Input) Fetches all inputs at the “H” edge.
CKE	Clock Enable (Input) Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
/CS	Chip Select (Input) Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE and UDQM, LDQM.
/RAS	Row Address Strobe (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
/CAS	Column Address Strobe (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
/WE	Write Enable (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
A12,A13 (BA0,BA1)	Bank Address (Input) Slects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time.
A0 to A11	Row & column multiplexed. (Input) Row address : RA0 – RA11 Column Address : CA0 – CA7
DQ0 to DQ15	3-state Data Bus (Input/Output)
UDQM, LDQM	DQ Mask (Input) Masks the read data of two clocks later when DQM are set “H” at the “H” edge of the clock signal. Masks the write data of the same clock when DQM are set “H” at the “H” edge of the clock signal. UDQM controls DQ15 to DQ8, LDQM controls DQ7 to DQ0.
VCC, VSS	Power Supply (Core), Ground (Core) The same power supply voltage must be provided to every VCC pin. The same GND voltage level must be provided to every VSS pin.
VCCQ, VSSQ	Power Supply (I/O), Ground (I/O) The same power supply voltage must be provided to every VCCQ pin. The same GND voltage level must be provided to every VSSQ pin.
NC	No Connection

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on Input/Output Pin Relative to VSS	VIN, VOUT	–0.5 to VCC+0.5	V
VCC Supply Voltage	VCC	–0.5 to 4.6	V
VCCQ Supply Voltage	VCCQ	–0.5 to 4.6	V
Power Dissipation (Ta=25°C)	PD	1000	mW
Short Circuit Output Current	IOS	50	mA
Storage Temperature	Tstg	–55 to 150	°C
Operating Temperature	Ta	0 to +70	°C

Notes: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
2. Functional operation should be restricted to recommended operating condition.
3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended Operating Conditions (1/2)

Voltages referenced to VSS = 0 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage (Core)	VCC	3.0	3.3	3.6	V	1,2
Power Supply Voltage (I/O)	VCCQ	3.0	3.3	3.6	V	1,2
Ground	VSS, VSSQ	0	0	0	V	

Notes: 1. The voltages are referenced to VSS.
2. The power supply voltages should input stable voltage. The power supply voltages should not input oscillated voltage. If voltages are oscillating, please insert capacitor near the power supply pins and stop oscillation of voltage.

Recommended Operating Conditions (2/2)

Ta= 0 to +70° C

Parameter	Symbol	Min.	Max.	Unit	Note
Input High Voltage	VIH	2.0	VCC + 0.3	V	1, 2
Input Low Voltage	VIL	–0.3	0.8	V	1, 3

Notes: 1. The voltages are referenced to VSS.
2. The input voltage is VCC + 0.5V when the pulse width is less than 20ns (the pulse width is with respect to the point at which VCC is applied).
3. The input voltage is – 0.5V when the pulse width is less than 20ns (the pulse width respect to the point at which VSS and VSSQ are applied).

Pin Capacitance

Ta = 25°C, VCC＝VCCQ＝3.3V, f＝1MHz

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	CCLK	—	2	pF
Input Capacitance (A0 to A13, /RAS, /CAS, /WE, /CS, CKE, UDQM, LDQM)	CIN	—	2	pF
Input/Output Capacitance (DQ0 to DQ15)	COUT	—	3.5	pF

DC Characteristics (Input/Output)

Ta= 0 to +70°C
VCC = VCCQ = 3.3V±0.3V

Parameter	Symbol	Condition	Min.	Max.	Unit
Output High Voltage	VOH	IOH = –0.2mA	2.4	—	V
Output Low Voltage	VOL	IOL = 0.2mA	—	0.4	V
Input Leakage Current	ILI	0V≦VIN≦VCCQ	–10	10	µA
Output Leakage Current	ILO	—	–10	10	µA

Note : The voltages are referenced to VSS.

DC Characteristics (Power Supply Current)

Ta= 0 to +70°C
VCC = VCCQ = 3.3V±0.3V

Parameter	Symbol	Condition			MD56V62160M-xxTA				Unit	Note
					-7	-7.5	-8	-10		
		Bank	CKE	Other	Max.	Max.	Max.	Max.		
Average Power Supply Current (Operating)	ICC1	One Bank Active	CKE≧VIH tCC = Min. tRC = Min. No Burst		100	90	80	70	mA	1, 2
Power Supply Current (Standby)	ICC2	All Banks Precharge	CKE ≧ VIH	t_{CC} = Min.	40	35	35	30	mA	3
Average Power Supply Current (Clock Suspension)	ICC3S	All Banks Active	CKE ≦ VIL	t_{CC} = Min.	3	3	3	3	mA	2
Average Power Supply Current (Active Standby)	ICC3	One Bank Active	CKE ≧ VIH	t_{CC} = Min.	45	40	40	35	mA	3
Power Supply Current (Burst)	ICC4	All Banks Active	CKE ≧ VIH	t_{CC} = Min.	140	130	120	100	mA	1, 2
Power Supply Current (Auto-Refresh)	ICC5	All Bank Active	CKE ≧ VIH	t_{CC} = Min. t_{RC} = Min.	140	130	120	100	mA	2
Average Power Supply Current (Self-Refresh)	ICC6	All Banks Precharge	CKE ≦ VIL	t_{CC} = Min.	2	2	2	2	mA	
Average Power Supply Current (Power Down)	ICC7	All Banks Precharge	CKE ≦ VIL	t_{CC} = Min.	2	2	2	2	mA	

Notes: 1. Measured with outputs open.
2. The address and data can be changed once or left unchanged during one cycle.
3. The address and data can be changed once or left unchanged during two cycles.

AC Characteristics (1/2)

Ta= 0 to +70°C
VCC = VCCQ = 3.3V±0.3V
Note1,2

Parameter		Symbol	MD56V62160M-xxTA								Unit	Note
			-7		-75		-8		-10			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Clock Cycle Time	CL=3	t_{CC3}	7	—	7.5	—	8	—	10		ns	
	CL=2	t_{CC2}	10	—	10	—	10	—	10		ns	
Access Time from Clock	CL=3	t_{AC3}	—	5.4	—	5.4	—	6	—	6	ns	3,4
	CL=2	t_{AC2}	—	5.4	—	5.4	—	6	—	6	ns	3,4
Clock High Pulse Time		tCH	2	—	2.5	—	3	—	3	—	ns	4
Clock Low Pulse Time		tCL	2	—	2.5	—	3	—	3	—	ns	4
Input Setup Time		tSI	1.5	—	1.5	—	2	—	2	—	ns	
Input Hold Time		tHI	0.8	—	0.8	—	1	—	1	—	ns	
Output Low Impedance Time from Clock		tOLZ	2	—	2	—	2	—	2	—	ns	
Output High Impedance Time from Clock		tOHZ	—	5.4	—	5.4	—	6	—	6	ns	
Output Hold from Clock		tOH	2	—	2	—	2	—	2	—	ns	3
Random Read or Write Cycle Time		tRC	60	—	65	—	70	—	70	—	ns	
RAS Precharge Time		tRP	18	—	18	—	20	—	20	—	ns	
RAS Pulse Width		tRAS	42	10^5	45	10^5	50	10^5	50	10^5	ns	
/RAS to /CAS Delay Time		tRCD	16	—	16	—	20	—	20	—	ns	
Write Recovery Time		tWR	2	—	2	—	2	—	2	—	Cycle	
/RAS to /RAS Bank Active Delay Time		tRRD	10	—	15	—	20	—	20	—	ns	
Refresh Time		tREF	—	64	—	64	—	64	—	64	ms	5
Power-down Exit setup Time		tPDE	t_{SI}+1CLK	—	t_{SI}+1CLK	—	tSI+1CLK	—	tSI+1CLK	—	ns	
Refresh cycle Time		tRCA	60	—	65	—	70	—	70	—	ns	

AC Characteristics (2/2)

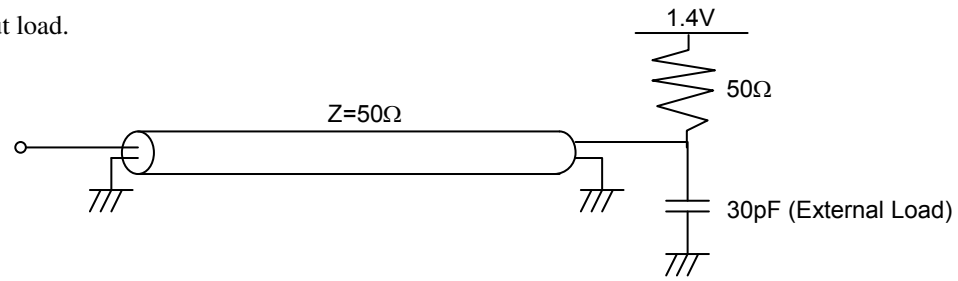
Ta= 0 to +70°C
VCC = VCCQ = 3.3V±0.3V
Note1,2

Parameter	Symbol	MD56V62160M-xxTA				Unit	Note
		-7	-7.5	-8	-10		
/CAS to /CAS Delay Time (Min.)	I_{CCD}	1	1	1	1	Cycle	
Clock Disable Time from CKE	I_{CKE}	1	1	1	1	Cycle	
Data Output High Impedance Time from UDQM, LDQM	I_{DOZ}	2	2	2	2	Cycle	
Dada Input Mask Time from UDQM, LDQM	I_{DOD}	0	0	0	0	Cycle	
Data Input Mask Time from Write Command	I_{DWD}	0	0	0	0	Cycle	
Data Output High Impedance Time from Precharge Command	I_{ROH}	CL	CL	CL	CL	Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	I_{MRD}	2	2	2	2	Cycle	
Write Command Input Time from Output	I_{OWD}	2	2	2	2	Cycle	

Notes: 1. AC measurements assume that tT = 1ns,.
2. Test condition

Parameter	Test Condition		Unit
Input voltage for AC measurement	2.4	0.4	V
Transition Time for AC measurement	tT＝1		ns
Reference level for timing of input signal (tT≤1ns)	1.4		V
Reference level for timing of input signal (tT>1ns)	VIH Min.	VIL Max.	V
Reference level for timing of output signal	1.4		V

3. Output load.



4. If tT is longer than 1ns, then the reference level for timing of input signals is VIH and VIL.
5. It is necessary to operate auto-refresh 4096 cycles within tREF.

POWER ON AND INITIALIZE

Power on Sequence

1. Apply power and attempt to maintain CKE="H" and other pins are NOP condition at the input.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200 μs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue mode register set command to initialize the mode register.
6. Issue extended mode register set command to initialize the extended mode register.

Mode Register Set Command (MRS)

The mode register stores the data for controlling the various operating modes. It programs the /CAS latency, burst type, burst length and write mode. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by mode register set command MRS. The state of address pins A13 to A0 in the same cycle as MRS is the data written in the mode register. Refer to the table for specific codes for various /CAS latencies, burst type, burst length and write mode.

MRS

CLK	n-1	n
CKE	H	**X**
/CS	X (Idle)	**L**
/RAS		**L**
/CAS		**L**
/WE		**L**
BA1(A12)	X	**0**
BA0(A13)	X	**0**
A11~A0	X	**V**

V: The value of mode register set

Extended Mode Register Set Command (EMRS)

The extended mode register stores the data for controlling output driver strength. The default value of the extended mode register is defined. Therefore the mode register must be written after power up to operate the SDRAM. The extended mode register is written by extended mode register set command EMRS. The state of address pins A13 to A0 in the same cycle as EMRS is the data written in the extended mode register. Refer to the table for specific codes for various self-Refresh operations.

EMRS

CLK	n-1	n
CKE	H	**X**
/CS	X (Idle)	**L**
/RAS		**L**
/CAS		**L**
/WE		**L**
BA1(A12)	X	**1**
BA0(A13)	X	**0**
A11~A0	X	**V**

V: The value of extended mode

Mode Register Field Table To Program Mode

Write Burst Mode		/CAS Latency				Burst Type		Burst Length				
A9	WM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Burst	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single	0	0	1	Reserved	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

Notes: 1. A13 and A12 should stay “0” during mode set cycle.
2. A7, A8, A10 and A11 should stay “0” during mode set cycle.
3. Don’t set address keys of “Reserved”.

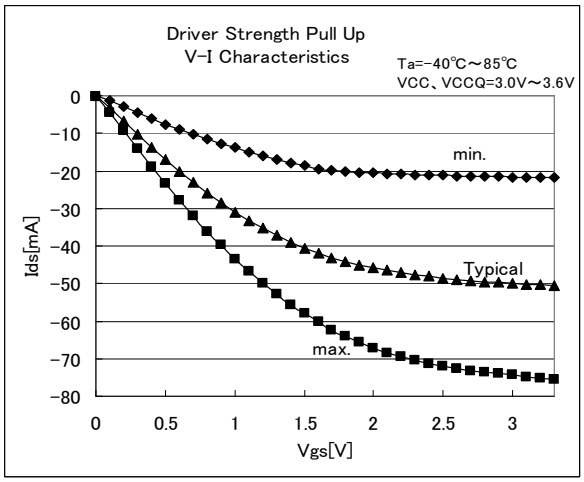
Extended Mode Register Set Address Keys

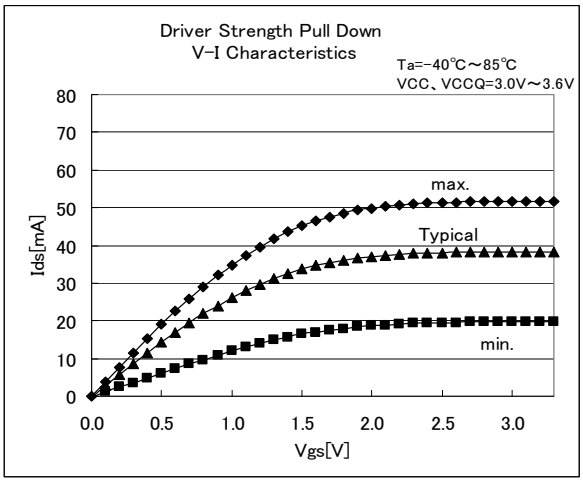
Output Driver Strength		
A6	A5	DS
0	0	Full (Default)
0	1	1/2
1	0	Reserved
1	1	1/4

Notes: 1. A12 should stay “H” and A13 should stay “0” during mode set cycle.
2. A0, A1, A2, A3, A4, A7, A8, A9, A10 and A11 should stay “0” during mode set cycle.
3. Don’t set address keys of “Reserved”.
4. If don’t set EMRS, DS is set to default (Full).

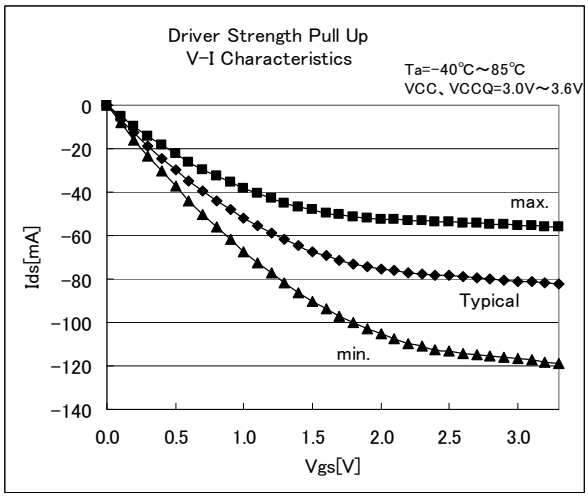
Output Driver Characteristics

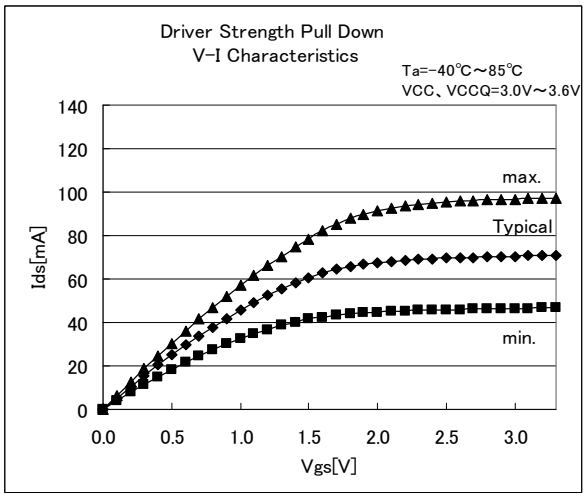
Output Driver Strengt=1/4



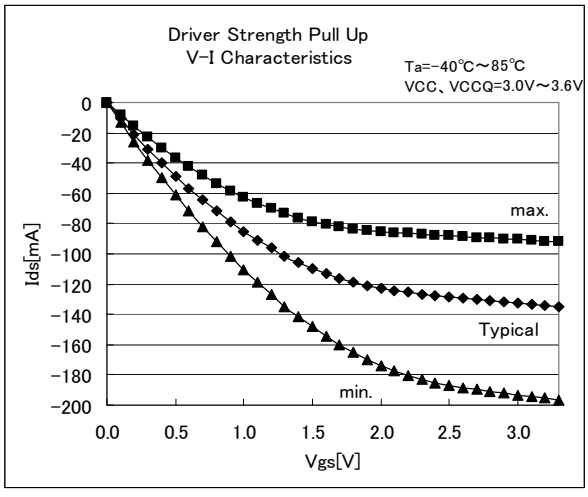


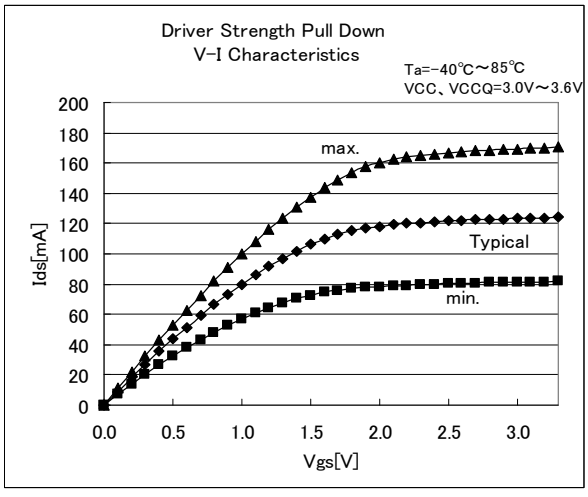
Output Driver Strengt=1/2





Output Driver Strengt= Full (Default)





Burst Mode

Burst operation is the operation to continuously increase a column address inputted during read or write command. The upper bits select a column address block,

		Access order in column address block				
		Start Address (Lower bit)			Burst Type	
					BT=Sequential	BT=Interleave
Burst Length	BL=2			A0		
				0	0, 1	0, 1
				1	1, 0	1, 0
	BL=4		A1	A0		
			0	0	0, 1, 2, 3	0, 1, 2, 3
			0	1	1, 2, 3, 0	1, 0, 3, 2
			1	0	2, 3, 0, 1	2, 3, 0, 1
			1	1	3, 0, 1, 2	3, 2, 1, 0
	BL=8	A2	A1	A0		
		0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
		0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
		0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
		1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
		1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
	BL=Full Page (256)	A7~A0				
		0			0, 1… 255	Non Support
		Yn			Yn, Yn+1… 255, 0… …Yn-1	

READ / WRITE OPERATION

Bank

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The A12 and A13 input is latched at the time of assertion of /RAS and /CAS to select the bank to be used for operation. The bank address A12 and A13 are latched at bank active, read, write, mode register set and precharge operations.

Bank Address

A12	A13	Bank
0	0	A
0	1	B
1	0	C
1	1	D

Activate

The bank activate command is used to select a random row in an idle bank. By asserting low on /RAS and /CS with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of tRCD(min) from the time of bank activation.

ACT

CLK	n-1	n
CKE	H	**X**
/CS	X (Idle)	**L**
/RAS		**L**
/CAS		**H**
/WE		**H**
A13,A12	X	**BA**
A11~A0	X	**RA**

BA: Bank Address
RA: Row Address (Page)

Precharge

The precharge operation is performed on an active bank by precharge command (PRE) with valid A13 and A12 of the bank to be precharged. The precharge command can be asserted anytime after tRAS(min) is satisfied from the bank active command in the desired bank. All bank can precharged at the same time by using precharge all command (PALL). Asserting low on /CS, /RAS and /WE with high on A10 after all banks have satisfied tRAS(min) requirement, performs precharge on al banks. At the end of tRP after performing precharge to all banks, all banks are in idle state.

PRE

CLK	n-1	n
CKE	H	**X**
/CS	X (Page Open)	**L**
/RAS		**L**
/CAS		**H**
/WE		**L**
A13,A12	X	**BA**
A10	X	**0**
A11,A9~A0	X	**X**

BA: Bank Address

PALL

CLK	n-1	n
CKE	H	**X**
/CS	X (Page Open)	**L**
/RAS		**L**
/CAS		**H**
/WE		**L**
A13,A12	X	**X**
A10	X	**1**
A11,A9~A0	X	**X**

Write / Write with Auto-Precharge

The write command is used to write data into the SDRAM on consecutive clock cycles in adjacent address depending on burst length and burst sequence. By asserting low on /CS, /CAS and /WE with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even through the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length.

WRT

CLK	n-1	n
CKE	H	**X**
/CS	X (Page Open)	**L**
/RAS		**H**
/CAS		**L**
/WE		**L**
A13, A12	X	**BA**
A10	X	**0**
A11,A9, A8	X	**X**
A7~A0	X	**CA**
DQ	X	**D-in**

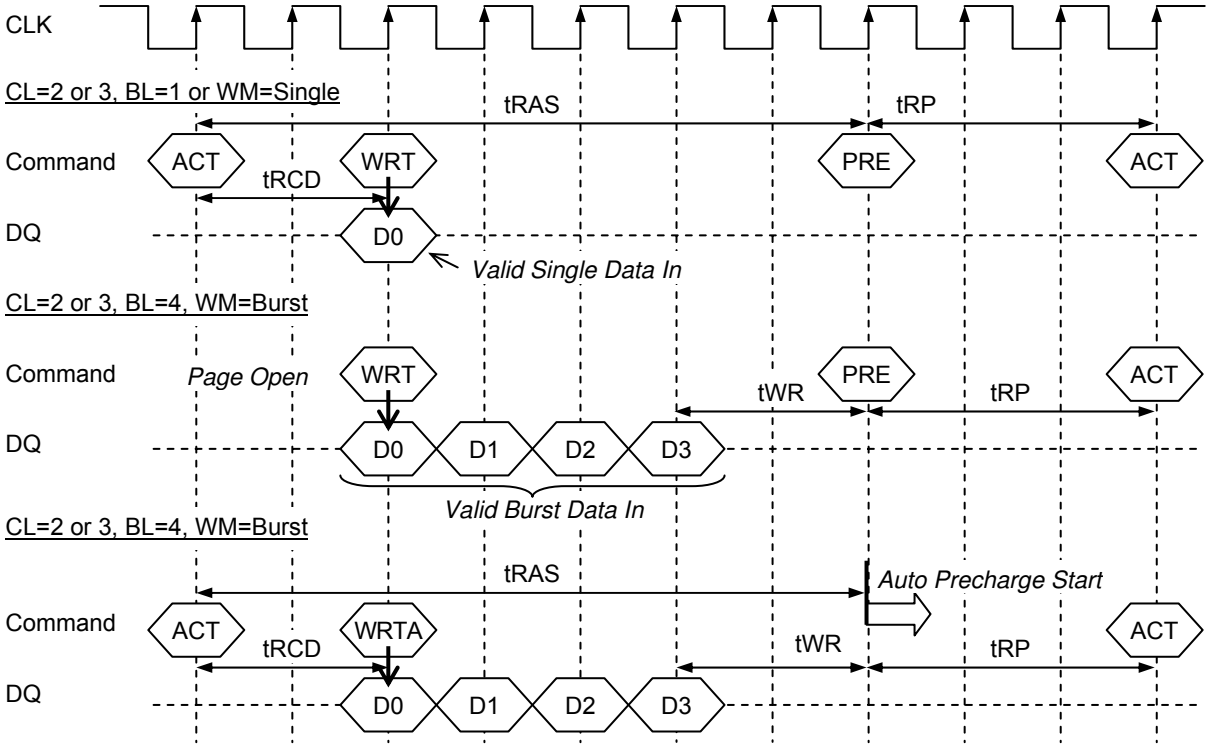
BA: Bank Address
CA: Column Address
D-in: Data inputs

WRTA

CLK	n-1	n
CKE	H	**X**
/CS	X (Page Open)	**L**
/RAS		**H**
/CAS		**L**
/WE		**L**
A13, A12	X	**BA**
A10	X	**1**
A11,A9, A8	X	**X**
A7~A0	X	**CA**
DQ	X	**D-in**

BA: Bank Address
CA: Column Address
D-in: Data inputs

Write Cycle



Read / Read with Auto-Precharge

The read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The read command is issued by asserting low on /CS and /CAS with /WE being high on the positive edge of the clock. The bank must be active for at least tRCD(min) before the read command is issued. The first output appears in /CAS latency number of clock cycles after the issue of read command. The burst length, burst sequence and latency from the read command are determined by the mode register that is already programmed.

RD

CLK	n-1	n
CKE	H	**X**
/CS	X (Page Open)	**L**
/RAS		**H**
/CAS		**L**
/WE		**H**
A13, A12	X	**BA**
A10	X	**0**
A11, A9, A8	X	**X**
A7~A0	X	**CA**
DQ	X	**X**

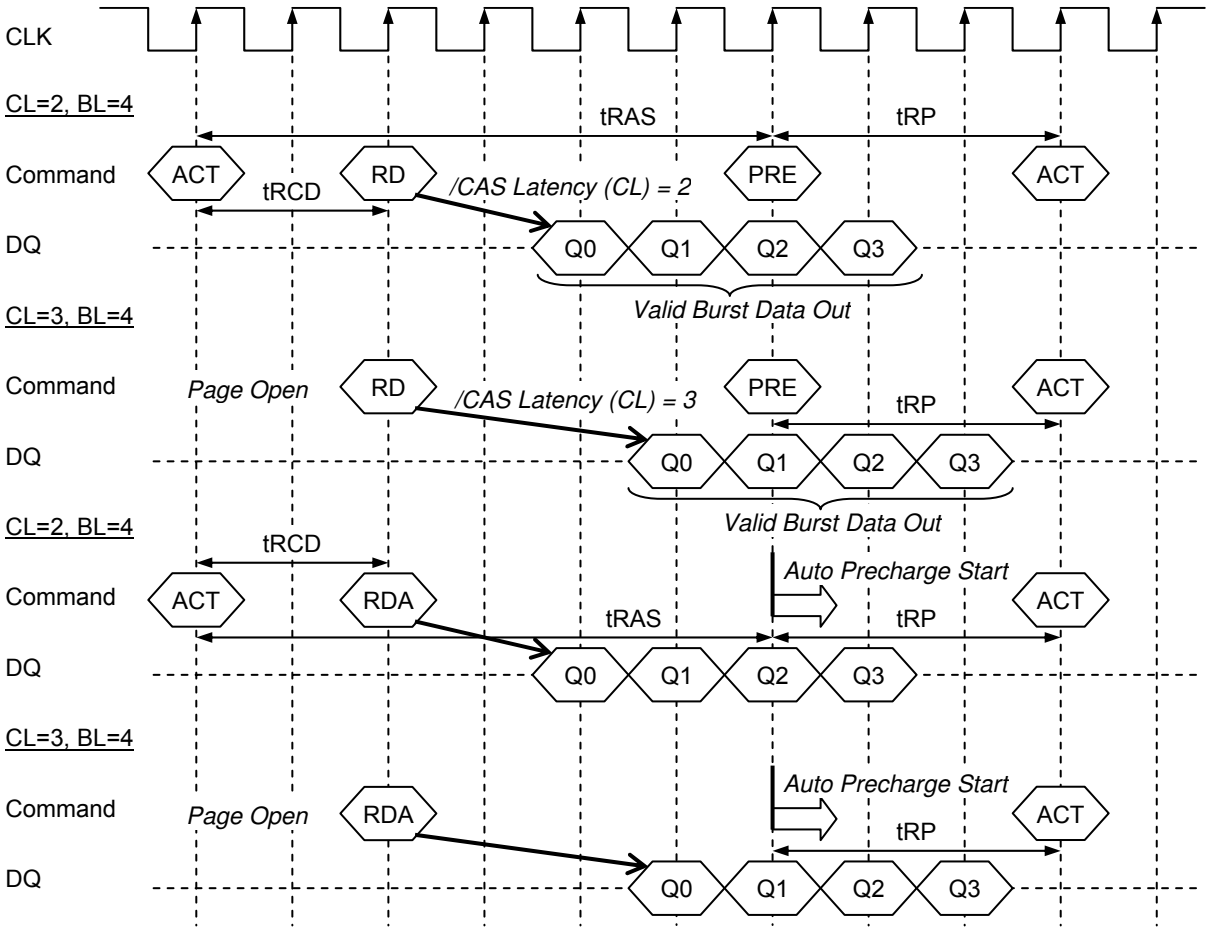
BA: Bank Address
CA: Column Address

RDA

CLK	n-1	n
CKE	H	**X**
/CS	X (Page Open)	**L**
/RAS		**H**
/CAS		**L**
/WE		**H**
A13, A12	X	**BA**
A10	X	**1**
A11, A9, A8	X	**X**
A7~A0	X	**CA**
DQ	X	**X**

BA: Bank Address
CA: Column Address

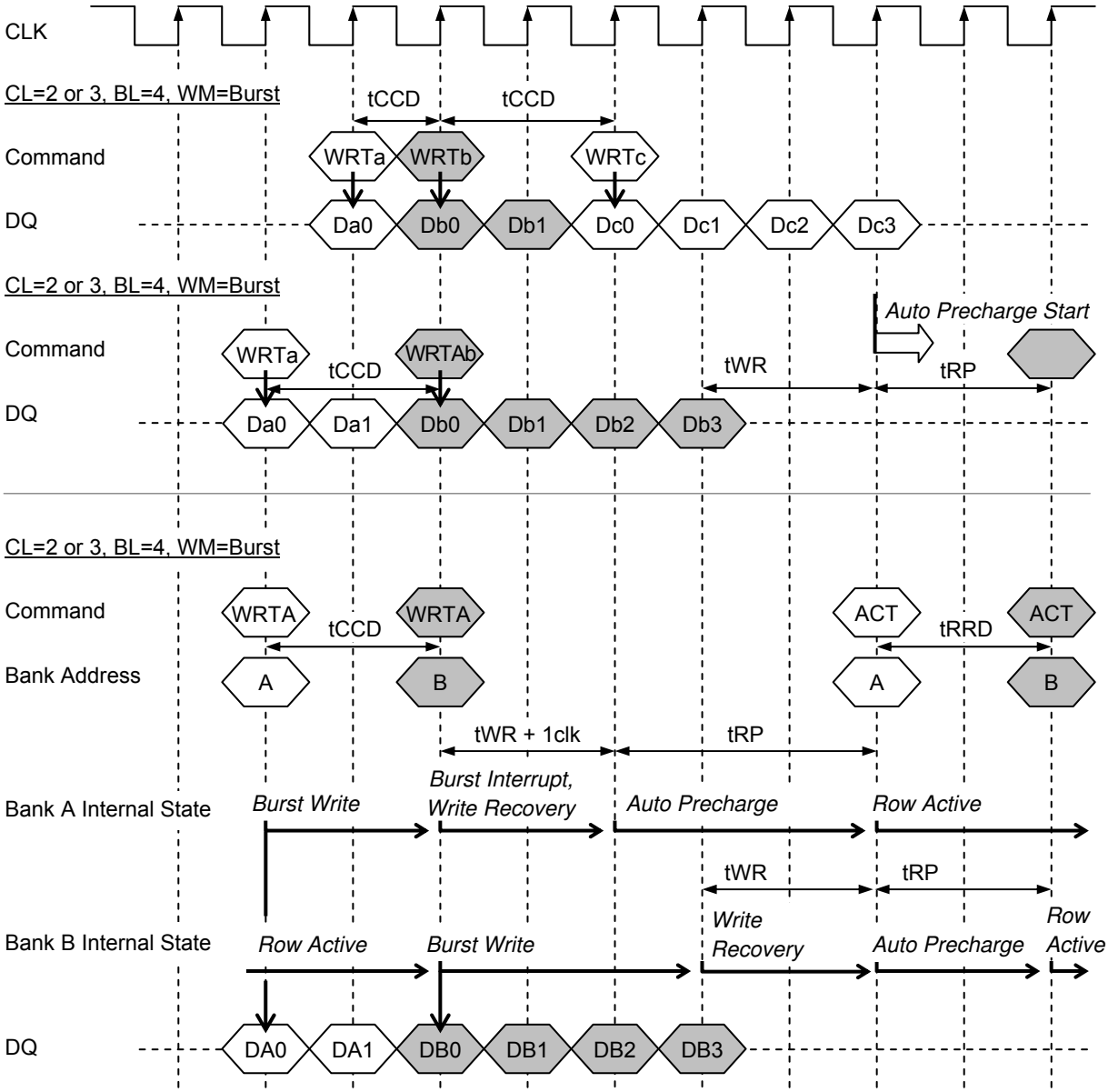
Read Cycle



Write / Write interrupt

When a new write command is issued to same bank during write cycle or another active bank, current burst write is terminated and new burst write start. When a new write command is issued to another bank during a write with auto-precharge cycle, current burst is terminated and a new write command start. Then, current bank is precharged after specified time. Don't issue a new write command to same bank during write with auto-precharge cycle.

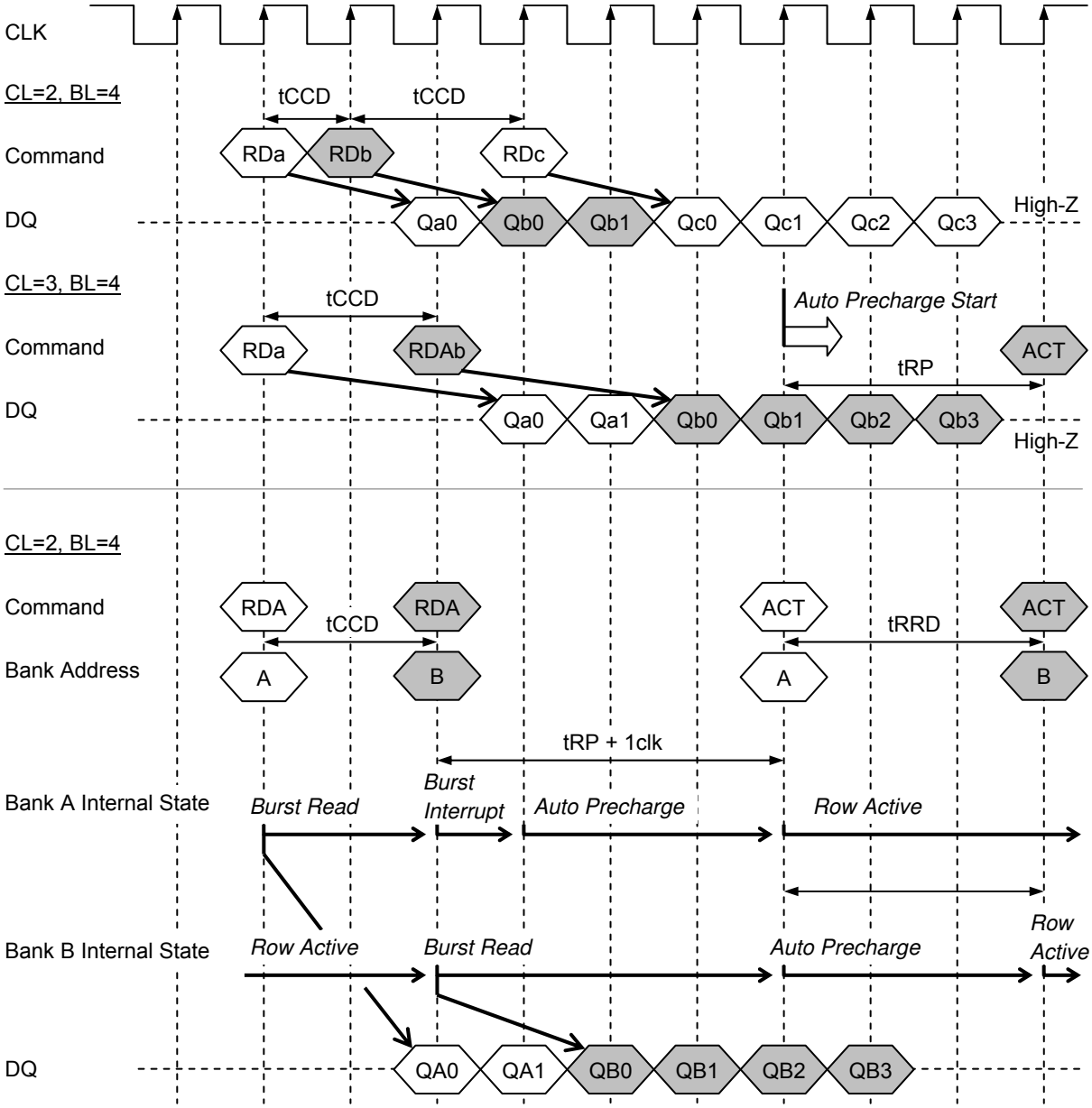
Write / Write interrupt cycle



Read / Read interrupt

When a new read command is issued to same bank during read cycle or another active bank, current burst read is terminated after the cycle same as /CAS latency and new burst read start. When a new read command is issued to another bank during a read with auto-precharge cycle, current burst is terminated after the cycle same as /CAS latency and a new read command start. Then, current bank is precharged after specified time. Don't issue a new read command to same bank during read with auto-precharge cycle.

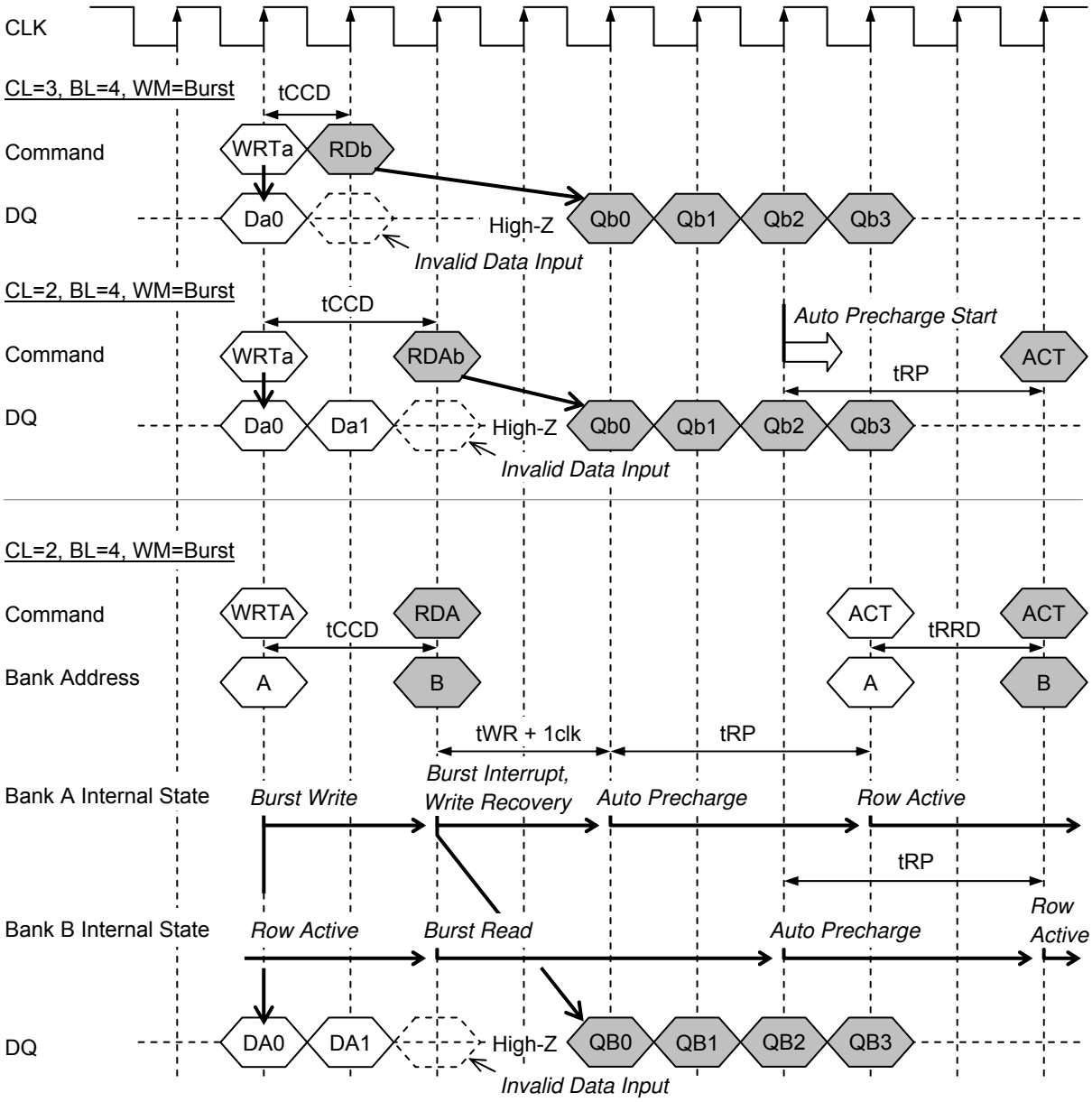
Read / Read interrupt cycle



Write / Read interrupt

When a new read command is issued to same bank during write cycle or another active bank, current burst write is terminated and new burst read start. When a new read command is issued to another bank during a write with auto-precharge cycle, current burst is terminated and a new read command start. Then, current bank is precharged after specified time. Don't issue a new read command to same bank during write with auto-precharge cycle. DQ must be hi-Z till 1 or more clock from first read data.

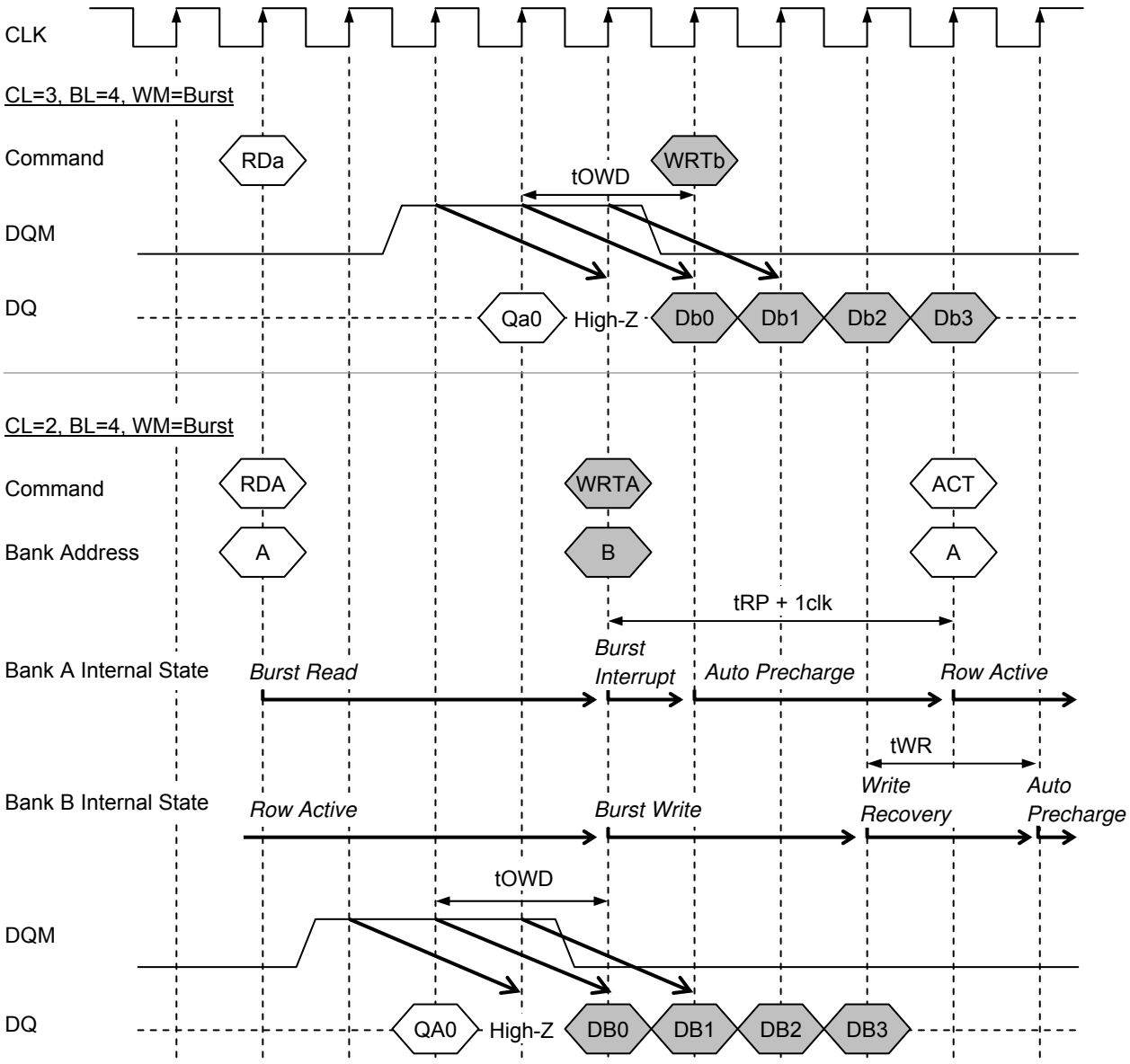
Write / Read interrupt cycle



Read / Write interrupt

When a new write command is issued to same bank during read cycle or another active bank, current burst read is terminated and new burst write start. When a new write command is issued to another bank during a read with auto-precharge cycle, current burst is terminated and a new write command start. Then, current bank is precharged after specified time. Don't issue a new write command to same bank during read with auto-precharge cycle. DQ must be Hi-Z till 1 or more clock from new write command. Therefore, DQM must be high till 3 clocks from new write command.

Read / Write interrupt cycle



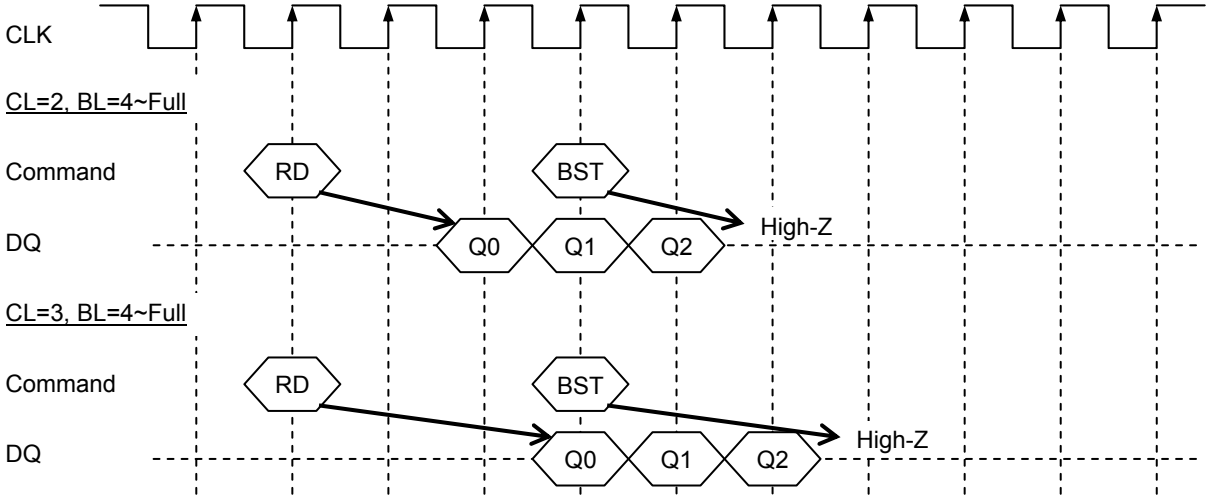
Burst Stop

When a burst stop command is issued during read cycle, current burst read is terminated. The DQ is to Hi-Z after the cycle same as /CAS latency and page keep open. When a burst stop command is issued during write cycle, current burst write is terminated. The input data is ignored after burst stop command. Don't issue burst stop command during read with auto-precharge cycle or write with auto-precharge cycle.

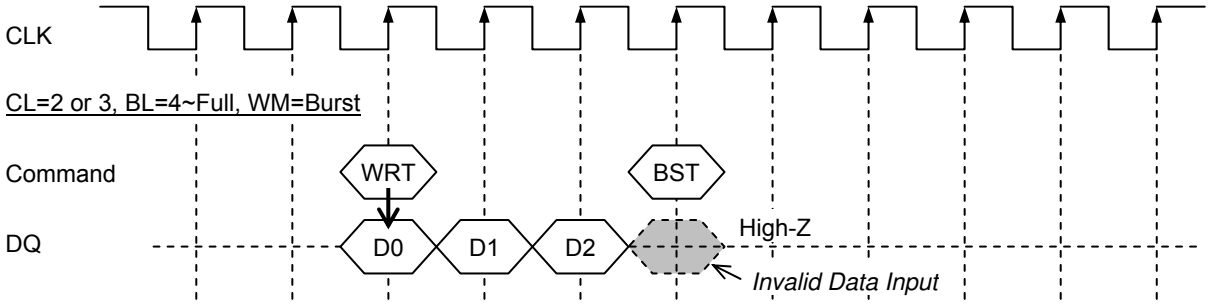
BST

CLK	n-1	n
CKE	H	**H**
/CS	X (Burst)	**L**
/RAS		**H**
/CAS		**H**
/WE		**L**
A13, A12	X	**X**
A11~A0	X	**X**

Read / Burst Stop cycle



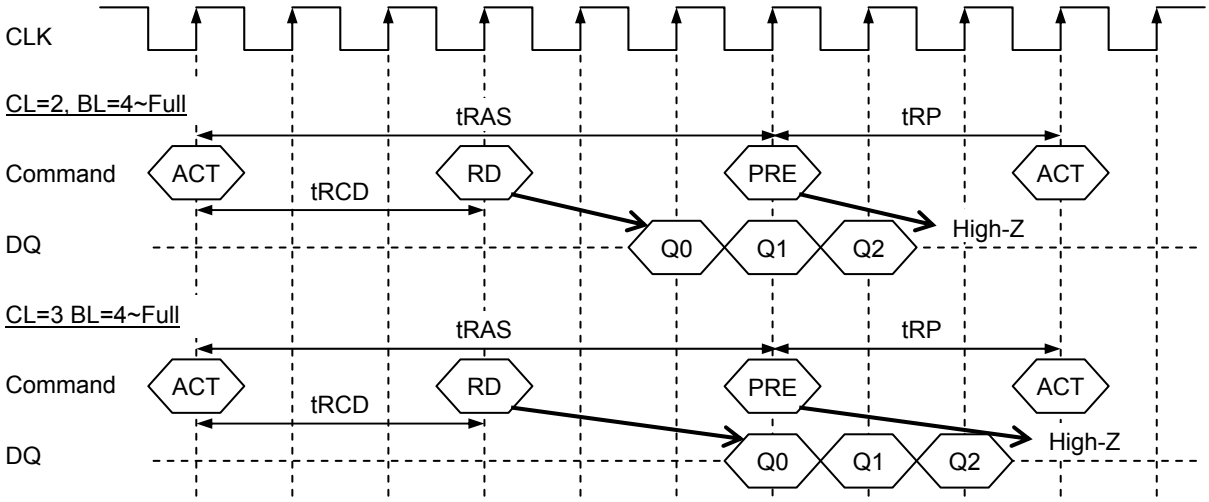
Write / Burst Stop cycle



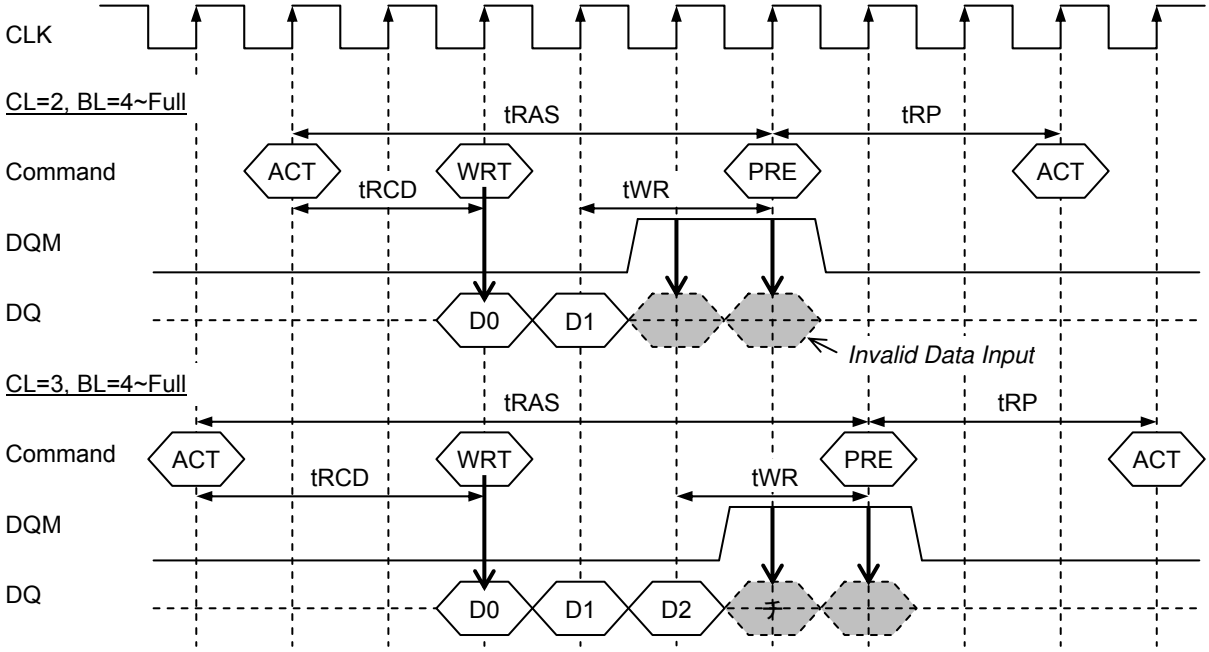
Precharge Break

When a precharge command is issued to the same bank during read cycle or precharge all command is issued, current burst read is terminated and DQ is to Hi-Z after the cycle same as /CAS latency. The objected bank is precharged. When a precharge command is issued to the same bank during write cycle or precharge all command is issued, current burst write is terminated and the objected bank is precharged. The input data after precharge command is ignored.

Read / Precharge Break cycle



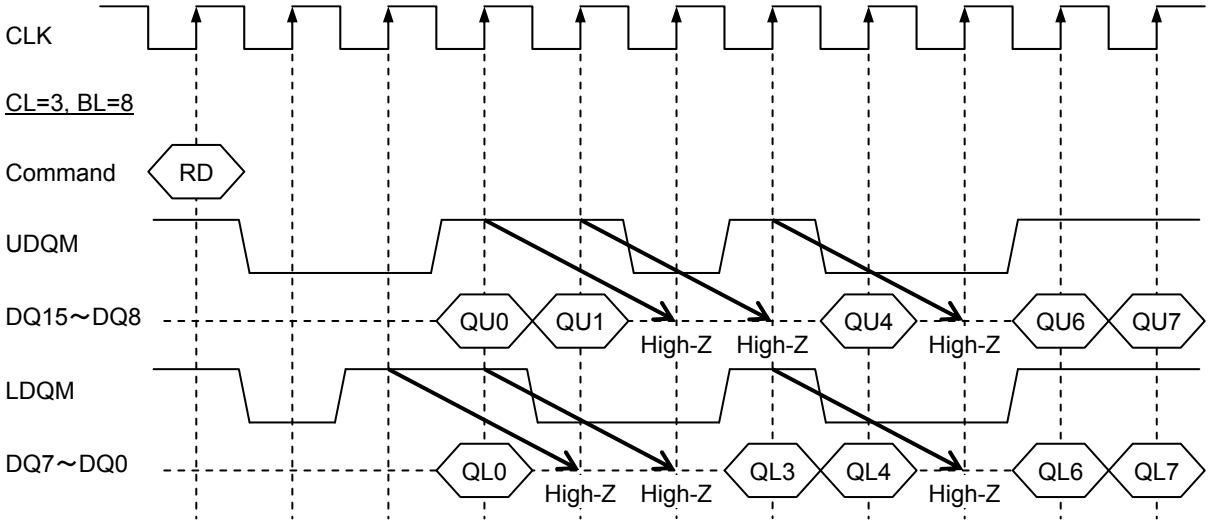
Write / Precharge Break cycle



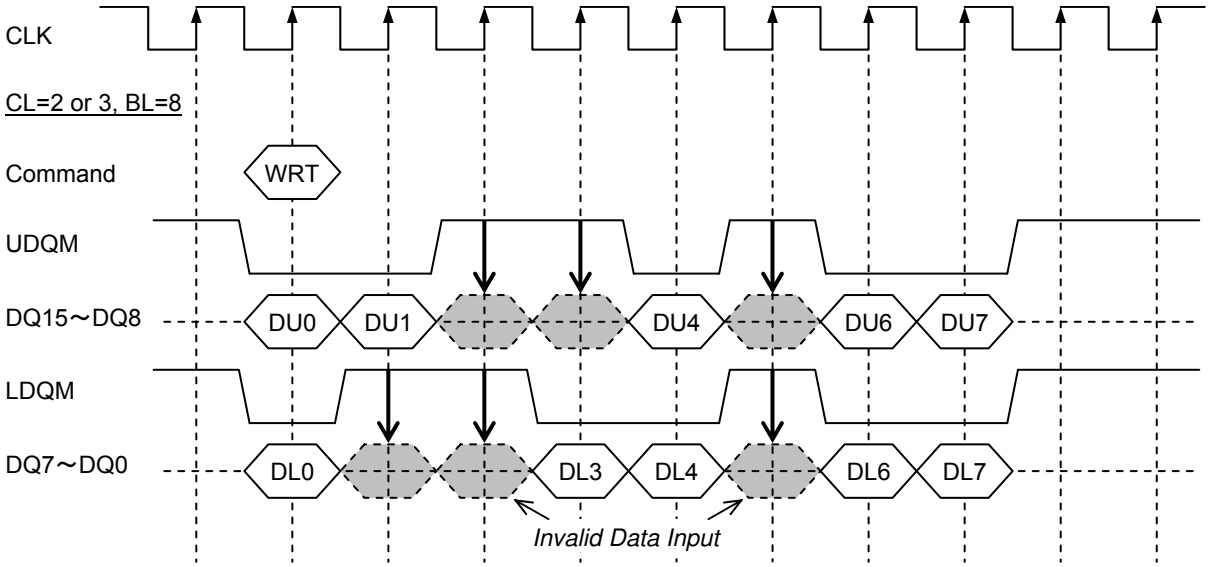
DQM Function

DQM masks input / output data at every byte. UDQM controls DQ15 to DQ8 and LDQM controls DQ7 to DQ0. During read cycle, DQM mask output data after 2 clocks. During write cycle, DQM mask input data at same clock.

Read / DQM Function



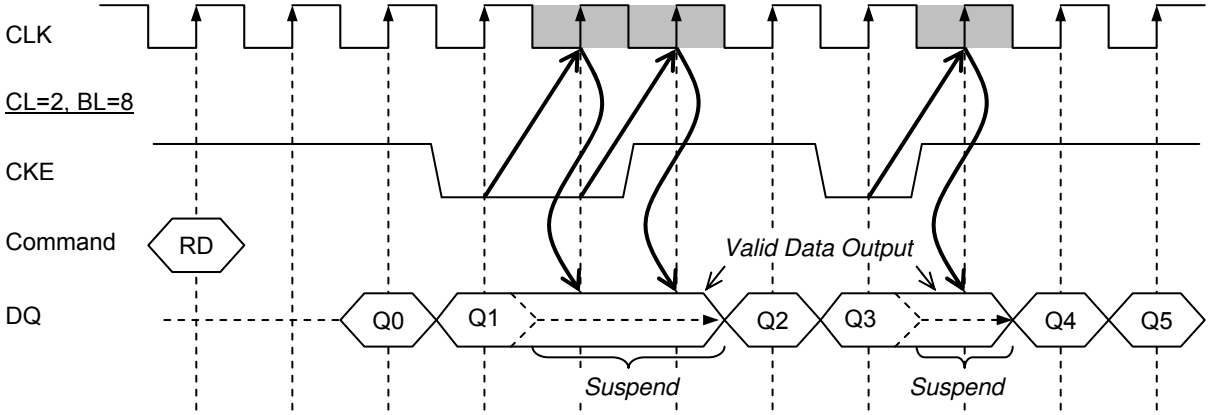
Write / DQM Function



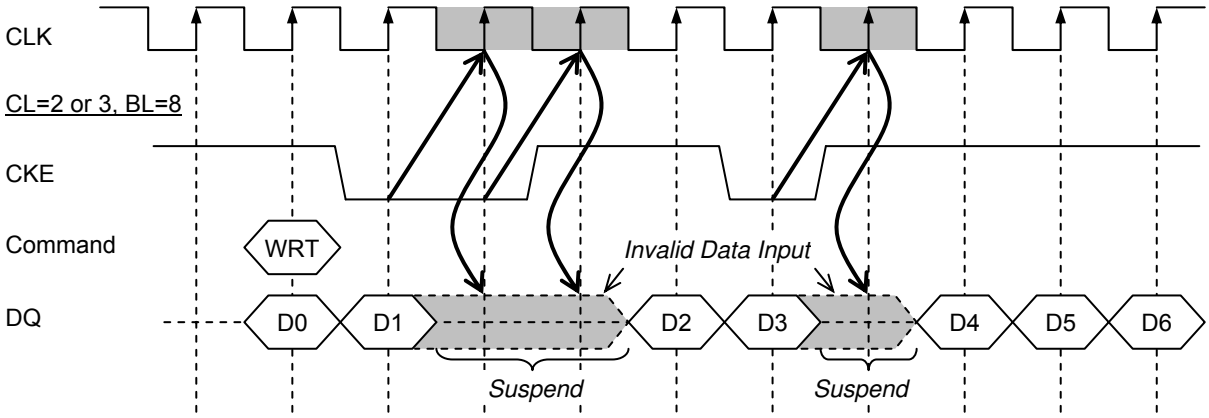
Clock Suspend

The read / write operation can be stopped by CKE temporarily. When CKE is set low, the next clock is ignored. When CKE is set low during read cycle, the burst read is stopped temporarily and the current output data is kept. When CKE is set high, burst read is resumed. When CKE is set low during write cycle, the burst write is stopped temporarily. When CKE is set high, burst write is resumed.

Read / Clock Suspend



Write / Clock Suspend



REFRESH

The data of memory cells are maintained by refresh operation. The refresh operation is to activate all row addresses within a refresh time. The method that row addresses are activated by activate and precharge command is called RAS only refresh cycle. This method needs to input row address with activate command. But, auto-refresh and self refresh don't need to input address. Because, row addresses are generated in SDRAM automatically.

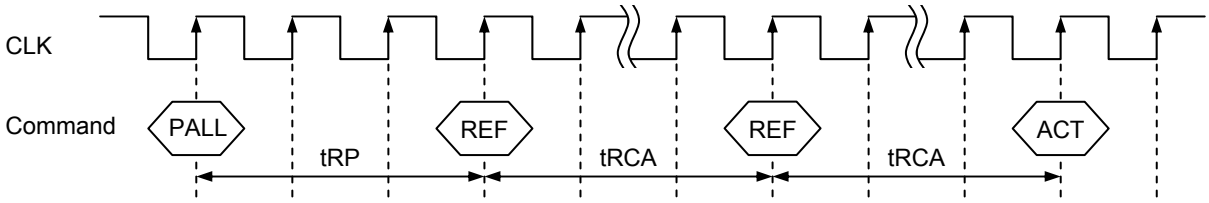
Auto Refresh

All memory area is refreshed by 4,096 times refresh command REF. The refresh command REF can be entered only when all the banks are in an idle state. SDRAM is in idle state after refresh cycle time tRCA.

REF

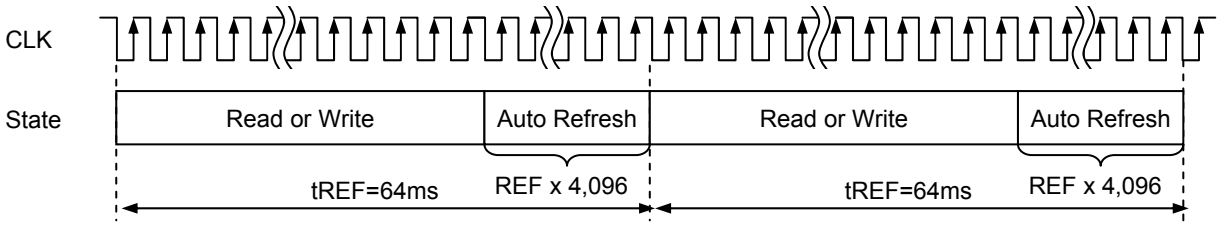
CLK	↑ n-1	↑ n
CKE	H	**H**
/CS	X (Idle)	**L**
/RAS		**L**
/CAS		**L**
/WE		**H**
A13, A12	X	**X**
A11~A0	X	**X**

Auto-Refresh Cycle



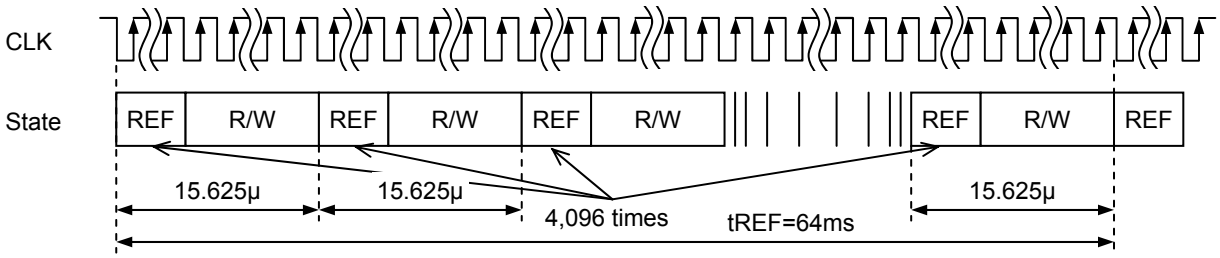
Intensive Refresh

4,096 times refresh command can be entered every refresh time t_{REF}.



Dispersed Refresh

Refresh command can be entered every 15.625µs (tREF 64ms / 4,096 cycles).



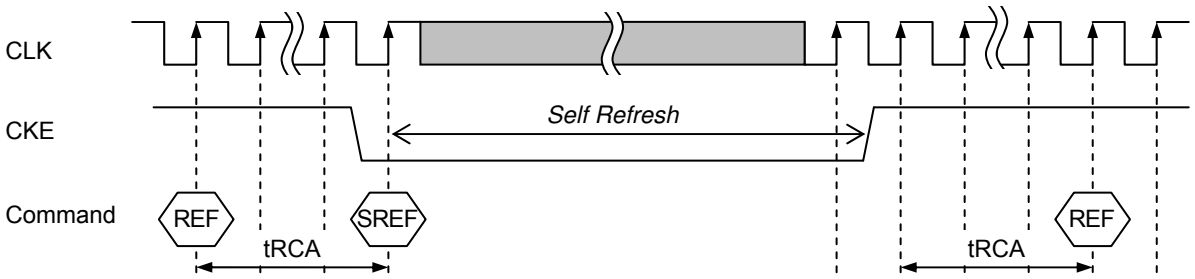
Self Refresh

When read or write is not operated in the long period, self refresh can reduce power consumption for refresh operation. Refresh operation is controlled automatically by refresh timer and row address counter during self refresh mode. All signals except CKE are ignored and data bus DQ is set Hi-Z during self refresh mode.
When CKE is set to high level, self refresh mode is finished. Then, CLK must be operated before 1 clock or more. And, maintain NOP condition within a period of tRCA(Min.) after CKE is set to be high level.

SREF

CLK	n-1	n
CKE	H	**L**
/CS		**L**
/RAS	X	**L**
/CAS	(Idle)	**L**
/WE		**H**
A13, A12	X	**X**
A11~A0	X	**X**

Self Refresh Cycle



Notes : 1. When intensive refresh is used, 4,096 times refresh must be issued before and after the self refresh.