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MEC1322

Keyboard and Embedded Controller for Notebook PC

Product Features

- ARM® Cortex®-M4 Processor Core
  - 32-Bit ARM v7-M Instruction Set Architecture
  - Hardware Floating Point Unit (FPU)
  - Single 4GByte Addressing Space (Von Neumann Model)
  - Little-Endian Byte Ordering
  - Bit-Banding Feature Included
  - NVIC Nested Vectored Interrupt Controller
    - Up to 240 Individually-Vectored Interrupt Sources Supported
    - 8 Levels of Priority, Individually Assignable By Vector
    - Chip-Level Interrupt Aggregator supported, to expand number of interrupt sources or reduce number of vectors
  - System Tick Timer
  - Complete ARM-Standard Debug Support
    - JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
    - Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
    - Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
  - Comprehensive ARM-Standard Trace Support
    - Full DWT Hardware Trace Functionality for Watchpoint and Performance Monitoring
    - Full ITM Hardware Trace Functionality for Instrumented Firmware Support and Profiling
    - Full ETM Hardware Trace Functionality for Instruction Trace
    - Full TPIU Functionality for Trace Output Communication
- 128K SRAM (Code or Data)
  - 96K Optimized for Code
  - 32K Optimized for Data
- LPC Interface
  - Supports LPC Bus frequencies of 19MHz to 33MHz
  - LPC I/O Cycles Decoded
  - LPC Memory Cycles Decoded
  - Clock Run Support
  - Serial IRQ
  - ACPI SCI interface
  - SMI# output
- Two SPI Memory Interfaces
  - 3-pin Full Duplex serial communication interface
  - Two Private and Two Shared Chip Selects
  - DMA Support
- 8042 Style Host Interface
  - Mailbox Registers Interface
    - Forty-three 8-Bit scratch registers
    - Two Register Mailbox Command Interface
    - Two Register SMI Source Interface
- Two ACPI Embedded Controller Interface
  - 1 or 4 Byte Data transfer capable
- ACPI Power Management Interface
  - SCI Event-Generating Functions
- Embedded Memory Interface
  - Host Serial IRQ Source
  - Provides Two Windows to On-Chip SRAM for Host Access
- Two Register Mailbox Command Interface
- Battery Backed (VCC0/VBAT) Resources
  - Power Fail Register
  - Power-Fail Status Register
  - Battery backed 64 byte memory
- Real Time Clock (RTC)
  - VCC0 (VBAT) Powered
  - 32KHz Crystal Oscillator
  - 32KHz Clock output available under VCC1 power
  - Time-of-Day and Calendar Registers
  - Programmable Alarms
  - Supports Leap Year and Daylight Savings Time
- Hibernation Timers
- General Purpose Analog to Digital Converter
  - 10-bit conversion precision
  - 10-bit conversion per channel is completed in less than 12us
  - 5 ADC channels
    - 10-bit Conversion with 2.9mV resolution
    - 0 to 3.3 VDC Conversion Range
  - Optional continuous sampling at a programmable rate
  - Internal Analog Voltage Reference (3.0V +/- 1%)
- Watch Dog Timer
- Four Programmable 16-bit and Two 32-bit Timers
  - Wake-capable Auto-reloading Timers
- Four Independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
- Four Programmable Pulse-Width Modulator Outputs
  - Independent Clock Rates
  - 16-Bit Duty Cycle Granularity
  - Operational in both Full on and Standby modes

- Four EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Controllers are Fully Operational on Standby Power
  - DMA-driven I^2C Network Layer Hardware
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
    - 400 KHz Fast-mode Capable
    - 1 Mbps Fast-mode Plus Capable
  - Hardware Bus Access "Fairness" Interface
  - SMBus Time-outs Interface
  - 5 Ports
  - 2 Port Flexible Multiplexing
- PECI 3.0 Interface
- Keyboard Matrix Scan Interface
  - 18 x 8 Interrupt/Wake Capable Multiplexed Keyboard Scan Matrix
  - Row Predrive Option
- Four Breathing/Blinking LED Interfaces
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
  - Operational in EC Sleep States
- Dual Fan Tachometer Inputs
- RPM-Based Fan Speed Control Algorithm
  - Utilizes one TACH input and one PWM output
  - 3% accurate from 500 RPM to 16k RPM
  - Automatic Tachometer feedback
  - Aging Fan or Invalid Drive Detection
  - Spin Up Routine
  - Ramp Rate Control
  - RPM-based Fan Speed Control Algorithm
- Fast GATEA20 & Fast CPU_RESET
- RSMRST# Functionality Supporting System Deep Sleep
  - Compatible with south bridge SUS-CLK/RSMRST# gating rules
  - Replacement 32K distribution available when RSMRST# is asserted
- Integrated Power-on Reset Generator
  - VCC1_RST# open drain output
  - Accepts External driven Reset
- Anti-Glitch Protection on Power-on
- All Blocks Support Low Power Sleep Modes
- General Purpose Input/Output Pins
  - Low Power
  - High Configurability
- Two pin Debug Port with standard 16C550A register interface
  - Accessible from both Host and EC
- BC-Link Interconnection Bus
  - One High Speed Bus Master Controller
- Package Options
  - 128-pin VTQFP
  - 132-pin DQFN
  - 144-pin WFBGA

Description

The MEC1322 incorporates a high-performance 32-bit ARM® Cortex®-M4 embedded microcontroller with 128 Kilobytes of SRAM and 32 Kilobytes of Boot ROM. It communicates with the system host using the Intel® Low Pin Count (LPC) bus.

The MEC1322 has two SPI memory interfaces that allow the EC to read its code from external SPI flash memory: private SPI and/or shared SPI. The Shared SPI interface allows for EC code to be stored in a shared SPI chip along with the system BIOS. The private SPI memory interface provides for a dedicated SPI flash that is only accessible by the EC.

The MEC1322 provides support for loading EC code from the private or shared SPI flash device on a VCC1 power-on. Before executing the EC code loaded from a SPI Flash Device, the MEC1322 validates the EC code using a digital signature encoded according to PKCS #1. The signature uses RSA-2048 encryption and SHA-256 hashing. This provides automated detection of invalid EC code that may be a result of malicious or accidental corruption. It occurs before each boot of the host processor, thereby ensuring a HW based root of trust not easily thwarted via physical replacement attack.

The MEC1322 is directly powered by two separate suspend supply planes (VBAT and VCC1) and senses the runtime power plane (VCC) to provide “Instant On” and system power management functions. It also contains an integrated VCC1 Reset Interface and a system Power Management Interface that supports low-power states and can drive state changes as a result of hardware wake events.

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Table of Contents

1.0 PIN CONFIGURATION

1.1 Description

The Pin Configuration chapter includes a Pin List, Pin Description, Pin Multiplexing and Package Outline.

1.2 Terminology and Symbols for Pins/Buffers

Term	Definition
Pin Ref. Number	There is a unique reference number for each pin name.
#	The '#' sign at the end of a signal name indicates an active-low signal
n	The lowercase 'n' preceding a signal name indicates an active-low signal
PWR	Power
I	Digital Input
IS	Input with Schmitt Trigger
I_AN	Analog Input
O	Push-Pull Output
OD	Open Drain Output
IO	Bi-directional pin
IOD	Bi-directional pin with Open Drain Output
PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output.
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1-1)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1-1)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1-1)
PCI_IO	Input/Output These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1-1)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 1-2)
PCI_PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1-1).
IO_PECI	PECI Input/Output. These pins are at the PECI V_{REF} level. See Chapter 37.0, "Electrical Specifications".

Note 1-1 See the "PCI Local Bus Specification," Revision 2.1, Section 4.2.2.

Note 1-2 See the "PCI Local Bus Specification," Revision 2.1, Section 4.2.2 and 4.2.3.

1.3 Pin List

The Pin List for the three package options is shown in Table 1-1, Table 1-2 and Table 1-3.

Note: The Pin Ref. Numbers are the same as the pin numbers in the "128 VTQFP Number" column in Table 1-1, "MEC1322 128 VTQFP Pin Configuration".

TABLE 1-1: MEC1322 128 VTQFP PIN CONFIGURATION

128 VTQFP Number	Pin Name	Pin Ref. Number	128 VTQFP Number	Pin Name	128 VTQFP Number	Pin Name
1	GPIO036	44	44	ADC0/GPIO056	87	GPIO165/TXD/SHD_CS1#
2	GPIO153/PVT_SCLK	45	45	AVSS	88	GPIO023/I2C1_DAT0
3	GPIO122/SHD_SCLK	46	46	LAD0/GPIO112	89	GPIO022/I2C1_CLK0
4	GPIO011/KSO16	47	47	VSS	90	GPIO021/I2C2_DAT0
5	KSO13/GPIO006	48	48	LAD1/GPIO114	91	GPIO020/I2C2_CLK0
6	KSO12/GPIO005	49	49	JTAG_RST#	92	GPIO105/TACH1
7	KSO11/GPIO107	50	50	LAD2/GPIO113	93	GPIO145
8	KSO10/GPIO004	51	51	LAD3/GPIO111	94	GPIO164/PVT_MISO
9	KSO09/GPIO106	52	52	LFRAME#/GPIO120	95	GPIO124/SHD_MISO
10	KSO08/GPIO003	53	53	LRESET#/GPIO116	96	GPIO146/PVT_CS0#
11	VSS	54	54	PCI_CLK/GPIO117	97	GPIO150/SHD_CS0#
12	KSO07/GPIO002	55	55	CLKRUN#/GPIO014	98	GPIO157/BC_CLK
13	KSO06/GPIO001	56	56	VSS	99	GPIO160/BC_DAT
14	VCC1	57	57	SER_IRQ/GPIO115	100	GPIO161/BC_INT#
15	CAP	58	58	VCC1	101	GPIO140/TACH2/TACH2PWM_IN
16	KSO05/GPIO104/TFDP_CLK	59	59	GPIO041	102	GPIO045/A20M/PVT_CS1#
17	KSO04/GPIO103/TFDP_DATA/XNOR	60	60	nRESET_OUT/GPIO121	103	GPIO053/PS2_CLK3
18	KSO03/GPIO102/JTAG_TDO	61	61	PS2_CLK1/GPIO050	104	VSS
19	KSO02/GPIO101/JTAG_TDI	62	62	PS2_DAT1/GPIO065	105	GPIO152/PS2_DAT3
20	KSO01/GPIO100/JTAG_TMS	63	63	GPIO035	106	VCC1
21	KSO00/GPIO000/JTAG_TCK	64	64	GPIO027	107	GPIO030
22	KSI7/GPIO043	65	65	GPIO033	108	GPIO012/KSO17
23	KSI6/GPIO042	66	66	PS2_CLK0/GPIO046	109	I2C0_DAT1/GPIO017
24	KSI5/GPIO040	67	67	PS2_DAT0/GPIO047	110	I2C0_CLK1/GPIO134
25	KSI4/GPIO142/TRACECLK	68	68	VBAT	111	I2C0_DAT0/GPIO016
26	KSI3/GPIO032/TRACEDATA0	69	69	XTAL2	112	I2C0_CLK0/GPIO015
27	KSI2/GPIO144/TRACEDATA1	70	70	VSS_VBAT	113	LED0/GPIO154
28	KSI1/GPIO126/TRACEDATA2	71	71	XTAL1	114	LED1/GPIO155
29	KSI0/GPIO125/TRACEDATA3	72	72	VCC_PWRGD/GPIO063	115	LED2/GPIO156
30	GPIO031	73	73	GPIO110	116	GPIO163
31	GPIO127/PECI_RDY	74	74	GPIO130	117	VSS
32	PS2_DAT2/GPIO052	75	75	32KHZ_OUT/GPIO013	118	GPIO136/PWM1
33	GPIO147	76	76	nEC_SCI/GPIO026	119	VCC1
34	GPIO151	77	77	VCC1_RST#/GPIO131	120	GPIO133/PWM0
35	PS2_CLK2/GPIO051	78	78	GPIO141/PWM3/LED3	121	GPIO034/PWM2/TACH2PWM_OUT
36	VSS	79	79	VREF_PECI	122	GPIO135/KBRST
37	VCC1	80	80	GPIO132/PECI_DAT	123	GPIO044/nSMI
38	ADC4/GPIO062	81	81	GPIO007/KSO14	124	GPIO066
39	ADC3/GPIO061	82	82	VSS	125	GPIO025/I2C3_DAT0
40	AVCC	83	83	GPIO010/KSO15	126	GPIO024/I2C3_CLK0
41	GPIO206	84	84	VCC1	127	GPIO054/PVT_MOSI
42	ADC2/GPIO060	85	85	GPIO143/RSMRST#	128	GPIO064/SHD_MOSI
43	ADC1/GPIO057	86	86	GPIO162/RXD		

Note 1: The XTAL2 pin can be used as a single ended clock input. See Note 9 in Section 1.6, "Notes for Tables in this Chapter," on page 39.

2: See Note 10 in Section 1.6, "Notes for Tables in this Chapter," on page 39 for information about the SPI pins.

3: The VCC1_RST#/GPIO131 pin cannot be used as a GPIO pin. The input path to the VCC1_RST# logic is always active and will cause a reset if this pin is set low in GPIO mode.

4: The GPIO041 pin defaults to output low. This pin must be reprogrammed to the GPIO function upon power-up.

Note: Table 1-2, "MEC1322 132 DQFN Pin Configuration" shows the mapping between Pin Ref. Number and 132 DQFN Number for the 132 DQFN package.

TABLE 1-2: MEC1322 132 DQFN PIN CONFIGURATION

Pin Ref. Number	132 DQFN Number	Pin Name
2	B1	GPIO153/PVT_SCLK
3	A1	GPIO122/SHD_SCLK
4	B2	GPIO011/KSO16
5	A2	KSO13/GPIO006
6	B3	KSO12/GPIO005
7	A3	KSO11/GPIO107
8	B4	KSO10/GPIO004
10	A4	KSO08/GPIO003
9	B5	KSO09/GPIO106
11	A5	VSS
12	B6	KSO07/GPIO002
13	A6	KSO06/GPIO001
14	B7	VCC1
15	A7	CAP
129	B8	GPIO067
130	A8	GPIO055
131	B9	GPIO210
16	A9	KSO05/GPIO104/TFDP_CLK
17	B10	KSO04/GPIO103/TFDP_DATA/XNOR
18	A10	KSO03/GPIO102/JTAG_TDO
19	B11	KSO02/GPIO101/JTAG_TDI
20	A11	KSO01/GPIO100/JTAG_TMS
21	B12	KSO00/GPIO000/JTAG_TCK
22	A12	KSI7/GPIO043
24	B13	KSI5/GPIO040
23	A13	KSI6/GPIO042
25	B14	KSI4/GPIO142/TRACECLK
26	A14	KSI3/GPIO032/TRACEDATA0
27	B15	KSI2/GPIO144/TRACEDATA1
28	A15	KSI1/GPIO126/TRACEDATA2
29	B16	KSI0/GPIO125/TRACEDATA3
30	A16	GPIO031
31	B17	GPIO127/PECI_RDY
32	B18	PS2_DAT2/GPIO052
33	A17	GPIO147
34	B19	GPIO151
132	A18	GPIO211
35	B20	PS2_CLK2/GPIO051
37	A19	VCC1
38	B21	ADC4/GPIO062
39	A20	ADC3/GPIO061
40	B22	AVCC
41	A21	GPIO206
42	B23	ADC2/GPIO060
43	A22	ADC1/GPIO057
44	B24	ADC0/GPIO056
45	A23	AVSS
46	B25	LAD0/GPIO112
133	A24	GPIO200
48	B26	LAD1/GPIO114
49	A25	JTAG_RST#
50	B27	LAD2/GPIO113
51	A26	LAD3/GPIO111
52	B28	LFRAME#/GPIO120
53	A27	LRESET#/GPIO116
54	B29	PCI_CLK/GPIO117
55	A28	CLKRUN#/GPIO014
134	B30	GPIO123
57	A29	SER_IRQ/GPIO115
58	B31	VCC1
59	A30	GPIO041
60	B32	nRESET_OUT/GPIO121
61	A31	PS2_CLK1/GPIO050
62	B33	PS2_DAT1/GPIO065
63	A32	GPIO035
64	B34	GPIO027

Pin Ref. Number	132 DQFN Number	Pin Name
65	B35	GPIO033
66	A33	PS2_CLK0/GPIO046
67	B36	PS2_DAT0/GPIO047
68	A34	VBAT
69	B37	XTAL2
70	A35	VSS_VBAT
71	B38	XTAL1
72	A36	VCC_PWRGD/GPIO063
73	B39	GPIO110
74	A37	GPIO130
75	B40	32KHZ_OUT/GPIO013
76	A38	nEC_SCI/GPIO026
77	B41	VCC1_RST#/GPIO131
78	A39	GPIO141/PWM3/LED3
79	B42	VREF_PECI
80	A40	GPIO132/PECI_DAT
81	B43	GPIO007/KSO14
136	A41	GPIO202
83	B44	GPIO010/KSO15
84	A42	VCC1
85	B45	GPIO143/RSMRST#
86	A43	GPIO162/RXD
87	B46	GPIO165/TXD/SHD_CS1#
88	A44	GPIO023/I2C1_DAT0
89	B47	GPIO022/I2C1_CLK0
90	A45	GPIO021/I2C2_DAT0
91	B48	GPIO020/I2C2_CLK0
92	A46	GPIO105/TACH1
93	B49	GPIO145
94	A47	GPIO164/PVT_MISO
95	B50	GPIO124/SHD_MISO
96	A48	GPIO146/PVT_CS0#
137	B51	GPIO201

Pin Ref. Number	132 DQFN Number	Pin Name
97	B52	GPIO150/SHD_CS0#
98	A49	GPIO157/BC_CLK
99	B53	GPIO160/BC_DAT
100	A50	GPIO161/BC_INT#
101	B54	GPIO140/TACH2/TACH2PWM_IN
102	A51	GPIO045/A20M/PVT_CS1#
103	B55	GPIO053/PS2_CLK3
139	A52	GPIO203
105	B56	GPIO152/PS2_DAT3
106	A53	VCC1
107	B57	GPIO030
108	A54	GPIO012/KSO17
109	B58	I2C0_DAT1/GPIO017
110	A55	I2C0_CLK1/GPIO134
111	B59	I2C0_DAT0/GPIO016
112	A56	I2C0_CLK0/GPIO015
113	B60	LED0/GPIO154
114	A57	LED1/GPIO155
115	B61	LED2/GPIO156
116	A58	GPIO163
141	B62	GPIO204
118	A59	GPIO136/PWM1
119	B63	VCC1
120	A60	GPIO133/PWM0
121	B64	GPIO034/PWM2/TACH2PWM_OUT
122	A61	GPIO135/KBRST
123	B65	GPIO044/nSMI
124	A62	GPIO066
125	B66	GPIO025/I2C3_DAT0
126	A63	GPIO024/I2C3_CLK0
127	B67	GPIO054/PVT_MOSI
128	A64	GPIO064/SHD_MOSI
1	B68	GPIO036

Note: Table 1-3, "MEC1322 144 WFBGA Pin Configuration" shows the mapping between Pin Ref. Number and 144 WFBGA ball number.

TABLE 1-3: MEC1322 144 WFBGA PIN CONFIGURATION

Pin Ref. Number	144 WFBGA Number	Pin Name
1	C3	GPIO036
2	F5	GPIO153/PVT_SCLK
3	F6	GPIO122/SHD_SCLK
4	A2	GPIO011/KSO16
5	A1	KSO13/GPIO006
6	B1	KSO12/GPIO005
7	B2	KSO11/GPIO107
8	C2	KSO10/GPIO004
9	C1	KSO09/GPIO106
10	D2	KSO08/GPIO003
11	D1	VSS
12	E2	KSO07/GPIO002
13	E1	KSO06/GPIO001
14	G5	VCC1
15	F1	CAP
16	G2	KSO05/GPIO104/TFDP_CLK
17	H3	KSO04/GPIO103/TFDP_DATA/XNOR
18	H1	KSO03/GPIO102/JTAG_TDO
19	J1	KSO02/GPIO101/JTAG_TDI
20	H2	KSO01/GPIO100/JTAG_TMS
21	J2	KSO00/GPIO000/JTAG_TCK
22	K1	KSI7/GPIO043
23	K3	KSI6/GPIO042
24	K2	KSI5/GPIO040
25	L1	KSI4/GPIO142/TRACECLK
26	L2	KSI3/GPIO032/TRACEDATA0
27	L3	KSI2/GPIO144/TRACEDATA1
28	M2	KSI1/GPIO126/TRACEDATA2
29	M1	KSI0/GPIO125/TRACEDATA3
30	N2	GPIO031
31	N1	GPIO127/PECI_RDY
32	M3	PS2_DAT2/GPIO052
33	N3	GPIO147
34	M4	GPIO151
35	L4	PS2_CLK2/GPIO051
36	E3	VSS
37	H5	VCC1
38	N5	ADC4/GPIO062
39	M5	ADC3/GPIO061
40	L5	AVCC
41	N6	GPIO206
42	M6	ADC2/GPIO060
43	L6	ADC1/GPIO057
44	N7	ADC0/GPIO056
45	M7	AVSS
46	N8	LAD0/GPIO112
47	A5	VSS
48	M8	LAD1/GPIO114
49	J3	JTAG_RST#
50	L8	LAD2/GPIO113
51	L9	LAD3/GPIO111
52	N9	LFRAME#/GPIO120
53	N10	LRESET#/GPIO116
54	M9	PCI_CLK/GPIO117
55	M10	CLKRUN#/GPIO014
56	F3	VSS
57	L10	SER_IRQ/GPIO115
58	J5	VCC1
59	N11	GPIO041
60	N12	nRESET_OUT/GPIO121
61	N13	PS2_CLK1/GPIO050
62	L11	PS2_DAT1/GPIO065
63	M12	GPIO035
64	M13	GPIO027
65	L12	GPIO033
66	K11	PS2_CLK0/GPIO046
67	J12	PS2_DAT0/GPIO047
68	K12	VBAT
69	L13	XTAL2
70	K13	VSS_VBAT
71	J13	XTAL1
72	J11	VCC_PWRGD/GPIO063

Pin Ref. Number	144 WFBGA Number	Pin Name
73	H13	GPIO110
74	H11	GPIO130
75	H12	32KHZ_OUT/GPIO013
76	G13	nEC_SCI/GPIO026
77	H8	VCC1_RST#/GPIO131
78	G8	GPIO141/PWM3/LED3
79	G12	VREF_PECI
80	G9	GPIO132/PECI_DAT
81	G11	GPIO007/KSO14
82	J9	VSS
83	F13	GPIO010/KSO15
84	J6	VCC1
85	F11	GPIO143/RSMRST#
86	D13	GPIO162/RXD
87	F7	GPIO165/TXD/SHD_CS1#
88	E13	GPIO023/I2C1_DAT0
89	E12	GPIO022/I2C1_CLK0
90	E11	GPIO021/I2C2_DAT0
91	D11	GPIO020/I2C2_CLK0
92	D12	GPIO105/TACH1
93	C13	GPIO145
94	F9	GPIO164/PVT_MISO
95	E9	GPIO124/SHD_MISO
96	F8	GPIO146/PVT_CS0#
97	E8	GPIO150/SHD_CS0#
98	B12	GPIO157/BC_CLK
99	B13	GPIO160/BC_DAT
100	A12	GPIO161/BC_INT#
101	A13	GPIO140/TACH2/TACH2PWM_IN
102	E7	GPIO045/A20M/PVT_CS1#
103	C11	GPIO053/PS2_CLK3
104	J8	VSS
105	A11	GPIO152/PS2_DAT3
106	H6	VCC1
107	A10	GPIO030
108	B10	GPIO012/KSO17
109	B9	I2C0_DAT1/GPIO017
110	A9	I2C0_CLK1/GPIO134
111	A8	I2C0_DAT0/GPIO016
112	C8	I2C0_CLK0/GPIO015
113	A7	LED0/GPIO154
114	B8	LED1/GPIO155
115	C7	LED2/GPIO156
116	B7	GPIO163
117	C10	VSS
118	A6	GPIO136/PWM1
119	G6	VCC1
120	B6	GPIO133/PWM0
121	C5	GPIO034/PWM2/TACH2PWM_OUT
122	A4	GPIO135/KBRST
123	B4	GPIO044/nSMI
124	C4	GPIO066
125	B3	GPIO025/I2C3_DAT0
126	A3	GPIO024/I2C3_CLK0
127	E6	GPIO054/PVT_MOSI
128	E5	GPIO064/SHD_MOSI
129	G3	GPIO067
130	F2	GPIO055
131	G1	GPIO210
132	N4	GPIO211
133	L7	GPIO200
134	J7	GPIO123
135	H7	VCC1
136	F12	GPIO202
137	C12	GPIO201
138	H9	VSS
139	B11	GPIO203
140	C9	VSS
141	C6	GPIO204
142	M11	NC
143	D3	VSS
144	B5	VSS

Note: The NC pin in the 144 WFBGA package should be left unconnected on the board.

The pin name to package ball mapping of the 144 pin WFBGA package is shown in FIGURE 1-1:

FIGURE 1-1: MEC1322 PIN NAME TO 144-PIN WFBGA BALL MAPPING (TOP)

	1	2	3	4	5	6	7
A	KSO13/GPIO006	GPIO011/KSO16	GPIO024/I2C3_CLK0	GPIO135/KBRST	VSS	GPIO136/PWM1	LED0/GPIO154
B	KSO12/GPIO005	KSO11/GPIO107	GPIO025/I2C3_DAT0	GPIO044/nSMI	VSS	GPIO133/PWM0	GPIO163
C	KSO09/GPIO106	KSO10/GPIO004	GPIO036	GPIO066	GPIO034/PWM2/TACH2PWM_OUT	GPIO204	LED2/GPIO156
D	VSS	KSO08/GPIO003	VSS	No Ball	No Ball	No Ball	No Ball
E	KSO06/GPIO001	KSO07/GPIO002	VSS	No Ball	GPIO064/SHD_MOSI	GPIO054/PVT_MOSI	GPIO045/A20M/PVT_CS1#
F	CAP	GPIO055	VSS	No Ball	GPIO153/PVT_SCLK	GPIO122/SHD_SCLK	GPIO165/TXD/SHD_CS1#
G	GPIO210	KSO05/GPIO104/TFDP_CLK	GPIO067	No Ball	VCC1	VCC1	No Ball
H	KSO03/GPIO102/JTAG_TDO	KSO01/GPIO100/JTAG_TMS	KSO04/GPIO103/TFDP_DATA/XNOR	No Ball	VCC1	VCC1	VCC1
J	KSO02/GPIO101/JTAG_TDI	KSO00/GPIO000/JTAG_TCK	JTAG_RST#	No Ball	VCC1	VCC1	GPIO123
K	KSI7/GPIO043	KSI5/GPIO040	KSI6/GPIO042	No Ball	No Ball	No Ball	No Ball
L	KSI4/GPIO142/TRACECLK	KSI3/GPIO032/TRACEDATA0	KSI2/GPIO144/TRACEDATA1	PS2_CLK2/GPIO051	AVCC	ADC1/GPIO057	GPIO200
M	KSI0/GPIO125/TRACEDATA3	KSI1/GPIO126/TRACEDATA2	PS2_DAT2/GPIO052	GPIO151	ADC3/GPIO061	ADC2/GPIO060	AVSS
N	GPIO127/PECI_RDY	GPIO031	GPIO147	GPIO211	ADC4/GPIO062	GPIO206	ADC0/GPIO056

8	9	10	11	12	13	
I2C0_DAT0/GPIO016	I2C0_CLK1/GPIO134	GPIO030	GPIO152/PS2_DAT3	GPIO161/BC_INT#	GPIO140/TACH2/TACH2PWM_IN	A
LED1/GPIO155	I2C0_DAT1/GPIO017	GPIO012/KSO17	GPIO203	GPIO157/BC_CLK	GPIO160/BC_DAT	B
I2C0_CLK0/GPIO015	VSS	VSS	GPIO053/PS2_CLK3	GPIO201	GPIO145	C
No Ball	No Ball	No Ball	GPIO020/I2C2_CLK0	GPIO105/TACH1	GPIO162/RXD	D
GPIO150/SHD_CS0#	GPIO124/SHD_MISO	No Ball	GPIO021/I2C2_DAT0	GPIO022/I2C1_CLK0	GPIO023/I2C1_DAT0	E
GPIO146/PVT_CS0#	GPIO164/PVT_MISO	No Ball	GPIO143/RSMRST#	GPIO202	GPIO010/KSO15	F
GPIO141/PWM3/LED3	GPIO132/PECI_DAT	No Ball	GPIO007/KSO14	VREF_PECI	nEC_SCI/GPIO026	G
VCC1_RST#/GPIO131	VSS	No Ball	GPIO130	32KHZ_OUT/GPIO013	GPIO110	H
VSS	VSS	No Ball	VCC_PWRGD/GPIO063	PS2_DAT0/GPIO047	XTAL1	J
No Ball	No Ball	No Ball	PS2_CLK0/GPIO046	VBAT	VSS_VBAT	K
LAD2/GPIO113	LAD3/GPIO111	SER_IRQ/GPIO115	PS2_DAT1/GPIO065	GPIO033	XTAL2	L
LAD1/GPIO114	PCI_CLK/GPIO117	CLKRUN#/GPIO014	NC	GPIO035	GPIO027	M
LAD0/GPIO112	LFRAME#/GPIO120	LRESET#/GPIO116	GPIO041	nRESET_OUT/GPIO121	PS2_CLK1/GPIO050	N

1.3.1 NON 5 VOLT TOLERANT PINS

There are no 5 Volt tolerant pins in the MEC1322.

1.3.2 POR GLITCH PROTECTED PINS

All pins in the MEC1322 have POR output glitch protection. POR output glitch protection ensures that pins will have a steady-state output during VCC1 POR.

In addition, signals in Table 1-4 have additional drive low POR circuitry. Signals in Table 1-4 refer to Pin Reference Numbers as defined in Table 1-1.

These pins are anti-glitch, driven low on VCC1 POR.

TABLE 1-4: GLITCH PROTECTED POR DRIVE LOW PINS

Pin Reference Number	Pin Name
60	nRESET_OUT/GPIO121
77	VCC1_RST#/GPIO131
85	GPIO143/RSMRST#
125	GPIO025/I2C3_DAT0

Note: The GPIO025/I2C3_DAT0 pin is driven low, glitch free, while VCC1 is coming up. However, after VCC1 is up and stable, the pin becomes an input (i.e., tri-stated Open Drain type), as shown in Table 1-37, “Multiplexing Table (16 of 18),” on page 36.

The following signals require a pull-down on the board:

- nRESET_OUT/GPIO121
- GPIO143/RSMRST#

Note: These glitch protected pins have no backdrive protection. See Section 1.3.3, "Non Backdrive Protected Pins".

1.3.3 NON BACKDRIVE PROTECTED PINS

Table 1-5 lists pins which do not have backdrive protection. Signals in Table 1-5 refer to Pin Reference Numbers as defined in Table 1-1.

These pins have no backdrive protection. If VCC1 is off must insure that none of these pins is above 0V to prevent backdrive onto the VCC1 supply.

TABLE 1-5: NON BACKDRIVE PROTECTED PINS

Pin Reference Number	Pin Name
38	ADC4/GPIO062
39	ADC3/GPIO061
42	ADC2/GPIO060
43	ADC1/GPIO057
44	ADC0/GPIO056
46	LAD0/GPIO112
48	LAD1/GPIO114
50	LAD2/GPIO113
51	LAD3/GPIO111
52	LFRAME#/GPIO120
53	LRESET#/GPIO116
54	PCI_CLK/GPIO117
55	CLKRUN#/GPIO014
57	SER_IRQ/GPIO115
60	nRESET_OUT/GPIO121
69	XTAL2
71	XTAL1
77	VCC1_RST#/GPIO131
79	VREF_PECI
80	GPIO132/PECI_DAT
85	GPIO143/RSMRST#
125	GPIO025/I2C3_DAT0

1.4 Pin Description

1.4.1 OVERVIEW

The following tables describe the signal functions in the MEC1322 pin configuration. See Section 1.6, "Notes for Tables in this Chapter," on page 39 for notes that are referenced in the Pin Description tables.

1.4.2 HOST INTERFACE

TABLE 1-6: HOST INTERFACE

HOST INTERFACE			(11 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
57	SER_IRQ	Serial IRQ	Note 1
53	LRESET#	LPC Reset. LRESET# is the same as the system PCI reset, PCIRST#	
54	PCI_CLK	PCI Clock	
52	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	
46	LAD0	LPC Multiplexed command, address and data bus Bit 0.	Note 1
48	LAD1	LPC Multiplexed command, address and data bus Bit 1.	Note 1
50	LAD2	LPC Multiplexed command, address and data bus Bit 2.	Note 1
51	LAD3	LPC Multiplexed command, address and data bus Bit 3.	Note 1
55	CLKRUN#	PCI Clock Control	
76	nEC_SCI	Power Management Event	
123	nSMI	SMI Output	

1.4.3 BC-LINK INTERFACE

TABLE 1-7: BC-LINK INTERFACE

BC-Link Interface			(3 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
98	BC_CLK	BC-Link Master clock	
99	BC_DAT	BC-Link Master data I/O	Note 7
100	BC_INT#	BC-Link Master interrupt	

1.4.4 JTAG INTERFACE

TABLE 1-8: JTAG INTERFACE

JTAG Interface			(5 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
21	JTAG_TCK	JTAG Test Clock	
19	JTAG_TDI	JTAG Test Data In	
18	JTAG_TDO	JTAG Test Data Out	
20	JTAG_TMS	JTAG Test Mode Select	
49	JTAG_RST#	JTAG Test Reset (active low)	Note 2

Note: JTAG_TDO is a push-pull output. This function is not configured through the associated GPIO Pin Control Register; however the drive strength is configured through the associated GPIO Pin Control Register 2.

1.4.5 MASTER CLOCK INTERFACE

TABLE 1-9: MASTER CLOCK INTERFACE

Master Clock Interface			(3 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
71	XTAL1	32.768 KHz Crystal Output	Note 9
69	XTAL2	32.768 KHz Crystal Input (single-ended 32.768 KHz clock input)	Note 9
75	32KHZ_OUT	32.768 KHz Digital Output	

1.4.6 ANALOG DATA ACQUISITION INTERFACE

TABLE 1-10: ANALOG DATA ACQUISITION

Analog Data Acquisition Interface			(5 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
44	ADC0	ADC channel 0	Note 8
43	ADC1	ADC channel 1	Note 8
42	ADC2	ADC channel 2	Note 8
39	ADC3	ADC channel 3	Note 8
38	ADC4	ADC channel 4	Note 8

1.4.7 FAN TACHOMETER AND PWM INTERFACE

TABLE 1-11: FAN TACHOMETER AND PWM INTERFACE

PWM & TACHOMETER			(6 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
92	TACH1	Fan Tachometer Input 2	
101	TACH2PWM_IN	Tach input to RPM-Based Fan Speed Control Algorithm	
120	PWM0	Pulse Width Modulator Output 0	
118	PWM1	Pulse Width Modulator Output 1	
78	PWM3	Pulse Width Modulator Output 3	
121	TACH2PWM_OUT	Pulse Width Modulator Output from RPM Based Fan Speed Control Algorithm	

1.4.8 GENERAL PURPOSE I/O INTERFACE

TABLE 1-12: GPIO INTERFACE

GPIO Interface			
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
See Pin Configuration Table	GPIO	General Purpose Input Output Pins	Note 12

Note: No GPIO pin should be left floating in a system. If a GPIO pin is not in use, it should be either tied high, tied low, or pulled to either power or ground through a resistor.

1.4.9 MISCELLANEOUS FUNCTIONS

TABLE 1-13: MISCELLANEOUS FUNCTIONS

MISC Functions			(13 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
102	A20M	KBD GATEA20 Output	
122	KBRST	CPU_RESET	
113	LED0	LED (Bllinking/Breathing PWM) Output 0	
114	LED1	LED (Bllinking/Breathing PWM) Output 1	
115	LED2	LED (Bllinking/Breathing PWM) Output 2	
78	LED3	LED (Bllinking/Breathing PWM) Output 3	
16	TFDP_CLK	Trace FIFO debug port - clock	
17	TFDP_DATA	Trace FIFO debug port - data	
60	nRESET_OUT	EC-driven External System Reset	Note 6
72	VCC_PWRGD	System Main Power Indication	
77	VCC1_RST#	Reset Generator Output	
85	RSMRST#	Resume Reset Output	Note 6
17	XNOR	Test Output	

Note 1: The KBRST pin function is the output of CPU_RESET described in Section 11.11.2, "CPU_RESET Hardware Speed-Up," on page 151.

2: The nRESET_OUT pin function is an external output signal version of the internal signal nSIO_RESET. See the iRESET_OUT bit in the Power Reset Control (PWR_RST_CTRL) Register on page 71 and nSIO_RESET in Table 3-7, “Definition of Reset Signals,” on page 52.

3: XNOR is a push-pull output. This function is not configured through the associated GPIO Pin Control Register; however the drive strength is configured through the associated GPIO Pin Control Register 2.

1.4.10 PS/2 INTERFACE

TABLE 1-14: PS/2 INTERFACE

PS/2 Interface			(8 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
35	PS2_CLK2	PS/2 clock 2	
32	PS2_DAT2	PS/2 data 2	
61	PS2_CLK1	PS/2 clock 1	
62	PS2_DAT1	PS/2 data 1	
66	PS2_CLK0	PS/2 clock 0	
67	PS2_DAT0	PS/2 data 0	
103	PS2_CLK3	PS/2 clock 3	
105	PS2_DAT3	PS/2 data 3	

1.4.11 POWER INTERFACE

TABLE 1-15: POWER INTERFACE

Power Interface			(18 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
70	VSS_VBAT	VBAT associated ground	
68	VBAT	VBAT supply	
15	CAP	Internal Voltage Regulator Capacitor	Note 3
11, 36, 47, 56, 82, 104, 117	VSS	VCC1 associated ground	
14, 37, 58, 84, 106, 119	VCC1	VCC1 supply	
45	AVSS	Analog ADC supply associated ground	
40	AVCC	Analog ADC VCC1 associated Supply	

APPLICATION NOTE: See FIGURE 3-1: Recommended Battery Circuit on page 49.

1.4.12 SMBUS INTERFACE

TABLE 1-16: SMBUS INTERFACE

SMBus Interface			(10 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
112	I2C0_CLK0	SMBus Controller 0 Port 0 Clock	
111	I2C0_DAT0	SMBus Controller 0 Port 0 Data	
110	I2C0_CLK1	SMBus Controller 0 Port 1 Clock	
109	I2C0_DAT1	SMBus Controller 0 Port 1 Data	
89	I2C1_CLK0	SMBus Controller 1 Clock	
88	I2C1_DAT0	SMBus Controller 1 Data	
91	I2C2_CLK0	SMBus Controller 2 Clock	
90	I2C2_DAT0	SMBus Controller 2 Data	
126	I2C3_CLK0	SMBus Controller 3 Clock	
125	I2C3_DAT0	SMBus Controller 3 Data	

1.4.13 PECI INTERFACE

TABLE 1-17: PECI INTERFACE

PECI Interface			(3 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
80	PECI_DAT	PECI Bus	
31	PECI_RDY	PECI Ready	
79	VREF_PECI	PECI Voltage Reference	

1.4.14 KEYBOARD SCAN INTERFACE

TABLE 1-18: KEYBOARD SCAN INTERFACE

Keyboard Scan Interface			(26 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
29	KSI0	Keyboard Scan Matrix Input 0	Note 11
28	KSI1	Keyboard Scan Matrix Input 1	Note 11
27	KSI2	Keyboard Scan Matrix Input 2	Note 11
26	KSI3	Keyboard Scan Matrix Input 3	Note 11
25	KSI4	Keyboard Scan Matrix Input 4	Note 11
24	KSI5	Keyboard Scan Matrix Input 5	Note 11
23	KSI6	Keyboard Scan Matrix Input 6	Note 11
22	KSI7	Keyboard Scan Matrix Input 7	Note 11
21	KSO00	Keyboard Scan Matrix Output 0	
20	KSO01	Keyboard Scan Matrix Output 1	
19	KSO02	Keyboard Scan Matrix Output 2	
18	KSO03	Keyboard Scan Matrix Output 3	
17	KSO04	Keyboard Scan Matrix Output 4	
16	KSO05	Keyboard Scan Matrix Output 5	
13	KSO06	Keyboard Scan Matrix Output 6	
12	KSO07	Keyboard Scan Matrix Output 7	
10	KSO08	Keyboard Scan Matrix Output 8	
9	KSO09	Keyboard Scan Matrix Output 9	
8	KSO10	Keyboard Scan Matrix Output 10	
7	KSO11	Keyboard Scan Matrix Output 11	
6	KSO12	Keyboard Scan Matrix Output 12	
5	KSO13	Keyboard Scan Matrix Output 13	
81	KSO14	Keyboard Scan Matrix Output 14	
83	KSO15	Keyboard Scan Matrix Output 15	
4	KSO16	Keyboard Scan Matrix Output 16	
108	KSO17	Keyboard Scan Matrix Output 17	

1.4.15 SPI CONTROLLER INTERFACE

TABLE 1-19: SPI CONTROLLER INTERFACE

SPI Controllers Interface			(10 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
3	SHD_SCLK	Shared SPI Clock	Note 10
128	SHD_MOSI	Shared SPI Output	Note 10
95	SHD_MISO	Shared SPI Input	Note 10
97	SHD_CS0#	Shared SPI Chip Select 0	Note 10
87	SHD_CS1#	Shared SPI Chip Select 1	
2	PVT_SCLK	Private SPI Clock	Note 10
127	PVT_MOSI	Private SPI Output	Note 10
94	PVT_MISO	Private SPI Input	Note 10
96	PVT_CS0#	Private SPI Chip Select 0	Note 10
102	PVT_CS1#	Private SPI Chip Select 1	

1.4.16 TRACE DEBUG INTERFACE

TABLE 1-20: TRACE DEBUG INTERFACE

Trace Debug Interface			(5 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
25	TRACECLK	Trace Clock	
26	TRACEDATA0	Trace Data 0	
27	TRACEDATA1	Trace Data 1	
28	TRACEDATA2	Trace Data 2	
29	TRACEDATA3	Trace Data 3	

The Trace Debug Interface is enabled using the TRACE_EN bit in the ETM TRACE Enable register defined in Chapter 35.0, "EC Subsystem Registers".

Note: These pins are push-pull outputs when enabled as the Trace Debug Interface pin functions. This functionality is not configured through the associated GPIO Pin Control Register; however the drive strength of these pins is configured through the associated GPIO Pin Control Register 2.

1.4.17 UART PORT

TABLE 1-21: UART PORT

UART Port			(2 Pins)
Pin Ref. Number	**Signal Name**	**Description**	**Notes**
86	RXD	UART Receive Data	
87	TXD	UART Transmit Data	

1.5 Pin Multiplexing

Multifunction Pin Multiplexing in the MEC1322 is controlled by the GPIO Interface and illustrated in the Multiplexing Tables that follow. See Section 1.6, "Notes for Tables in this Chapter," on page 39 for notes that are referenced in the Pin Multiplexing tables. See Section 20.8.1, "Pin Control Register," on page 250 for Pin Multiplexing programming details. See also Section 20.7, "Pin Multiplexing Control," on page 248.

Pin signal functions that exhibit power domain emulation (see Multiplexing Tables below) have a different power supply designation in the “Emulated Power Well” column and “Signal Power Well“ columns of the Multiplexing Tables in Section 1.5.2.

1.5.1 VCC2 POWER DOMAIN EMULATION

The System Runtime Supply power VCC2 is not connected to the MEC1322. The VCC_PWRGD signal is used to indicate when power is applied to the System Runtime Supply.

Pin signal functions with VCC2 power domain emulation are documented in the Multiplexing Tables as “Signal Power Well“= VCC1 and “Emulated Power Well” = VCC2. These pins are powered by VCC1 and controlled by the VCC_PWRGD signal input. Outputs on VCC2 power domain emulation pin signal functions are tri-stated when VCC_PWRGD is not asserted and are functional when VCC_PWRGD is active. Inputs on VCC2 power domain emulation pin signal functions are gated according as defined by the Gated State column in the following tables.

Power well emulation for GPIOs and for signals that are multiplexed with GPIO signals is controlled by the Power Gating Signals field in the GPIO Pin Control Register.

1.5.2 MULTIPLEXING TABLES

In the following tables, the columns have the following meanings:

MUX

If the pin has an associated GPIO, then the MUX column refers to the Mux Control field in the GPIO Pin Control Register. Setting the Mux Control field to value listed in the row will configure the pin for the signal listed in the Signal column on the same row. The row marked “Default” is the setting that is assigned on system reset.

If there is no GPIO associated with a pin, then the pin has a single function.

Signal

This column lists the signals that can appear on each pin, as configured by the MUX control.

Buffer Type

Pin buffer types are defined in Table 37-4, “DC Electrical Characteristics,” on page 391.

Note that all GPIO pins are of buffer type PIO, which may be configured as input/output, push-pull/OD etc. via the GPIO Pin Control Register and Pin Control Register 2. There are some pins where the buffer type is configured by the alternate function selection, in which case that buffer type is shown in this column.

Default Operation

This column gives the pin behavior following the power-up of VCC1. All GPIO pins are programmable after this event. This default pin behavior corresponds to the row marked “Default” in the MUX column.

Note:	An internal pull-up resistor is indicated by (PU) and and internal pull-down is indicated by (PD). These are configured via the GPIO Pin Control Register.

Signal Power Well

This column defines the power well that powers the pin.

Emulated Power Well

Power well emulation for GPIOs and for signals that are multiplexed with GPIO signals is controlled by the Power Gating Signals field in the GPIO Pin Control Register.

Power well emulation for signals that are not multiplexed with GPIO signals is defined by the entries in this column.

See Section 1.5.1, "VCC2 Power Domain Emulation".

Note:	The Glitch Protected POR Drive Low Pins are configured as “always on”, as indicated by “ON” in this column.

Gated State

This column defines the internal value of an input signal when either its emulated power well is inactive or it is not selected by the GPIO alternate function MUX. A value of “No Gate” means that the internal signal always follows the pin even when the emulated power well is inactive.

Note:	Gated state is only meaningful to the operation of input signals. A gated state on an output pin defines the internal behavior of the GPIO MUX and does not imply pin behavior.

TABLE 1-22: MULTIPLEXING TABLE (1 OF 18)

Pin Ref. Number	MUX	Signal	Buffer Type	Default Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
1	Default: 0	GPIO036	PIO	I (PU)	VCC1	VCC1	No Gate	
1	1	Reserved	Reserved		Reserved	Reserved		
1	2	Reserved	Reserved		Reserved	Reserved		
1	3	Reserved	Reserved		Reserved	Reserved		
2	Default: 0	GPIO153	PIO	I	VCC1	VCC1	No Gate	Note 10
2	1	PVT_SCLK	PIO		VCC1	VCC1		Note 10
2	2	Reserved	Reserved		Reserved	Reserved		
2	3	Reserved	Reserved		Reserved	Reserved		
3	Default: 0	GPIO122	PIO	I (PD)	VCC1	VCC1	No Gate	Note 10
3	1	SHD_SCLK	PIO		VCC1	VCC1		Note 10
3	2	Reserved	Reserved		Reserved	Reserved		
3	3	Reserved	Reserved		Reserved	Reserved		
4	Default: 0	GPIO011	PIO	IOD (PD)	VCC1	VCC1	No Gate	
4	1	Reserved	Reserved		Reserved	Reserved		
4	2	Reserved	Reserved		Reserved	Reserved		
4	3	KSO16	PIO		VCC1	VCC1		
5	0	GPIO006	PIO		VCC1	VCC1	No Gate	
5	1	Reserved	Reserved		Reserved	Reserved		
5	2	Reserved	Reserved		Reserved	Reserved		
5	Default: 3	KSO13	PIO	O-4mA	VCC1	VCC1		
6	0	GPIO005	PIO		VCC1	VCC1	No Gate	
6	1	Reserved	Reserved		Reserved	Reserved		
6	2	Reserved	Reserved		Reserved	Reserved		
6	Default: 3	KSO12	PIO	O-4mA (PD)	VCC1	VCC1		
7	0	GPIO107	PIO		VCC1	VCC1	No Gate	
7	1	Reserved	Reserved		Reserved	Reserved		
7	2	Reserved	Reserved		Reserved	Reserved		
7	Default: 3	KSO11	PIO	O-4mA	VCC1	VCC1		
8	0	GPIO004	PIO		VCC1	VCC1	No Gate	
8	1	Reserved	Reserved		Reserved	Reserved		
8	2	Reserved	Reserved		Reserved	Reserved		
8	Default: 3	KSO10	PIO	O-4mA	VCC1	VCC1		

TABLE 1-23: MULTIPLEXING TABLE (2 OF 18)

Pin Ref. Number	MUX	Signal	Buffer Type	Default Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
9	0	GPIO106	PIO		VCC1	VCC1	No Gate	
9	1	Reserved	Reserved		Reserved	Reserved		
9	2	Reserved	Reserved		Reserved	Reserved		
9	Default: 3	KSO09	PIO	O-4mA	VCC1	VCC1		
10	0	GPIO003	PIO		VCC1	VCC1	No Gate	
10	1	Reserved	Reserved		Reserved	Reserved		
10	2	Reserved	Reserved		Reserved	Reserved		
10	Default: 3	KSO08	PIO	O-4mA	VCC1	VCC1		
11		VSS	PWR		PWR	PWR		
11								
11								
11								
12	0	GPIO002	PIO		VCC1	VCC1	No Gate	
12	1	Reserved	Reserved		Reserved	Reserved		
12	2	Reserved	Reserved		Reserved	Reserved		
12	Default: 3	KSO07	PIO	O-4mA	VCC1	VCC1		
13	0	GPIO001	PIO		VCC1	VCC1	No Gate	
13	1	Reserved	Reserved		Reserved	Reserved		
13	2	Reserved	Reserved		Reserved	Reserved		
13	Default: 3	KSO06	PIO	O-4mA	VCC1	VCC1		
14		VCC1	PWR		PWR	PWR		
14								
14								
14								
15		CAP	PWR		PWR	PWR		Note 3
15								
15								
15								
16	0	GPIO104	PIO		VCC1	VCC1	No Gate	
16	1	TFDP_CLK	PIO		VCC1	VCC1		
16	2	Reserved	Reserved		Reserved	Reserved		
16	Default: 3	KSO05	PIO	O-4mA	VCC1	VCC1		

TABLE 1-24: MULTIPLEXING TABLE (3 OF 18)

Pin Ref. Number	MUX	Signal	Buffer Type	Default Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
17	0	GPIO103	PIO		VCC1	VCC1	No Gate	
17	1	TFDP_DATA	PIO		VCC1	VCC1		
17	2	Reserved	Reserved		Reserved	Reserved		
17	Default: 3	KSO04	PIO	O-4mA	VCC1	VCC1		
18	0	GPIO102	PIO		VCC1	VCC1	No Gate	
18	1	Reserved	Reserved		Reserved	Reserved		
18	2	Reserved	Reserved		Reserved	Reserved		
18	Default: 3	KSO03	PIO	O-4mA	VCC1	VCC1		
19	0	GPIO101	PIO		VCC1	VCC1	No Gate	
19	1	Reserved	Reserved		Reserved	Reserved		
19	2	Reserved	Reserved		Reserved	Reserved		
19	Default: 3	KSO02	PIO	O-4mA	VCC1	VCC1		
20	0	GPIO100	PIO		VCC1	VCC1	No Gate	
20	1	Reserved	Reserved		Reserved	Reserved		
20	2	Reserved	Reserved		Reserved	Reserved		
20	Default: 3	KSO01	PIO	O-4mA	VCC1	VCC1		
21	0	GPIO000	PIO		VCC1	VCC1	No Gate	
21	1	Reserved	Reserved		Reserved	Reserved		
21	2	Reserved	Reserved		Reserved	Reserved		
21	Default: 3	KSO00	PIO	O-4mA	VCC1	VCC1		
22	0	GPIO043	PIO		VCC1	VCC1	No Gate	
22	1	Reserved	Reserved		Reserved	Reserved		
22	2	Reserved	Reserved		Reserved	Reserved		
22	Default: 3	KSI7	PIO	I	VCC1	VCC1	Low	Note 11
23	0	GPIO042	PIO		VCC1	VCC1	No Gate	
23	1	Reserved	Reserved		Reserved	Reserved		
23	2	Reserved	Reserved		Reserved	Reserved		
23	Default: 3	KSI6	PIO	I	VCC1	VCC1	Low	Note 11
24	0	GPIO040	PIO		VCC1	VCC1	No Gate	
24	1	Reserved	Reserved		Reserved	Reserved		
24	2	Reserved	Reserved		Reserved	Reserved		
24	Default: 3	KSI5	PIO	I	VCC1	VCC1	Low	Note 11

TABLE 1-25: MULTIPLEXING TABLE (4 OF 18)

Pin Ref. Number	MUX	Signal	Buffer Type	Default Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
25	0	GPIO142	PIO		VCC1	VCC1	No Gate	
25	1	Reserved	Reserved		Reserved	Reserved		
25	2	Reserved	Reserved		Reserved	Reserved		
25	Default: 3	KSI4	PIO	I	VCC1	VCC1	Low	Note 11
26	0	GPIO032	PIO		VCC1	VCC1	No Gate	
26	1	Reserved	Reserved		Reserved	Reserved		
26	2	Reserved	Reserved		Reserved	Reserved		
26	Default: 3	KSI3	PIO	I	VCC1	VCC1	Low	Note 11
27	0	GPIO144	PIO		VCC1	VCC1	No Gate	
27	1	Reserved	Reserved		Reserved	Reserved		
27	2	Reserved	Reserved		Reserved	Reserved		
27	Default: 3	KSI2	PIO	I	VCC1	VCC1	Low	Note 11
28	0	GPIO126	PIO		VCC1	VCC1	No Gate	
28	1	Reserved	Reserved		Reserved	Reserved		
28	Default: 2	KSI1	PIO	I	VCC1	VCC1	Low	Note 11
28	3	Reserved	Reserved		Reserved	Reserved		
29	0	GPIO125	PIO		VCC1	VCC1	No Gate	
29	1	Reserved	Reserved		Reserved	Reserved		
29	Default: 2	KSI0	PIO	I	VCC1	VCC1	Low	Note 11
29	3	Reserved	Reserved		Reserved	Reserved		
30	Default: 0	GPIO031	PIO	I (PU)	VCC1	VCC1	No Gate	
30	1	Reserved	Reserved		Reserved	Reserved		
30	2	Reserved	Reserved		Reserved	Reserved		
30	3	Reserved	Reserved		Reserved	Reserved		
31	Default: 0	GPIO127	PIO	I	VCC1	VCC1	No Gate	
31	1	PECI_RDY	PIO		VCC1	VCC1	High	
31	2	Reserved	Reserved		Reserved	Reserved		
31	3	Reserved	Reserved		Reserved	Reserved		
32	0	GPIO052	PIO		VCC1	VCC1	No Gate	
32	1	Reserved	Reserved		Reserved	Reserved		
32	Default: 2	PS2_DAT2	PIO	IOD-12mA	VCC1	VCC1	Low	
32	3	Reserved	Reserved		Reserved	Reserved		

TABLE 1-26: MULTIPLEXING TABLE (5 OF 18)

Pin Ref. Number	MUX	Signal	Buffer Type	Default Operation	Signal Power Well	Emulated Power Well	Gated State	Notes
33	Default: 0	GPIO147	PIO	I (PU)	VCC1	VCC1	No Gate	
33	1	Reserved	Reserved		Reserved	Reserved		
33	2	Reserved	Reserved		Reserved	Reserved		
33	3	Reserved	Reserved		Reserved	Reserved		
34	Default: 0	GPIO151	PIO	I (PU)	VCC1	VCC1	No Gate	
34	1	Reserved	Reserved		Reserved	Reserved		
34	2	Reserved	Reserved		Reserved	Reserved		
34	3	Reserved	Reserved		Reserved	Reserved		
35	0	GPIO051	PIO		VCC1	VCC1	No Gate	
35	1	Reserved	Reserved		Reserved	Reserved		
35	Default: 2	PS2_CLK2	PIO	IOD-12mA	VCC1	VCC1	Low	
35	3	Reserved	Reserved		Reserved	Reserved		
36		VSS	PWR		PWR	PWR		
36								
36								
36								
37		VCC1	PWR		PWR	PWR		
37								
37								
37								
38	0	GPIO062	PIO		VCC1	VCC1	No Gate	
38	Default: 1	ADC4	I_AN	I_AN	AVCC1_ADC	AVCC1_ADC	Low	Note 8
38	2	Reserved	Reserved		Reserved	Reserved		
38	3	Reserved	Reserved		Reserved	Reserved		
39	0	GPIO061	PIO		VCC1	VCC1	No Gate	
39	Default: 1	ADC3	I_AN	I_AN	AVCC1_ADC	AVCC1_ADC	Low	Note 8
39	2	Reserved	Reserved		Reserved	Reserved		
39	3	Reserved	Reserved		Reserved	Reserved		
40		AVCC	PWR		PWR	PWR		
40								
40								
40								