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MEC140x/1x

Keyboard and Embedded Controller Products for Notebook PC

Common Features

- 3.3V Operation
- ACPI 3.0 Compliant
- PC2001 compliant
- VTR (standby) and VBAT Power Planes
  - Low Standby Current in Sleep Mode
- Connected Standby Support
- 32kHz Clock Source
  - Internal 32kHz Oscillator
  - External 32kHz Clock Source
    - 32kHz Crystal (XTAL) Supported
    - Single-Ended 32kHz Clock Source
- LPC Host Interface
  - LPC Specification 1.1 Compatible
  - LPC I/O and Memory Cycles Decoded
  - Supports optional signals: CLKRUN#, LPCPD#, SERIRQ, SMI#, EC_SCI# (ACPI PME Event)
  - Supports 19.2 MHz to 33 MHz nominal bus clock speeds
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - EC-Programmable Base Address
- 8042 Emulated Keyboard Controller
  - 8042 Style Host Interface
  - Port 92 Legacy A20M Support
  - Fast GATEA20 & Fast CPU_RESET
- System to EC Message Interface
  - One Embedded Memory Interface
    - Host Serial or Parallel IRQ Source
    - Provides Two Windows to On-Chip SRAM for Host Access
    - Two Register Mailbox Command Interface
  - Mailbox Registers Interface
    - Thirty-two 8-Bit Scratch Registers
    - Two Register Mailbox Command Interface
    - Two Register SMI Source Interface
  - Five ACPI Embedded Controller Interfaces
    - Four EC Interfaces
    - One Power Management Interface
- MIPS32® M14K™ Microcontroller Core
  - microMIPS-Compatible Instruction Set
  - High-performance Multiply/Divide Unit
  - Programmable clock frequencies: 48MHz, 12MHz, 3MHz, and 1MHz
  - Sleep mode
  - 2-wire Debug Interface (ICSP)
    - 6 Breakpoints (4-instruction; 2-data)
    - Enhanced to Support Debug in Heavy and Deep Sleep States
- Trace FIFO Debug Port (TFDP)
- Internal DMA Controller
  - Hardware or Firmware Flow Control
  - Firmware Initiated Memory-to-Memory transfers
  - 7-Hardware DMA Channels support three SMBus Master/Slave Controllers and one SPI Controller
  - Hardware CRC-32 Generator on Channel 0
- Secure Boot ROM Loader
  - 4 Code Images in Shared Flash Supported
  - Crisis Recovery over Keyboard matrix Scan Pins
  - Supports CRC-32 and AES-128 Encryption
- Vectored Interrupt Controller
  - Maskable Interrupt controller
  - Maskable Hardware Wake-Up Events
  - Supports legacy aggregated mode
  - Supports Vector Generation per Status Bit
- Programmable 16-bit Counter/Timer Interface
  - Four 16-bit Auto-reloading Counter/Timer Instances
  - Two Operating Modes per Instance: Timer and One-shot.
- 32-bit RTOS Timer
  - Runs Off 32kHz Clock Source
  - Continues Counting in all the Chip Sleep States Regardless of Processor Sleep State
  - Counter is Halted when Embedded Controller is Halted (e.g., JTAG debugger active, break points)
  - Generates wake-capable interrupt event
- Watch Dog Timer (WDT)
- Hibernation Timer Interface
  - One 32.768 KHz Driven Timer
  - Programmable Wake-up from 0.5ms to 128 Minutes
- Week Timer
  - System Power Present Input Pin

  - Week Alarm Event only generated when System Power is Available
  - Power-up Event
  - Week Alarm Interrupt with 1 Second to 8.5 Year Time-out
  - Sub-Week Alarm Interrupt with 0.50 Seconds - 72.67 hours time-out
  - 1 Second and Sub-second Interrupts
- Battery-Powered General Purpose Output (BGPO)
- VBAT-Powered Control Interface (VCI)
  - 2 Active-low VCI Inputs
  - 1 Active-high VCI Input
  - 1 Active-high VCI Output Pin
  - Optional filter and latching
- Power-Fail Status Register
- Port 80 BIOS Debug Port
  - Two Ports, Assignable to Any LPC IO Address
  - 24-bit Timestamp with Adjustable Timebase
  - 16-Entry FIFO
- PECI Interface 3.0
- Two Programmable Comparators
  - 8 Bit Resolution
  - Independent Outputs per Comparator
  - Option to Use Pin or Programmable Voltage Reference Input
  - Can be used for Thermistor Voltage Sensing
- Integrated Standby Power Reset Generator
- XNOR Test Mode

Product Dependent Features

- Enhanced Serial Peripheral Interface (eSPI)
  - Intel eSPI Specification compliant
  - Supports four channels/interfaces:
    - Peripheral channel Interface
    - Virtual Wire Interface
    - Out of Band Channel Interface
    - Flash Channel Interface
  - Supports EC Bus Master to Host Memory
- Internal Memory
  - Boot ROM
  - 32 kB Data Optimized SRAM
  - Code Optimized SRAM Options from 96 kB to 160 kB
  - 64 Bytes Battery Powered SRAM
- Keyboard Matrix Scan Controller
  - Supports 18x8 Matrix
  - Pre-Drive Mode Supported
- Up To Three EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Controllers are Fully Operational on Standby Power
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
  - 1 MHz Capable
  - SMBus Time-outs Interface
  - Up to 6 Port Flexible Multiplexing
    - Up to 5 ports with 1.8V or 3.3V Configurable Input Threshold
    - 1 port with VTT level signaling (i.e., AMD SB-TSI Port)
  - Supports DMA Network Layer
- Up To Two PS/2 Controllers
  - Independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
  - 3.6V Tolerant I/O Suitable for Internal Board Routing
- General Purpose I/O Pins
  - Inputs
    - Asynchronous rising and falling edge wakeup detection Interrupt High or Low Level
  - Outputs:
    - Push Pull or Open Drain output
    - Programmable power well emulation
  - Pull up or pull down resistor control
    - Automatically disabling pull-up resistors when output driven low
    - Automatically disabling pull-down resistors when output driven high
  - Group- or individual control of GPIO data.
- Up To Three LEDs
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
    - Provides for programmable rise and fall waveforms
  - Operational in EC Sleep States
- One Serial Peripheral Interface (SPI) Controller
  - Master Only SPI Controller
  - Mappable to three ports (only 1 port active at a time)
    - 1 shared SPI Interface.
    - 1 General Purpose SPI Interface (package dependent)
    - 1 Crisis recovery SPI Interface (located on Keyboard Matrix Scan connector)
  - Dual and Quad I/O Support

  - Flexible Clock Rates
  - SPI Burst Capable
  - SPI Controller Operates with Internal DMA Controller with CRC Generation
- Up To Two BC-Link Interconnection Bus
- ADC Interface
  - Up to 8 Channels
  - 10-bit Conversion in 10µs
  - Integral Non-Linearity of ±0.5 LSB; Differential Non-Linearity of ±0.5 LSB
  - External Analog Voltage Reference
- DAC Interface
  - Up to 2 Channels
  - 8 Bit Resolution
  - External Analog Voltage Reference
- FAN Support
  - Up to 8 Programmable Pulse-Width Modulator (PWM) Outputs, for Fan or General Use
    - Multiple Clock Rates
    - 16-Bit ON & 16-Bit OFF Counters
  - Up to Two Fan Tachometer Inputs,
    - 16 Bit Resolution
- Universal Asynchronous Receiver Transmitter (UART)
  - Full function Serial Port or 2-Pin Debug Port (product dependent)
  - High Speed NS16C550A Compatible UART with Send/Receive 16-Byte FIFOs
  - Accessible from Host and EC
  - Full Duplex Operation
  - Programmable Input/output Pin Polarity Inversion
  - Programmable Main Power or Standby Power Functionality
  - Standard Baud Rates to 115.2 Kbps, Custom Baud Rates to 1.5 Mbps
- Package
  - 128 VTQFP RoHS Compliant Package
  - 144 WFBGA RoHS Compliant Package

Products

Note: This table shows the total number of instances available per product. However, not all features may be used simultaneously since they are multiplexed on the same pins. See the Pin Description chapter to determine specific chip configuration options.

Catalog Part Number	Package	Host Interfaces	SRAM Memory (Code + Data)	Keyboard Matrix Scan Controller	SMBus 2.0 Ports	PS/2 Controllers	GPIOs	SPI Interfaces	BC-Link Interfaces	ADCs	DAC	PWMs	TACHs	UART
MEC1404-NU	128-VTQFP	• LPC • I2C	128 kB	Yes	6	2	106	3	2	8	2	8	2	full
MEC1404-SZ	144-WFBGA													
MEC1406-NU	128-VTQFP	• LPC • I2C	160 kB	Yes	6	2	106	3	2	8	2	8	2	full
MEC1406-SZ	144-WFBGA													
MEC1408-NU	128-VTQFP	• LPC • I2C	192 kB	Yes	6	2	106	3	2	8	2	8	2	full
MEC1408-SZ	144-WFBGA													
MEC1414-NU	128-VTQFP	• LPC • I2C • eSPI	128 kB	Yes	6	2	106	3	2	8	2	8	2	full
MEC1414-SZ	144-WFBGA													
MEC1416-NU	128-VTQFP	• LPC • I2C • eSPI	160 kB	Yes	6	2	106	3	2	8	2	8	2	full
MEC1416-SZ	144-WFBGA													
MEC1418-NU	128-VTQFP	• LPC • I2C • eSPI	192 kB	Yes	6	2	106	3	2	8	2	8	2	full
MEC1418-SZ	144-WFBGA													

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Table Of Contents

1.0 GENERAL DESCRIPTION

The MEC140x/1x is a family of keyboard and embedded controller designs customized for notebooks and tablet platforms. The MEC140x/1x family is a highly-configurable, mixed signal, advanced I/O controller architecture. Every device in the family incorporates a 32-bit MIPS32 M14K Microcontroller core with a closely-coupled SRAM for code and data. A secure boot-loader is used to download the custom firmware image from the system's shared SPI Flash device, thereby allowing system designers to customize the device's behavior.

The MEC140x/1x products may be configured to communicate with the system host through one of three host interfaces: Intel Low Pin Count (LPC), eSPI, or I2C. Note that this functionality is product dependent. To see which features apply to a specific part in the family see Products on page 3. The document defines the features for all devices in the family.

The MEC140x/1x products are designed to operate as either a stand-alone I/O device or as an EC Base Component of a split-architecture Advanced I/O Controller system which uses BC-Link communication protocol to access up to two BC bus companion components. The BC-Link protocol is peer-to-peer providing communication between the MEC140x/1x embedded controller and registers located in a companion device.

The MEC140x/1x is directly powered by a minimum of two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on' and system power management functions. In addition, this family of products has the option to connect the VTR_33_18 power pin to either a 3.3V VTR power supply or a 1.8V power supply. This option may only be used with the eSPI Host Interface or the I2C Host Interface. In systems using the I2C Host Interface, ten GPIOs are powered by VTR_33_18, thereby allowing them to operate at either 3.3V or 1.8V. All the devices are equipped with a Power Management Interface that supports low-power states and are capable of operating in a Connected Standby system.

The MEC140x/1x family of devices offer a software development system interface that includes a Trace FIFO Debug port, a host accessible serial debug port with a 16C550A register interface, a Port 80 BIOS Debug Port, and an In-circuit Serial Programming (ICSP) interface.

1.1 Boot ROM

Following the release of the EC_PROC_RESET# signal, the processor will start executing code in the Boot ROM. The Boot ROM executes the SPI Flash Loader, which downloads User Code from an external SPI Flash and stores it in the internal Code RAM. Upon completion, the Boot ROM jumps into the User Code and starts executing.

1.2 Initialize Host Interface

By default, this device powers up all the interfaces, except the VBAT powered interfaces and select signals, to GPIO inputs. The Boot ROM is used to download code from an external flash via either the Shared Flash Interface, the eSPI flash channel or the Private Flash Interface. The downloaded code must configure the device's pins according to the platform's needs. This includes initializing the Host Interface.

Once the device is configured for operation, the downloaded code must deassert the system's RSMRST# (Resume Reset) signal. Any GPIO may be selected for the RSMRST# function. This is up to the system board designer. The only requirement is that the board designer attach an external pull-down on the GPIO pin being used for the RSMRST# function. This will ensure the RSMRST# pin is asserted low by default and does not glitch during power-up.

This family of devices has up to three Host Interface options. It may be configured as an LPC Device, an eSPI Device, or I2C device. See Products on page 3 for the features supported in each device.

On a VTR POR, all the host interface pins default to GPIO inputs.

1.2.1 CONFIGURE LPC INTERFACE

The downloaded firmware must configure the GPIO Pin Control registers for the LPC alternate function, configure the LPC Base Address Register (BAR), and activate the LPC block.

Example:

- GPIO034 Pin Control Register = 0x1000; //ALT FUNC1 – PCI_CLK
- GPIO040 Pin Control Register = 0x1000; //ALT FUNC1 – LAD0
- GPIO041 Pin Control Register = 0x1000; //ALT FUNC1 – LAD1
- GPIO042 Pin Control Register = 0x1000; //ALT FUNC1 – LAD2
- GPIO043 Pin Control Register = 0x1000; //ALT FUNC1 – LAD3
- GPIO044 Pin Control Register = 0x1000; //ALT FUNC1 – LFRAME_N

- GPIO061 Pin Control Register = 0x1000; //ALT FUNC1 – LPC_PD_N
- GPIO063 Pin Control Register = 0x1000; //ALT FUNC1 – SER_IRQ
- GPIO064 Pin Control Register = 0x1000; //ALT FUNC1 – PCI_RESET
- GPIO067 Pin Control Register = 0x1000; //ALT FUNC1 – CLKRUN
- LPC Interface (Configuration Port) BAR = 0x002E_8C01; //set bit 15
- LPC Activate Register = 0x01;

1.2.2 CONFIGURE ESPI INTERFACE

The downloaded firmware must configure the GPIO Pin Control registers for the eSPI alternate function, configure the eSPI I/O Component (Configuration Port) Base Address Register (BAR), and activate the eSPI block.

Example:

- GPIO034 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_CLK
- GPIO044 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_CS#
- GPIO040 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO0
- GPIO041 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO1
- GPIO042 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO2
- GPIO043 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_IO3
- GPIO063 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_ALERT#
- GPIO061 Pin Control Register = 0x2000; //ALT FUNC2 – ESPI_RESET#
- eSPI I/O Component (Configuration Port) BAR = 0x002E_0001; //set bit 15
- eSPI Activate Register = 0x01;

1.2.3 CONFIGURE I2C INTERFACE

Similar to the LPC and eSPI interfaces, the downloaded firmware must configure the GPIO Pin Control registers for the SMBus alternate function and activate the associated SMB/I2C Controller.

1.3 Initialize Peripheral Interfaces

This will be system dependent, however, this section outlines some recommendations when enabling certain interfaces.

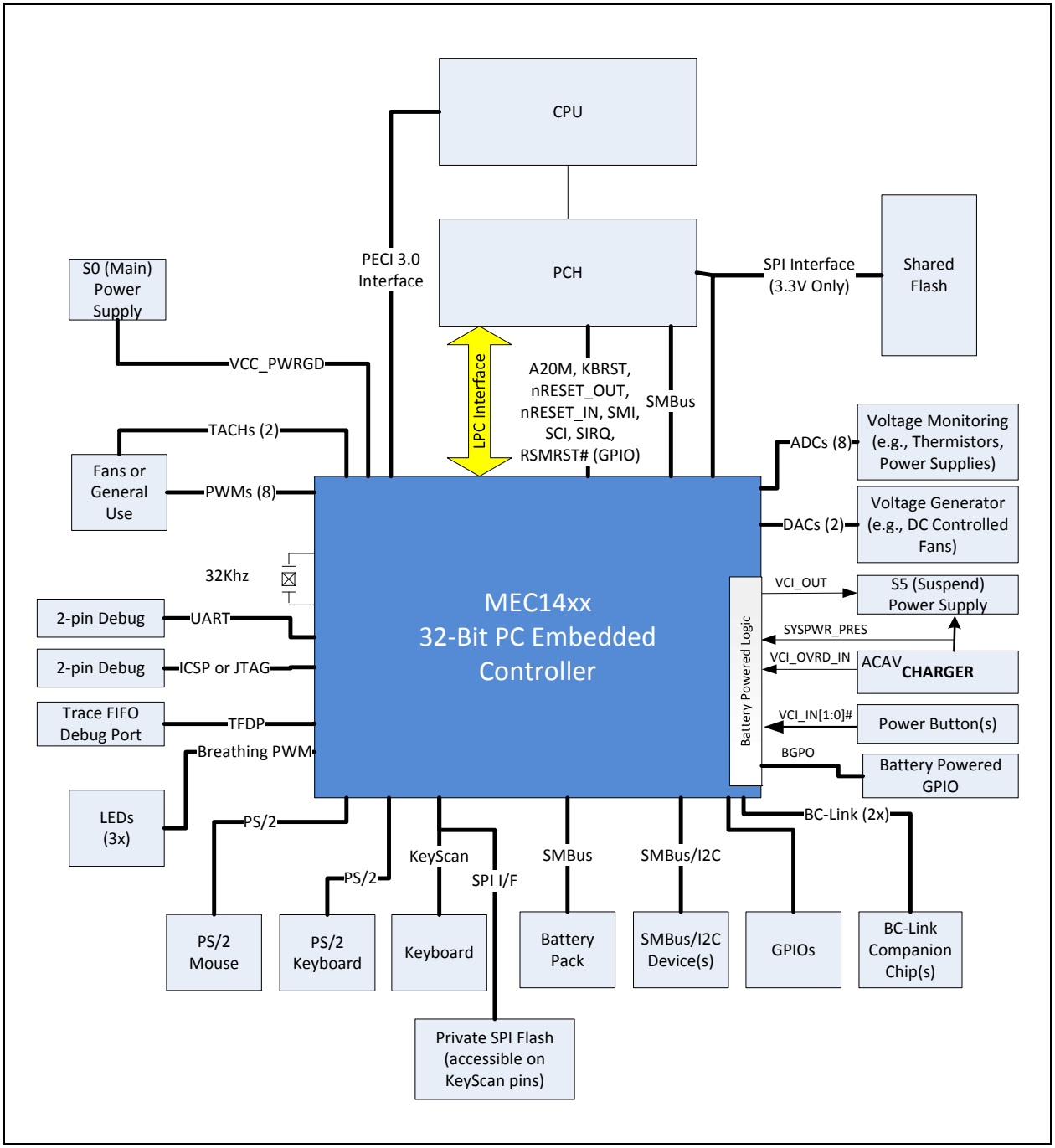
1.3.1 KEYBOARD SCAN INTERFACE

The Keyboard Scan Interface has been multiplexed onto GPIO pins. Internal pull-up resistors, enabled via the GPIO Pin Control Registers", may be used on the KSI and KSO pins instead of external pull-ups. However, if internal pull-ups are used then the PreDrive Mode must be enabled. The GPIO Pin Control register format is defined in Section 22.6.1.1, "Pin Control Register," on page 329. The PreDrive Mode is defined in Section 30.10.2, "PreDrive Mode," on page 406.

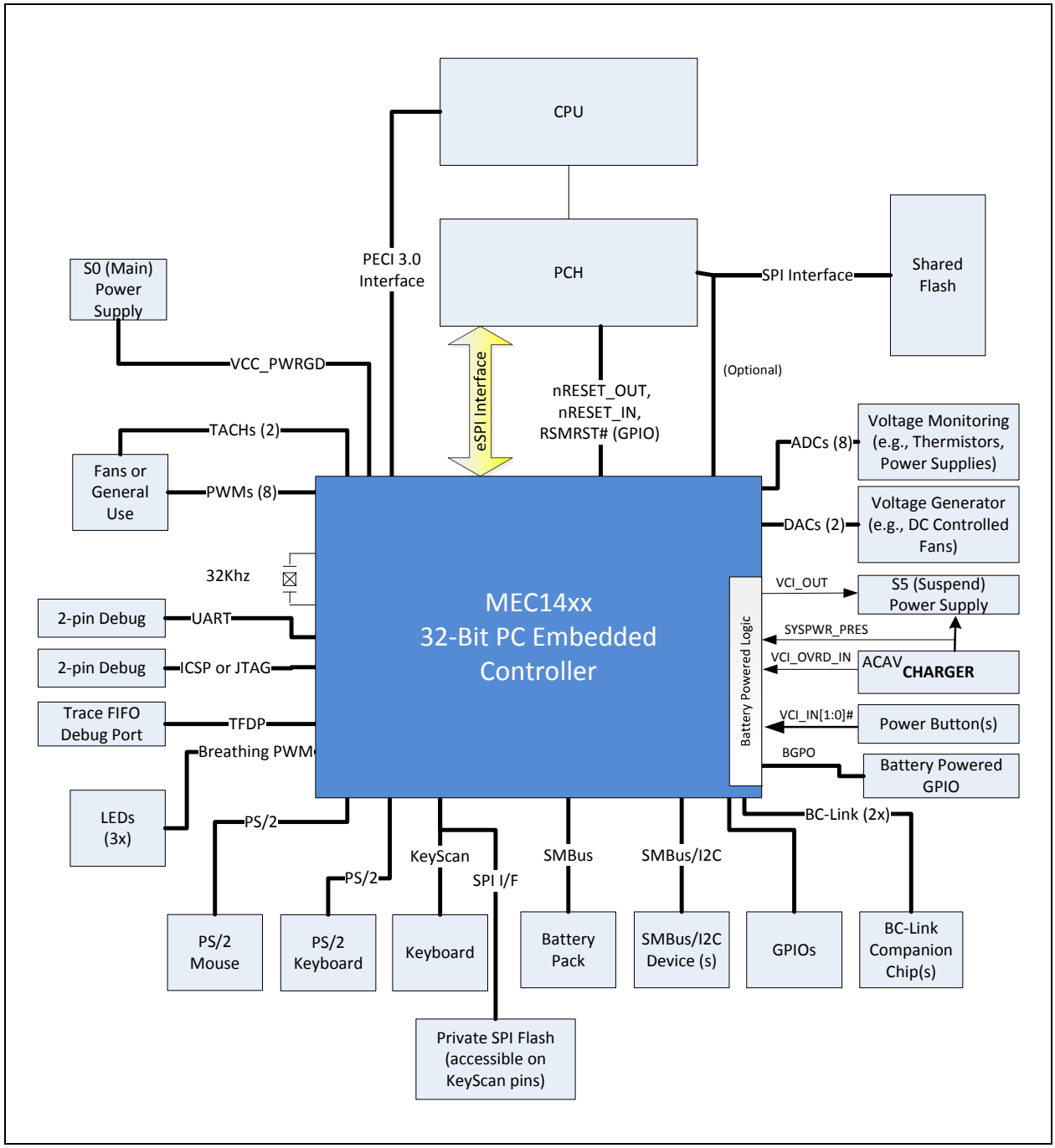
1.4 System Block Diagrams

Note:	Not all features shown are available on all devices. Refer to Products on page 3 for a list of the features by device.

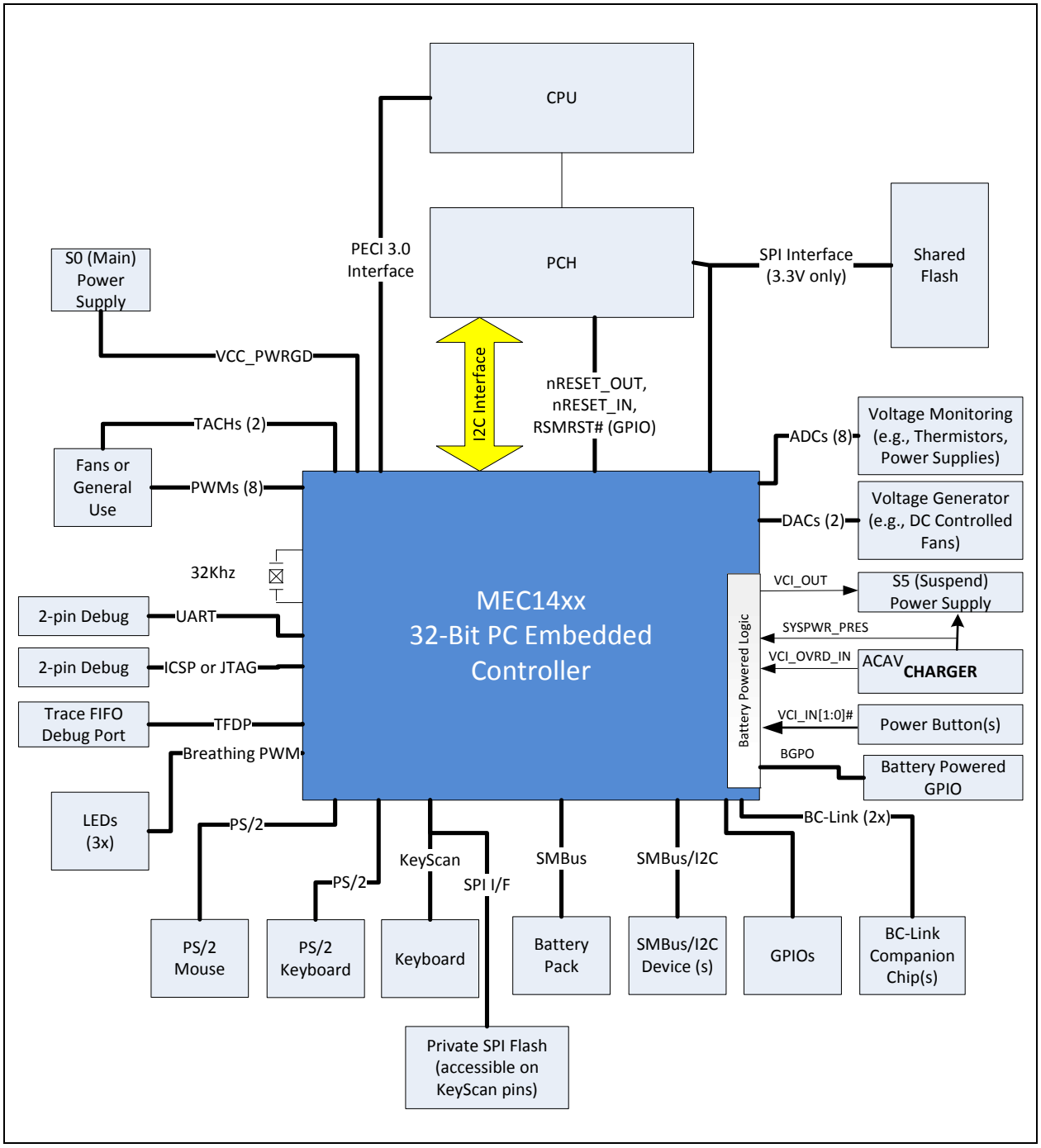
1.4.1 LPC HOST SYSTEM BLOCK DIAGRAM



1.4.2 ESPI HOST SYSTEM BLOCK DIAGRAM



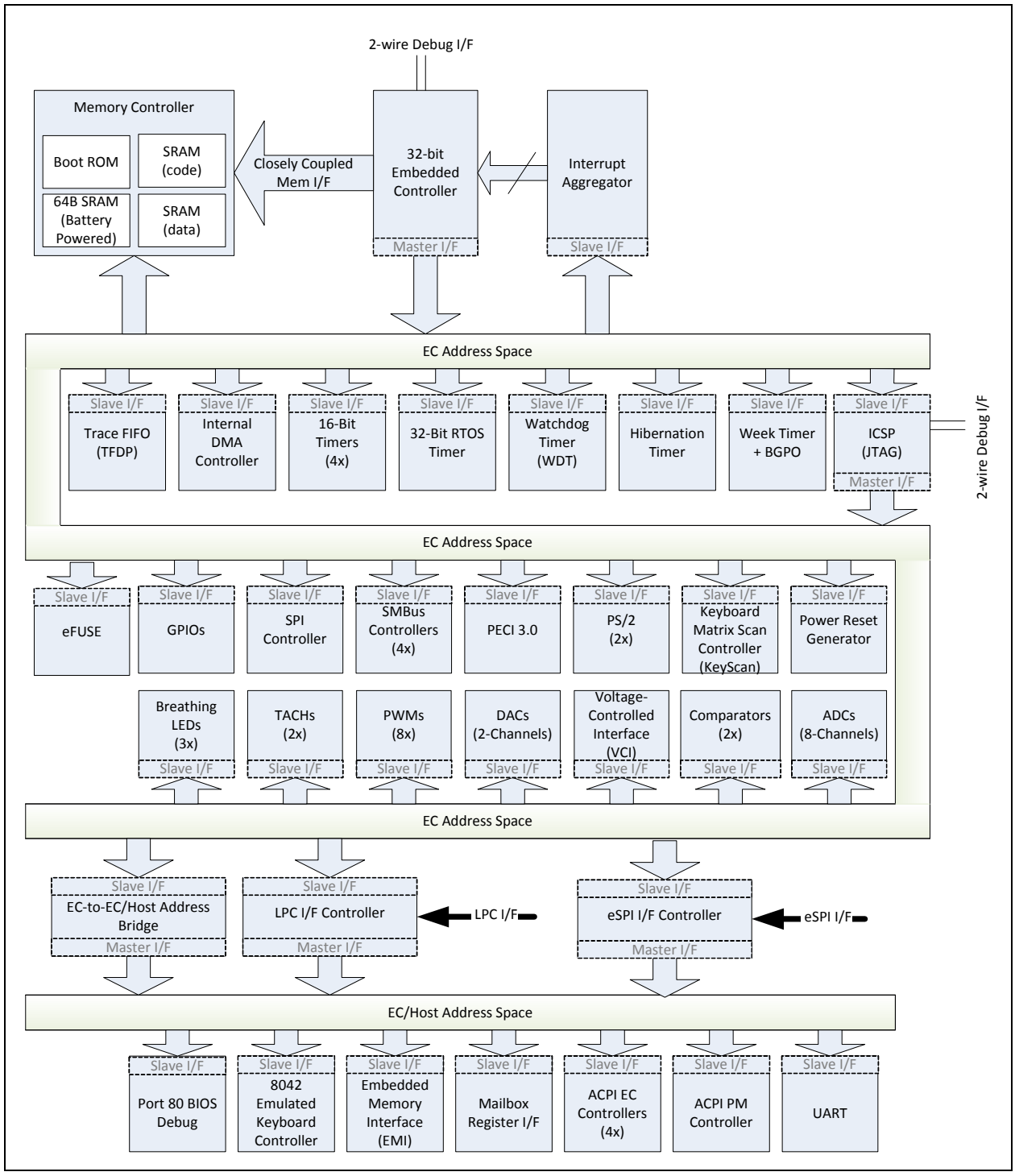
1.4.3 I2C HOST SYSTEM BLOCK DIAGRAM



1.5 MEC140x Internal Address Spaces

The Internal Embedded Controller can access any register in the EC Address Space or Host Address Space. The LPC and eSPI Host Controllers can directly access peripheral registers in the Host Address Space. If the I2C interface is used as the Host Interface, access to all the IP Peripherals is dependent on the EC firmware.

Note:	The eSPI and LPC Host Controllers also have access to the SRAM data space via the SRAM Memory BARs, which is not illustrated below.



Note: Not all features shown are available on all devices. Refer to Products on page 3 for a list of the features by device.

2.0 PIN CONFIGURATION

2.1 Description

The Pin Configuration chapter includes Pin Lists, Pin Description, Pin Multiplexing, Notes for Tables in this Chapter, Pin States After VTR Power-On, and Packages.

2.2 Terminology and Symbols for Pins/Buffers

2.2.1 BUFFER TERMINOLOGY

Term	Definition
Pin Ref. Number	There is a unique reference number for each pin name.
#	The '#' sign at the end of a signal name indicates an active-low signal
n	The lowercase 'n' preceding a signal name indicates an active-low signal
PWR	Power
I	Digital Input
IS	Input with Schmitt Trigger
I_AN	Analog Input
O	Push-Pull Output
OD	Open Drain Output
IO	Bi-directional pin
IOD	Bi-directional pin with Open Drain Output
PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output.
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 2-1)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 2-1)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 2-1)
PCI_IO	Input/Output These pins meet the PCI 3.3V AC and DC Characteristics. (Note 2-1)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2-2)
PCI_PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 2-1).
PECI_IO	PECI Input/Output. These pins operate at the processor voltage level (VREF_CPU)
SB-TSI	SB-TSI Input/Output. These pins operate at the processor voltage level (VREF_CPU)

Note 2-1 See the "PCI Local Bus Specification," Revision 2.1, Section 4.2.2.

Note 2-2 See the "PCI Local Bus Specification," Revision 2.1, Section 4.2.2 and 4.2.3.

2.2.2 PIN NAMING CONVENTIONS

1. Pin Name is composed of the multiplexed options separated by '/'. E.g., GPIOxxxx/SignalA/SignalB.
2. The first signal shown in a pin name is the default signal. E.g., GPIOxxxx/SignalA/SignalB means the GPIO is the default signal.
3. Parenthesis '()' are used to list aliases or alternate functionality for a single mux option. E.g. GPIOxxx(Alias)/SignalA/SignalB. The Alias is the intended usage for a specific GPIO. E.g., GPIOxxx(ICSP_DATA) is intended to indicate that ICSP_DATA signal may come out on this pin when the Mux Control is set for GPIOxxx. In this case, enabling the test mode takes precedence over the Mux Control selection.
4. Square brackets '[ ]' are used to indicate there is a Strap Option on a pin. This is always shown as the last signal on the Pin Name.
5. Signal Names appended with a numeric value indicates the Instance Number, except for SMBus Pins. E.g., PWM0, PWM1, etc. indicates that PWM0 is the PWM output for PWM Instance 0, PWM1 is the PWM output for PWM Instance 1, etc. Note that this same instance number is shown in the Register Base Address tables linking

the specific PWM block instance to a specific signal on the pinout. The instance number may be omitted if there in only one instance of the IP block implemented.

Note: The numeric value appended to the end of the SMBus pins indicates they are 1.8V I/O signaling. E.g. SMB03_DATA vs SMB03_DATA18. The SMB03_DATA signal uses standard 3.3V I/O signaling. The SMB03_DATA18 signal operates at 1.8V I/O signaling levels.

6. SMBus Port pins can be mapped to any SMB Controller. The number in the SMBus signal names (SMBxx_DATA) indicates the port value. E.g. SMB01_DATA represents SMBus Data Port 1

2.3 Notes for Tables in this Chapter

Note	Description
Note 1	The LAD and SER_IRQ pins require an external weak pull-up resistor of 10k-100k ohms.
Note 2	The ICSP_MCLR pin is used to enable JTAG. There is an internal pull-up on this pin to keep it from entering debug mode. When debug mode is entered the ICSP_DATA and ICSP_CLOCK signals are automatically enabled on their respective pins. The System Board Designer should leave the ICSP_MCLR pin as a no-connect.
Note 3	An external cap must be connected as close to the CAP pin/ball as possible with a routing resistance and CAP ESR of less than 100mohms. The capacitor value is 1uF and must be ceramic with X5R or X7R dielectric. The cap pin/ball should remain on the top layer of the PCB and traced to the CAP. Avoid adding vias to other layers to minimize inductance.
Note 4	This SMBus ports supports 1 Mbps operation as defined by I2C. For 1 Mbps I2C recommended capacitance/pull-up relationships from Intel, refer to the Shark Bay platform guide, Intel ref number 486714. Refer to the PCH - SMBus 2.0/SMLink Interface Design Guidelines, Table 20-5 Bus Capacitance/Pull-Up Resistor Relationship.
Note 5	RESET_OUT# pin must be pulled to ground via an external 8.2k ohm resistor. This will ensure the glitch-free tristate GPIO input will not glitch high on a power on reset (POR) event.
Note 6	In order to achieve the lowest leakage current when both PECI and SB TSI are not used, set the VREF_CPU Disable bit to 1.
Note 7	The BC DAT pin requires a weak pull up resistor (100 K Ohms).
Note 8	The voltage on the ADC pins must not exceed 3.6 V or damage to the device will occur.
Note 9	The XTAL1 pin should be left floating when using the XTAL2 pin for the single ended clock input.
Note 10	The Boot ROM manipulates the pins associated with the Shared SPI interface and the Private SPI interface to access the external flash. Before exiting, the Boot ROM tristates these interfaces by returning them to their default hardware state (i.e., GPIO input).
Note 11	When the SMBxx_xxxx18 functions are selected, the pins operate at 1.8V I/O signal levels.
Note 12	The GPIO assignment on this pin only provides interrupt and wakeup capability. This is provided by the Interrupt Detection field in the Pin Control register. The Mux control field in the Pin Control Register should not be set to 00 = GPIO or undesirable results may occur. In order to emphasize the prohibition on using the GPIO Signal Pin Function, the Pin Chapter does not list the GPIO signal pin function assigned to this pin; however, the GPIO chapter does so the interrupt can be used.
Note 13	This signal is a test signal used to detect when the internal 48MHz clock is toggling or stopped in heavy and deepest sleep modes.
Note 14	The VCI pins may be used as GPIOs. The VCI input signals are not gated by selecting the GPIO alternate function. Firmware must disable (i.e., gate) these inputs by writing the bits in the VCI Input Enable Register when the GPIO function is enabled.

Note	Description
Note 15	The KSI and KSO Key Scan pins require pull-up resistors. The system designer may opt to use either use the internal pull-up resistors or populate external pull-up resistors.
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.
Note 17	If the eSPI Flash Channel is used for booting, the GPIO135/SHD_IO2 pin must be used to determine that the primary power rails are stable before RSMRST# can be de-asserted. See the MEC140X/1X eSPI Addendum document for more details.
Note 18	If certain blocks are not used, then the associated voltage reference pin may be connected to ground, as follows: • if the ADC is not used and the block is disabled, ADC_VREF can be connected to VSS • if the DAC is not used and the block is disabled, DAC_VREF can be connected to VSS • if both PECI and SB TSI are not used and the GPIO033/PECI_DAT/SB_TSI_DAT and GPIO035/ SB-TSI_CLK pins are configured as GPIOs, then VREF_CPU can be connected to VSS.

2.4 Pin Lists

Note: The GPIO Pin Control registers for the Pads that are not bonded out to pins or balls in the smaller package have been defaulted to their inactive state and are read-only. These pins cannot be modified by the downloaded firmware located in SRAM. No special handling required.

2.4.1 MEC140X PIN LIST

MEC140x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
1	L10	GPIO157/LED0/TST_CLK_OUT
2	N13	GPIO027/KSO00/PVT_IO1
3	M12	GPIO001/SPI_CS#/32KHZ_OUT
4	M10	GPIO002/PWM7
5	G5	VTR
6	M13	GPIO005/SMB00_DATA/SMB00_DATA18/KSI2
7	L12	GPIO006/SMB00_CLK/SMB00_CLK18/KSI3
8	K11	GPIO007/SMB01_DATA/SMB01_DATA18
9	J11	GPIO010/SMB01_CLK/SMB01_CLK18
10	G9	GPIO011/nSMI/nEMI_INT
11	J7	GPIO012/SMB02_DATA/SMB02_DATA18
12	H12	GPIO013/SMB02_CLK/SMB02_CLK18
13	H8	nRESET_IN/GPIO014
14	L11	GPIO015/KSO01/PVT_CS#
15	H11	GPIO016/KSO02/PVT_SCLK
16	J12	GPIO017/KSO03/PVT_IO0
17	C9	VSS
18	F1	VR_CAP
19	H5	VTR
20	G11	GPIO020/CMP_VIN0

MEC140x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
21	H13	GPIO021/CMP_VIN1
22	G12	DAC_VREF
23	G13	GPIO160/DAC_0
24	F12	GPIO161/DAC_1
25	F11	GPIO165/CMP_VREF0
26	E11	GPIO166/CMP_VREF1/UART_CLK
27	F13	GPIO123/SHD_CS#
28	E12	GPIO133/SHD_IO0
29	D12	GPIO134/SHD_IO1
30	E13	GPIO135/SHD_IO2
31	C11	GPIO136/SHD_IO3
32	D13	GPIO126/SHD_SCLK
33	D11	GPIO062/SPI_IO3
34	C12	GPIO030/BCM_INT0#/PWM4
35	C13	GPIO031/BCM_DAT0/PWM5
36	B13	GPIO032/BCM_CLK0/PWM6
37	B11	GPIO045/BCM_INT1#/KSO04
38	B12	GPIO046/BCM_DAT1/KSO05
39	B10	GPIO047/BCM_CLK1/KSO06
40	A13	GPIO050/TACH0
41	A12	GPIO051/TACH1
42	A11	GPIO052/SPI_IO2
43	H6	VTR
44	C8	GPIO053/PWM0
45	B9	GPIO054/PWM1
46	A10	GPIO055/PWM2/KSO08/PVT_IO3
47	A9	GPIO056/PWM3
48	B8	GPIO057/VCC_PWRGD
49	B7	GPIO060/KBRST
50	A8	GPIO025/KSO07/PVT_IO2
51	C10	VSS
52	C7	GPIO026/PS2_CLK1B
53	A7	GPIO061/LPCPD#
54	H7	VTR_33_18
55	C6	GPIO063/SER_IRQ
56	B6	GPIO064/LRESET#
57	A6	GPIO034/PCI_CLK
58	B5	GPIO044/LFRAME#
59	A5	GPIO040/LAD0
60	A4	GPIO041/LAD1
61	C5	GPIO042/LAD2
62	C4	GPIO043/LAD3
63	B4	GPIO067/CLKRUN#
64	D1	VSS

MEC140x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
65	J5	VTR
66	C3	GPIO100/nEC_SCI
67	C2	GPIO101/SPI_CLK
68	A3	GPIO102/KSO09[CR_STRAP]
69	B3	GPIO103/SPI_IO0
70	A2	GPIO104/LED2
71	E2	GPIO105/SPI_IO1
72	C1	GPIO106/KSO10
73	D2	GPIO107/nRESET_OUT
74	B2	GPIO110/KSO11
75	F2	GPIO111/KSO12
76	A1	GPIO112/PS2_CLK1A/KSO13
77	G3	GPIO113/PS2_DAT1A/KSO14
78	E1	GPIO114/PS2_CLK0
79	B1	GPIO115/PS2_DAT0
80	G1	GPIO116/TFDP_DATA/UART_RX
81	G2	GPIO117/TFDP_CLK/UART_TX
82	J6	VTR
83	H2	GPIO120/CMP_VOUT1
84	D3	VSS
85	H1	GPIO124/CMP_VOUT0
86	H3	GPIO125/KSO15
87	K1	ICSP_MCLR
88	J1	GPIO127/PS2_DAT1B
89	K2	GPIO130/SMB03_DATA/SMB03_DATA18
90	J2	GPIO035/SB-TSI_CLK
91	L1	GPIO131/SMB03_CLK/SMB03_CLK18
92	M1	GPIO132/KSO16
93	N1	GPIO140/KSO17
94	K3	GPIO033/PECI_DAT/SB_TSI_DAT
95	L5	VREF_CPU
96	J3	GPIO141/SMB04_DATA/SMB04_DATA18
97	L3	GPIO142/SMB04_CLK/SMB04_CLK18
98	L4	GPIO143/KSI0/DTR#
99	L2	GPIO144/KSI1/DCD#
100	F3	VSS
101	M2	GPIO145(ICSP_CLOCK)
102	M3	GPIO146(ICSP_DATA)
103	G6	VTR
104	N2	GPIO147/KSI4/DSR#
105	M4	GPIO150/KSI5/RI#
106	N3	GPIO156/LED1
107	N4	GPIO151/KSI6/RTS#
108	N5	GPIO152/KSI7/CTS#

MEC140x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
109	N6	GPIO153/ADC4
110	L7	GPIO154/ADC3
111	M6	GPIO155/ADC2
112	M7	AVSS
113	L6	GPIO122/ADC1
114	N7	GPIO121/ADC0
115	M5	ADC_VREF
116	N8	GPIO022/ADC5
117	L9	GPIO023/ADC6/A20M
118	N9	GPIO024/ADC7
119	N10	BGPO/GPIO004
120	M9	SYSPWR_PRES/GPIO003
121	M8	VCI_OUT/GPIO036
122	K12	VBAT
123	J13	XTAL1
124	E3	VSS_VBAT
125	L13	XTAL2
126	N12	VCI_IN1#/GPIO162
127	N11	VCI_IN0#/GPIO163
128	M11	VCI_OVRD_IN/GPIO164
	H9	VSS
	J8	VSS
	J9	VSS
	K13	VSS
	E5	No Connect
	E6	No Connect
	E7	No Connect
	E8	No Connect
	E9	No Connect
	F5	No Connect
	F6	No Connect
	F7	No Connect
	F8	No Connect
	F9	No Connect
	G8	No Connect
	L8	No Connect

2.4.2 MEC141X PIN LIST

MEC141x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
1	L10	GPIO157/LED0/TST_CLK_OUT
2	N13	GPIO027/KSO00/PVT_IO1
3	M12	GPIO001/SPI_CS#/32KHZ_OUT
4	M10	GPIO002/PWM7
5	G5	VTR
6	M13	GPIO005/SMB00_DATA/SMB00_DATA18/KSI2
7	L12	GPIO006/SMB00_CLK/SMB00_CLK18/KSI3
8	K11	GPIO007/SMB01_DATA/SMB01_DATA18
9	J11	GPIO010/SMB01_CLK/SMB01_CLK18
10	G9	GPIO011/nSMI/nEMI_INT
11	J7	GPIO012/SMB02_DATA/SMB02_DATA18
12	H12	GPIO013/SMB02_CLK/SMB02_CLK18
13	H8	nRESET_IN/GPIO014
14	L11	GPIO015/KSO01/PVT_CS#
15	H11	GPIO016/KSO02/PVT_SCLK
16	J12	GPIO017/KSO03/PVT_IO0
17	C9	VSS
18	F1	VR_CAP
19	H5	VTR
20	G11	GPIO020/CMP_VIN0
21	H13	GPIO021/CMP_VIN1
22	G12	DAC_VREF
23	G13	GPIO160/DAC_0
24	F12	GPIO161/DAC_1
25	F11	GPIO165/CMP_VREF0
26	E11	GPIO166/CMP_VREF1/UART_CLK
27	F13	GPIO123/SHD_CS# [BSS_STRAP]
28	E12	GPIO133/SHD_IO0
29	D12	GPIO134/SHD_IO1
30	E13	GPIO135/SHD_IO2
31	C11	GPIO136/SHD_IO3
32	D13	GPIO126/SHD_SCLK
33	D11	GPIO062/SPI_IO3
34	C12	GPIO030/BCM_INT0#/PWM4
35	C13	GPIO031/BCM_DAT0/PWM5
36	B13	GPIO032/BCM_CLK0/PWM6
37	B11	GPIO045/BCM_INT1#/KSO04
38	B12	GPIO046/BCM_DAT1/KSO05
39	B10	GPIO047/BCM_CLK1/KSO06
40	A13	GPIO050/TACH0
41	A12	GPIO051/TACH1
42	A11	GPIO052/SPI_IO2

MEC141x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
43	H6	VTR
44	C8	GPIO053/PWM0
45	B9	GPIO054/PWM1
46	A10	GPIO055/PWM2/KSO08/PVT_IO3
47	A9	GPIO056/PWM3
48	B8	GPIO057/VCC_PWRGD
49	B7	GPIO060/KBRST
50	A8	GPIO025/KSO07/PVT_IO2
51	C10	VSS
52	C7	GPIO026/PS2_CLK1B
53	A7	GPIO061/LPCPD#/ESPI_RESET#
54	H7	VTR_33_18
55	C6	GPIO063/SER_IRQ/ESPI_ALERT#
56	B6	GPIO064/LRESET#
57	A6	GPIO034/PCI_CLK/ESPI_CLK
58	B5	GPIO044/LFRAME#/ESPI_CS#
59	A5	GPIO040/LAD0/ESPI_IO0
60	A4	GPIO041/LAD1/ESPI_IO1
61	C5	GPIO042/LAD2/ESPI_IO2
62	C4	GPIO043/LAD3/ESPI_IO3
63	B4	GPIO067/CLKRUN#
64	D1	VSS
65	J5	VTR
66	C3	GPIO100/nEC_SCI
67	C2	GPIO101/SPI_CLK
68	A3	GPIO102/KSO09[CR_STRAP]
69	B3	GPIO103/SPI_IO0
70	A2	GPIO104/LED2
71	E2	GPIO105/SPI_IO1
72	C1	GPIO106/KSO10
73	D2	GPIO107/nRESET_OUT
74	B2	GPIO110/KSO11
75	F2	GPIO111/KSO12
76	A1	GPIO112/PS2_CLK1A/KSO13
77	G3	GPIO113/PS2_DAT1A/KSO14
78	E1	GPIO114/PS2_CLK0
79	B1	GPIO115/PS2_DAT0
80	G1	GPIO116/TFDP_DATA/UART_RX
81	G2	GPIO117/TFDP_CLK/UART_TX
82	J6	VTR
83	H2	GPIO120/CMP_VOUT1
84	D3	VSS
85	H1	GPIO124/CMP_VOUT0
86	H3	GPIO125/KSO15

MEC141x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
87	K1	ICSP_MCLR
88	J1	GPIO127/PS2_DAT1B
89	K2	GPIO130/SMB03_DATA/SMB03_DATA18
90	J2	GPIO035/SB-TSI_CLK
91	L1	GPIO131/SMB03_CLK/SMB03_CLK18
92	M1	GPIO132/KSO16
93	N1	GPIO140/KSO17
94	K3	GPIO033/PECI_DAT/SB_TSI_DAT
95	L5	VREF_CPU
96	J3	GPIO141/SMB04_DATA/SMB04_DATA18
97	L3	GPIO142/SMB04_CLK/SMB04_CLK18
98	L4	GPIO143/KSI0/DTR#
99	L2	GPIO144/KSI1/DCD#
100	F3	VSS
101	M2	GPIO145(ICSP_CLOCK)
102	M3	GPIO146(ICSP_DATA)
103	G6	VTR
104	N2	GPIO147/KSI4/DSR#
105	M4	GPIO150/KSI5/RI#
106	N3	GPIO156/LED1
107	N4	GPIO151/KSI6/RTS#
108	N5	GPIO152/KSI7/CTS#
109	N6	GPIO153/ADC4
110	L7	GPIO154/ADC3
111	M6	GPIO155/ADC2
112	M7	AVSS
113	L6	GPIO122/ADC1
114	N7	GPIO121/ADC0
115	M5	ADC_VREF
116	N8	GPIO022/ADC5
117	L9	GPIO023/ADC6/A20M
118	N9	GPIO024/ADC7
119	N10	BGPO/GPIO004
120	M9	SYSPWR_PRES/GPIO003
121	M8	VCI_OUT/GPIO036
122	K12	VBAT
123	J13	XTAL1
124	E3	VSS_VBAT
125	L13	XTAL2
126	N12	VCI_IN1#/GPIO162
127	N11	VCI_IN0#/GPIO163
128	M11	VCI_OVRD_IN/GPIO164
	H9	VSS
	J8	VSS

MEC141x		
128-pin VTQFP	**144-pin WFBGA**	**Pin Name**
	J9	VSS
	K13	VSS
	E5	No Connect
	E6	No Connect
	E7	No Connect
	E8	No Connect
	E9	No Connect
	F5	No Connect
	F6	No Connect
	F7	No Connect
	F8	No Connect
	F9	No Connect
	G8	No Connect
	L8	No Connect

2.5 Non 5 Volt Tolerant Pins

There are no 5 Volt tolerant pins in the MEC140x/1x.

2.6 1.8V or 3.3V I/O Pins

The following signals are powered by the VTR_33_18 power supply. This supply determines the operating voltage range for these signals.

Note: The LPC Interface signals require the VTR_33_18 power pin to be connected to the 3.3V VTR rail. The eSPI Interface signals require the VTR_33_18 power pin to be connected to the 1.8V rail. The GPIO signals on these pins may operate at either 1.8V or 3.3V.

- GPIO061/LPCPD#/ESPI_RESET#
- VTR_33_18
- GPIO063/SER_IRQ/ESPI_ALERT#
- GPIO064/LRESET#
- GPIO034/PCI_CLK/ESPI_CLK
- GPIO044/LFRAME#/ESPI_CS#
- GPIO040/LAD0/ESPI_IO0
- GPIO041/LAD1/ESPI_IO1
- GPIO042/LAD2/ESPI_IO2
- GPIO043/LAD3/ESPI_IO3
- GPIO067/CLKRUN#

2.7 POR Glitch Protected Pins

All pins have POR output glitch protection. POR output glitch protection ensures that pins will have a steady-state output during a VTR POR.

2.8 Non Backdrive Protected Pins

TABLE 2-1: lists pins which do not have backdrive protection. If the power supply used to power the buffer of the pin (VTR or VTR_33_18) is off none of these pins are allowed to be above 0V to prevent back-drive onto the associated power supply. The Power Supply used to power the buffer is shown in the Signal Power Well column of the Pin Multiplexing Tables in **Section 2.0 "Pin Configuration"**.

TABLE 2-1: MEC140X/1X NON BACKDRIVE PROTECTED PINS

Pin Name
DAC_VREF
GPIO160/DAC_0
GPIO161/DAC_1
GPIO165/CMP_VREF0
GPIO166/CMP_VREF1/UART_CLK
GPIO020/CMP_VIN0
GPIO021/CMP_VIN1
GPIO035/SB-TSI_CLK
GPIO033/PECI_DAT/SB_TSI_DAT
VREF_CPU
ADC_VREF
GPIO153/ADC4
GPIO154/ADC3
GPIO155/ADC2
GPIO122/ADC1
GPIO121/ADC0
GPIO022/ADC5
GPIO023/ADC6/A20M
GPIO024/ADC7
GPIO040/LAD0
GPIO041/LAD1
GPIO042/LAD2
GPIO043/LAD3
GPIO063/SER_IRQ
XTAL1
XTAL2

2.9 Pin Description

Note: See Section 2.3, "Notes for Tables in this Chapter," on page 13 for notes that are referenced in the Pin Description table.

Interface	Signal Name	Description	Notes
Analog Data Acquisition Interface	ADC0	ADC channel 0	Note 8
Analog Data Acquisition Interface	ADC1	ADC channel 1	Note 8
Analog Data Acquisition Interface	ADC2	ADC channel 2	Note 8

Interface	Signal Name	Description	Notes
Analog Data Acquisition Interface	ADC3	ADC channel 3	Note 8
Analog Data Acquisition Interface	ADC4	ADC channel 4	Note 8
Analog Data Acquisition Interface	ADC5	ADC channel 5	Note 8
Analog Data Acquisition Interface	ADC6	ADC channel 6	Note 8
Analog Data Acquisition Interface	ADC7	ADC channel 7	Note 8
BC-Link Interface	BCM_CLK0	BC-Link Master clock	
BC-Link Interface	BCM_CLK1	BC-Link Master clock	
BC-Link Interface	BCM_DAT0	BC-Link Master data I/O	Note 7
BC-Link Interface	BCM_DAT1	BC-Link Master data I/O	Note 7
BC-Link Interface	BCM_INT0#	BC-Link Master interrupt	
BC-Link Interface	BCM_INT1#	BC-Link Master interrupt	
Comparator Interface	CMP_VIN0	Comparator 0 Positive Input	
Comparator Interface	CMP_VIN1	Comparator 1 Positive Input	
Comparator Interface	CMP_VOUT0	Comparator 0 Output	
Comparator Interface	CMP_VOUT1	Comparator 1 Output	
Comparator Interface	CMP_VREF0	Comparator 0 Negative Input	
Comparator Interface	CMP_VREF1	Comparator 1 Negative Input	
Digatal to Analog (DAC) Interface	DAC_0	DAC channel 0	
Digatal to Analog (DAC) Interface	DAC_1	DAC channel 1	
eSPI HOST INTERFACE	ESPI_ALERT#	eSPI Alert	
eSPI HOST INTERFACE	ESPI_CLK	eSPI Clock	
eSPI HOST INTERFACE	ESPI_CS#	eSPI Chip Select	
eSPI HOST INTERFACE	ESPI_IO0	eSPI Data Pin 0	
eSPI HOST INTERFACE	ESPI_IO1	eSPI Data Pin 1	
eSPI HOST INTERFACE	ESPI_IO2	eSPI Data Pin 2	
eSPI HOST INTERFACE	ESPI_IO3	eSPI Data Pin 3	
eSPI HOST INTERFACE	ESPI_RESET#	eSPI Reset	
GPIO Interface	GPIO	General Purpose Input Output Pins	
ICSP Interface	ICSP_CLOCK	2-Wire Debug Clock	
ICSP Interface	ICSP_DATA	2-Wire Debug Data	
ICSP Interface	ICSP_MCLR	2-Wire Debug Master Reset	Note 2
Keyboard Scan Interface	KSI0	Keyboard Scan Matrix Input 0	Note 15
Keyboard Scan Interface	KSI1	Keyboard Scan Matrix Input 1	Note 15
Keyboard Scan Interface	KSI2	Keyboard Scan Matrix Input 2	Note 15
Keyboard Scan Interface	KSI3	Keyboard Scan Matrix Input 3	Note 15
Keyboard Scan Interface	KSI4	Keyboard Scan Matrix Input 4	Note 15
Keyboard Scan Interface	KSI5	Keyboard Scan Matrix Input 5	Note 15
Keyboard Scan Interface	KSI6	Keyboard Scan Matrix Input 6	Note 15
Keyboard Scan Interface	KSI7	Keyboard Scan Matrix Input 7	Note 15
Keyboard Scan Interface	KSO00	Keyboard Scan Matrix Output 0	Note 15

Interface	Signal Name	Description	Notes
Keyboard Scan Interface	KSO01	Keyboard Scan Matrix Output 1	Note 15
Keyboard Scan Interface	KSO02	Keyboard Scan Matrix Output 2	Note 15
Keyboard Scan Interface	KSO03	Keyboard Scan Matrix Output 3	Note 15
Keyboard Scan Interface	KSO04	Keyboard Scan Matrix Output 4	Note 15
Keyboard Scan Interface	KSO05	Keyboard Scan Matrix Output 5	Note 15
Keyboard Scan Interface	KSO06	Keyboard Scan Matrix Output 6	Note 15
Keyboard Scan Interface	KSO07	Keyboard Scan Matrix Output 7	Note 15
Keyboard Scan Interface	KSO08	Keyboard Scan Matrix Output 8	Note 15
Keyboard Scan Interface	KSO09	Keyboard Scan Matrix Output 9	Note 15
Keyboard Scan Interface	KSO10	Keyboard Scan Matrix Output 10	Note 15
Keyboard Scan Interface	KSO11	Keyboard Scan Matrix Output 11	Note 15
Keyboard Scan Interface	KSO12	Keyboard Scan Matrix Output 12	Note 15
Keyboard Scan Interface	KSO13	Keyboard Scan Matrix Output 13	Note 15
Keyboard Scan Interface	KSO14	Keyboard Scan Matrix Output 14	Note 15
Keyboard Scan Interface	KSO15	Keyboard Scan Matrix Output 15	Note 15
Keyboard Scan Interface	KSO16	Keyboard Scan Matrix Output 16	Note 15
Keyboard Scan Interface	KSO17	Keyboard Scan Matrix Output 17	Note 15
LPC HOST INTERFACE	CLKRUN#	PCI Clock Control	
LPC HOST INTERFACE	LAD0	LPC Multiplexed command, address and data bus Bit 0.	Note 1
LPC HOST INTERFACE	LAD1	LPC Multiplexed command, address and data bus Bit 1.	Note 1
LPC HOST INTERFACE	LAD2	LPC Multiplexed command, address and data bus Bit 2.	Note 1
LPC HOST INTERFACE	LAD3	LPC Multiplexed command, address and data bus Bit 3.	Note 1
LPC HOST INTERFACE	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	
LPC HOST INTERFACE	LPCPD#	LPC Power Down	
LPC HOST INTERFACE	LRESET#	LPC Reset. LRESET# is the same as the system PCI reset, PCIRST#	
LPC HOST INTERFACE	nEC_SCI	Power Management Event	
LPC HOST INTERFACE	nEMI_INT	EMI Interrupt Output	
LPC HOST INTERFACE	nSMI	SMI Output	
LPC HOST INTERFACE	PCI_CLK	PCI Clock	
LPC HOST INTERFACE	SER_IRQ	Serial IRQ	Note 1
Master Clock Interface	XTAL1	32.768 KHz Crystal Output	
Master Clock Interface	XTAL2	32.768 KHz Crystal Input (single-ended 32.768 KHz clock input)	
MISC Functions	32KHZ_OUT	32.768 KHz Digital Output	
MISC Functions	A20M	KBD GATEA20 Output	
MISC Functions	KBRST	CPU_RESET	
MISC Functions	LED0	LED (Bllinking/Breathing PWM) PWM Output 0	
MISC Functions	LED1	LED (Bllinking/Breathing PWM) PWM Output 1	

Interface	Signal Name	Description	Notes
MISC Functions	LED2	LED (Bllinking/Breathing PWM) PWM Output 2	
MISC Functions	nRESET_IN	External System Reset Input	
MISC Functions	nRESET_OUT	EC-driven External System Reset Output	Note 5
MISC Functions	TFDP_CLK	Trace FIFO debug port - clock	
MISC Functions	TFDP_DATA	Trace FIFO debug port - data	
MISC Functions	VCC_PWRGD	System Main Power Indication	
MISC Functions	XNOR	Test Output	
PECI Interface	PECI_DAT	PECI Bus	Note 12
Power Interface	ADC_VREF	ADC Reference Voltage	Note 18
Power Interface	AVSS	Analog ADC supply associated ground	
Power Interface	DAC_VREF	DAC Reference Voltage	Note 18
Power Interface	VBAT	VBAT supply	
Power Interface	VR_CAP	Internal Voltage Regulator Capacitor	Note 3
Power Interface	VREF_CPU	Processor Interface Voltage Reference	Note 6, Note 18
Power Interface	VSS	VTR associated ground	
Power Interface	VSS_VBAT	VBAT associated ground	
Power Interface	VTR	VTR Suspend Power Supply	
Power Interface	VTR_33_18	Host Interface Power Supply	
PS/2 Interface	PS2_CLK0	PS/2 clock 0 (PS2_CLK)	
PS/2 Interface	PS2_CLK1A	PS/2 clock 1 - Port A (PS2_CLK)	
PS/2 Interface	PS2_CLK1B	PS/2 clock 1 - Port B (PS2_CLK)	
PS/2 Interface	PS2_DAT0	PS/2 data 0 (PS2_DAT)	
PS/2 Interface	PS2_DAT1A	PS/2 data 1 - Port A (PS2_DAT)	
PS/2 Interface	PS2_DAT1B	PS/2 data 1 - Port B (PS2_DAT)	
PWM	PWM0	Pulse Width Modulator Output 0	
PWM	PWM1	Pulse Width Modulator Output 1	
PWM	PWM2	Pulse Width Modulator Output 2	
PWM	PWM3	Pulse Width Modulator Output 3	
PWM	PWM4	Pulse Width Modulator Output 4	
PWM	PWM5	Pulse Width Modulator Output 5	
PWM	PWM6	Pulse Width Modulator Output 6	
PWM	PWM7	Pulse Width Modulator Output 7	
Tachometer	TACH0	Fan Tachometer Input 0	
Tachometer	TACH1	Fan Tachometer Input 1	
SMBus Interface	SB_TSI_DAT	SMBus Controller AMD-TSI Port Data	Note 12
SMBus Interface	SB-TSI_CLK	SMBus Controller AMD-TSI Port Clock	
SMBus Interface	SMB00_CLK	SMBus Controller Port 0 Clock	Note 4, Note 11
SMBus Interface	SMB00_DATA	SMBus Controller Port 0 Data	Note 4, Note 11