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MFRC523

Standard performance ISO/IEC 14443 A/B frontend

Rev. 4.2 — 27 April 2016
115242

Product data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC523.

1.1 Different available versions

The MFRC523 is available in two versions:

- MFRC52302 (HVQFN32), hereafter named as version 2.0
- MFRC52301 (HVQFN32), hereafter named as version 1.0

The differences of the version 1.0 to the version 2.0 are summarized in Section 11.

2. General description

The MFRC523 is a highly integrated reader/writer for contactless communication at 13.56 MHz. The MFRC523 reader supports ISO/IEC 14443 A/MIFARE mode.

The MFRC523's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

All protocol layers of the ISO/IEC 14443 A and ISO/IEC 14443 B communication standards are supported:

- additional components, such as the oscillator, power supply, coil etc are correctly applied
- standardized protocols, such as ISO/IEC 14443-4 and/or ISO/IEC 14443 B anticollision are correctly implemented

The MFRC523 supports contactless communication using MIFARE higher baud rates (see Section 8.3.4.11 on page 22) at transfer speeds up to 848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependent on pin voltage supply)
- I^2C-bus interface

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE
- Supports ISO/IEC 14443 B Read/Write modes
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MIFARE Mini, MIFARE 1K and MIFARE 4K encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication at 212 kBd, 424 kBd and 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage			2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V		-	6.5	9	mA

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32		−25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MFRC52302HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52302HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52301HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52301HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in one tray.

[2] Delivered in five trays.

6. Block diagram

The analog interface manages the modulation and demodulation of the analog signals. The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfers to/from the host and the contactless UART.

Various host interfaces are implemented to meet different customer requirements.

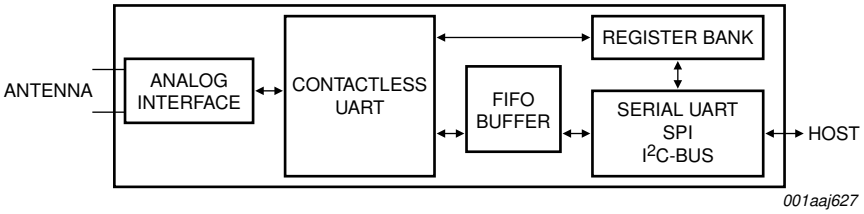


Fig 1. Simplified block diagram of the MFRC523

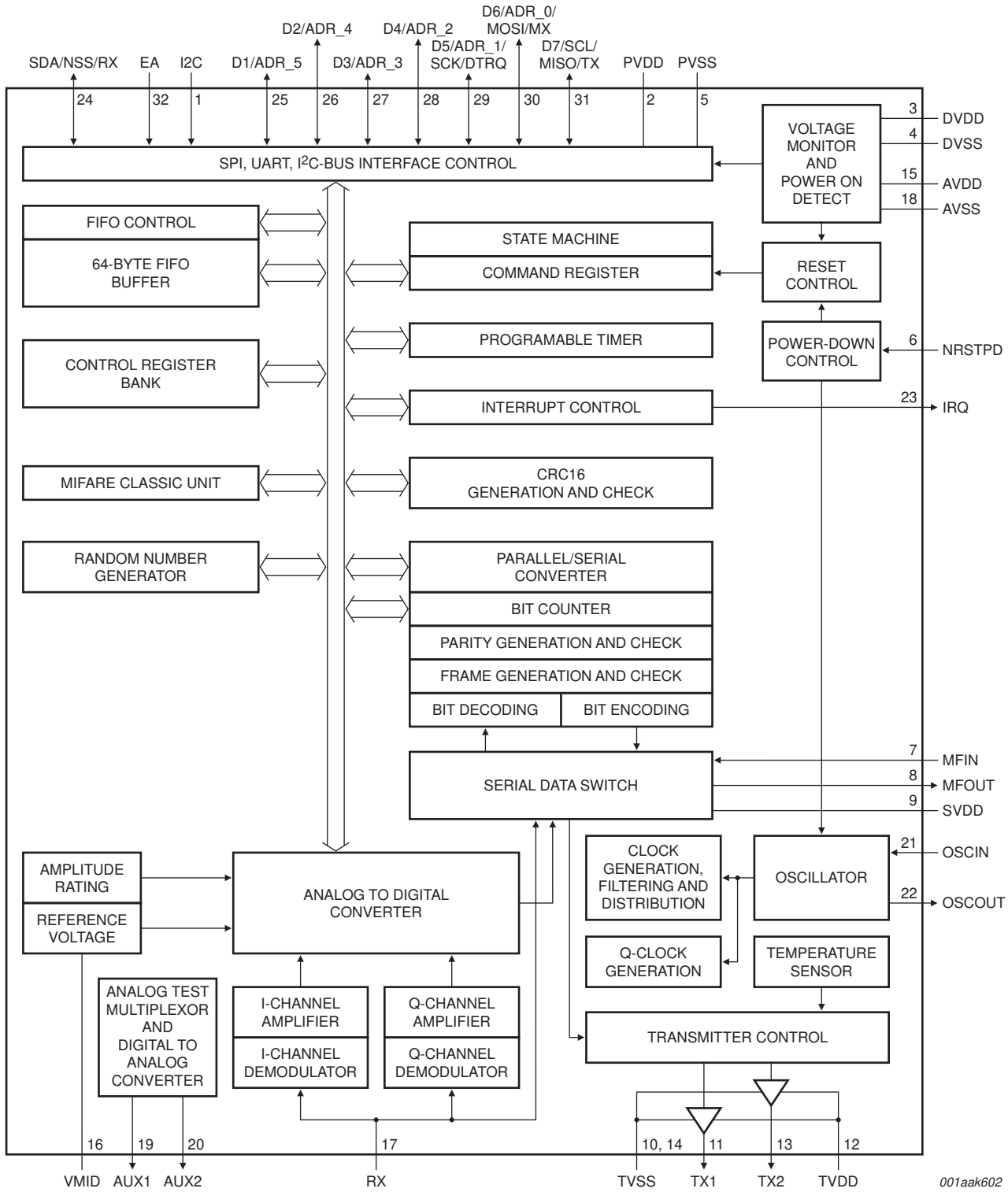
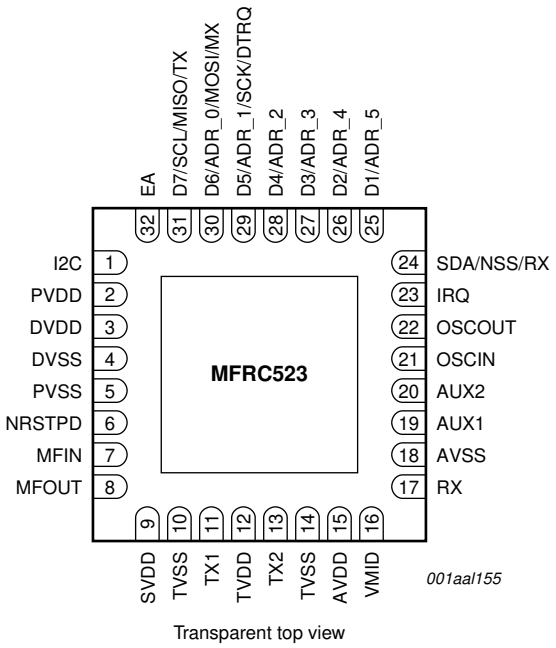


Fig 2. Detailed block diagram of the MFRC523

7. Pinning information



Transparent top view

Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type[1]	Description
1	I2C	I[2]	I^2C-bus enable input
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G[3]	digital ground
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: reset: enabled by a positive edge power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply

Table 3. Pin description *...continued*

Pin	Symbol	Type[1]	Description
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (f_{clk} = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA[2]	I/O	I^2C-bus serial data line input/output
	NSS[2]	I	SPI signal input
	RX[2]	I	UART address input
25	D1[2]	I/O	test port
	ADR_5[2]	I/O	I^2C-bus address 5 input
26	D2	I/O	test port
	ADR_4[2]	I	I^2C-bus address 4 input
27	D3	I/O	test port
	ADR_3[2]	I	I^2C-bus address 3 input
28	D4	I/O	test port
	ADR_2[2]	I	I^2C-bus address 2 input
29	D5	I/O	test port
	ADR_1[2]	I	I^2C-bus address 1 input
	SCK[2]	I	SPI serial clock input
	DTRQ[2]	O	UART request to send output to microcontroller
30	D6	I/O	test port
	ADR_0[2]	I	I^2C-bus address 0 input
	MOSI[2]	I/O	SPI master out, slave in
	MX[2]	O	UART output to microcontroller
31	D7	I/O	test port
	SCL[2]	I/O	I^2C-bus clock input/output
	MISO[2]	I/O	SPI master in, slave out
	TX[2]	O	UART data output to microcontroller
32	EA[2]	I	external address input for coding I^2C-bus address

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in Section 8.3 “Digital interfaces”.

[3] Connection of heatsink pad on package underside is not necessary. Optional connection to pin DVSS is possible.

8. Functional description

The MFRC523 transmission module supports ISO/IEC 14443 A and ISO/IEC 14443 B Read/Write mode at various transfer speeds and modulation protocols.

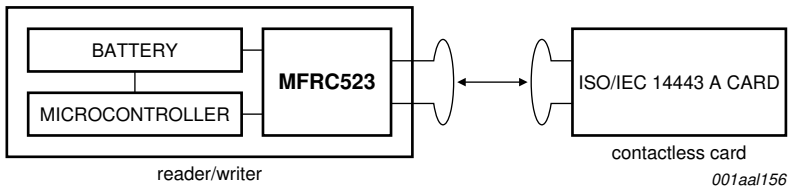
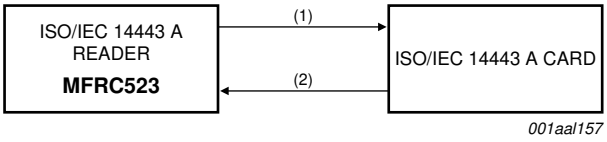


Fig 4. MFRC523 Read/Write mode

8.1 ISO/IEC 14443 A functionality

The physical level communication is shown in Figure 5.



(1) Reader to card (MFRC523 sends data to a card).

(2) Card to reader (card sends data to the MFRC523).

Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (MFRC523 sends data to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 µs)	64 (13.56 µs)	32 (13.56 µs)	16 (13.56 µs)
Card to reader (card sends data to the MFRC523)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MFRC523's contactless UART and dedicated external host must manage the ISO/IEC 14443 A protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443 A.

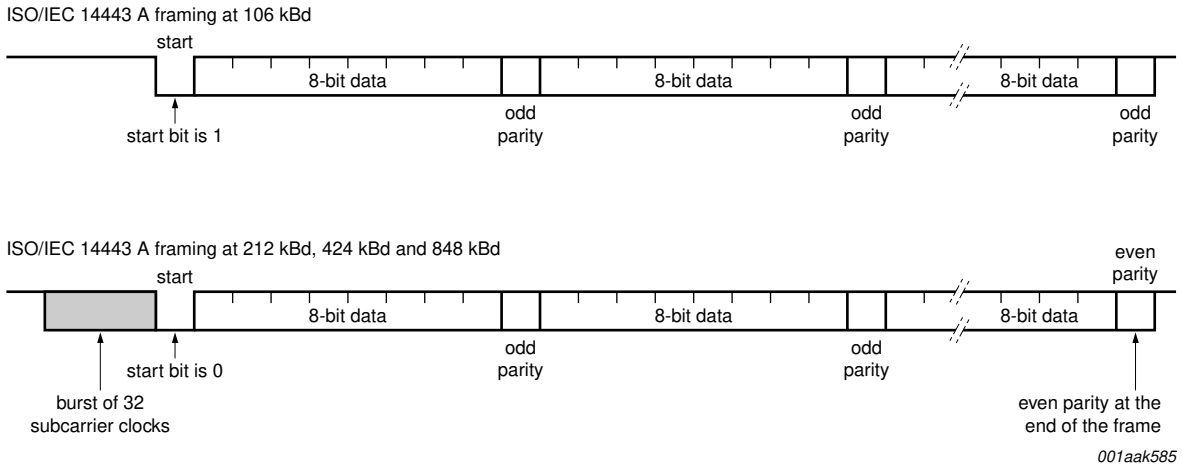


Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally based on the transfer speed. Automatic parity generation can be switched off using the ManualRCVReg register's ParityDisable bit.

8.2 ISO/IEC 14443 B functionality

The MFRC523 reader IC fully supports the ISO 14443 international standard which includes the communication schemes ISO 14443 A and ISO 14443 B. Refer to the ISO 14443 reference documents *Identification cards - Contactless integrated circuit cards - Proximity cards* (parts 1 to 4).

8.3 Digital interfaces

8.3.1 Automatic microcontroller interface detection

The MFRC523 supports direct interfacing to hosts using SPI, I^2C-bus or serial UART interfaces. The MFRC523 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset.

The MFRC523 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 5 shows the different pin connection configurations.

Table 5. Connection protocol for detecting different interface types

Pin	Interface type		
	UART (input)	SPI (output)	I²C-bus (I/O)
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.3.2 Serial Peripheral Interface

The 5-wire Serial Peripheral Interface (SPI) is supported and enables high-speed communication with the host. The interface can manage data speeds up to 10 Mbit/s. When communicating with a host, the MFRC523 acts as a slave. As such, it receives data from the external host for register settings, sends and receives data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC523 and a microcontroller. The implemented interface meets with the SPI standard.

The timing specification is given in Section 15.1 on page 78.

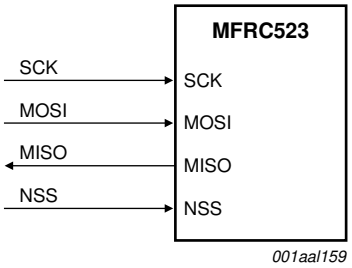


Fig 7. SPI connection to host

The MFRC523 acts as a slave during SPI communication and is timed using the SPI clock signal (SCK) generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC523 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is sent by the MFRC523 on the falling clock edge and is stable during the rising clock edge.

8.3.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 6 to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n – 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

8.3.2.2 SPI write data

To write data to the MFRC523 using SPI requires the byte order shown in Table 7. It is possible to write up to n-data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

8.3.2.3 SPI Read and Write address byte

The read address byte must meet the following criteria:

- the Most Significant Bit (MSB) of the first byte sets the mode. To read data from the MFRC523, the MSB is set to logic 1; see Table 8
- bits [6:1] define the address
- the Least Significant Bit (LSB) should be set to logic 0

Table 8. SPI read address

Address (MOSI)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
byte 0	1	address	address	address	address	address	address	0

The write address byte must meet the following criteria:

- the MSB of the first byte sets the mode. To write data to the MFRC523, the MSB is set to logic 0; see Table 9
- bits [6:1] define the address
- the LSB should be set to logic 0

Table 9. SPI write address

Address line (MOSI)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
byte 0	0	address	address	address	address	address	address	0

8.3.3 UART interface

8.3.3.1 Connection to a host

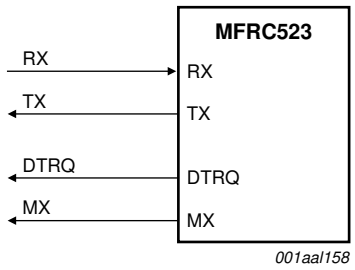


Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.3.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with the RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 10. Examples of different transfer speeds and the relevant register settings are given in Table 11.

Table 10. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 11. Selectable UART transfer speeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	−0.25
9.6	235	EBh	0.32
14.4	218	DAh	−0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	−0.25
115.2	122	7Ah	−0.25
128	116	74h	−0.06
230.4	90	5Ah	−0.25
460.8	58	3Ah	−0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in Table 11 are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR\_T0 + 1)} \quad (1)$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{\frac{(BR\_T1 + 33)}{2^{(BR\_T0 - 1)}}} \right) \quad (2)$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

8.3.3.3 UART framing

Table 12. UART framing

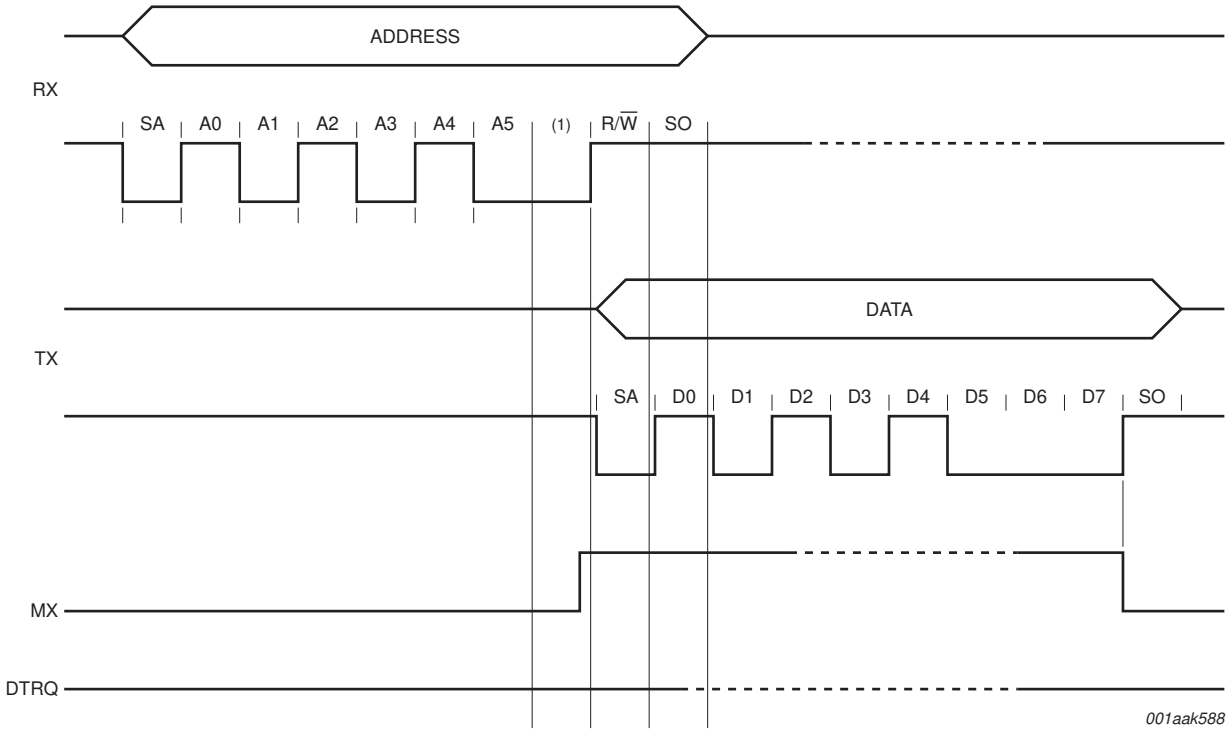
Bit	Length	Value
Start	1-bit	0
Data	8-bit	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

To read data using the UART interface, the flow shown in Table 13 must be used. The first byte sent defines both the mode and the address.

Table 13. Read data byte order

Pin	Byte 0	Byte 1
RX	address	-
TX	-	data 0



(1) Reserved.

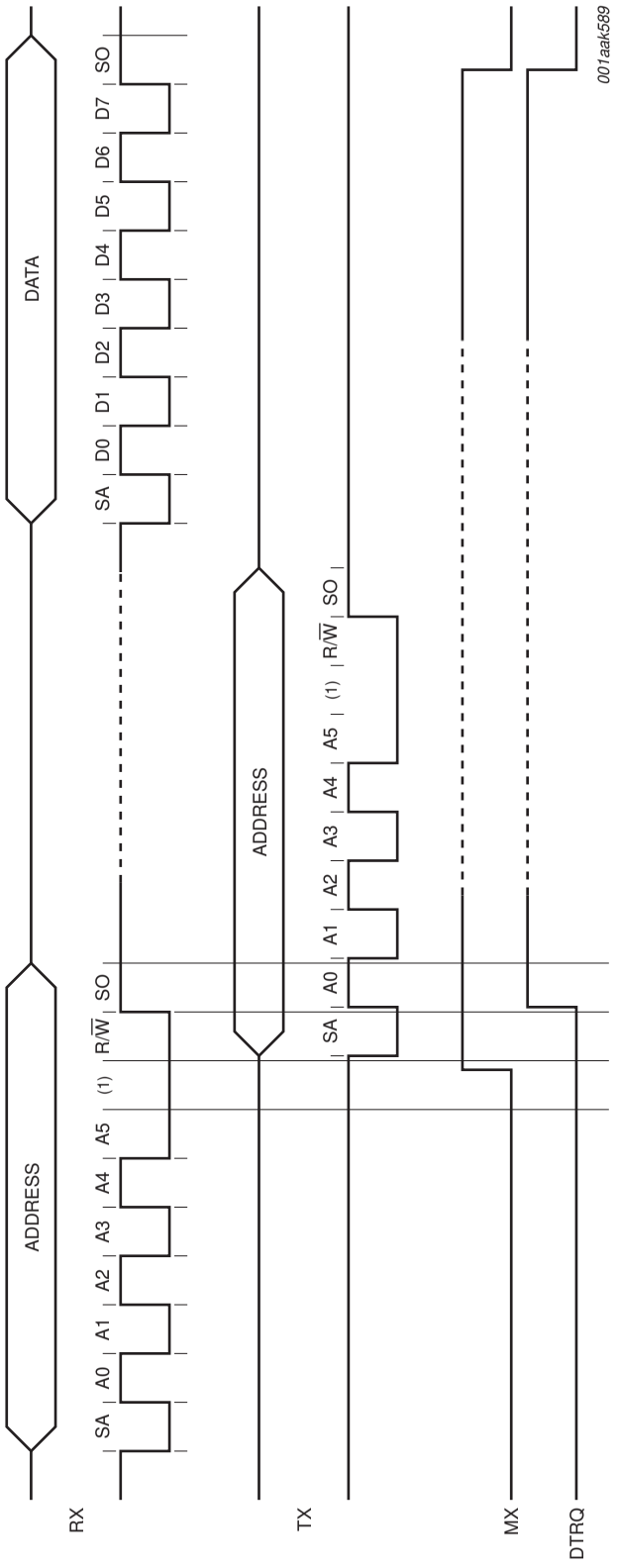
Fig 9. UART read data timing diagram

To write data to the MFRC523 using the UART interface, the structure shown in Table 14 must be used.

The first byte sent defines both the mode and the address.

Table 14. Write data byte order

Pin	Byte 0	Byte 1
RX	address 0	data 0
TX	-	address 0



(1) Reserved.

Remark: The data byte can be sent directly after the address byte on pin RX.

Fig 10. UART write data timing diagram

The address byte must meet the following formats:

- the MSB of the first byte sets the mode used
  - the MSB is set to logic 0 to write data to the MFRC523
  - the MSB is set to logic 1 to read data from the MFRC523
- bit 6 is reserved for future use
- bits [5:0] define the address; see Table 15

Table 15. Address byte 0 register; address MOSI

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
1 or 0	reserved	address	address	address	address	address	address

8.3.4 I²C Bus Interface

An I²C-bus interface is supported and enables implementation of a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented based on NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in slave mode. Therefore the MFRC523 does not perform clock generation or access arbitration.

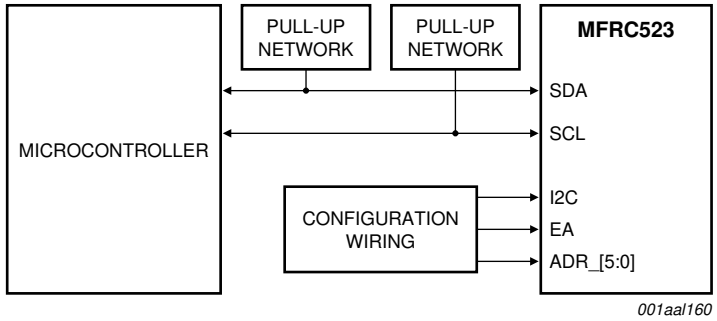


Fig 11. I²C-bus interface

The MFRC523 can act as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC523 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See Table 156 on page 79 for timing requirements.

8.3.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

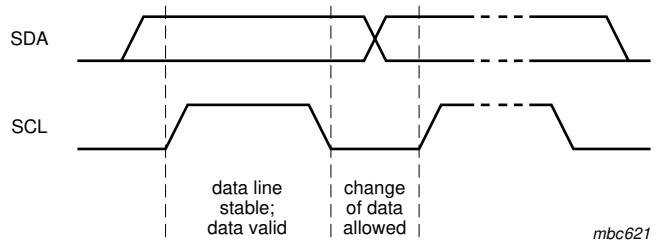


Fig 12. Bit transfer on the I²C-bus

8.3.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

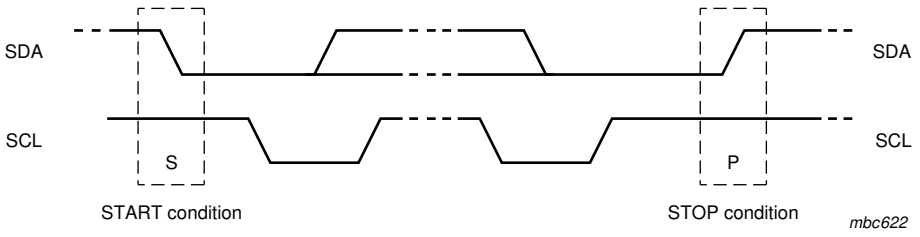


Fig 13. START and STOP conditions

8.3.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 16. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

8.3.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

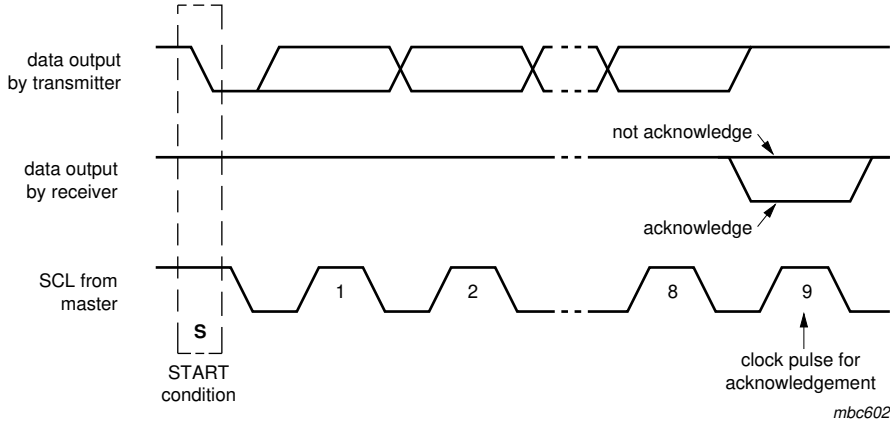


Fig 14. Acknowledge on the I²C-bus

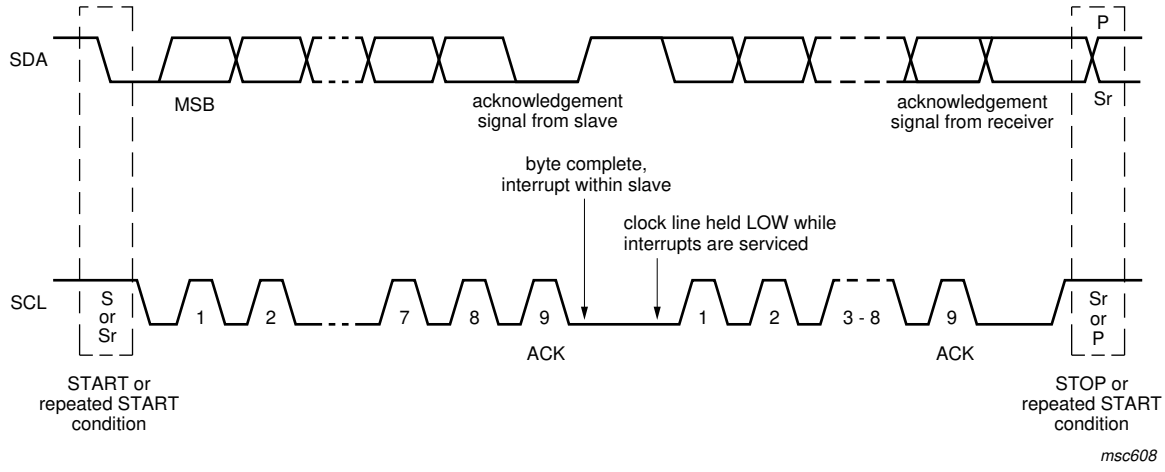


Fig 15. Data transfer on the I²C-bus

8.3.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all MFRC523 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to Table 5 on page 10. ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.

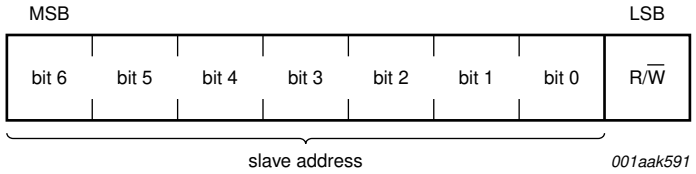


Fig 16. First byte following the START procedure

8.3.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the MFRC523 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame, all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to logic 0.

8.3.4.7 Register read access

To read out data from a specific register address in the MFRC523, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I²C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the MFRC523. In response, the MFRC523 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to logic 1.

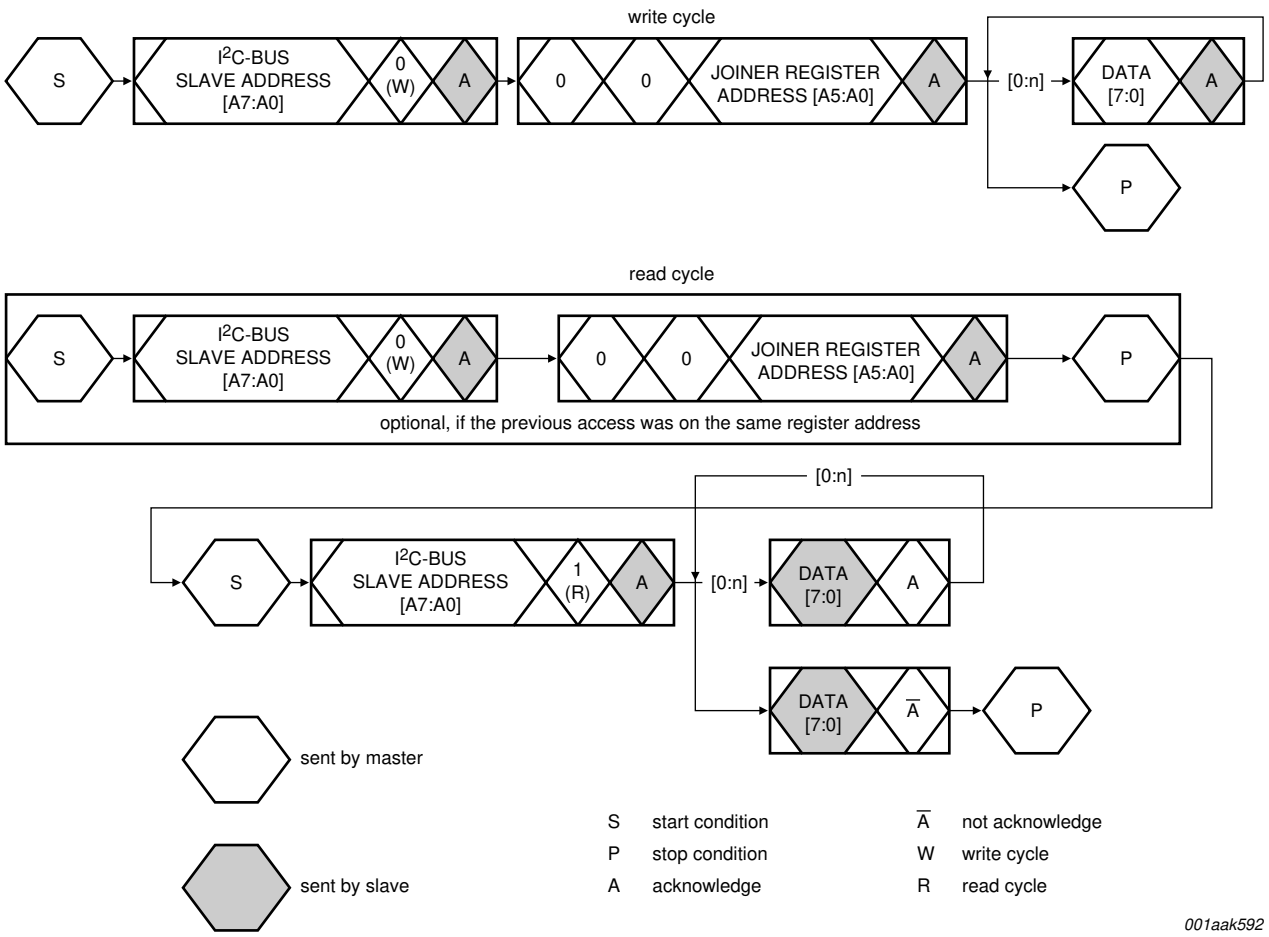


Fig 17. Register read and write access

8.3.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard modes (F/S modes) for bidirectional communication in a mixed-speed bus system.

8.3.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.3.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I^2C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001 XXXb)
3. Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected MFRC523.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

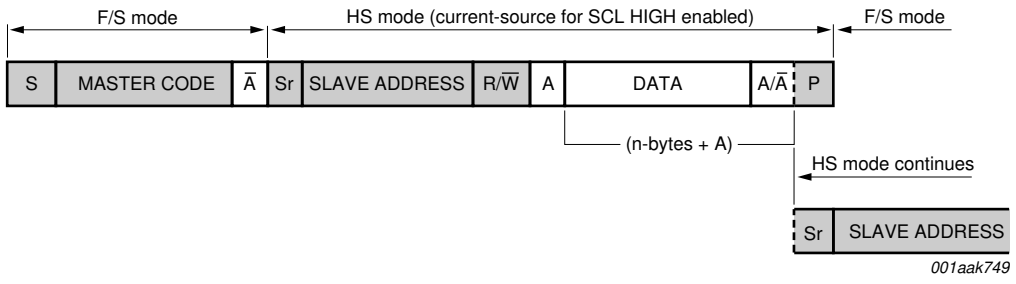


Fig 18. I^2C-bus HS mode protocol switch

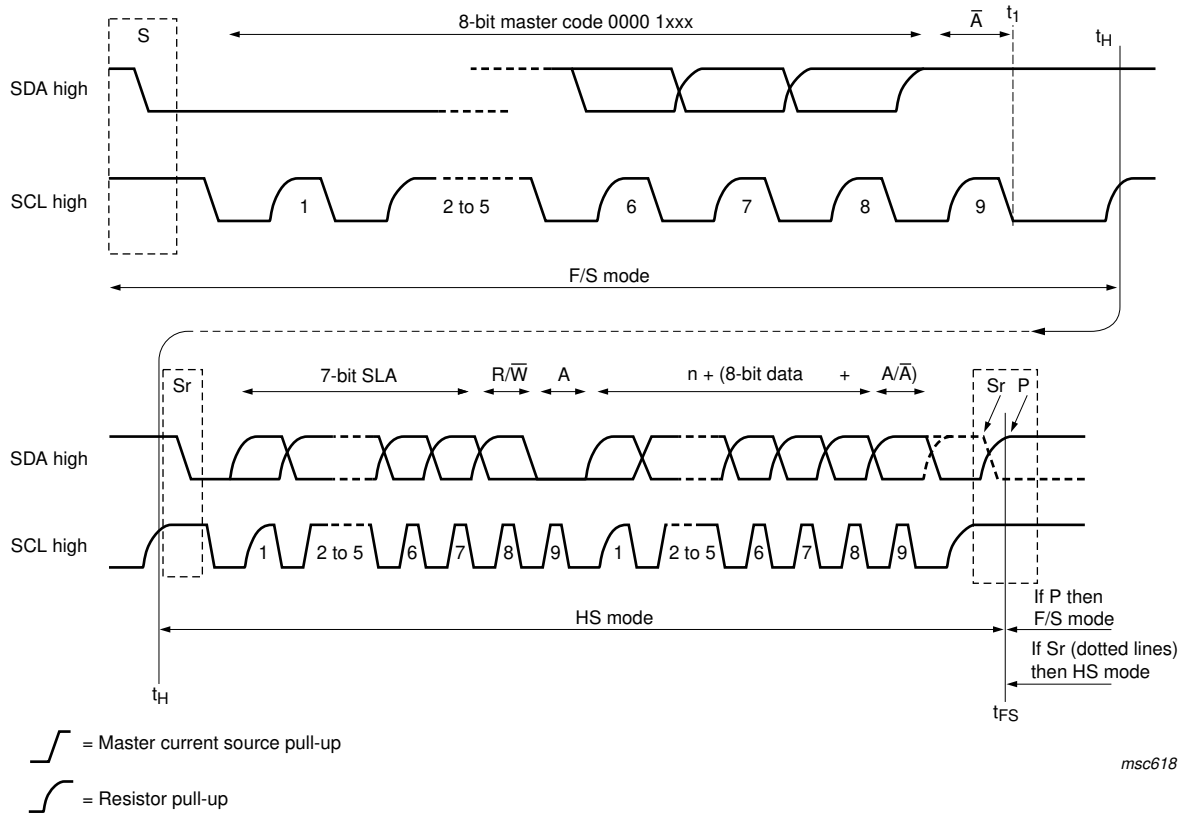


Fig 19. I²C-bus HS mode protocol frame

8.3.4.11 Switching between F/S mode and HS mode

After reset and initialization, the MFRC523 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected MFRC523 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I²C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I²CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I²C-bus lines must be avoided because of the reduced spike suppression.

8.3.4.12 MFRC523 in lower speed modes

MFRC523 is fully downward-compatible and can be connected to an F/S mode I²C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

8.4 Analog interface and contactless UART

8.4.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART manage the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it manages error detection such as parity and CRC, based on the various supported contactless communication protocols.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

8.4.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see Section 16 on page 81. The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see Section 9.2.2.5 on page 49.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 16. Register and bit settings controlling the signal on pin TX1

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	X[1]	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0, independently of the InvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X[1]	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X[1]	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

[1] X = Do not care.

Table 17. Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	0	X[1]	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X[1]	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	conductance always CW for the Tx2CW bit
			1	X[1]	X[1]	RF_n	pCW	nCW	
	1	0	0	X[1]	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOn/InvTx2RFOff bits)
					1	RF	pCW	nCW	
			1	X[1]	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	
			1	X[1]	X[1]	RF_n	pCW	nCW	

[1] X = Do not care.

The following abbreviations have been used in Table 16 and Table 17:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = Do not care

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

8.4.3 Serial data switch

Two main blocks are implemented in the MFRC523. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT. This topology allows the analog block of the MFRC523 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for TX1 and TX2.

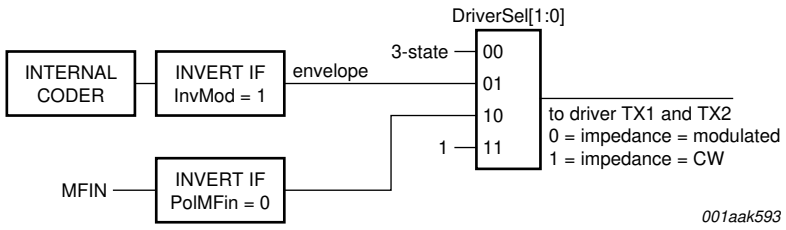


Fig 20. Serial data switch for TX1 and TX2

8.4.4 MFIN and MFOUT interface support

The MFRC523 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic, etc. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured to enable the interfacing signals to be routed to pins MFIN and MFOUT; see Figure 21 on page 26. This configuration is implemented using TxSelReg register's MFOutSel[3:0]/DriverSel[1:0] bits and RxSelReg register's UARTSel[1:0] bits. This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for testing purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MFRC523's digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

Remark: Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS.